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Preprint

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APPLICATIONS OF ADMITTANCE SPECTROSCOPY IN PHOTOVOLTAIC DEVICES BEYOND MAJORITY-CARRIER TRAPPING DEFECTS

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ABSTRACT

Admittance spectroscopy is commonly used to characterize majority- carrier trapping defects. In today's practical photovoltaic devices, however, a number of other physical mechanisms may contribute to the admittance measurement and interfere with the data interpretation. Such challenges arise due to the violation of basic assumptions of conventional admittance spectroscopy such as single- junction, ohmic contact, highly conductive absorbers, and measurement in reverse bias. We exploit such violations to devise admittance spectroscopy- based methods for studying the respective origins of "interference": majority- carrier mobility, non-ohmic contact potential barrier, minority- carrier inversion at hetero-interface, and minority- carrier lifetime in a device environment. These methods are applied to a variety of photovoltaic technologies: CdTe, $Cu(In,Ga)Se_2$, Si HIT cells, and organic photovoltaic materials.

INTRODUCTION

Defects are undoubtedly among the most critical physical issues to address for the photovoltaic (PV) industry. Admittance spectroscopy, among other capacitance-based techniques such as capacitance-voltage and deep-level transient spectroscopy, is commonly used to characterize majority-carrier trapping defects in PV materials and devices. Admittance spectroscopy inspects the current response of a device to small AC bias voltage modulation and its dependence on frequency and temperature, presumably due to the capture and emission of the electrically active defects. In a simple single-junction device, it is possible to extract defect parameters such as activation energy, capture cross-section, and density of states [1],[2].

The photovoltaic community depends on maintaining the integrity that the signals measured by admittance spectroscopy and reported as defects are truly due to majority-carrier traps. Without that, ensuing confusion will certainly mislead the research effort. Unfortunately, only in certain simple devices can it be safely assumed that admittance spectroscopy reflects nothing but majority-carrier traps. Today's PV devices are sophisticatedly engineered with inclusion of building blocks such as polycrystalline absorbers, heterojunctions, and non-ideal contacts. The complex nature of these practical PV devices determines that other mechanisms may also contribute to the admittance measurement. Therefore, one should be careful not to attribute all admittance spectroscopy measurements to majority-carrier trapping defects.

On the other hand, there is an urgent need to evaluate a host of other material and device properties besides defects. In this work, we focus on majority-carrier mobility, non-ohmic contact potential barrier, minority-carrier inversion at certain heterojunction, and minority-carrier lifetime in a device environment (i.e., after the device fabrication is completed, rather than at the intermediate stage of wafer or thin-film level). Such properties are usually important to PV device operation and could be difficult to characterize by other techniques. Here, we recognize unique opportunities for extracting these non-majority-trap-related properties by admittance spectroscopy. We develop characterization methods and apply them to various PV technologies: CdTe, $Cu(In,Ga)Se_2$ (CIGS), silicon heterojunction cells with an intrinsic thin (HIT) amorphous silicon layer, and poly(3-hexylthiophene) organic photovoltaic (OPV) material.

EXPERIMENT

We conducted admittance spectroscopy measurements using an Agilent 4294A impedance analyzer. The AC modulation voltage was nominally 35 mV_{rms}. A Lakeshore 331A temperature controller was used to stabilize and sense the cold-finger temperature (ranging from 14 – 400 K) of a close-loop He cryostat. At each temperature setting, we recorded the sample temperature from a second temperature sensor attached directly to the sample side of the substrate. (The other side is in contact with the copper stage of the cold figure.) At each fixed temperature, we applied a series of DC bias voltages to the device. A logarithmic frequency scan was carried out at each DC bias voltage. When required, we also conducted current-density-voltage (JV) measurement at each temperature using an HP 4140 semiconductor parameter analyzer.

The fabrication process of CdTe thin-film devices was similar to previous report [3] with the addition that gold is also experimented with as the back-contact metal. The $Cu(In,Ga)Se_2$ thin-film device was fabricated using the standard process [4], except that the growth temperature for the $Cu(In,Ga)Se_2$ film in this study was 435°C. This growth temperature was selected to produce low carrier density in the absorber so that its dielectric relaxation frequency is below 100 MHz. The Si heterojunction cells with an intrinsic thin layer were grown on n-type wafers. The samples were taken from a previously reported sample set, the fabrication details of which were reported

elsewhere [5]. The poly(3-hexylthiophene) (P3HT) polymer sample was fabricated by spin coating P3HT from solution onto a poly(3,4-ethylenedioxythiophene) poly (styrene-sulfonate) (PEDOT:PSS) layer on top of indium tin oxide-coated glass. The other contact is aluminum.

Application of admittance spectroscopy to deep levels in the absorber of a typical PV device usually assumes that several conditions are satisfied: 1) the absorber is conductive enough and the dielectric relaxation frequency of bulk absorber material is out of the range of interest; 2) only one junction is present and both contacts are ohmic; 3) only majority-carrier traps are observed; and 4) the junction is in reverse bias. With these simplifications, it is safe to consider that admittance spectroscopy reflects the behavior of majority-carrier trapping defects. However, the complex nature of most practical PV devices means that one or more of these conditions may often be violated in the admittance measurement.

Figure 1 shows the admittance spectroscopy spectrum taken from a CdTe solar cell using temperature derivative representation [6]. Three peaks are labeled. At first sight, it appears that there are three peaks—hence, three majority-carrier trapping defects. However, only peak 3 (~0.55 eV) is a deep level due to Cu. This peak is present when Cu is added to the back-contact formation process. It is absent when the back-contact formation process is intentionally deprived of Cu. As we will explain in the following text, peaks 1 and 2 are not signatures of deep levels.
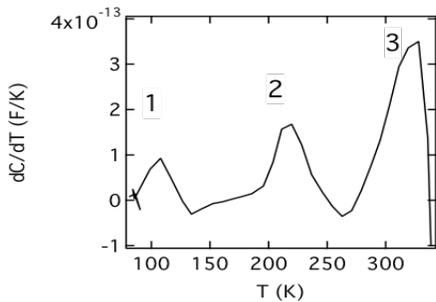

Figure 1 The temperature differential capacitance measured at 43.7 kHz from a CdTe solar cell.

If the free carrier density and mobility of the absorber are not high enough—a probable situation in CdTe due to the low free carrier density—the first condition about dielectric relaxation may not be met. The dielectric relaxation of a bulk semiconductor is given by $\omega_{dr}=1/\rho\varepsilon$, where ρ is the resistivity and ε is the permittivity. In the case of high absorber resistivity or low measurement temperature, the dielectric relaxation frequency may fall into the range of interest. Indeed, peak 1 in Fig. 1 is due to dielectric relaxation (or freeze-out) of the CdTe absorber at low temperatures. The hallmark of this type of frequency response is the following: at a temperature lower (or frequency higher) than the transition point, the capacitance approaches the geometrical capacitance value (data not shown here).

In the presence of the junction depletion capacitance (Fig. 2), the dielectric relaxation frequency of the absorber is modified [7] by a factor of W/t, where W is the depletion width and t is the absorber thickness. Because W varies with bias voltage, the modified dielectric relaxation frequency becomes bias dependent. We developed a method to measure mobility from the bias dependence of the dielectric relaxation frequency (Fig. 3) [8]. The hole mobility (T = 300 K) of the CIGS device measured is 0.66 cm^2/V/s. Figure 4 shows the bias dependence of the square of the modified dielectric relaxation frequency in a P3HT sample. From there, the mobility of holes in a series of P3HT samples at room temperature is extracted to be in the range of high 10^{-6} to low 10^{-4} cm^2/V/s, consistent with measurements using other techniques [9]. This method works well on other low-mobility devices such as CdTe (at low temperature) [8] and a-Si.
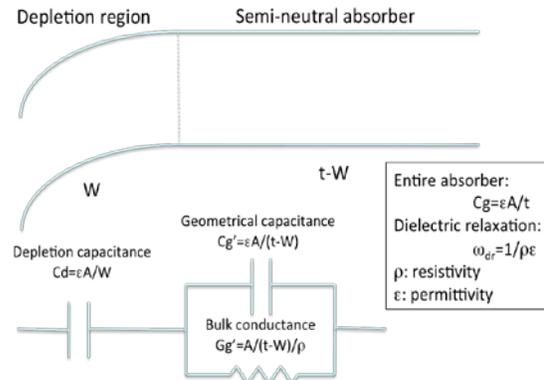

Figure 2 Band diagram and equivalent circuit of a solar cell with a depletion region and a neutral absorber connected in series.
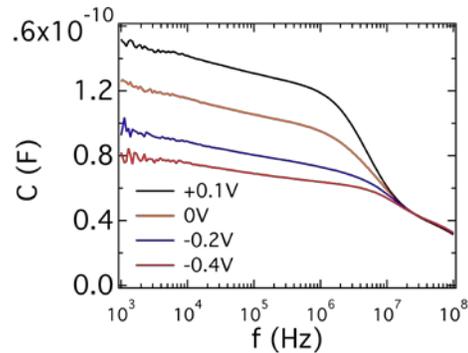

Figure 3 Frequency dependence of the capacitance of a CIGS solar cell measured under various biases.
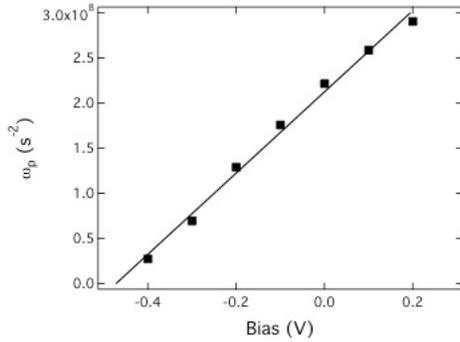
Figure 4 Bias dependence of the square of the dielectric relaxation frequency from a P3HT device.

It is also possible to violate the second condition, which demands that only one junction is present in the device. CdTe thin-film devices are prime candidates because of the difficulty of forming a high-quality, ohmic back contact. Peak 2 in Fig. 1 is actually due to the back-contact barrier. The activation energy extracted from Peak 2 data consistently agrees with that from the rollover feature seen in JVT curves (Fig. 5), which has been identified as attributable to the back-contact barrier [10]-[12]. For example, the CdTe device with a gold contact yielded a back-contact barrier height of 422 ± 5 meV from admittance spectroscopy and 424 ± 20 meV from the JVT experiment. In contrast, the back-contact barrier height for NREL's devices with graphite contacts is 494 ± 9 meV from admittance spectroscopy and 552 ± 10 from the JVT experiment. The JVT experiment serves as a useful correlated experiment to identify the secondary potential barrier.
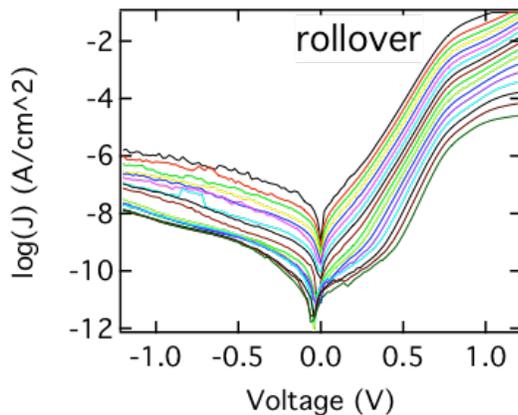

Figure 5 The JVT curves taken from a CdTe device showing rollover due to the back-contact barrier.

Under most circumstances, admittance spectroscopy measures contributions from the response of majority carriers. There are usually not enough minority carriers to have a significant capacitance contribution. In certain devices with highly asymmetrical doping, especially with the presence of a suitable heterointerface, it is possible for inversion to occur in a region where the minority-carrier density is significant. The CdS/CIGS heterointerface is

such an example [13]. The inversion layer reduces interface recombination by repelling the majority carriers.

Recently, there has also been an increasing interest in understanding the inversion phenomenon at the amorphous (a-Si) and crystalline (c-Si) interface in a HIT cell. We show in Figure 6 the band diagram of a HIT cell fabricated on n-type substrate. An activation energy of 0.14-0.28 eV is observed in these devices. There is no known bulk defect of this energy in the crystalline silicon. After further ruling out the valence-band offset (~0.45 eV), we conclude that this activation energy is the measurement Fermi level at the a-Si/c-Si interface. The band bending is large enough at the interface such that that region is strongly inverted. The exchange of holes—whose density is comparable with that of electrons in the bulk, between the valence band and the Fermi level—can thus significantly contribute to an observable admittance spectroscopy signal. Unfortunately, there is no simple method to distinguish the inverted carrier-induced signal from that of the majority-carrier traps. We note that the above interpretation can be proven by calculating the band bending from measured carrier density and built-in voltage.
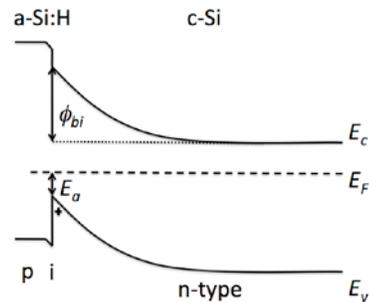

Figure 6 Band diagram of an n-type HIT cell showing the inverted region at the a-Si/c-Si interface.

Admittance spectroscopy is usually carried out with the device in reverse bias to avoid interference from the diffusion capacitance. If the diffusion capacitance cannot be neglected, then the basic physical assumptions of capacitance-voltage technique and admittance spectroscopy technique are violated. However, one can also exploit the diffusion capacitance to study the properties of the injected minority carriers. The diffusion capacitance, which depends exponentially on the forward bias, dominates over the depletion capacitance at sufficiently high forward bias. Beyond this point, the frequency dependence of the diffusion capacitance is dictated by the effective lifetime of the injected minority carriers [14]. Figure 7 shows such a frequency dependence measured from a HIT cell fabricated on an n-type CZ substrate. The hole lifetime is $1/2\pi f_{pk} = 82.6$ μs, which is consistent with values measured by other techniques such as open-circuit voltage decay (~130 μs). The effective lifetime of the holes in c-Si is enhanced by surface passivation by the intrinsic a-Si layer.
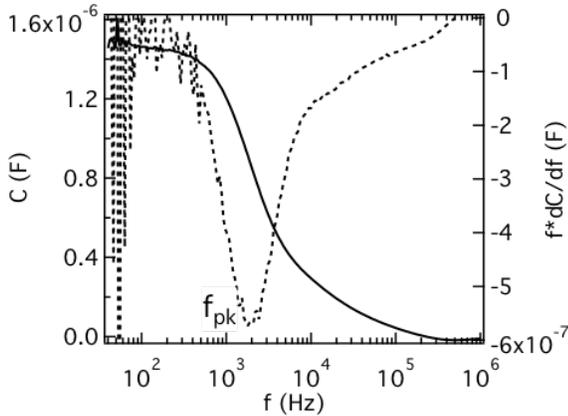
Figure 7 Frequency dependence of capacitance (solid) and differential capacitance (dashed) due to minority-carrier lifetime at 0.6 V bias in a HIT device.

CONCLUSION

In conclusion, we show that many physical mechanisms other than majority-carrier trapping defects contribute to admittance spectroscopy measurements. This contribution occurs because the breakdown of certain assumptions of conventional admittance spectroscopy, namely: single junction, ideal contacts, majority carrier only, and measurement in reverse bias. This work first identifies the possible physical origins of "interference" and distinguishes them from the real defect signatures. More importantly, we take advantage of such "interference" and devise methods to extract important material and device characteristics using admittance spectroscopy. We study several non-majority-trap-related properties that are commonly seen in admittance spectroscopy measurement of PV devices: majority-carrier mobility, freeze-out of majority-carrier density or mobility, contact potential barrier height, density of inverted minority carriers, and lifetime of injected minority carriers. Such properties are usually important to PV device operation and could be difficult to characterize by other techniques. The validity and applicability of these methods are demonstrated by application to a variety of PV technologies: CdTe, Cu(In,Ga)Se$_2$ (CIGS), silicon heterojunction cells with an intrinsic thin (HIT) amorphous silicon layer, and poly(3-hexylthiophene) organic photovoltaic devices.

ACKNOWLEDGMENT

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