April 2000 • NREL/SR-520-27591

Subcontractor Report

Specific PVMaT R&D on Siemens Cz Silicon Product Manufacturing

Annual Subcontract Report
June 1998 — June 1999

T.L. Jester
Siemens Solar Industries
Camarillo, California

National Renewable Energy Laboratory

1617 Cole Boulevard
Golden, Colorado 80401-3393

NREL is a U.S. Department of Energy Laboratory
Operated by Midwest Research Institute • Battelle • Bechtel

Contract No. DE-AC36-99-GO10337

April 2000 • NREL/SR-520-27591

Specific PVMaT R&D on Siemens Cz Silicon Product Manufacturing

Annual Subcontract Report June 1998 — June 1999

T.L. Jester
Siemens Solar Industries
Camarillo, California

NREL Technical Monitor: R.L. Mitchell

Prepared under Subcontract No. ZAX-8-17647-14

National Renewable Energy Laboratory

1617 Cole Boulevard
Golden, Colorado 80401-3393

NREL is a U.S. Department of Energy Laboratory
Operated by Midwest Research Institute • Battelle • Bechtel

Contract No. DE-AC36-99-GO10337

NOTICE

This report was prepared as an account of work sponsored by an agency of the United States government. Neither the United States government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States government or any agency thereof.

Available electronically at http://www.doe.gov/bridge

Available for a processing fee to U.S. Department of Energy
and its contractors, in paper, from:

U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831-0062
phone: 865.576.8401
fax: 865.576.5728
email: reports@adonis.osti.gov

Available for sale to the public, in paper, from:

U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Road
Springfield, VA 22161
phone: 800.553.6847
fax: 703.605.6900
email: orders@ntis.fedworld.gov
online ordering: http://www.ntis.gov/ordering.htm

Printed on paper containing at least 50% wastepaper, including 20% postconsumer waste

Preface

This report describes work done by Siemens Solar Industries (SSI) from June 1998 to June 1999 during Phases I of a three-phase Photovoltaic Manufacturing Technology (PVMaT 5A2) subcontract from DOE/NREL. The work focuses on improvements in the cost per watt of Cz modules and improved PV module manufacturing technology. The focus for the three year program is to implement a 17% efficient, 125 micron thick cell with a 30% reduction in manufacturing cost. In addition, the program will develop a prototype 200 mm diameter cell with low cost module packaging. A final deliverable is a 50% reduction in slurry use for wafer slicing through recycling , and a 70% reduction in caustic waste.

Acknowledgments

Many people have contributed to the work under this contract. Thanks are due especially to Rick Mitchell, NREL technical monitor; to Ruben Balanga, Dave Bender, Eberth Covarrubia, Heinrich Eichermüller, Chet Farris, Bryan Fickett, Jean Hummel, Dave Jeffrey, Waltraut Klein, Greg Mihalik, Alex Mikonowicz, Jeff Nickerson, Ken Sandland, Maria Tsimanis, Elena Woodard, and others in the Engineering, Quality, Manufacturing, and Finance groups at SSI.

This work was funded in part by DOE/NREL Subcontract # ZAX-8-17647-14.

Summary

Work focused on reducing the cost per watt of Cz silicon photovoltaic modules under Siemens Solar Industries' DOE/NREL PVMaT 5A2 phase I subcontract is described in this report. Work on cell thickness reduction, the required electrical and mechanical changes to accommodate these thinner cells, the improvement of electrical efficiency, larger ingot production, and the reduction of chemical waste are described in this report. The status of the program is shown in table i, where the major tasks of proving 14% efficiency, 200 mm ingot production and the re-use of recycling of slurry materials are all demonstrated.

Table i. Program Plans and Results
Phase I Complete

	Phase I 1st Year	Phase II 2nd Year	Phase III 3rd Year
Thin Cell	16% efficient 125 micron prototype cells ***95% complete***	16.5% efficient 125 micron prototype cells	17% efficient 125 micron production cells
200 mm Product	12 " section of ingot sliced into wafers ***95% Complete Ingot Grown***	Prototype cells and modules	4.5 Watt Cell in pilot production
Recycling and Reduction of Chemicals	10% increase of slurry materials recycling and re-use ***Complete***	20% increase of slurry materials recycling and re-use 13% reduction in caustic waste	50% increase of slurry materials recycling and re-use 70% reduction in caustic waste

Table of Contents

Table of Figures

Introduction

Program Goals

The Photovoltaic Manufacturing Technology (PVMaT) project is sponsored by the U.S. Department of Energy (DOE) through the National Renewable Energy Laboratory (NREL) in order to assist the photovoltaic industry in improvement of module manufacturing and reduction of module manufacturing cost. The objective of the DOE/NREL PVMaT subcontract with Siemens Solar Industries (SSI) is to continue the advancement of Siemens Solar Industries' photovoltaic manufacturing technology in order to achieve a 30% reduction in module cost per watt at the end of three phases of work. Each phase lasts a year as shown in Table 1. Phase I of this subcontract began in June of 1998. The program addresses the reduction in cost per watt with a three part development contract: a significant reduction in wafer thickness from approximately 400 microns at the start of the program to a finished cell thickness of 125 microns at the end of the three years, a significant increase in the size of the cells produced up to 200 mm diameter, a significant reduction of the use of slurry materials, and a 70% reduction in caustic waste.

Table 1. Goals of Siemens Solar Industries' PVMaT 5A2 Subcontract from DOE/NREL

	Phase I 1st Year	Phase II 2nd Year	Phase III 3rd Year
Thin Cell	16% efficient 125 micron prototype cells	16.5% efficient 125 micron prototype cells	17% efficient 125 micron production cells
200 mm Product	12 " section of ingot sliced into wafers	Prototype cells and modules	4.5 Watt Cell in pilot production
Recycling and Reduction of Chemicals	10% increase of slurry materials recycling and re-use	20% increase of slurry materials recycling and re-use 13% reduction in caustic waste	50% increase of slurry materials recycling and re-use 70% reduction in caustic waste

Approaches

The first step toward reducing cost in this PVMat 5A2 program at SSI is to reduce wafer thickness. In PVMat 4, wafers were made larger at 150 mm in diameter. This wafer has the potential to be the lowest cost wafer as the Cz growth process produces round ingot. This wafer is the best candidate to make thinner, however the yield losses at 150 micron thickness have been found to be excessive. For this reason, the approach has been a two step reduction in thickness, from 385 microns to 250 micron cells, and then from 250 microns to 125 micron cells during Phase II.

The larger cells are made, the lower the potential dollar per watt manufacturing costs. SSI has initiated the development and growth of 200 mm ingot to be fabricated into wafers and eventually cells. These larger cells continue to show the best cost structure as it optimizes the watts per kilogram consumed in producing the cells. Module designs for lower cost contribution have been started.

Hazardous waste reduction is attacked in two ways, the largest consumable item aside from polysilicon is Silicon Carbide (SiC) used in the wafer slicing process. This SiC use can be reduced significantly through recycling and re-use. This program approach is well underway at SSI. The largest hazardous waste volume at SSI is the caustic waste generated in the wafer etching processes. The reduction of this waste will be accomplished using subcontractors with extensive environmental compliance experience such that the solution is driven by best available techniques, lowering operating cost as a secondary motive.

These three areas of focus, thinner cells, larger cells and modules and hazardous waste reduction have the potential of reducing cost by approximately 30% per watt.

Thin/High Efficiency Cells

Thinner Cells

This section describes the work done on producing thinner cells in high volume manufacturing. This work has proceeded based on work done in PVMat 4 which focused on yields and improved module designs. In analyzing costs during this program, it became apparent that a significant cost reduction opportunity lay in making wafers and cells thinner. With the nature of the Czochralski process for producing ingots, or for cast Silicon for that matter, the slicing operation of wafers determines the productivity of the ingot used in making solar cells. In simple terms, the more wafers obtained per length of ingot, the more watts produced per ingot produced. The breakdown of costs is shown in Figure 1 which totals 50% of cumulative cost by the time a wafer is produced. If this wafer can be cut thinner, the 30% cost incurred at the ingot level can be reduced in total percentage.

Figure 2 shows the percent reduction possible for thinner wafers referenced to 315 micron thickness, moving down to 150 micron thickness. Siemens Solar started PVMat 5A2 with wafers on one product, the 103 mm wafer, at 315 microns, and with two products, the 125 mm wafers and 150 mm wafers at 385 microns cut thickness. For the two larger wafers, the savings would obviously be increased, from 16% savings to over 25% savings, provided no yield is lost in wafering, cell fabrication, or module production. All savings assume a constant kerf loss in slicing wafers of 180 microns.

The motivation to go to thinner wafers is clear, more productive crystal growth, more watts produced in wafering, and a subsequent reduction in overall cost per watt. In addition to yields needing to be maintained to get the full advantage of these thinner wafer cost reductions, the electrical performance of the cells must be maintained.

As Cz cells are made thinner, the cells require a Back Surface Field (BSF). Figure 3 shows the performance of thinner cells with and without a BSF process addition. As can be seen from the chart, making thinner cells drops the power up to 15% if no BSF is applied. The upper curve shows the performance improvement with a BSF which not only recovers the lost performance, but enhances it by as much as 10% electrically.

The challenge of yield is a large one. Figure 4 shows the potential gain in cells at 100% yield in moving from 400 micron wafer thickness to less than 150 microns. The chart shows four lines, the theoretical maximum cell gain on the top, followed by the yielded cell data for the 103 mm, 125 mm, and 150 mm wafers produced at SSI. This work was started under PVMat 4 and showed that it is not certain that yields can be maintained. The chart shows that for a given amount of ingot, the potential productivity gain is as high as 180%. As can be seen from the bottom three lines, however, as the cells get thinner and get larger, the yield losses are greater. This experiment is a compilation of work done in wafer slicing (Figure 5), and cell fabrication (Figure 6), which shows the same trend lines, the yield of wafers and cells less than 250 microns thick suffer dramatically. For this reason, SSI chose to work on the largest wafers first, the 150 mm (6 inch) diameter wafers. The starting point for change was chosen to be 250 microns, to first implement thinner wafers, then move to a 150 micron wafer as a subsequent step.

This challenge of thinner wafers is solely a challenge for the solar industry. The semiconductor industry has solved making larger diameter wafers at high yield by continuously increasing the wafer thickness.

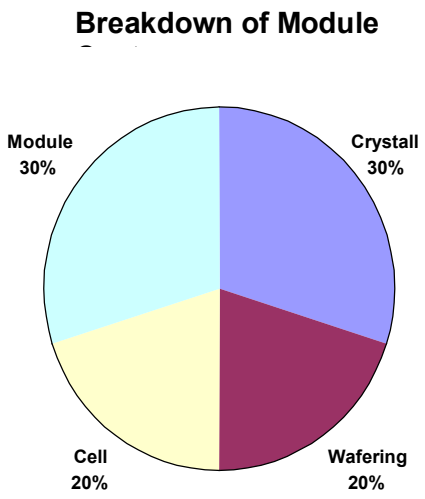

Figure 1. Cost of Cz Manufacturing

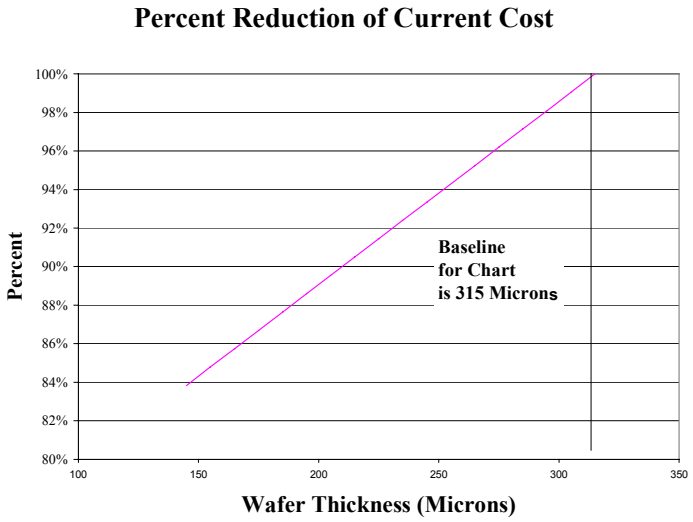

Figure 2. Cost Reduction vs. Wafer Thickness

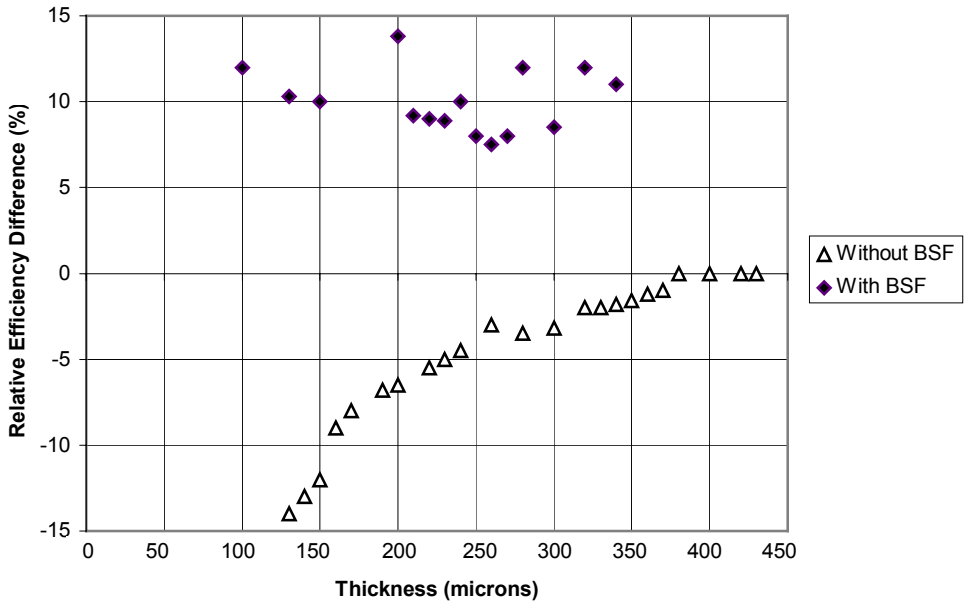

Figure 3. Cell Electrical Performance vs. Thickness

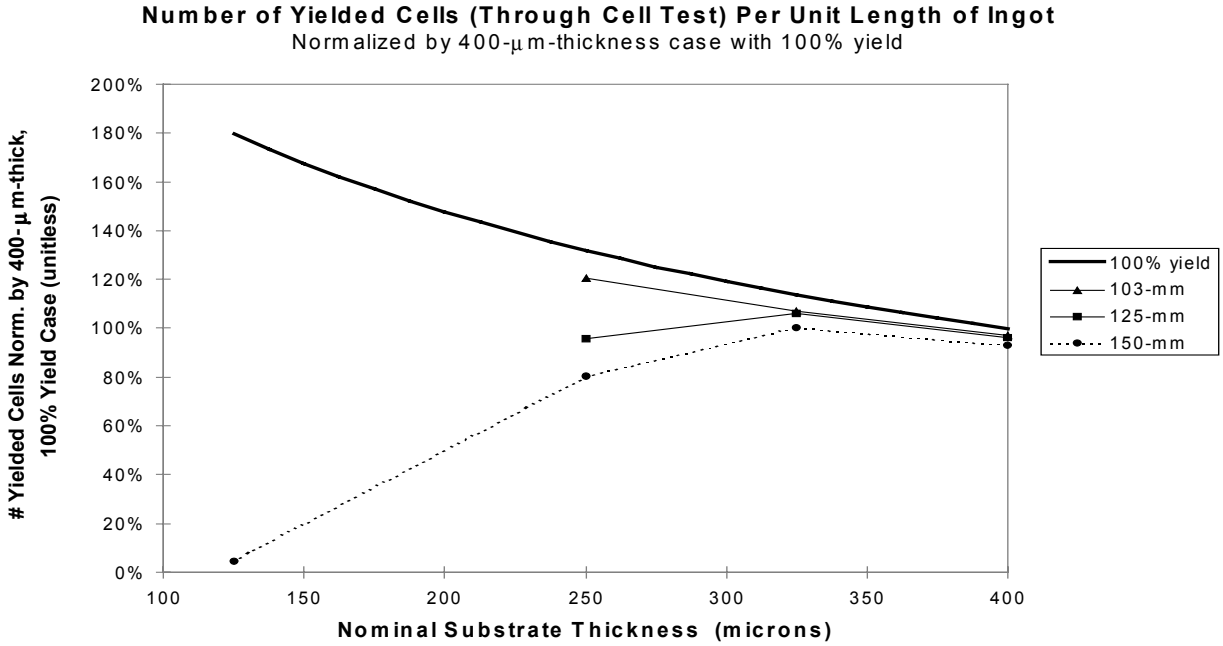

Figure 4. Increased Productivity vs. Yield

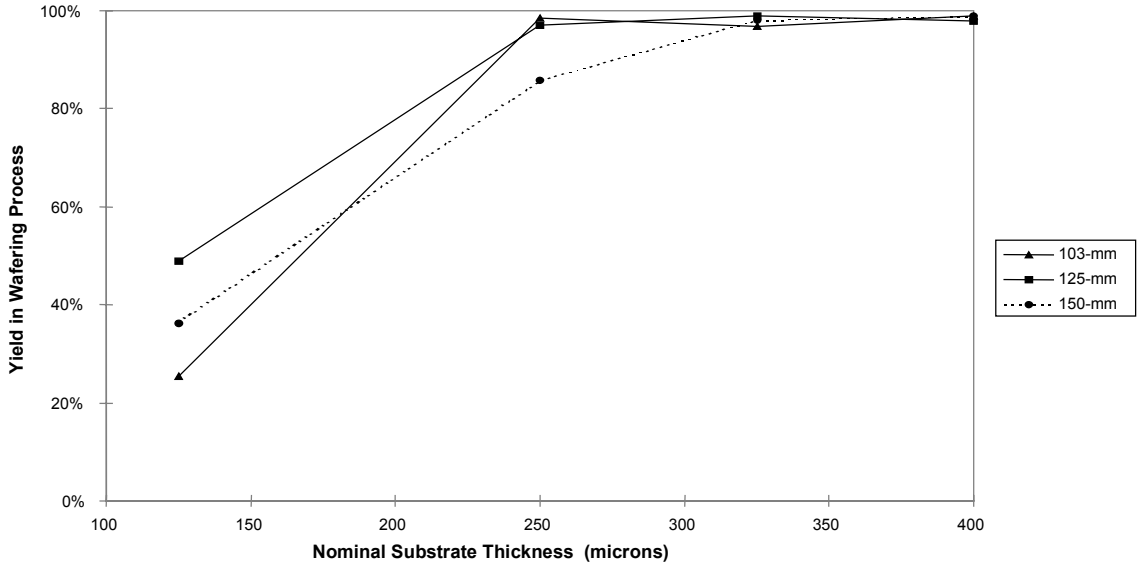

Figure 5. Wafering Yield vs. Size and thickness

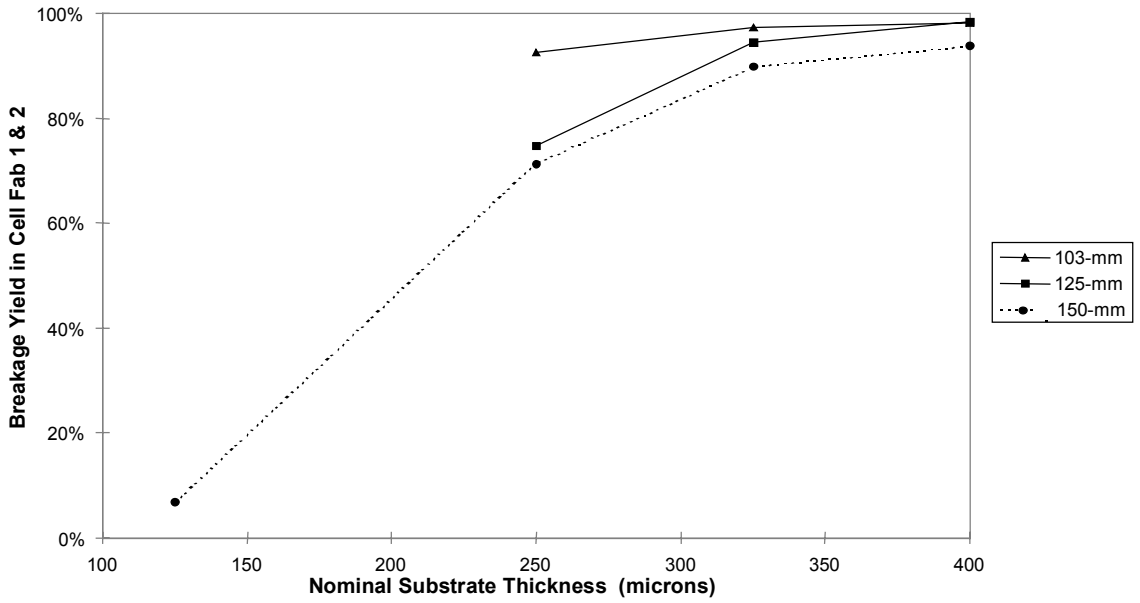

Figure 6. Cell Yield vs. size and thickness

Figure 7 shows fracture force vs. wafer thickness, obviously increasing force as the wafers get thicker. The thickness range for solar cell makers is shown on the left hand side of this graph, amplified in Figure 8. Figure 8 also shows that the wafer bow is increased as the thickness is decreased up to fracture. This bow may be a benefit when handling ultra-thin wafers.

To improve the yield of thinner cells, several things have been initiated by SSI. The use of a different type of crystal structure, tri-crystal, has shown a benefit in strength when compared to Cz wafers. Figure 9 shows a simple test run with different wafers, treated with different damage etch conditions, tested for breakage at 320 microns thick. As can be seen from the chart, the tri-crystal wafers have shown the highest fracture strength of wafers tested. Another confirmation of tri-crystal strength was shown in an experiment of 100 micron wafers through the processing line. Figure 10 shows the percentage broken in the test, with tri-crystal wafers breaking 10% less in total, mainly in the wire saw process where the wafers are weakest.

In producing 150 mm cells at 250 microns thick, a series of tests were run to look at ingot contribution to breakage. Figure 11 summarizes a test where wafers were pulled at random and tested for breakage strength, these were identified as a control lot of wafers. Two additional sets of wafers were tested, a population of wafers which exhibited “oil canning” or non-flat wafers which were stressed in the crystal growth process, and a population of wafers adjacent to a broken cell in ingot position. As can be seen by the Weibull plot in Figure 11, no significant difference was seen between the control wafers and wafers adjacent to broken cells. The control wafers and adjacent wafers were very similar in breakage strength, the oil canned wafers were weaker overall, however, not significantly so.

In another effort to reduce breakage, a series of experiments were performed on several lots of 150 mm, 250 micron cells throughout the process line. Figure 12 shows the breakage for a control lot, an edge ground lot, a non-edge ground lot, wafers from vendor 1, and from vendor 2. As can be seen in the chart, vendor 1 and vendor 2 wafers exhibited the most amount of breakage, while the edge ground SSI wafers showed the least amount of breakage. The data is summarized in a simpler chart, Figure 13, which shows the influence of edge treatment on percent broken in the process line. SSI’s standard process has 5% more yield loss than those of edge polished wafers, which is a semi-conductor edge treatment process. The rough edge and moderately smoother edge surfaces were found to be the use of non-compliant ingot smoothing tools at the vendor factory. An investigation of the viability in cost and productivity of edge grinding equipment has been initiated based on these test results.

Overall, the challenge continues to be reduction in wafer thickness being offset by yield losses. The losses shown in Figures 10 and 12 can be offset with better handling tools. This effort is described later in this report. SSI has moved the production of 150 mm cells to 250 microns thickness, and introduced a back surface field which is also described later in this report. Yield issues continue to be the biggest focus in stabilizing the process at this thinner value. The yield effort will be addressed in more detail in Phase II.

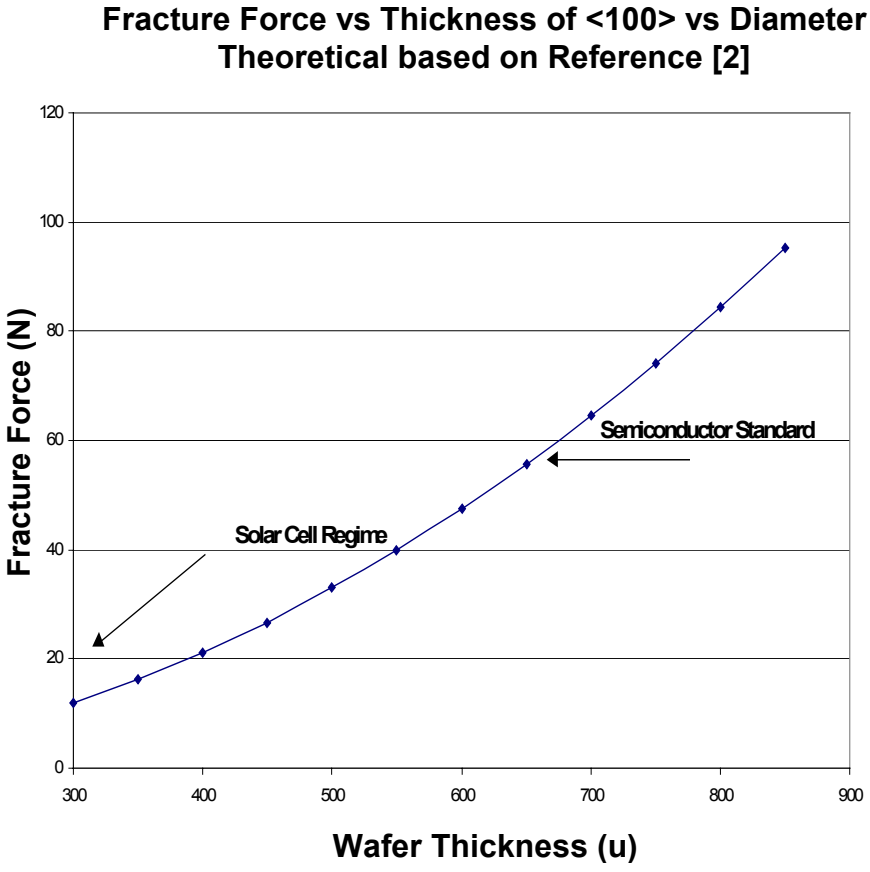

Figure7. Fracture Force vs. Wafer Thickness

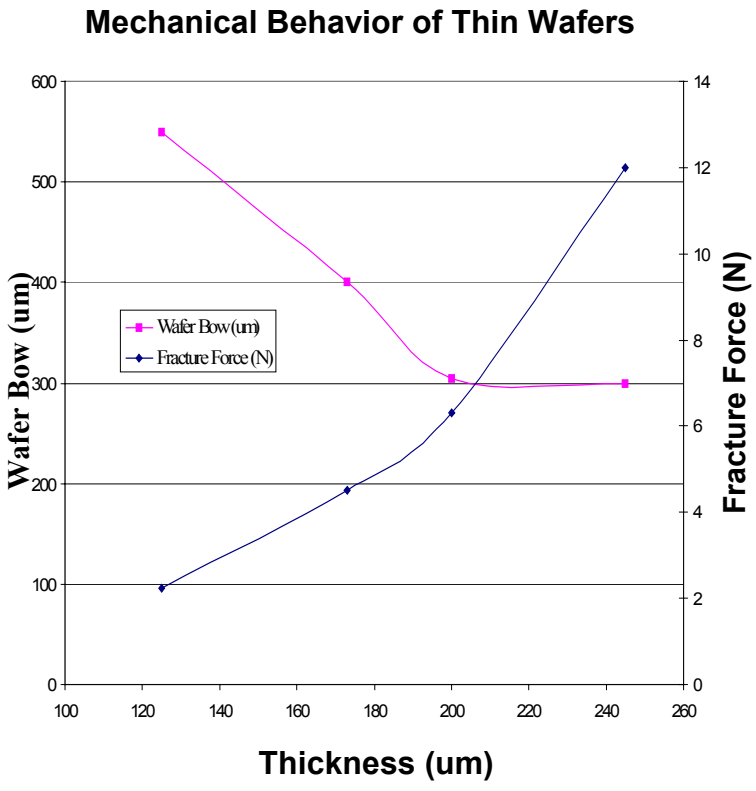

Figure 7. Thin Wafer Behavior

Influence of Material/Processing on Wafer Strength
(100 samples/test, size10x10cm^2, 320um thick)

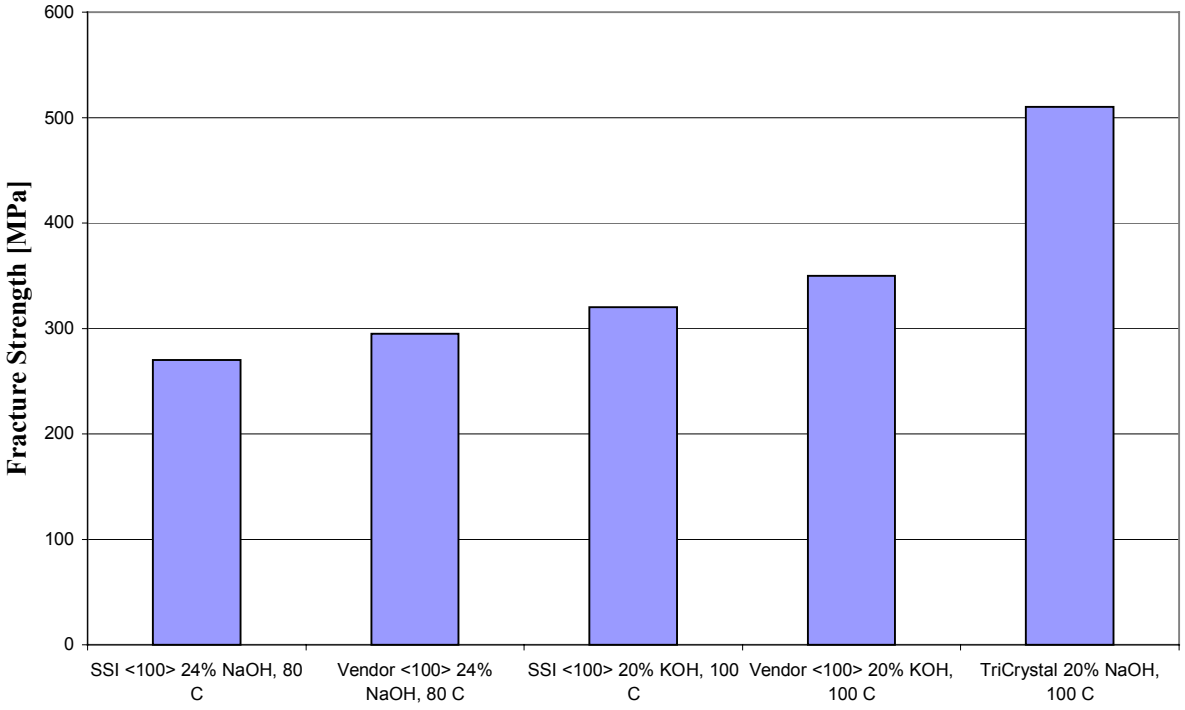

Figure 9. Tri Crystal Test

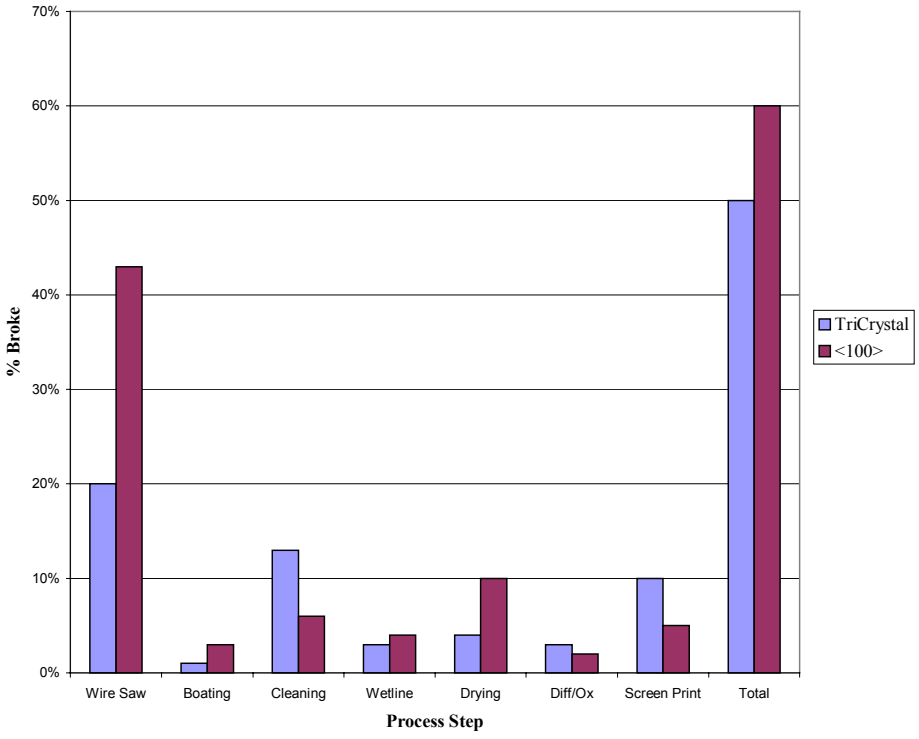

Figure 10. Tri Crystal Yield in the Process Line

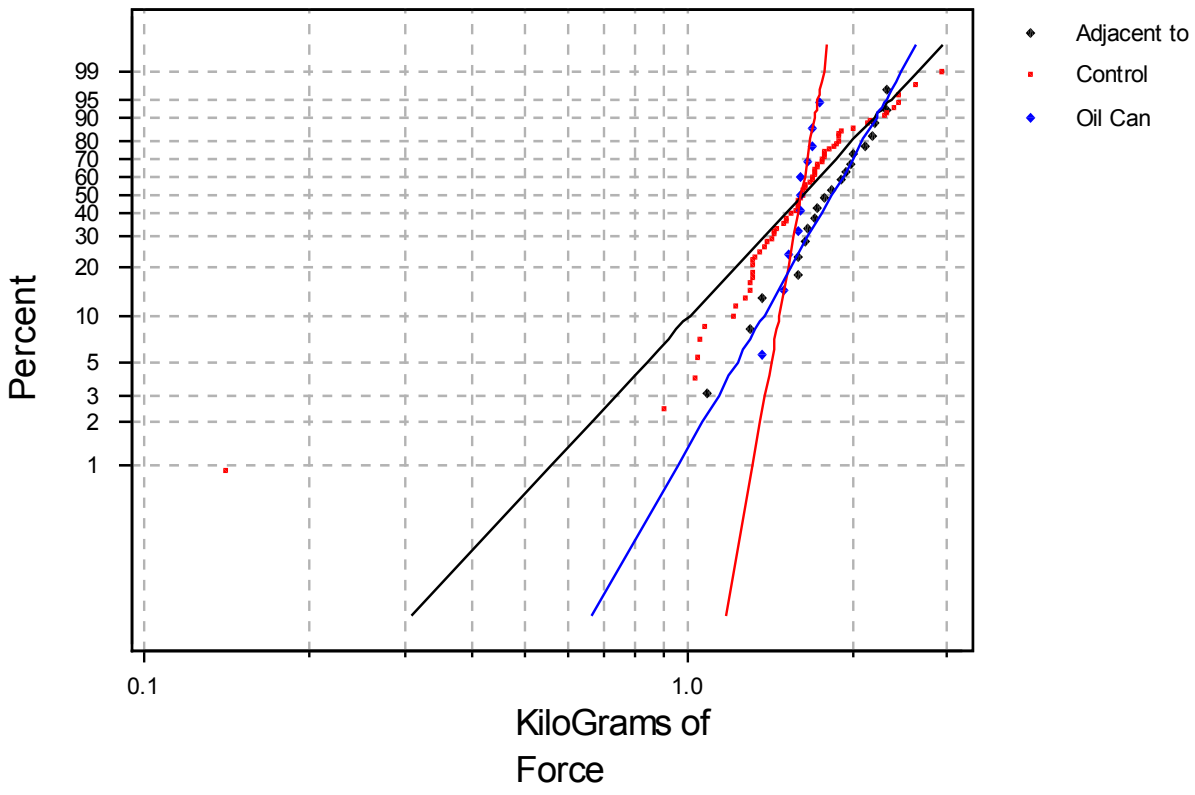

Figure 11. Weibull Plot of Wafer Strength Test vs. Ingot Position

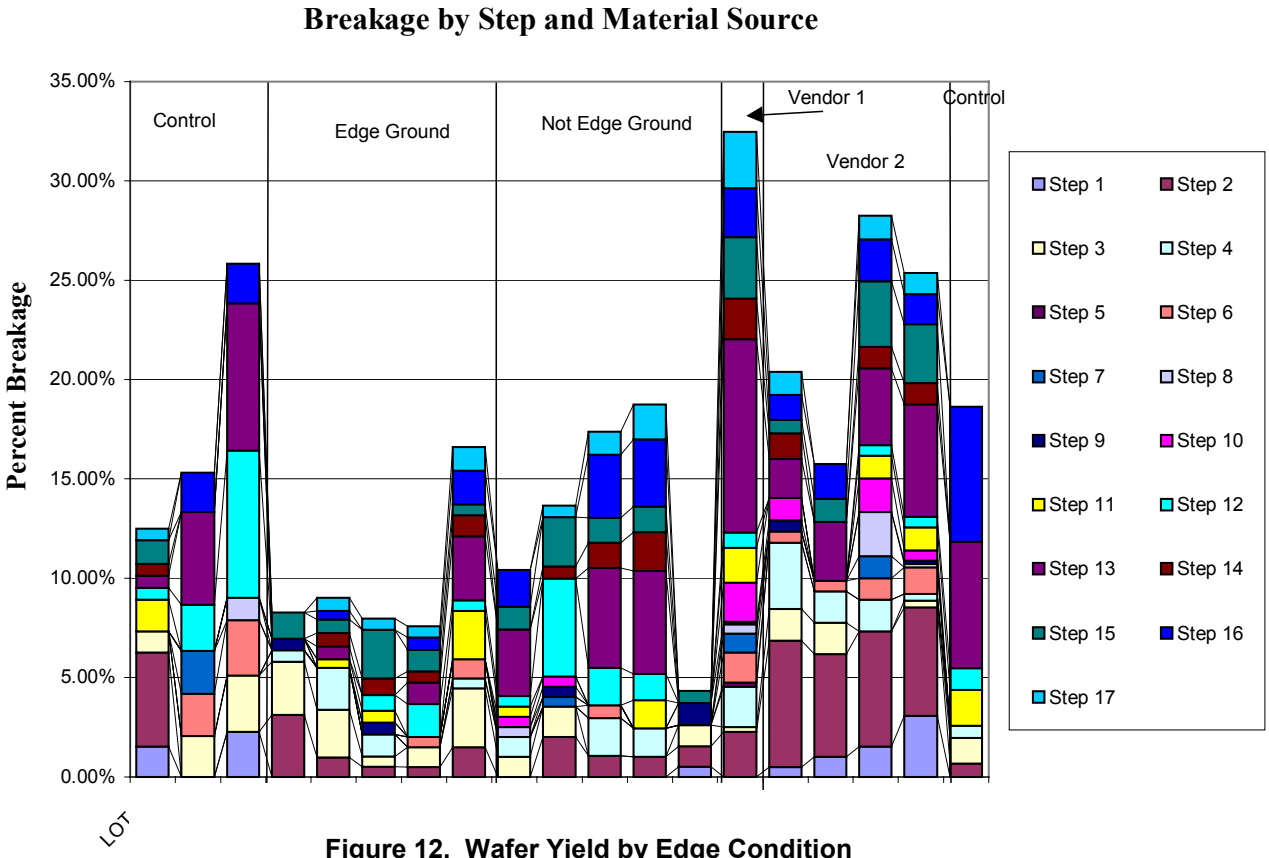

Figure 12. Wafer Yield by Edge Condition

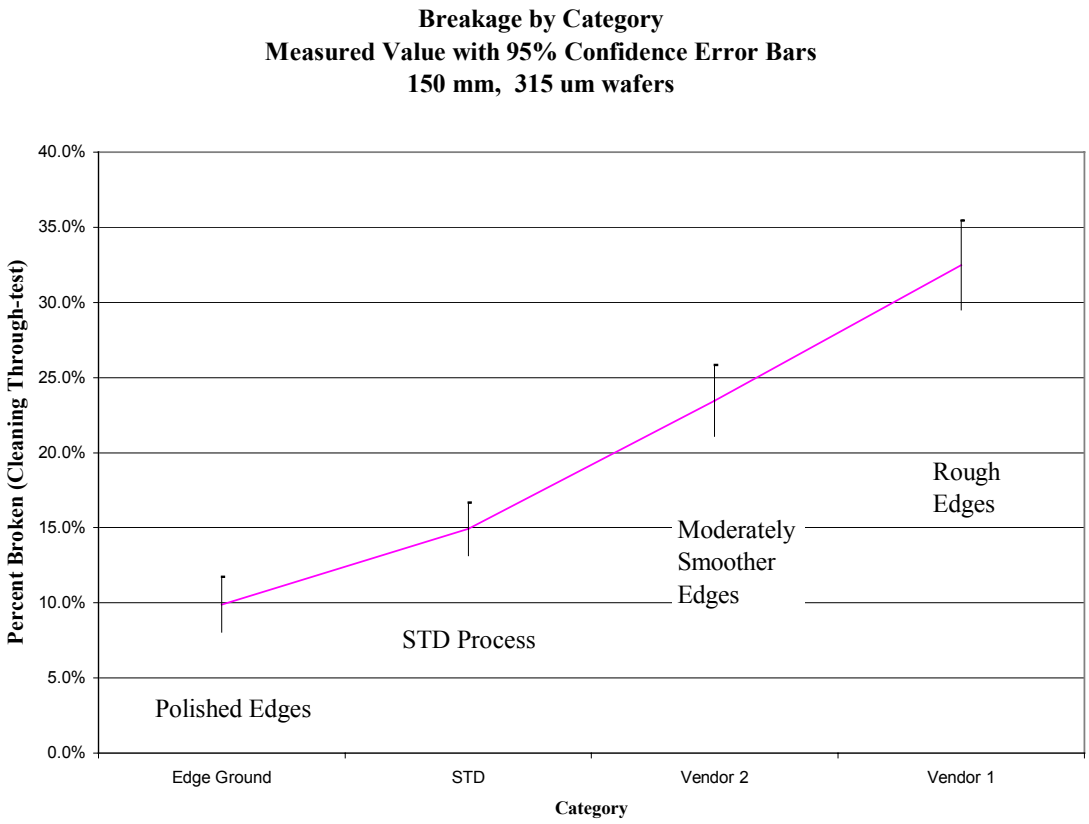

Figure 13. Breakage by Edge Condition

Tri-Crystal

Work on tri-crystal has progressed in our Vancouver facility. Figure 14 shows work on experiments to obtain defect free lengths (DFL) of crystals up to and exceeding 400 mm in length. As can be seen from the chart, defect free lengths are averaging between 200 and 300 mm. Experimentation is currently focusing on slowing the pull speed, slowing the necking and tailing procedures, and overall control during the growth of the crystal.

The investigation of tri-crystal growth records showed that the crucible position unintentionally was not held constant throughout the initial experiments. The analysis of the growth data showed that a lower crucible position is significantly more favorable for tri-crystal growth. As the cone growth experiments had been carried out at the higher crucible position, a new series of experiments was started focusing on the growth at lower crucible positions with thin fast necks and predefined cone shapes. These runs yielded ingots of record high structural quality: ingots of a 400 mm length with DFL of 330 mm and 1% visible defects as well as two long (525 mm/580 mm) ingots with DFL=305 mm to 315 mm and 15% visible defects at the tri-crystalline bottom. The process performance is shown in Figure 15 where longer DFL or defect free length is preferred.

The growth of tri-crystal ingots continues in our Vancouver facility, with the focus on runs with heat shields and multiple recharges.

Wafers sliced from Vancouver grown tri-crystal runs at 250 microns thick have been produced with greater than 97% slicing yield. Slicing of 150 micron wafers will be done during Phase II.

The first cell results have been obtained with tri-crystal cells. The basic process used was the same as a standard Cz process which includes no back surface field effect. The expectation is that the tri-crystal cells would have lower electrical output due to the fact that the pyramid surface texture of Cz wafers cannot be performed on the tri-crystal wafers.

The experiment with tri-crystal cells focused on a control lot, along with multiple experiments on firing these tri-crystal cells. The wafers were cut at 250 microns and processed through the standard Camarillo cell process. The results are shown in Figure 16 where four groups, textured single crystal cells, untextured single crystal cells, textured tri-crystal cells and untextured tri-crystal cells are compared for Ivr or test current at .484 volts

The results show that the tri-crystal is 0.24 amps lower than the single crystal cells. A test was run to laminate these cells in module packages to see if any additional light trapping can offset the lack of pyramid structure on the tri-crystal cells.

The cells made from tri-crystal wafers showed no significant differences in power after lamination whether texture etched or not.

More recent testing of tri-crystal cells with BSF processing yielded cells greater than 14% efficient. Pilot runs of tri-crystal cells with BSF processing will be conducted during Phase II of the program.

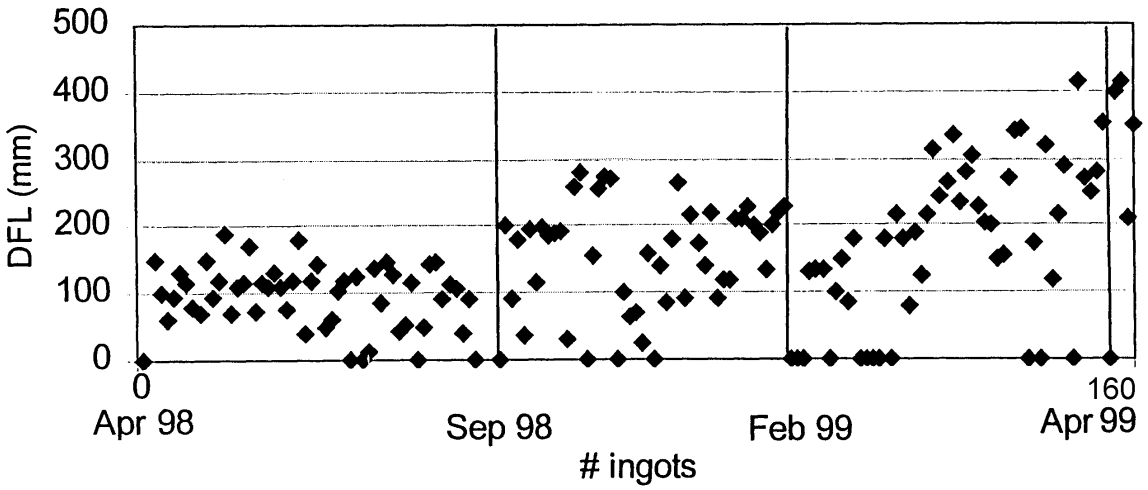

Figure 14. Defect Free Length over Time

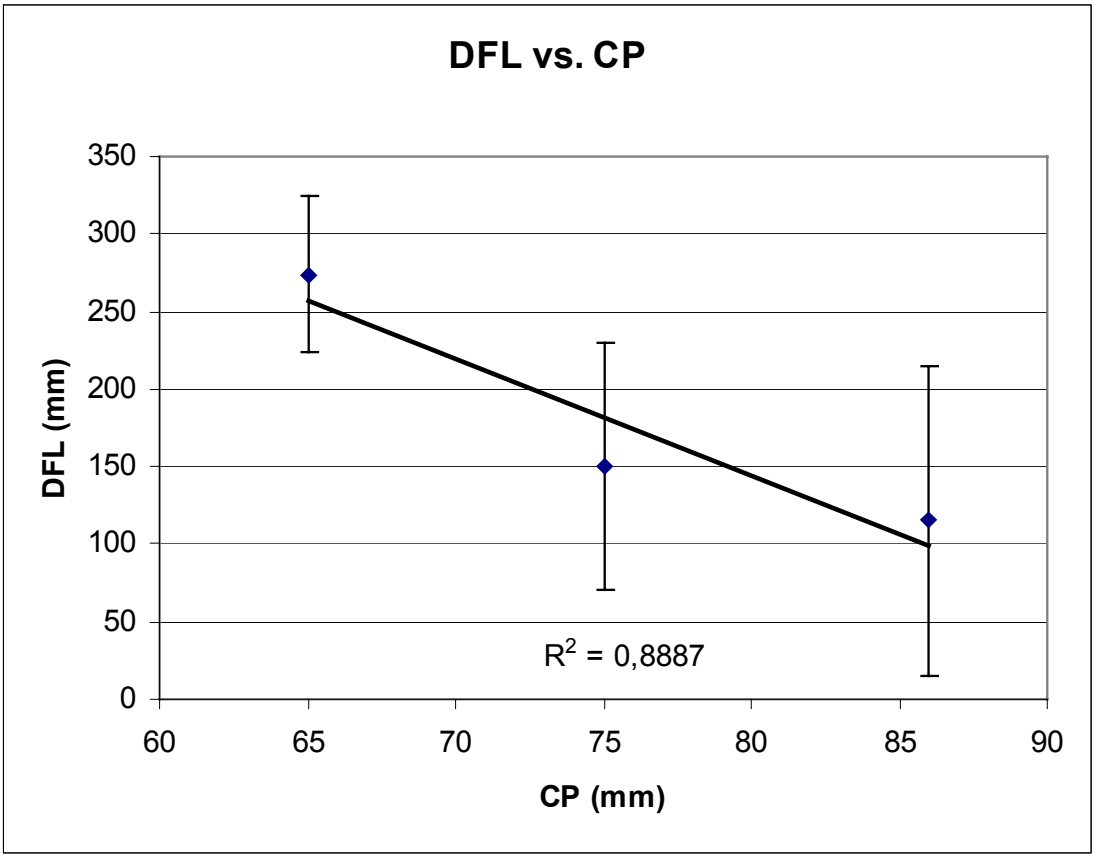

Figure 15. Defect Free Length vs. Crucible Position (CP)

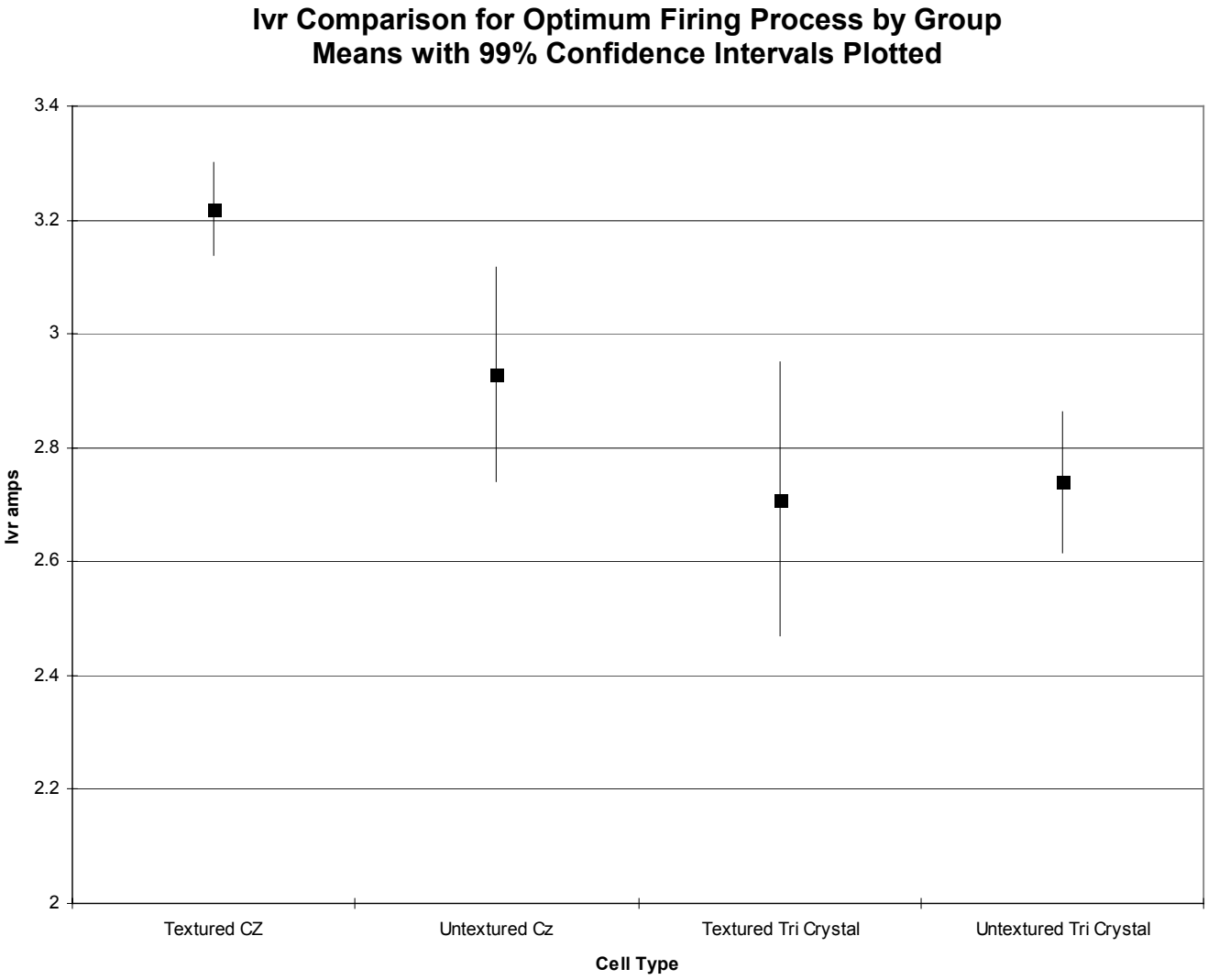

Figure 16. Tri-Crystal Cell Performance in First Test

Back Surface Fields in Production

Testing of back surface field processes have been done during Phase I of the program. Two types of BSF processes have been worked, a Boron BSF process, and an Aluminum BSF process. Both processes and the results to date are described here.

Boron BSF processes are accomplished in SSI using a spin on dopant source, then a drive in process in quartz diffusion tubes. This process has yielded cells greater than 16% efficient in lab scale testing, and over 15.5% in pilot production. In working with thinner cells, the requirement for a BSF has been outlined above, and SSI implemented a Boron BSF process on it's thin 250 micron 150 mm cells, beginning in the July/August time frame of 1998. The electrical distribution is shown in Figure 17 by month, and shows the significant gains in type 1 and type 2 (higher electrical bin values) as the process was better understood and training of all shift personnel was accomplished. As with most production start-ups, there were several bad runs, but the details of the process are stable now. Over 700,000 cells have been processed using this Boron BSF process to date, and SSI intends to continue this process with it's 150 mm product.

The environmental data for the Boron BSF is shown in Table 2, which shows the passing of all tests with these modules. This test confirmation has been repeated more than five times in the last year with results similar to those in the table.

Experiments on various aluminum pastes for creation of a back surface field have been done with good success. Figure 18 shows the test current for populations of cells, which have been run in production furnaces under engineering control. The advantage of the aluminum paste over the Boron spin on approach is the availability of equipment already on the manufacturing floor, and the simplicity of a print and fire process compared to a diffusion process addition. This histogram represents an approximate 5% gain in efficiency relative to the standard non-BSF process.

The testing of pastes showed the performance enhancing effect of the aluminum back paste with the Ferro fritted Al back paste, #53-034 performing 0.24 amps better on average than the standard paste and the Ferro fritted Al, optimized for 800-900^{o}C, performing 0.19 amps better.

The beneficial effect on the Ivr is the result of the improved Isc and Voc and a reduction in the leakage current.

The Aluminum BSF process has been optimized with redesigned screens, the data of more recent testing shown in Figure 19, this time giving a 6% relative gain in efficiency. Optimizing Isc was done looking at belt speed and screen mesh. Figure 20 shows Isc vs. belt speed for two different screen meshes. The 325 mesh was chosen, with a belt speed in the range of 9.5 feet per minute.

The aluminum backed BSF modules have been submitted to environmental testing. Figures 21 and 22 show the Damp Heat (85/85) test results for control modules and the aluminum BSF modules respectively. The controls and the test modules behaved the same, which confirms the use of the Aluminum BSF process on modules. This test has been repeated again with the same results. The Aluminum backed cells in modules pass all of the environmental tests.

Work continues on Boron BSF process in a run-off with the Aluminum paste process. The Boron process is working in pilot production giving 6-8% more power per cell. The biggest problem encountered thus far is the wrap around of boron on the front surface of the cell. Set up of the spin coater is proving to be a critical item for operations personnel.

The Aluminum is more compatible with production processes which SSI is familiar with, however, the Aluminum has some draw backs with ultra-thin cells which tend to warp with Aluminum paste applied on the back. Soldering on the back of Boron BSF cells is very easy compared to the Aluminum/Silver pad combination.

Another issue with the BSF process is the slicing of thinner wafers. The yield for the wafering process slicing 150 mm wafers is still 8% below the comparable yields for thicker wafers. Additionally, cell fab yields continue to be a challenge with thin cells. Work to improve these yields is planned through better handling tools described below.

Boat to Boat System

A design and prototyping effort was started during Phase I to automate the boat to boat transfer operation, again a necessary step for transitioning to thin wafers and cells. Prototype boats and tooling have been ordered, and implemented in the SSI line. These new plastic and quartz boats support the wafers and cells more uniformly around the edges. They also allow for tighter tolerances on the outside dimensions which is required for automation tooling. The automation of the boat to boat transfer has been piloted in production using a system purchased from a semiconductor company. The system is shown in sketch form in Figure 23, with the details of the four boat stations shown in Figure 24. The principal operation of the machine is to take four boats at a time and transfer from plastic to quartz or from quartz to plastic. This is accomplished by “raising combs” which are shown in Figures 25 and 26 in more detail. These “combs” lift and transfer 25-35 cells at once with a gentle motion. The machine is intended to minimize contact with the edges of the cells, and to not have the cells bang into either boat surface. SSI will pilot this machine during Phase II of the program.

Auto Boating System

Wafering yields at Siemens Solar continue at approximately 97% for over 15 Million wafers sliced. The loss of 3% is dominated by breakage at the point where wafers are removed from the carrier piece of glass to which the ingot has been mounted. This becomes an even bigger problem as wafers are made thinner. The “boating” of wafers from glass support beam to plastic boats for cleaning is a messy and extremely labor intensive process. This process is also hard to control as it is all up to the operator dexterity and manipulation abilities of the individual. Preliminary design contracts have been let to two companies, Ensor Engineering and Wright Industries for auto boating design and prototyping. The approaches differ in the level or automation deployed. One is fully automated with removal and insertion into the plastic boat, and one approach is manual removal from the glass beam with automatic boat insertion. Design documentation has been received, and prototypes have been built. More work is required to allow for ingot separation and boat insertion. This work will be done during Phase II.

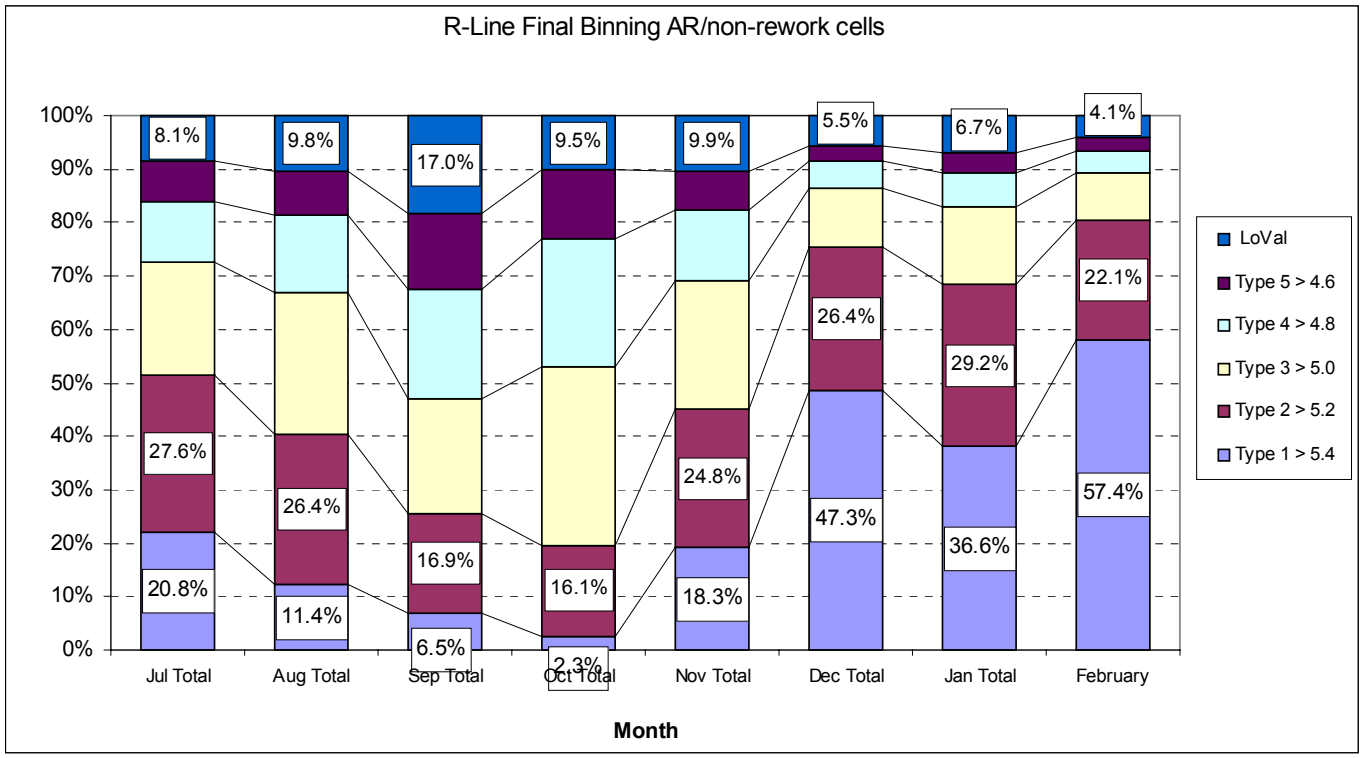

Figure 17. Boron BSF cell distribution over time

Table 2. Environmental Test Results of Boron BSF

T200	SerNo	Voc	Isc	FF	Vmax	Imax	Pmax	Cntl.Delta
Initial	**2**	22.22	6.33	72.69	17.64	5.79	102.20	
Post Test	T1	22.08	6.19	71.95	17.25	5.70	98.33	
%Change		-0.6%	-2.2%	-1.0%	-2.2%	-1.6%	-3.8%	-0.7%
Initial	**7**	22.03	6.03	73.12	17.50	5.55	97.15	
Post Test	T3	21.91	5.92	72.02	17.35	5.39	93.45	
%Change		-0.5%	-1.8%	-1.5%	-0.9%	-3.0%	-3.8%	-0.7%
Initial	**3**	21.96	6.06	70.15	17.19	5.43	93.34	
Post Test	T4	21.68	5.92	69.44	17.04	5.23	89.14	
%Change		-1.3%	-2.3%	-1.0%	-0.9%	-3.6%	-4.5%	-1.4%
T50,10HF	**SerNo**	**Voc**	**Isc**	**FF**	**Vmax**	**Imax**	**Pmax**	
Initial	**4**	22.20	6.14	72.86	17.88	5.71	102.20	
Post Test	T1	22.10	6.24	72.11	17.46	5.70	99.51	
%Change		-0.5%	1.8%	-1.0%	-2.3%	-0.2%	-2.6%	0.5%
Initial	**6**	22.48	6.22	73.87	17.91	5.77	103.40	
Post Test	T2	22.07	6.16	73.04	17.56	5.65	99.24	
%Change		-1.8%	-1.1%	-1.1%	-2.0%	-2.1%	-4.0%	-0.9%
Initial	**8**	21.78	5.93	71.91	16.94	5.48	92.86	
Post Test	T3	21.68	5.89	71.02	17.07	5.31	90.63	
%Change		-0.5%	-0.7%	-1.2%	0.8%	-3.1%	-2.4%	0.7%
Initial	**5**	21.76	5.83	70.96	17.10	5.26	90.01	
Post Test	T4	21.57	5.76	69.79	16.87	5.14	86.76	
%Change		-0.9%	-1.2%	-1.6%	-1.3%	-2.3%	-3.6%	-0.5%
DH1000	**SerNo**	**Voc**	**Isc**	**FF**	**Vmax**	**Imax**	**Pmax**	
Initial	**1**	21.92	6.06	73.07	17.38	5.58	97.02	
Post Test	T1	21.98	6.09	70.74	17.34	5.46	94.73	
%Change		0.3%	0.5%	-3.2%	-0.2%	-2.1%	-2.4%	0.8%
Initial	**9**	22.04	6.09	73.88	17.53	5.66	99.22	
Post Test	T3	21.98	6.01	71.64	17.24	5.49	94.65	
%Change		-0.3%	-1.4%	-3.0%	-1.7%	-3.0%	-4.6%	-1.5%
Initial	**11**	22.19	6.18	71.91	17.71	5.57	98.65	
Post Test	T4	22.00	6.05	69.86	17.47	5.32	92.96	
%Change		-0.9%	-2.2%	-2.9%	-1.4%	-4.5%	-5.8%	-2.6%

9/22/98
J. Coleman, G Xavier

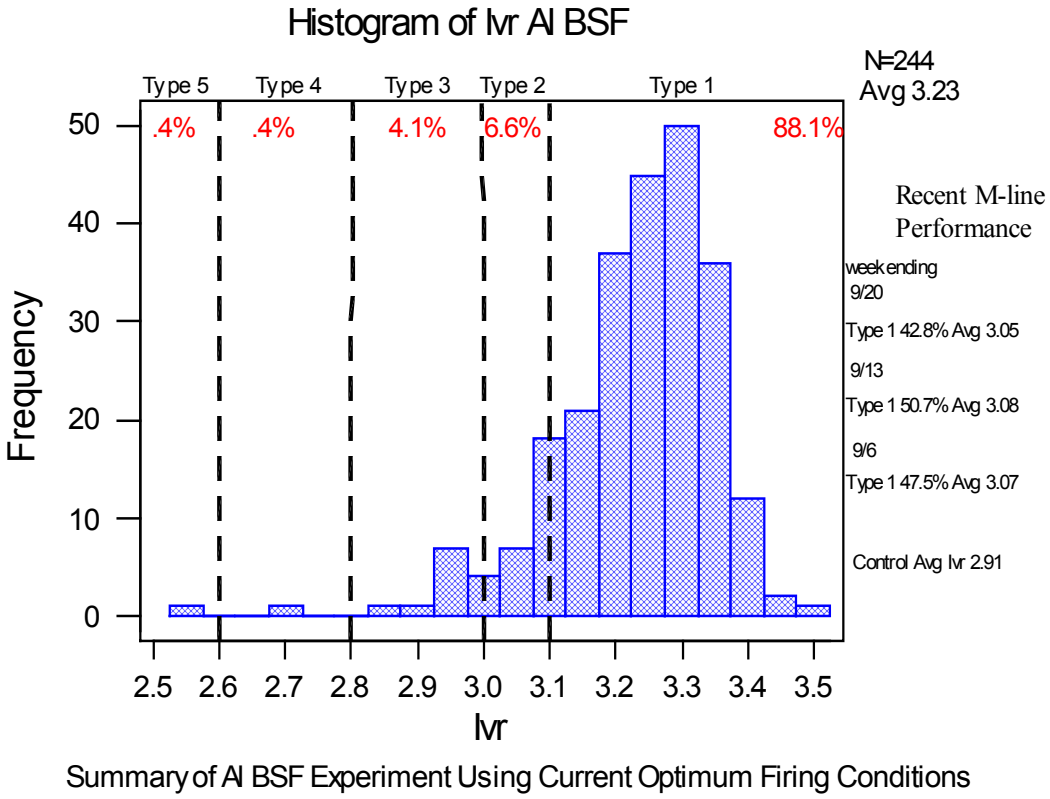

Figure 18. Aluminum BSF Performance

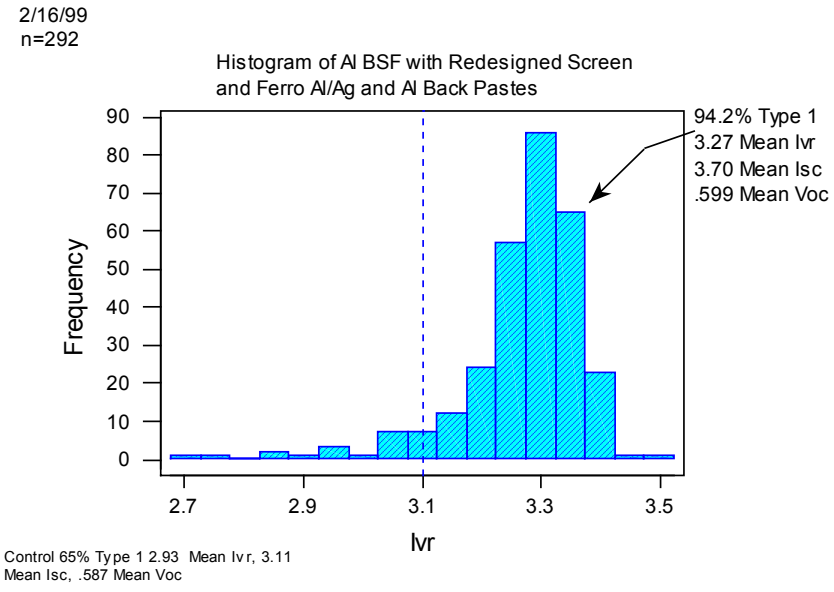

Figure 19. Aluminum BSF with Re-designed Screens

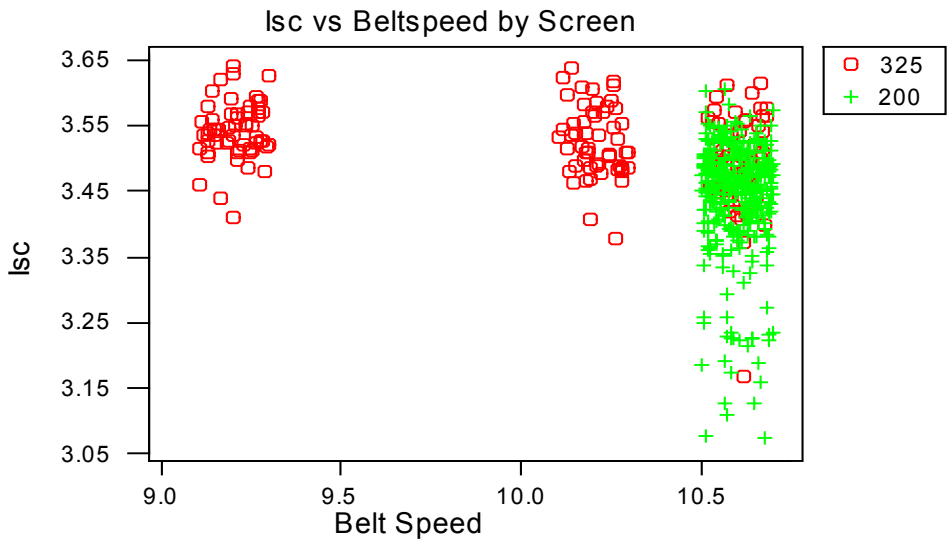

Figure 20. Isc vs. Beltspeed and Screen Mesh

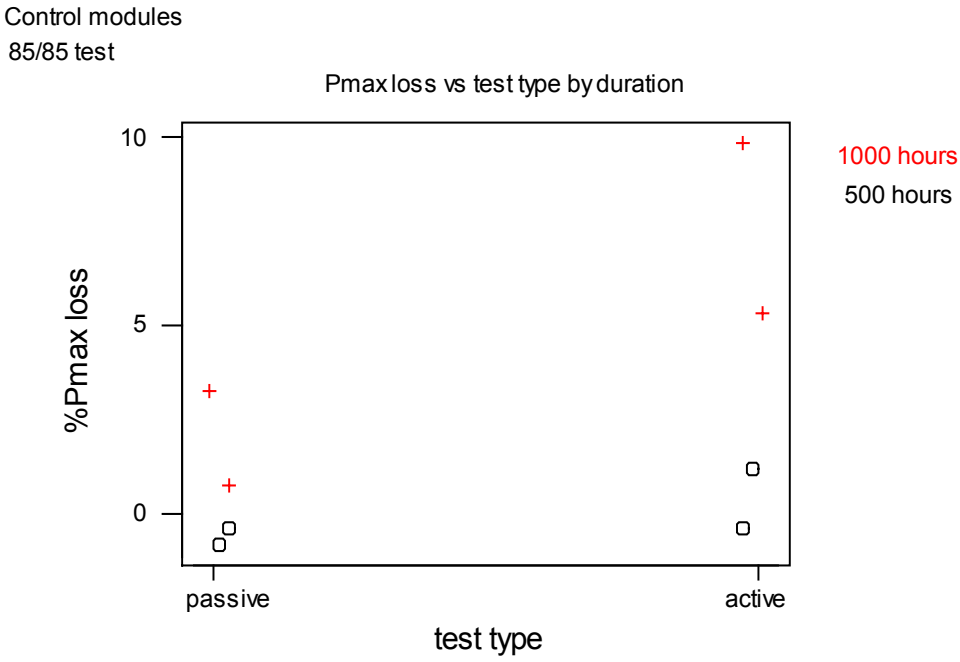

Figure 21. Pmax loss on Control Modules

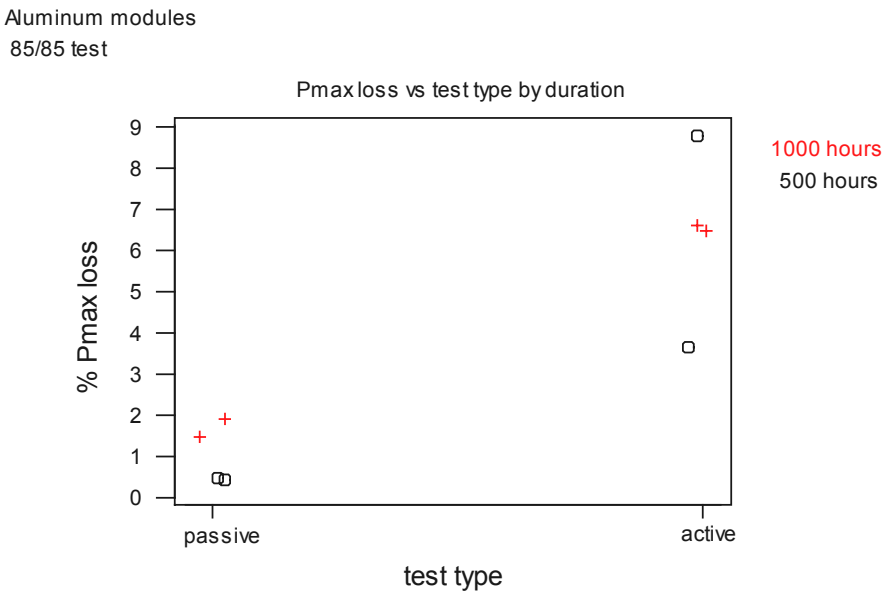

Figure 22. Pmax loss on Aluminum BSF Modules

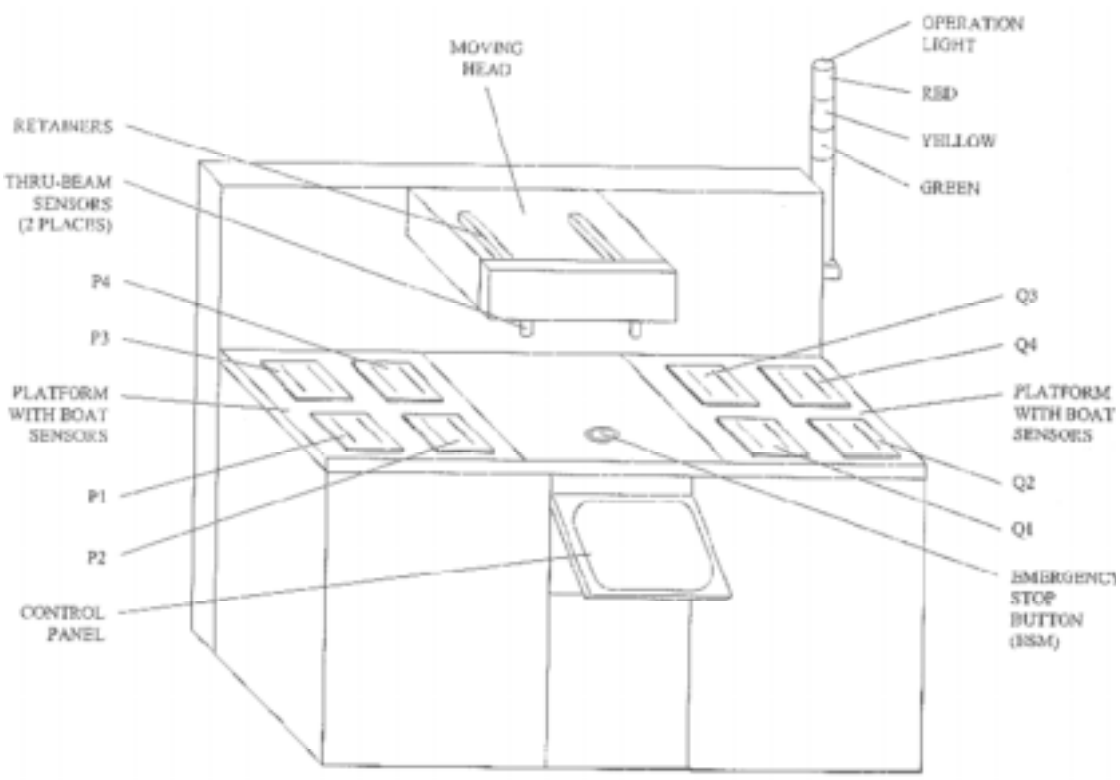

Figure 23. Sketch of Boat to Boat transfer tool

Figure 24. Four boat transfer Bench

Figure 25. "Comb" Transfer Arm

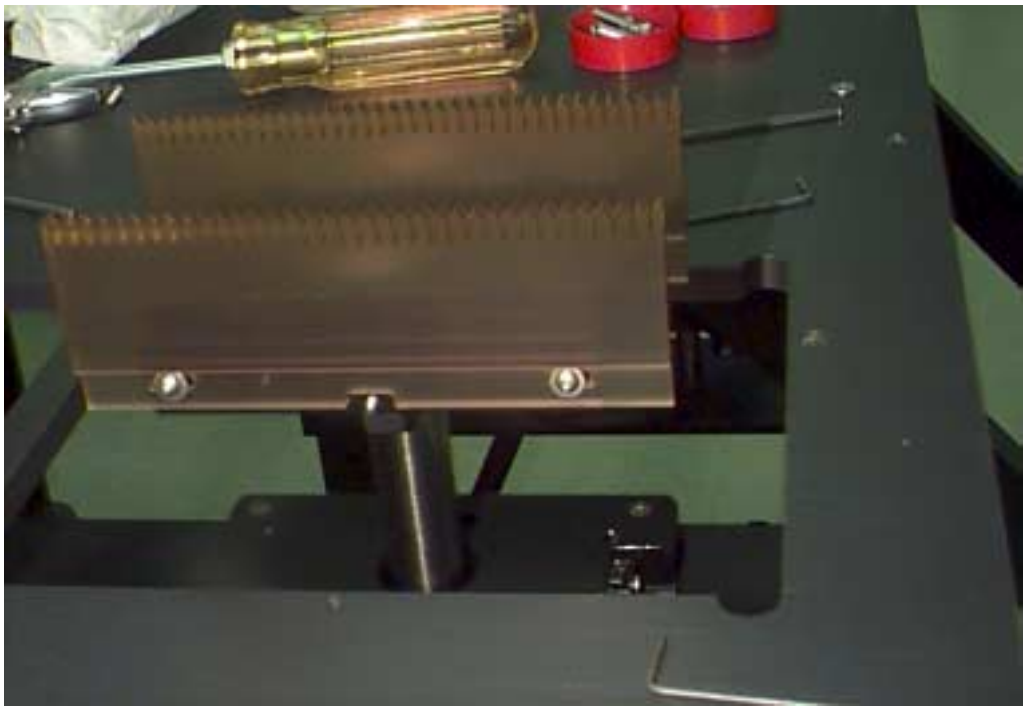

Figure 26. Transfer Arm close up

Large Area Cells/Large Area Modules

200 mm Ingot Growth

The start of large area cells in Phase I was to attempt to grow 200 mm ingots in the crystal growers currently deployed by SSI. The ingot growth was successful with ingots being pulled in the automated CG6000 machines. The ingots, a sample of which is shown in Figure 27 and 28 were well formed and had good tops and tails. An ingot was shipped to NREL this spring as a deliverable under the contract.

Future work in this area has been hampered by the fact that the ingots are too big to shape in SSI's line. Outsourcing the shaping has been investigated and it is believed at the time of report writing that a suitable vendor has been found to shape the ingots.

The plan for phase II is to grow more ingots, and to shape and wafer them for cell production. Module layouts have been done as shown in Figure 29 which will be upwards of 160 Watts per module. As mentioned, ingot shaping has slowed the progress of this deliverable. More progress is planned in Phase II.

Figure 27. 200 mm ingot

Figure 28. Side view of 200 mm ingot

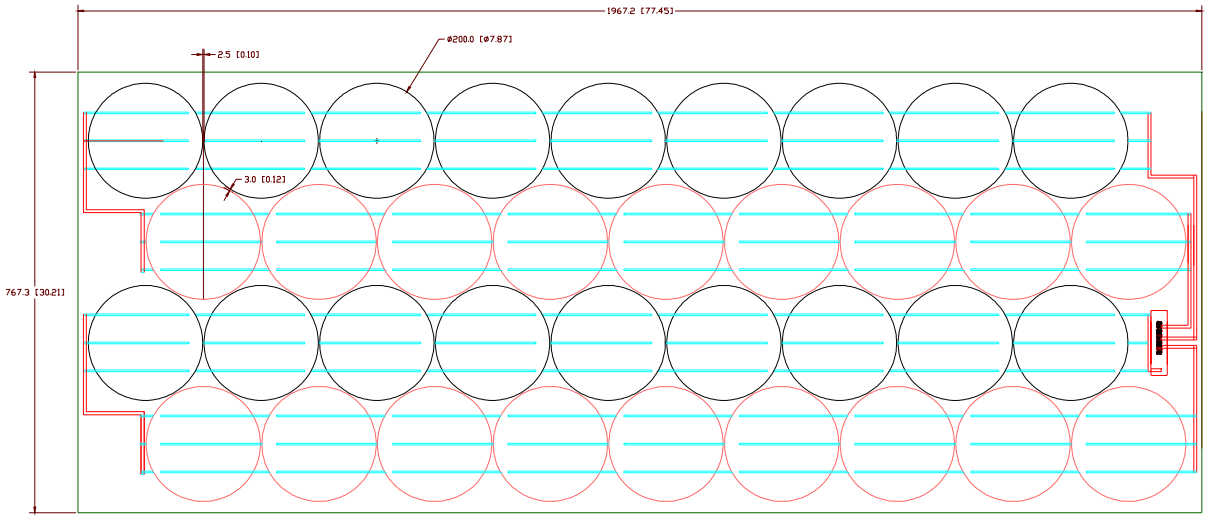

Figure 29. 160 Watt 200 mm laminate, 77 inches long by 30 inches wide

Hazardous Waste Reduction

Silicon Carbide Recovery

Silicon Carbide (SiC) is one of the highest dollar materials consumed in manufacturing at SSI. The recovery of SiC has a steep savings curve. Figure 30 shows the savings in dollars for three different production volumes, 720k, 820k, and 920k wafers per month. The net savings is shown vs. yield loss. At a run rate of 2 MW/month, the savings are in excess of $35,000 per month or approximately $450,000 per year net labor, machine cost and waste reduction.

A prototype system for recovery and re-use of Silicon Carbide was tested in PVMat 4, with good results on a small number of pilot wafering runs. A larger production system has been specified based on these tests for use in manufacturing. A leased system has been received from GTI in New Hampshire for pilot and production use. Based on the production data a permanent production system will be specified and purchased during the latter part of the contract.

The machine was started up at one run per day while data was gathered on wafering yield with this material use. Over 50,000 wafers were cut with comparable yields to the non-recycled SiC mixes. Figure 31 shows a statistical analysis of the recycled SiC runs vs. the non-recycled runs, where M is the M-line standard yield, P is the P-line standard yield, RM is recycled SiC yield for M-line, and RP is recycled SiC yield for P-line. As can be seen from the data, the mean yield is comparable on the M line (97.31 vs. 97.83), where the P-line showed a drop from 97.21 to 95.99.

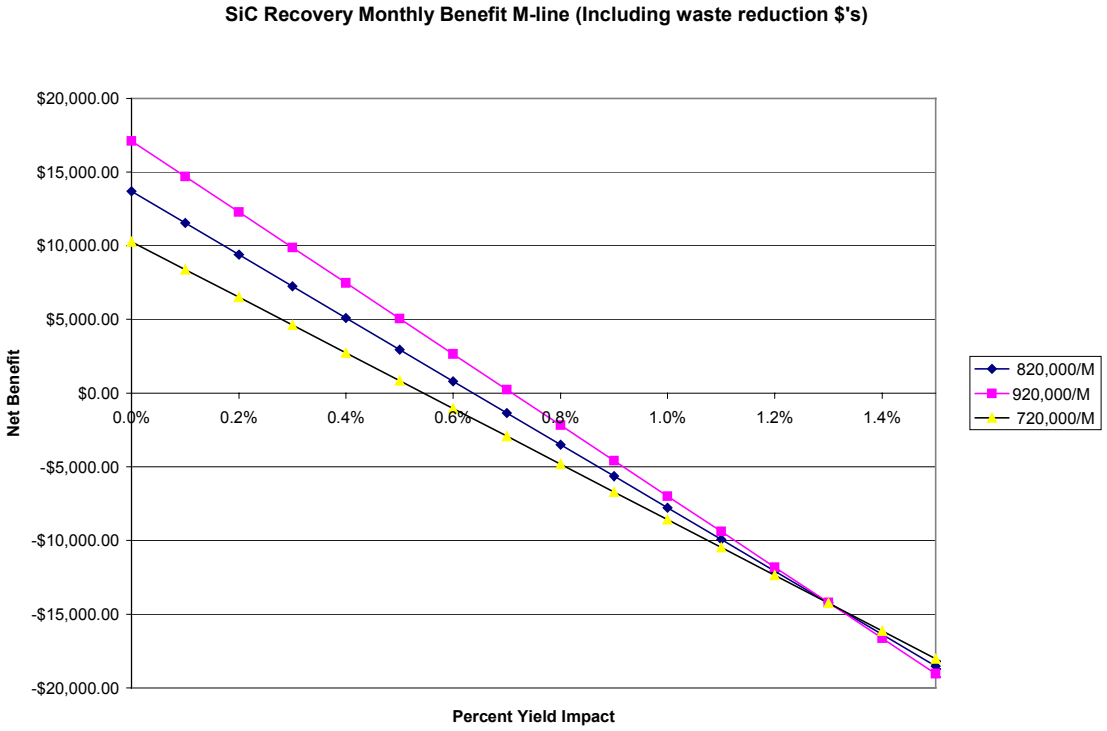

Figure 30. SiC recovery benefit

One-way Analysis of Variance

Analysis of Variance for yld

Source	DF	SS	MS	F	P
dev.vs.t	3	52.7	17.6	0.28	0.836
Error	912	56230.9	61.7		
Total	915	56283.7			

Individual 95% CIs For Mean Based on Pooled StDev

Leve	N	Mean	StDev	-+---------+---------+---------+-----
M	497	**97.31**	5.20	(-*--)
P	379	**97.21**	10.46	(--*--)
RM	10	**97.83**	3.91	(----------*----------)
RP	30	**95.99**	6.77	(--------*--------)

-+---------+---------+---------+-----

Pooled StDev=7.85 93.0 96.0 99.0 102.0

Figure 31. Recycled SiC Yield Analysis

This was shown again in continued use of the machine, where over 200,000 wafers have been cut with recycled SiC. The yields are shown in Figure 32 with the three product lines M, P and R line shown on the x axis, slurry run number shown in the legend. The m-line or 103 mm product and p-line or 125 mm product have the highest yields with the r-line or 150 mm product being the lowest. The histogram of the yield with recycled SiC is shown in Figure 33 showing that a few very bad runs contribute to this effect with a majority of the runs running very high. A focus on removing the bad runs is underway through better training and uptime of the recycling system.

The continued use of the machine is shown over time in Figure 34, where the percentage of recycled SiC used is shown by week and product type (M, P, and R). As can be seen from the chart, over 25% of the SiC is being recycled at SSI.

Caustic Waste Reduction

Preliminary work has started to outline and quantify the caustic reduction plan for our cell fabrication area. Several vendors have been contacted to do a study of what type of recycling or reduction system is appropriate for our volume and physical location.

Two companies, Sierra Pacific and Woodard Clyde have been contracted to aid in recommending either systems or techniques for caustic waste reduction. Reporting on their progress will take place during Phase II.

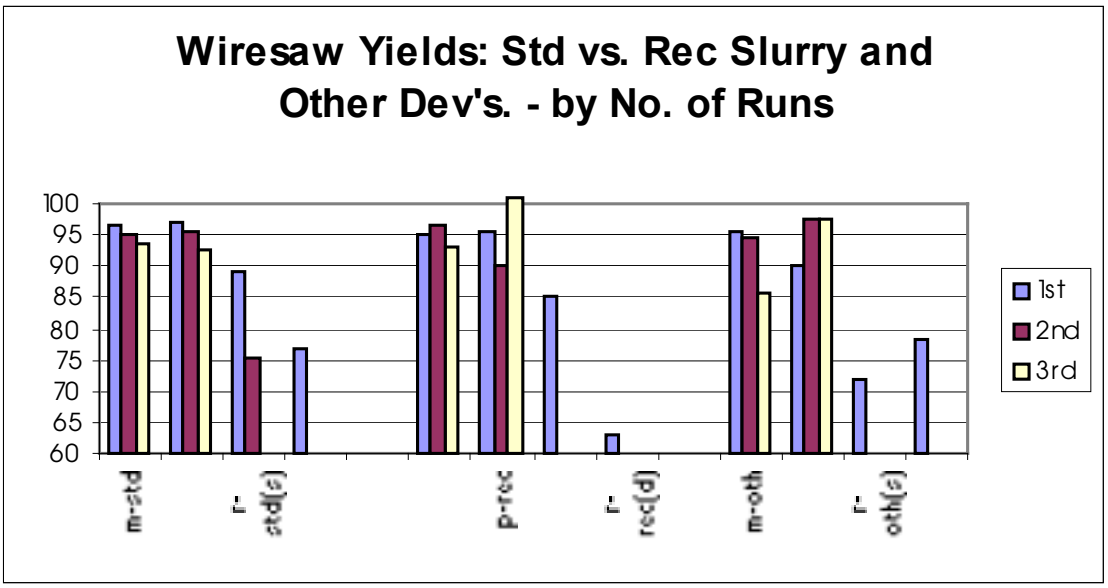

Figure 32. Recycled SiC Yield by Product type

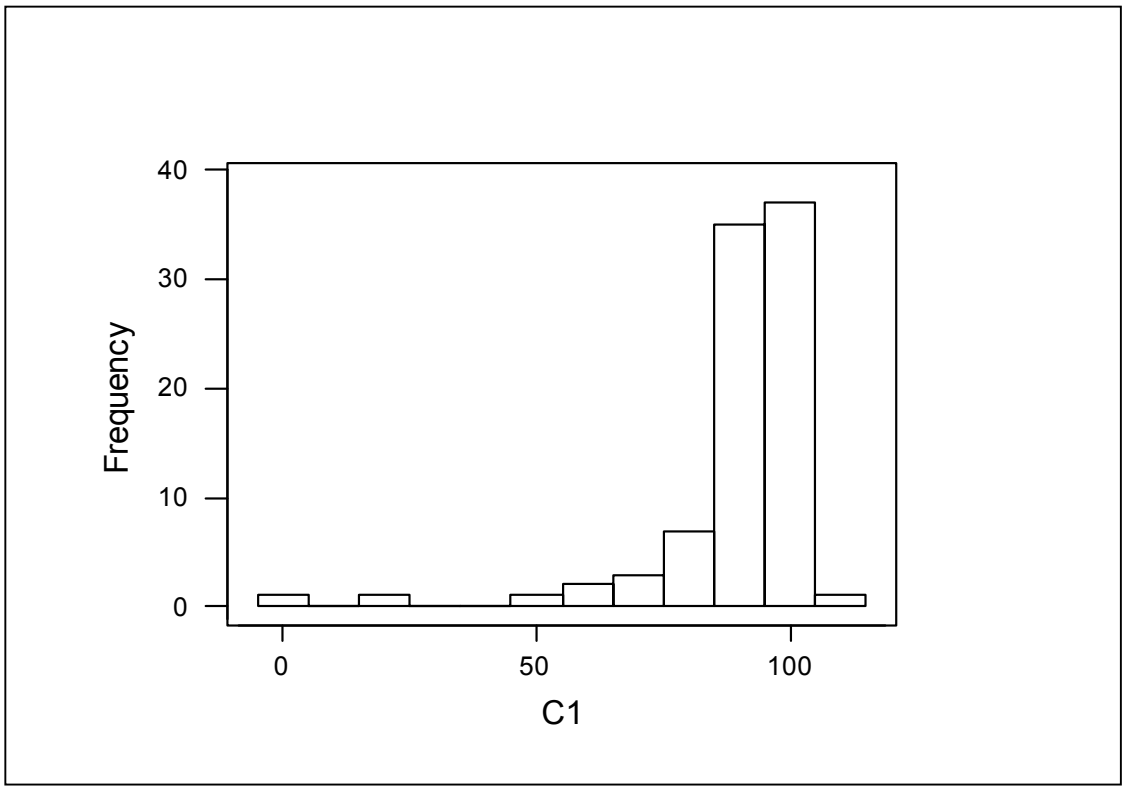

Figure 33. Yield Histogram showing bad runs

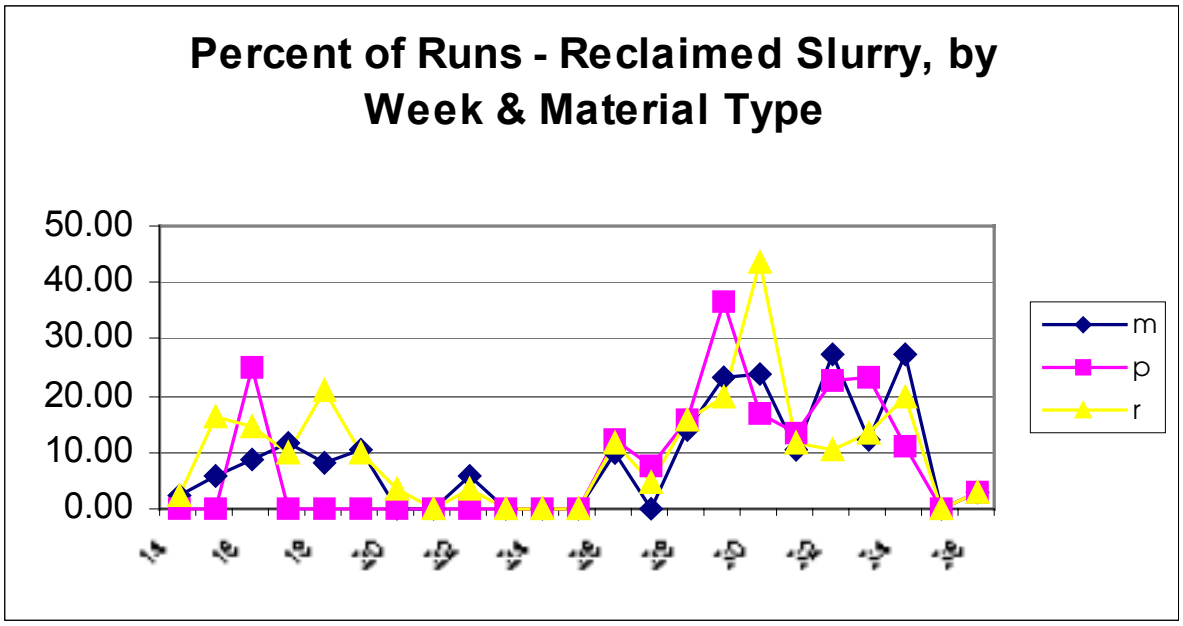

Figure 34. Percentage of Recycled SiC over time

Conclusions

The first step toward reducing cost in this PVMat 5A2 has been to reduce wafer thickness. The original plan to start piloting wafers at 150 microns showed excessive yield losses. For this reason, the approach has been a two step reduction in thickness, from 385 microns to 250 micron cells, and then from 250 microns to 125 micron cells during Phase II. During Phase I the handling tools, the Back Surface Field (BSF) process, and the confirmation of the environmental integrity of thinner wafers has all been accomplished. Cells with efficiency over 15.5% have been demonstrated in high volume production.

The larger cells are made, the lower the potential dollar per watt. SSI has initiated the development and growth of 200 mm ingot to be fabricated into wafers and eventually cells. This larger ingot has proven to be a product which can be grown in the larger crystal growers which SSI has in it's Vancouver facility. The ingot shaping has shown to be a bottle neck though, and the solution to this problem is being worked now. Large area cells and modules have been designed, and the wafering of these ingots is not expected to be a significant development issue. These larger cells continue to show the best cost structure as it optimizes the watts per kilogram consumed in producing the cells. Module designs for lower cost contribution have been started. The making of cells and modules with 200 mm cells will commence during Phase II.

Hazardous waste reduction has been attacked in two ways, the largest consumable item aside from polysilicon is Silicon Carbide (SiC) used in the wafer slicing process. This SiC use has been reduced significantly through recycling and re-use. This program approach is well underway at SSI, with over 25% of the SiC used being recycled. The largest hazardous waste volume at SSI is the caustic waste generated in the wafer etching processes. The reduction of this waste has been started with the use of subcontractors with extensive environmental compliance experience, such that the solution is driven by best available techniques.

These three areas of focus, thinner cells, larger cells and modules and hazardous waste reduction have the potential of reducing cost by approximately 30% per watt. This first phase of large 150 mm, 250 micron cells has demonstrated a potential for 10% cost reduction with the final yield improvements being implemented in the SSI line now. The follow-on work during Phase II with thinner cells, larger cells and continued waste reduction will allow the 30%, three year goal to be met.

References

Jester, T. L. (February 1999). "*Photovoltaic Cz Silicon Module Improvements, Final Subcontract Report, 9 November 1996- 8 November 1998.* Work performed by Siemens Solar Industries, Camarillo, CA. Golden, CO: National Renewable Energy Laboratory.

Bawa, M.S., Petro, E.F., Grimes, H.M. (November 1995), *"Fracture Strength of Large Diameter Silicon Wafers"*, Semiconductor International.

REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	April 2000	Annual Subcontract Report, June 1998 – June 1999

4. TITLE AND SUBTITLE
Specific PVMaT R&D on Siemens Cz Silicon Product Manufacturing;
Annual Subcontract Report, June 1998 – June 1999

5. FUNDING NUMBERS
C: ZAX-8-17647-14
TA: PV006101

6. AUTHOR(S)
T.L. Jester

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Siemens Solar Industries
4650 Adohr Lane
Camarillo, CA 93012

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
SR-520-27591

11. SUPPLEMENTARY NOTES
NREL Technical Monitor: R. Mitchell

12a. DISTRIBUTION/AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

This report describes work done by Siemens Solar Industries (SSI) from June 1998 to June 1999 during Phase I of a three-phase Photovoltaic Manufacturing Technology (PVMaT 5A2) subcontract from DOE/NREL. The work focuses on improvements in the cost per watt of Cz modules and improved PV module manufacturing technology. The first step toward reducing cost was to reduce wafer thickness. The approach has been a two-step reduction in thickness, from 385 microns to 250 micron cells, and then from 250 microns to 125 micron cells during Phase II. During Phase I, the handling tools, the back-surface-field process, and the confirmation of the environmental integrity of thinner wafers have all been accomplished. Cells with efficiency over 15.5% have been demonstrated in high-volume production. SSI has initiated the development and growth of 200-mm ingot to be fabricated into wafers and eventually cells. Cell and module production with 200-mm cells will begin during Phase II. Hazardous waste reduction has been attacked in two ways. The largest consumable item aside from polysilicon is silicon carbide (SiC) used in the wafer-slicing process. This SiC use has been reduced significantly through recycling and re-use. This program approach is well under way at SSI, with more than 25% of the SiC used being recycled. The largest hazardous waste volume at SSI is the caustic waste generated in the wafer etching processes. The reduction of this waste will be accomplished using subcontractors with extensive environmental compliance experience such that the solution is driven by best available techniques, lowering operating cost as a secondary motive. These three areas of focus—thinner cells, larger cells and modules, and hazardous waste reduction—have the potential to reduce cost by about 30% per watt. This first phase of large 150-mm-thinner 250-micron cells has demonstrated a potential for 10% cost reduction, with the final yield improvements being implemented in the SSI line now. The follow-on work during Phase II, with thinner cells, larger cells, and continued waste reduction, will allow the 30%, three-year goal to be met.

14. SUBJECT TERMS
photovoltaics ; Photovoltaic Manufacturing Technology ; PVMaT ; PV modules ; module manufacturing ; hazardous waste reduction ; Czochralski

15. NUMBER OF PAGES

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL