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Subcontractor Report

Optimization of Processing and Modeling Issues for Thin Film Solar Cell Devices

Final Report
February 3, 1997 — September 1, 1998

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Summary

The overall mission of the Institute of Energy Conversion is the development of thin film photovoltaic cells, modules, and related manufacturing technology and the education of students and professionals in photovoltaic technology. The objectives of this 20 month NREL subcontract are to advance the state of the art and the acceptance of thin film PV modules in the areas of improved technology for thin film deposition, device fabrication, and material and device characterization and modeling, relating to solar cells based on $CuInSe_2$ and its alloys, on a-Si and its alloys, and on CdTe.

$CuInSe_2$-based Solar Cells

$Cu(InGa)Se_2$-based devices, having absorber layers with $Ga/(In+Ga) \approx 0.25$ and bandgaps (Eg) of 1.15 eV, typically have open circuit voltages < 0.65V. Higher Ga concentrations increase the $Cu(InGa)Se_2$ bandgap and may result in a trade-off of higher open circuit voltage and lower short circuit current which may allow increased cell efficiency. Further, module performance should be improved due to lower resistive losses, thinner ZnO with less optical loss and/or greater interconnect spacing with reduced associated area-related losses.

There are many technical issues that need to be addressed to effectively enable the transfer of $Cu(InGa)Se_2$ deposition and device fabrication technology from the laboratory to manufacturing scale. In general, these issues provide a means to reduce thin film semiconductor process costs. Shorter deposition time can be achieved with reduced film thickness and increased deposition rate. Thinner absorber films reduce the total amount of material used and allow faster process throughput. The minimum thickness of the $Cu(InGa)Se_2$ absorber layer may be determined by the nucleation of the film to form a continuous layer or by the film morphology. From a device perspective, the minimum thickness may be determined by the minority carrier diffusion length and optical absorption coefficient of the $Cu(InGa)Se_2$ or the ability to incorporate optical confinement.

Performance of Devices with $Cu(InGa)Se_2$ Absorber Layers

We have previously demonstrated $Cu(InGa)Se_2$ solar cells with 15% efficiency for $Ga/(In+Ga) \leq 0.5$ or $Eg \leq 1.3$ eV [1, 2]. With higher bandgap a decrease in cell efficiency was shown to be caused by poor collection of light generated minority carriers in the $Cu(InGa)Se_2$ absorber layers [3, 4]. Reasons for decreasing performance with increasing Ga content were investigated in detail [5]. Solar cells have been made from uniform $Cu(In,Ga)Se_2$ films deposited by elemental evaporation with two different Ga compositions, $Ga/[In+Ga] = 0.30$ and 0.65. The solar cells fabricated from these uniform films have 15% efficiency for $Ga/[In+Ga] = 0.30$, but the device efficiency is less than expected for the high Ga content due primarily to a decrease in fill factor and open circuit voltage. Analysis of current-voltage results have shown that the main cause of this decrease is a voltage dependent light generated current, $J_L(V)$. Devices were fabricated with both standard (1 μm) and semi-transparent (0.04 μm) Mo contacts. Bi-facial spectral response measurements were made and analyzed on the devices with the semi-transparent Mo contacts in order to determine the changes in collection efficiency as a function of changing Ga composition and applied voltage. This analysis determined that the decrease in the light generated current

with increasing voltage is primarily due to a reduction in minority carrier diffusion length, L, from about 0.8 to 0.1 μm.

Reduced $Cu(InGa)Se_2$ Deposition Temperature and Thickness

Lower substrate temperature (T_{ss}) can lower processing costs by reducing thermally induced stress on the substrate, allowing faster heat-up and cool-down, and decreasing the heat load and stress on the entire deposition system. In addition, with lower substrate temperature, stress on the glass substrate can be reduced and alternative substrate materials, like a flexible polymer web, could be utilized.

We have addressed the need to improve process throughput by reducing the $Cu(InGa)Se_2$ thickness and deposition temperature [6]. The approach during this work has been to first define a baseline process for $Cu(InGa)Se_2$ deposition by multisource elemental evaporation and solar cell fabrication. Substrate temperature (T_{ss}) is varied from $600 \geq T_{ss} \geq 350$°C using fixed elemental fluxes. The grain size decreases over the entire range but Na incorporation from the soda lime glass substrate doesn't change. Solar cell efficiency decreases slowly for $550 \geq T_{ss} \geq 400$°C. At T_{ss} below 400°C there is a change in composition attributed to a change in the re-evaporation of In and Ga species in the growing film. Device performance is shown to be unaffected by reducing the film thickness from 2.5 to less than 1.5 μm. Finally, a kinetic reaction model is presented for the growth of $CuInSe_2$ by multisource elemental evaporation that provides quantitative predictions of the time to grow $CuInSe_2$ films as a function of substrate temperature and delivery rate.

Analysis of Chemical Kinetics and Growth of Cu-In-Se-S Containing Thin Films

Preliminary results have been obtained on the growth and characterization of Cu-In-Se-S thin films formed by reaction of Cu-In layers with a H_2Se/H_2S gas mixture. The approach was to first develop a process to grow device quality $CuInS_2$ films by reaction of a Cu-In layer in H_2S. This process was then modified to form alloyed $CuIn(Se,S)_2$ films. A quantitative model for the reaction of Cu-In films in a CVD reactor with a mixed H_2S-H_2Se flowing gas was developed and verified. The composition of the $CuIn(Se,S)_2$ film can be controlled by the concentration H_2Se + H_2S and/or Se_2 + S_2 in the gas phase. Graded films can be made by annealing either $CuInSe_2$ or $CuInS_2$ films in a controlled Se and/or S containing atmosphere. Expanding this to include Ga in the films will provide a basis for engineering film compositions and bandgaps [7].

$CuInSe_2$ Team Participation

IEC is an active member of four sub-teams under the National CIS Team for the NREL Thin Film Partnership Program. The CIS team was restructured into sub-teams designed to directly support the industrial partners. IEC is active with the following:

Global Solar Energy. This team is focusing on helping GSE develop a low temperature process for the roll-to-roll deposition of $Cu(InGa)Se_2$. IEC is providing direct support through materials characterization and device fabrication and characterization.

ISET. IEC is assisting in the development of improved performance of ISET's CIS-based materials by investigating the use of sulfur incorporation to increase the voltages in the devices and modules.

Siemens Solar Industries. This sub-team is addressing reliability and transient effects in SSI's cells and modules. Specifically, IEC is completing device measurements and analysis of cells and mini-modules subjected to light exposure, thermal stress, and voltage bias.

Unisun. IEC is providing detailed materials characterization, device fabrication and characterization to support Unisun's development of particle-based processes for deposition of $Cu(InGa)Se_2$.

CdTe-based Solar Cells

Production of reliable and reproducible CdS/TCO window layers and contacts for stable, high performance CdS/CdTe solar cells are the key issues confronting development of thin-film CdTe solar cells. Meeting these objectives with manufacturing-compatible processes is crucial to satisfying the overall NREL program goals and requires an understanding of the controlling properties and mechanisms. IEC research in this phase was concentrated on: 1) investigation of alternative TCO configurations; 2) quantifying and controlling CdS-CdTe interaction; and 3) separating effects in device behavior after stress-induced degradation. The approach utilizes PVD deposited semiconductor layers and post-deposition processes in which chemical and thermal effects are separated. Through interaction with the National CdTe R&D Team, the applicability of the results and processes to CdS/CdTe cells made by different techniques has been demonstrated, enabling a consistent framework to be used for understanding the relationship between device fabrication and operation.

Devices with Thin CdS

During this phase, it was shown that a high resistance transparent layer between CdS and the TCO allows V_{oc} and FF to be maintained as d(CdS) is reduced, resulting in higher short circuit current densities and performance. Compared to devices with single layer conductive ITO or SnO_2, those incorporating high resistivity (>10 Ω-cm) interlayers of ITO, In_2O_3, SnO_2, or Zn_2SnO_4 have yielded devices in which V_{oc} remains > 700 mV and FF > 60% for final CdS thickness less than 80 nm.

Quantification of CdS-CdTe Interdiffusion

Fundamental issues confronting fabrication of devices with ultra-thin CdS were investigated, resulting in a more quantitative understanding of the CdS-CdTe diffusion process [8, 9]. In particular: 1) additional points were added to the CdS-CdTe *T-x* phase diagram at T = 625˚C to establish the miscibility gap from 625˚C to 400˚C at fixed $CdCl_2$:O_2 partial pressures; 2) the rate of CdS consumption in device structures was determined for a range of processing temperatures and time and oxygen partial pressures; and 3) the thermochemistry of the CdS-CdTe-$CdCl_2$-O_2 system was investigated.

Contact to CdTe

Vapor $CdCl_2$:O_2 treatment of CdTe/CdS yields surfaces with very low residual oxygen and chlorine species, allowing contacts to be fabricated without the use of wet etch or reaction steps. This all-vapor process has become the baseline process for PVD cells. The role of Cu-Te species as the primary contact to CdTe in both wet and vapor processes was further elucidated by relating contact processing chemistry to measured surface phases and device J-V behavior. Linear forward bias behavior was correlated with Cu_2Te, and curvature in the J-V curve near V_{oc} was correlated with CuTe surface phases.

CdTe/CdS cells held in open circuit condition in air at T ~ 100C for ~150 hours exhibit degraded behavior: V_{oc} is reduced by 100-150 mV; FF is reduced 10% points; series resistance increases from 1-2 to 10-20 Ohm-cm^2; and curvature develops in the forward bias portions of dark and light J-V curves. In these devices, the surface Cu-Te phase converts from predominantly Cu_2Te to CuTe. Re-contacting this surface after a weak etch in bromine-methanol restores Cu_2Te and dark and light forward bias linearity but not V_{oc}, leading to the conclusion that the back surface chemistry and back contact electrical behavior are coupled. CdTe/CdS structures with no contact in place held at similar stress conditions and then contacted exhibited high performance with no evidence of stress degradation, leading to the conclusion that the degradation mechanism for V_{oc} is linked to the presence of the Cu-containing contact during the stress.

Contacts to p-type CdTe were analyzed using current-voltage-temperature (J-V-T) and glancing-incidence x-ray diffraction measurements. The electrical properties of the CdTe/contact and those of the main CdS/CdTe junction were modeled with a series connected equivalent circuit consisting of a temperature independent resistance, a leaky diode representing the contact and a diode representing the main CdS/CdTe junction. The barrier heights of the CdS/CdTe junction diode and the CdTe contact diode were determined from J-V measurements made as a function of temperature. Barrier heights of 1.4 eV and 0.3 eV were found for the CdS/CdTe junction and the CdTe contact, respectively. The 0.3 eV barrier height of the CdTe contact junction is consistent with a CdTe/Cu_xTe junction. The existence of a layer containing copper tellurides in working devices was confirmed by glancing incidence x-ray diffraction analysis of the CdTe surface prior to metallization [10].

Team Participation

IEC has actively participated in the National CdTe R&D Team by depositing CdTe films for analysis, fabricating contacts and stressing devices for the stability sub-team, and fabricating devices for the CdS sub-team using different high resistance transparent layers between CdS and the TCO. Brian McCandless has reported these results through presentations and written reports at Team Meetings.

a-Si:H-based Solar Cells

The focus of the a-Si research was on deposition of more conductive p-layers and electrical properties of contacts between doped layers and TCO. The Si:C:H p-layers were deposited by RF CVD. The effect of H_2, SiH_4 and CH_4 flow rates, boron dopant source gas, and RF power on microcrystallinity and conductivity was studied. Crystallinity was characterized by Raman

spectroscopy. This work is motivated by the need for a wide bandgap highly conductive p-layer material to simultaneously increase V_{oc} and blue response of superstrate p-i-n solar cells. Regarding contacts, a new method was developed to determine the contact resistance between the p-layer and the underlying transparent conductive oxide (TCO) and also changes in the TCO sheet resistance due to the p-layer deposition in p-i-n superstrate modules and devices. We also showed the need to match the n-layer properties with the TCO/metal back reflector so that gains in J_{sc} due to the improved light trapping were not compromised by losses in FF due to poor contact. Incorporating a μc-n-layer allows both high J_{sc} and FF to be achieved simultaneously.

Preparation and Characterization of Microcrystalline Si:C:H p-Layers

Initial results were obtained from a study to develop SiC p-layers compatible with a superstrate p-i-n cell structure, deposited in an RF PECVD system. Experimental variables were dopant gas, CH_4 and H_2 gas flows normalized to the sum of SiH_4 and CH_4 flows, and the power. Compared to B_2H_6, doping with $B(CH_3)_3$ lowered the conductivity by a factor of 40 and reduced the fraction of crystallinity from 87% to 53%. The c-Si fraction decreased strongly with increasing CH_4 flow. No evidence of Si-C bonding was identified in the Raman spectra. It was demonstrated that high conductivity p-layers (>1 S/cm) having high c-Si volume fraction (~85%) can be deposited on glass at low power density (84 mW/cm^2) which is compatible with deposition on TCO substrates for device fabrication.

Characterization of the TCO/p Contact Resistance and Sheet Resistance in Superstrate Solar Cells

A novel method was developed to characterize the TCO/p contact and the TCO sheet resistance in a-Si based p-i-n superstrate devices. It requires having scribed TCO strips, which are electrically isolated before a-Si deposition, then fabricating rows of individual devices on each strip. Analysis of 4-terminal measurements in different V-sensing configurations yields the TCO/p contact and TCO sheet resistance in a straightforward manner. The method is applied to devices fabricated on 3 brands of commercial SnO_2 substrates. The TCO/p contact resistance is found to be ~2 Ω-cm^2 and the sheet resistance decreases by 2-4 Ω/sq after a-Si deposition on all three brands of SnO_2 substrates.

Optimization of n/TCO/metal Back Contacts

A comprehensive study of the n-layer and back contact for superstrate (glass/textured SnO2/p-i-n/TCO/metal) a-Si solar cells was performed [11]. The difference between a-Si and μc-Si n-layers was found to be significant. The results showed that the solar cell efficiency can be improved from 7% to 10% (absolute) by optimizing the back contact layers to incorporate a good optical back reflector. At T = 25°C, a rectifying contact is formed between the TCO and a-Si n-layer which reduces FF. A μc-Si n-layer is required to avoid forming a blocking n/TCO contact. Large variations in device performance with TCO processing are inconsistent with the small changes in bulk TCO properties, suggesting the n/TCO interface has a controlling influence. ZnO gives ~1 mA/cm^2 higher J_{sc} compared to ITO. The best contacts are μc-Si/ZnO/metal, with Ag or Cu giving comparable performance.

a-Si Team Participation

IEC is a member of the National a-Si Team under the Thin Film Partnership Program. Steve Hegedus is the leader of the Multijunction Device sub-team. The work on characterization of the TCO/p contact resistance was performed as part of the Teaming activities in collaboration with Solarex. During this contract period, IEC collaborated with: Gautam Ganguly at Solarex by characterizing the TCO/p contact resistance on their sub-modules having different textured SnO_2; Bhushan Sopori at NREL by fabricating back reflector structures on textured TCO/a-Si substrates from Solarex for analysis by PVOPTICS; and Eric Schiff at Syracuse University by providing him with special TCO/i-n device structures for electroabsorption measurements. These teaming collaborations lead to co-authoring three publications at the Spring 1999 Materials Research Society Conference.

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1. Introduction

Photovoltaic modules based on thin film systems of a-Si:H and its alloys, $CuInSe_2$ and its alloys, and CdTe are promising candidates to meet DOE long-range efficiency, reliability and manufacturing cost goals. The commercial development of these modules is at different stages and there are generic research issues that need to be addressed:

- quantitative analysis of processing steps to provide information for efficient commercial scale equipment design and operation;
- device characterization relating the device performance to materials properties and process conditions;
- development of alloy materials with different bandgaps to allow improved device structures for stability and compatibility with module design;
- development of improved window/heterojunction layers and contacts to improve device performance and reliability; and
- evaluation of cell stability with respect to illumination, temperature and ambient and with respect to device structure and module encapsulation.

The critical issues that were addressed under this NREL program for the specific thin film materials system are discussed below.

1.1 $CuInSe_2$-based Solar Cells

$CuInSe_2$ has a bandgap of 1 eV and the devices typically have V_{oc} less than 0.5 V. This bandgap is about 0.5 eV less than required for a single junction device to have optimal efficiency for terrestrial applications. Further, the high J_{sc} of these devices reduces module performance because of higher cell spacing and series resistance losses, and because devices with low operating losses typically suffer larger fractional losses as the devices are operated under real PV module operating conditions (module operating temperatures of 50˚ to 60˚C) as compared to operation under standard measurement conditions (25˚C). Champion cells have been made with bandgaps of about 1.2 eV through the addition of Ga. It is desirable to further increase the bandgap from 1.4 to 1.6 eV for improved module performance.

Presently, most companies developing $CuInSe_2$ for modules form the $CuInSe_2$ films by the selenization of Cu/In films in either an H_2Se or Se atmosphere. Progress has been made in characterizing the chemical pathways to film growth and estimating the reaction rate constants. As the process evolves to include the $CuInSe_2$ alloys, characterization of the reaction chemistry and kinetics needs to be extended to the alloys. While reaction pathways have been identified that lead to the formation of near stoichiometric $CuIn_{1-x}Ga_xSe_2$ when the processing temperatures are limited to below 400˚C, all cells with record-level efficiencies were produced by reacting the absorber layers at temperatures above 500˚C. Such high processing temperatures limit the

choice of substrate materials (e.g., lightweight Kapton foil) and make processing and substrate handling in general more difficult.

1.2 CdTe-based Solar Cells

Instability of CdTe-based solar cells and modules is commonly assumed to be related to the rear contact, especially if this contact is Cu-doped. There is a need to further develop a stable ohmic contact for CdTe compatible with monolithic integration technologies. New contacts must be tested and a method developed to rapidly characterize stability. It appears likely that the optimization of such a contact depends also on the details of the other layers used in the device (CdTe, CdS, SnO_2, and type of glass).

The effects of high temperature processing, either during deposition or after film growth, and $CdCl_2$ treatments on the operation of the device are not well characterized. Of particular concern are the uniformity of large-area modules and the "robustness" of such processes. Questions concerning CdS-CdTe interdiffusion, O and Cl doping, and chemical reactions between $CdCl_2$ and CdTe need to be addressed quantitatively.

Although many researchers have produced devices with 12% efficiency, few have exceeded 14%. The challenge is to obtain high values for J_{sc} without loss of V_{oc}, and a good spectral response at short wavelengths ($\lambda < 500$ nm) without sacrificing the spectral response at longer wavelengths. It is important to understand which factors lead to cells in which such losses can be avoided. It has been established that cell parameters are sensitive to the details of the CdS/CdTe interface. Understanding the mechanisms in detail would accelerate device optimization, which is more and more realized to be an interactive process requiring the optimization of each layer in the device depending on all the other layers present.

1.3 a-Si:H-based Solar Cells

Amorphous silicon (a-Si) PV modules were the first thin-film PV modules to be commercially produced and are presently the only thin-film technology that had an impact on the overall PV markets. However, the efficiencies of these modules have not yet reached the levels that were predicted in the 1980s. To a significant degree this is due to the intrinsic degradation of a-Si under illumination. The amount of light-induced degradation can be limited to 20 to 30% in modules operating under prevailing outdoor conditions. Both material processing schemes and device design schemes have been developed to improve the stabilized solar cell efficiency of a-Si solar cells. The use of multijunction devices (allowing the use of thinner absorber layers in the component cells) and the use of light-trapping appear to be the most powerful device design schemes to improve stabilized device performance.

The US industry is currently using these approaches to build a-Si-based modules. The so-called substrate type devices are built on stainless steel foil, covered with a "back reflector." The superstrate devices are built on glass coated with transparent conductors (TCO). The texture and transparency of the TCO contacts are critical to improve light trapping and J_{sc}. Reducing optical losses in the TCO will allow thinner i-layers to generate the same J_{sc}, thus improving stability.

Presently, all superstrate devices use an a-SiC p-layer while substrate devices use a "μc-Si" p-layer, which is in fact a mixture of a-Si and μc-Si phases. Fabricating devices with p-layers having wider bandgaps is expected to lead to higher blue response and, hence, increased J_{sc}. Further, such highly conductive and transparent layers will reduce electrical and optical losses at the n/p interconnect junction of multijunction devices. Thus, improvements in back reflectors and p-layers would benefit both superstrate and substrate device technologies, in either single or multijunction configurations.

1.4 Training and Education

During the period of this subcontract (from February 1997 to September 1998), IEC provided training and education for the following: six visiting professionals; seven post-doctoral candidates; 13 graduate students; and nine undergraduate students. Two of our visiting professionals were Fulbright scholars. Names are given in the list of contributors.

1.5 Publications

As a result of research performed under this subcontract, IEC published 23 papers, 3 in refereed journals and 20 in conference proceedings.

1.6 Organization of the Report

This report is organized into three technical sections: $CuInSe_2$-based solar cells, a-Si:H-based solar cells, and CdTe-based solar cells. Each section describes the progress made at IEC in addressing the critical issues discussed above during the 19-month period of this subcontract.

2. $CuInSe_2$-based Solar Cells

2.1 Chemical Kinetics and Equilibrium Analysis of Cu-In-Se-S

2.1.1 Introduction

$CuInSe_2$ based solar cells and modules have demonstrated the highest performance of any of the thin film PV technologies, with small area cell efficiency over 17% and module efficiency over 11% [12]. These results should be viewed as proof of concept, pointing to the manufacturing potential of this material. However, 15 years after Mickelsen and Chen reported the first 10% cell [13], there is no large scale manufacturing facility. The translation of laboratory results to first-time manufacturing has been much more difficult than expected due to the complexity of the processes involved for making thin film polycrystalline PV modules. This is compounded by the limited scientific basis to complement R&D, since $CuInSe_2$ based thin films are primarily used for PV. Further, most of the research activities were driven by the need to improve device performance and not to develop the fundamental scientific and engineering base required to properly engineer manufacturing equipment.

The primary issues that have inhibited the development of manufacturing processes for copper indium gallium diselenide based PV modules are: 1) the design, operation & control of commercial scale equipment required for the deposition of the $CuInSe_2$; 2) analytical instrumentation for monitoring film growth; and 3) the difficulty of maintaining uniformity over large areas.

To address these issues, research at IEC has been directed towards developing quantitative models relating processing parameters and film growth chemistry to provide the scientific and engineering basis for effective design of commercial equipment. The research has focused on the Cu-In-Ga-Se-S materials system since all high efficiency $CuInSe_2$ based solar cells use $Cu(In,Ga)(Se,S)_2$ films. Further, wider bandgap materials are needed for improved module performance and for next generation multijunction devices. However, solar cell performance drops in $CuInGaSe_2$ devices when Ga/(Ga+In) is above ~50%, where Eg > 1.3 eV [1, 5]. The goal of the research is to alloy $CuInSe_2$ with appropriate amounts of Ga and S to control the bandgap of the material and maintain the broad 'single' phase regime of $CuInSe_2$. The bandgap of the ternaries are:

$CuInSe_2$	1.0 eV	$CuGaSe_2$	1.7 eV
$CuInS_2$	1.5 eV	$CuGaS_2$	2.5 eV.

Since these materials form solid solutions with each other, there is the potential for 'engineering materials' with a bandgap from 1.-0 to 2.5 eV.

Previously, we reported on reaction analysis of the Cu-In-Se materials system where the reaction chemistry was evaluated and the rate constants and activation energies were determined [14]. A process for forming single phase $CuInGaSe_2$ films by selenization was developed and the Cu-In-Ga-Se materials system characterized [15]. A reactor analysis for a multiple source PVD system was performed and the mathematical models developed were used for the design of commercial

scale equipment [16]. In this section, preliminary results are present on the growth and characterization of Cu-In-Se-S thin films formed by reaction with H_2Se and H_2S. The approach was to first develop a process to grow $CuInS_2$ films by reaction of a Cu-In layer in H_2S that was suitable for fabricating moderately efficient solar cells. This process was then modified and quantitatively characterized with respect to growth of mixed Se-S films.

2.1.2 Experimental

Cu and In precursor layers were deposited by sputtering on Mo coated Corning 7059 glass substrates. About 2500Å of Cu were deposited followed by In to give a Cu-In ratio of about 1 and a final film thickness of about 2μm. The precursors were reacted in a laminar flow CVD tubular reactor described previously [17] which had been upgraded to allow delivery of both H_2Se and H_2S. The growth parameters used were:

Flow rate: 1320 sccm	$H_2S + H_2Se = 0.5\% - 2.0\%$ in Ar
Velocity: 76 cm/min.	$O_2/(H_2S+H_2Se) = 0.01$
Holding time: 1 min.	$T_{reaction} = 350^{\circ}C$ to $450^{\circ}C$
Reaction Time: 5 to 120 min.	

The films were evaluated by scanning electron microscopy (SEM) to characterize their morphology and by energy dispersive x-ray spectroscopy (EDS) to determine elemental composition. The films were analyzed by x-ray diffraction (XRD) to identify chemical species present in the films and to estimate the S/Se+S in the $CuIn(Se,S)_2$ film. The sensitivity of the EDS and XRD methods used was $\pm$1%.

2.1.3 Results and Analysis

$CuInS_2$ films suitable for solar cells were grown in a two-step process. The Cu-In layer was reacted at 350˚C for 30 min. in a 0.5% H_2S gas concentration followed by a 60 min. reaction at 450˚C. The two-step process results in denser films than in a single step process at 450˚C. Films were slightly Cu rich, from 25 to 27 atomic % of Cu. It is important to note that $CuInS_2$ has a narrow single phase regime extending ~2% from stoichiometry towards Cu_2S [18]. Before fabricating devices, the film was etched in 0.2 molar solution of KCN at 40˚C for 1 min. to remove Cu-S phases. CdS /ZnO was used as the window layer to fabricate the devices. Solar cells were made with efficiencies over 8% and the best cell had a $V_{oc} = 0.65$ V, $J_{sc} = 19.7$ and FF = 65.5%. This was used as a validation of the process for growing the films.

The reaction of the Cu-In layer at 450˚C for times from 5 to 120 min. in mixed H_2Se-H_2S flows was analyzed by XRD and the results can be qualitatively summarized as follows: 1) for time less than 10 min. binary indium selenides and sulfides are formed along with what appear to be ternary copper selenide-sulfide; 2) for intermediate times of 10 to 20 min. mixed Cu-In-Se-S phases are present; and 3) for 120 min. *uniform* $CuIn(Se,S)_2$ films in steady state equilibrium with H_2S/H_2Se gas composition are formed. This is consistent with previous work where the precursors and any intermediates occurring in the formation of $CuInSe_2$ [17] and $CuInS_2$ [19] are consumed within 10 to 15 min. In addition to the existing proposed reaction paths for the formation of $CuInSe_2$ [20] and $CuInS_2$ [21], replacement reactions with H_2S and H_2Se may occur resulting in a film composed of $CuInSe_2$, $CuInS_2$ and/or $CuIn(Se,S)_2$. If these constituents are

taken to be a continuous solid solution of $CuInSe_2$ and $CuInS_2$, it is proposed that they will react with the hydride gases according to the reversible reaction,

$$2H_2Se + CuInS_2 \Leftrightarrow 2H_2S + CuInSe_2 . \quad (1)$$

The equilibrium constant, *K,* is given by the ratio of the rate constants, k_1 and k_2, for the reaction

$$K = \frac{k_1}{k_2} = \frac{[H_2S]^2[CuInSe_2]}{[H_2Se]^2[CuInS_2]} = \left(\frac{x}{1-x}\right)^2\left(\frac{1-y}{y}\right) \quad (2)$$

where

$$x = \frac{[H_2S]}{[H_2S]+[H_2Se]} \quad (3)$$

and

$$y = \frac{S}{Se+S} \text{ (in the film).} \quad (4)$$

The equilibrium constant is calculated from the Gibbs free energy using,

$$K = \exp(-\Delta G / kT) . \quad (5)$$

The free energy for each component of the reaction was calculated from published data shown in Table I. The resulting total Gibbs free energy for the reaction was found to be -12.90 kcal/mol, resulting in an equilibrium constant of 7957 for a temperature of 450˚C, which implies an equilibrium favoring the presence of $CuInSe_2$.

Table I. Gibbs Free Energies for Reaction Constituents at 450˚C.

Constituent	Free Energy @ 450°C (kcal/mol)	Reference
$CuInS_2$	-89.71	[22]
$CuInSe_2$	-83.43	[23]
H_2S	-42.31	[24]
H_2Se	-32.73	[24]
S_2	-10.46	[24]
Se_2	-11.58	[24]
O_2	-37.00	[24]
H_2O	-84.44	[24]

Experimentally, *x*, the fractional concentration of H_2S, can be set and *y*, the fractional concentration of S in the film, measured. Figure 1 shows the predicted solid-vapor phase equilibrium based on the above analysis.

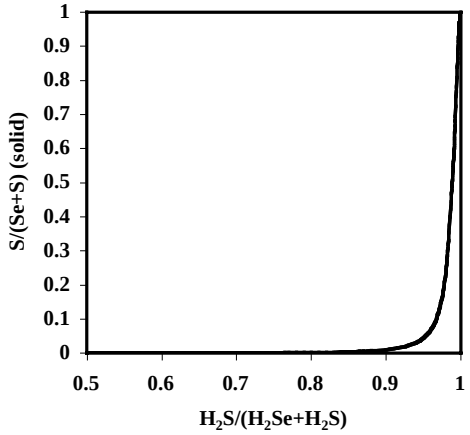


Figure 1. Steady state model for $H_2Se + H_2S$.

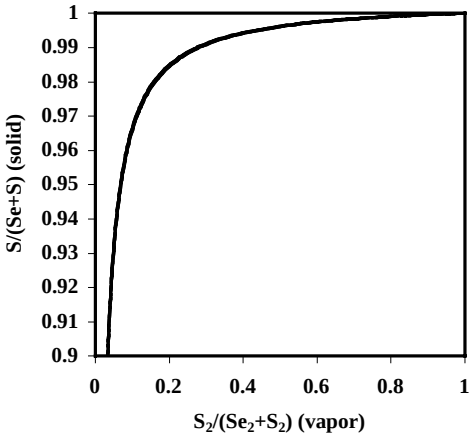


Figure 2. Steady state model for Se_2 S_2.

Experimentally, oxygen is introduced at the beginning of the process to prevent the agglomeration of liquid indium during the ramp up to reaction temperature and is present during the reaction at a ratio of $O_2/(H_2S+H_2Se) = 0.01$. Oxygen reacts in the gas phase with the hydride gases by the reaction,

$$nH_2S(e) + \frac{n}{2}O_2 \rightarrow S(e)_n + nH_2O. \quad (6)$$

Since the dimer is more reactive than the other existing polymers, n is assumed to be 2 to estimate the maximum effect of O_2. The Gibbs free energy is calculated using values from Table I for the following reactions:

$$2H_2S + O_2 \blacklozenge S_2 + 2H_2O \quad \Delta G_{rxn}(450°C) = -57.5 \text{ kcal/mol} \quad (7)$$

and

$$2H_2Se + O_2 \blacklozenge Se_2 + 2H_2O \quad \Delta G_{rxn}(450°C) = -78.0 \text{ kcal/mol}. \quad (8)$$

These reactions are strongly driven and it is assumed that all the O_2 reacts with the hydride resulting in Se_2 and S_2 in the gas phase which reacts with the film by the reaction,

$$S_2 + CuInSe_2 \Leftrightarrow Se_2 + CuInS_2 \quad \Delta G_{rxn}(450°C) = -8.62 \text{ kcal/mol}, \tag{9}$$

resulting in an equilibrium that favors the presence of $CuInS_2$. Using the same method as above for the calculation of the equilibrium constant, K is found to be 406. Figure 2 shows the predicted solid-vapor phase equilibrium for Se_2 and S_2. However, the ratio $O_2/(H_2S+H_2Se)$ is typically 0.01 and has a small effect on the steady state equilibrium in these experiments. Figure 3 shows the predicted and experimentally determined values for the fractional H_2S concentration in the gas phase compared to the fractional S concentration in the solid phase. The heavy solid line includes the contributions due to the hydride gases plus the presence of O_2. Contribution due to oxygen alone is represented by the dotted line. The data, represented by open boxes, match the model well over the range of interest. The presence of free S_2 and Se_2 results in a minimum sulfur incorporation over the relative hydride concentration range, falling off to zero where the gas phase reaction with O_2 becomes concentration limited at the low H_2S extreme. The experimental data also reflect these results.

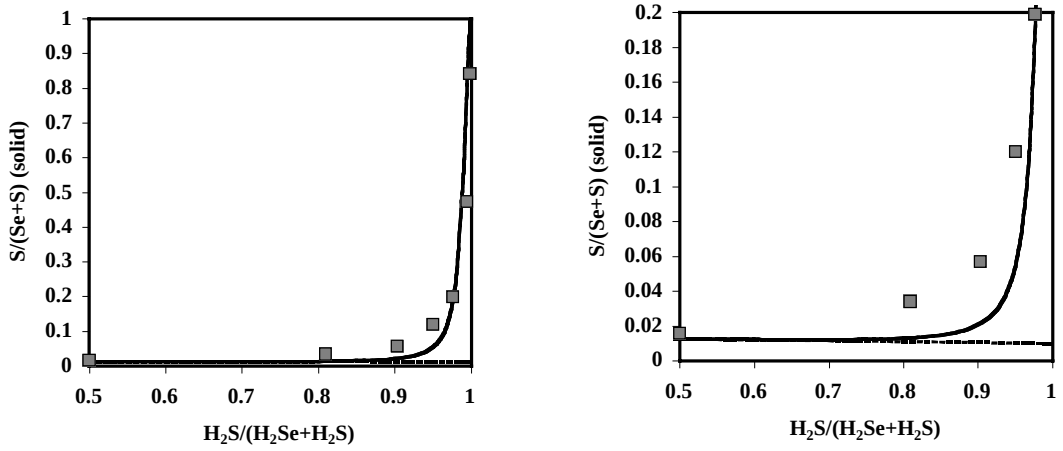


Figure 3. Steady state model for H_2Se + H_2S with 0.01 O_2.

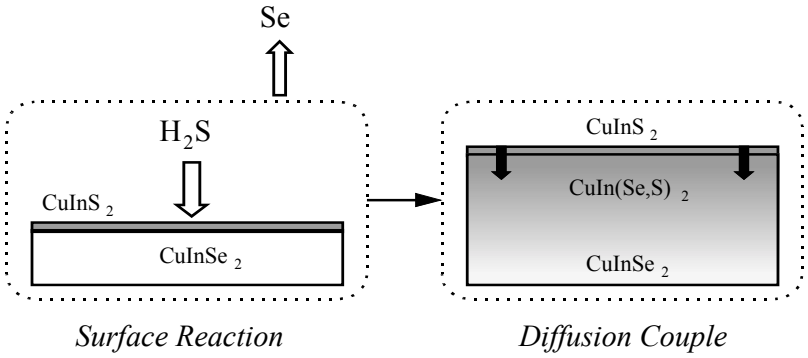


Figure 4. Proposed two-step diffusion process.

Based on the thermochemical analysis, films with graded composition (i.e., graded bandgap) can be formed by annealing $CuInSe_2$ or $CuInS_2$ films in a sulfur or selenium atmosphere, respectively. Preliminary data show that $CuInS_2$ films annealed at 450˚C in H_2Se completely convert to $CuInSe_2$ after approximately 10 min. or more. $CuInSe_2$ films annealed in H_2S, however, only partially convert after 120 min. at the same temperature. It is expected, based on the thermochemical analysis, that $CuInSe_2$ films can be converted moderately fast to $CuInS_2$ film in an elemental S atmosphere. Figure 4 depicts a proposed two-step process for the conversion of a $CuInSe_2$ film. First, a surface reaction that is kinetically controlled occurs, forming as a $CuInS_2$ layer. This is followed by an inter-diffusion process between the $CuInS_2$ and CuInSe layers. Presently, experiments are under way to verify the proposed model.

2.1.4 Conclusions

A quantitative model for reaction of Cu-In films in a mixed H_2S-H_2Se flowing gas system has been developed and verified by IEC. The composition of $CuIn(Se,S)_2$ film can be controlled by the concentration H_2S+H_2Se and/or Se_2+S_2. Graded films can be made by annealing either $CuInSe_2$ or $CuInS_2$ films in a controlled Se and/or S containing atmosphere. Expanding this to include Ga in the films will provide a basis for engineering film compositions and bandgaps.

2.2 Analysis of Cu(In,Ga)Se_2 Solar Cells: Why Performance Decreases with Increasing Ga Content

2.2.1 Introduction

It has been demonstrated that the loss in efficiency of $Cu(In,Ga)Se_2$ solar cells with increasing Ga content is due to a decrease in fill factor, and to a lesser extent V_{OC} which is caused by a drop in the light generated current with increasing forward voltage [1, 3].

Devices were fabricated with semi-transparent (0.04 μm) Mo contacts and bi-facial spectral response measurements were made and analyzed in order to determine the changes in collection efficiency as a function of changing Ga composition and applied voltage. This analysis can determine whether the decrease of light generated current with increasing voltage, $J_L(V)$, is primarily due to a reduction in minority carrier diffusion length (L) or a decrease in the width (w) of the space charge collection region near the $Cu(In,Ga)Se_2$/CdS junction [25].

2.2.2 Device Structure and Preparation

The $Cu(In,Ga)Se_2$ films were deposited by elemental evaporation from four Knudsen type sources to independently control the fluxes of Cu, In, Ga, and Se. The substrates were soda lime glass coated by DC sputtering with 0.04 and 1 μm thick Mo layers. Solar cells were fabricated by the sequential deposition of CdS, ZnO:Al and Ni-Al grids on the glass/Mo/$Cu(In,Ga)Se_2$ [1]. Cell areas were delineated by mechanical scribing to give individual cells with an area of 0.47 cm^2.

The elemental composition of the $Cu(In,Ga)Se_2$ films was determined by energy dispersive X-ray spectroscopy (EDS) and the Ga/[In+Ga] composition ratio was used to determine E_g. Electrical characterization of the devices included the total area current-voltage (J–V) response measured at

28˚C under AM1.5 illumination (Table II) and quantum efficiency (QE) measured through both the ZnO/CdS (frontwall) and the Glass/semi-transparent Mo (backwall) as a function of voltage bias. Normalized transmission through the ZnO and Mo are shown in Figure 5 in the wavelength region of interest (750 - 1050 nm).

Table II. Summary film and device parameters of the solar cells discussed in this paper Cu/(In+Ga) = 0.9 for all films.

Mo thk. (μm)	$Cu(In,Ga)Se_2$ thk. (μm)	Ga/(In+Ga)	E_G (eV)	Eff. (%)	FF (%)	V_{OC} (V)	J_{SC} (mA/cm^2)
1	3.0	0.30	1.2	14.9	73.5	0.627	32.4
1	2.3	0.65	1.4	10.1	68.1	0.755	19.6
.04	3.0	0.30	1.2	13.1	70.5	0.622	30.0
.04	2.3	0.65	1.4	10.0	68.7	0.734	19.9

2.2.3 Analysis

From Reference 26, the following internal quantum efficiency formulae apply to a uniform semiconductor under either frontwall (FW) or backwall (BW) illumination with: (1) minority carrier collection at a transparent front junction, (2) high or infinite surface recombination at the back, (3) thickness t, (4) diffusion length L, (5) optical absorption coefficient α and (6) total collection in a space charge width w, near the junction.

$$IQE_{FW} = 1 - e^{-\alpha w} + \frac{\alpha L e^{-\alpha w}}{(\alpha L)^2 - 1}\left[\alpha L - \frac{\left[\cosh\left(\frac{t-w}{L}\right) - e^{-\alpha(t-w)}\right]}{\sinh\left(\frac{t-w}{L}\right)}\right] \tag{10}$$

$$IQE_{BW} = \left(1 - e^{-\alpha w}\right)e^{-\alpha(t-w)} + \frac{\alpha L}{(\alpha L)^2 - 1}\left[\frac{1 - \cosh\left(\frac{t-w}{L}\right)e^{-\alpha(t-w)}}{\sinh\left(\frac{t-w}{L}\right)} - \alpha L e^{-\alpha(t-w)}\right] \tag{11}$$

These equations are used to represent the minority carrier collection in the $Cu(In,Ga)Se_2$ solar cells.

If the internal quantum efficiencies can be determined from the measured spectral responses of $Cu(In,Ga)Se_2$ devices equations, Equations 10 and 11 can be applied to find L, w and α. The calculated and measured QE's can then be compared for consistency. Because the optical absorption of the ZnO/CdS is fairly small and constant (Figure 5) in the wavelength region of interest (750 - 1050 nm), the measured QE_{FW} and IQE_{FW} will differ only by a constant. This constant can be determined to a good approximation by the maximum value of the measured QE_{FW}, by assuming 100% collection in the $Cu(In,Ga)Se_2$ at short wavelengths. Because of the absorption coefficient of $Cu(In,Ga)Se_2$ approaches 10^5 cm^{-1} at energies above the band gap, this is a reasonable assumption.

$$IQE_{FW}(\lambda) = \frac{QE_{FW}(\lambda)}{QE_{FW}(max)} \tag{12}$$

By noting that IQE_{FW} and IQE_{BW} must be the same for uniform light absorption, the constant to correct QE_{BW} can be determined from QE measurements at longer wavelengths (this is in the wavelength region where the value of QE_{FW} is on the order of 10^{-2} to 10^{-3}).

$$IQE_{BW}(\lambda) = \left\{ \frac{IQE_{FW}}{QE_{BW}}(\lambda_{long}) \right\} QE_{BW}(\lambda) \tag{13}$$

2.2.4 Results

The measured bi-facial spectral responses at different voltage biases for the $Cu(In,Ga)Se_2$ solar cells with semi-transparent Mo contacts of Table II are shown in Figure 6. The bi-facial internal quantum efficiencies are shown in Figure 7. Also shown in Figure 7 are the internal quantum efficiencies calculated from fitting the measured data to Equations 10 and 11. Table III and Figure 8 give the parameters used for the calculated internal quantum efficiencies.

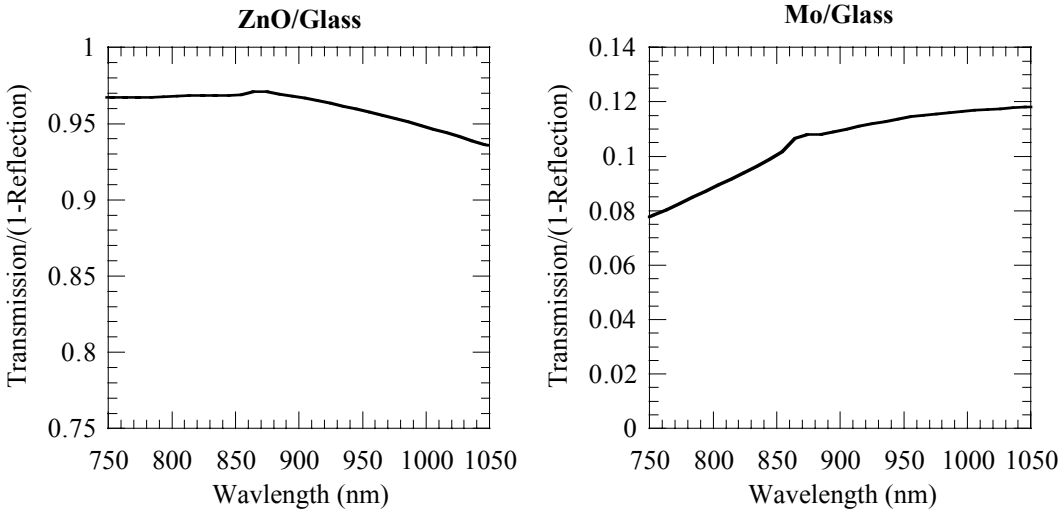


Figure 5. Optical absorption measured through both the ZnO and 0.04 µm thick semi-transparent Mo in the wavelength region of analysis.

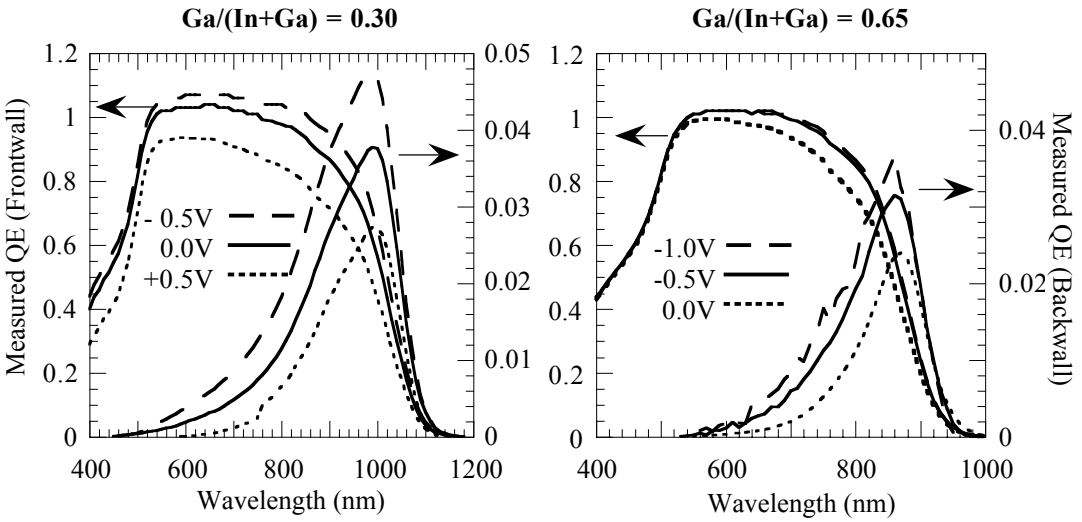


Figure 6. Spectral responses measured at different voltage biases through both the ZnO/CdS (frontwall) and semi-transparent Mo contact (backwall) for cells containing 30% and 65% Ga.

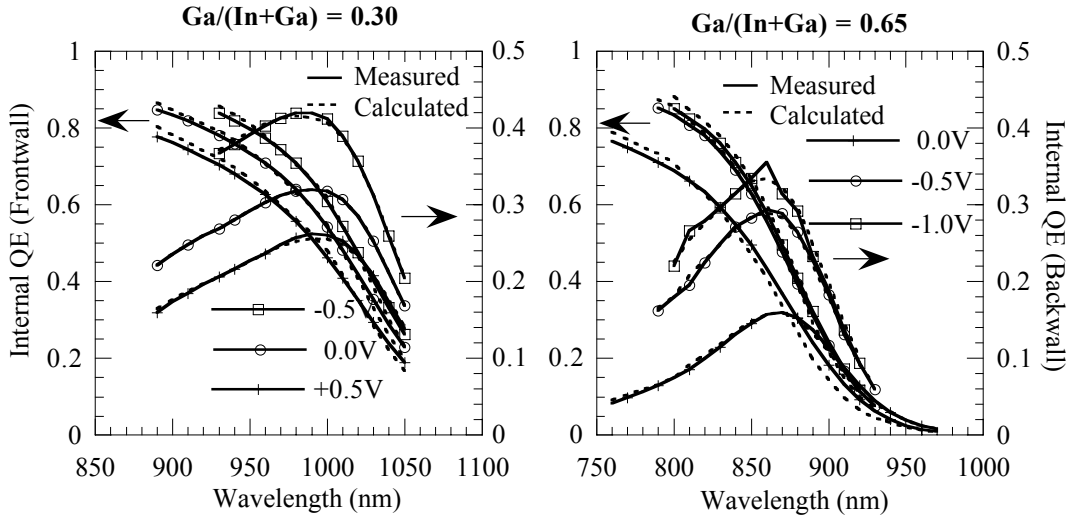


Figure 7. Calculated (from the parameters in Table III) and measured internal quantum efficiencies at different voltage biases through both the ZnO/CdS (frontwall) and semi-transparent Mo contact (backwall) for cells containing 30% and 65% Ga.

Table III. Diffusion lengths and collection widths from the calculated internal quantum efficiencies (Figure 7) and optical absorption coefficients (Figure 8).

		Collection Width: w (μm) Voltage Bias (Volts)			
Ga/(In+Ga)	**L (μm)**	**-1.0**	**-0.5**	**0.0**	**+0.5**
0.30	0.8		1.4	1.0	0.7
0.65	0.1	1.3	1.2	0.7	

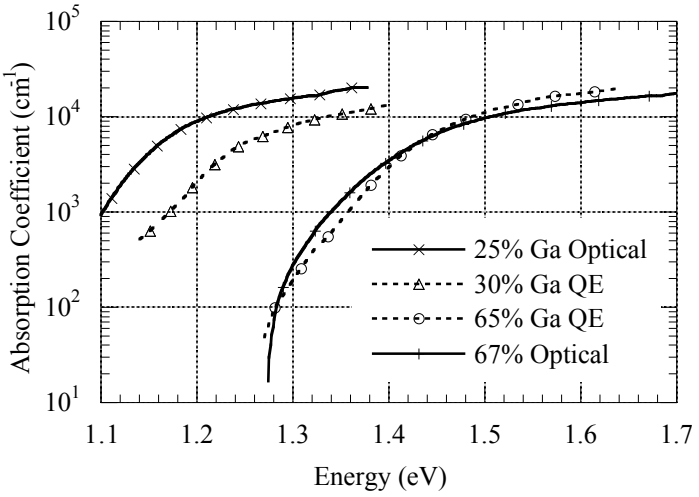


Figure 8. Optical absorption coefficients derived from measured optical data for films containing 25% and 67% Ga and from the internal quantum efficiency measurements for the cells containing 30% and 65% Ga.

2.2.5 Conclusions

The results of Table III show why there is a decrease in the light generated current with increasing voltage for samples with higher Ga content. If the total width for minority carrier collection is w + L (drift + diffusion), then this quantity is already less than 1 μm at J_{SC} (0.0V) for 65% Ga. Because this width is dominated by drift, it will continue to decrease with increasing forward bias, leading to a lowered FF and a substantial $J_L(V)$.

This method also produces the optical absorption coefficient (α) for the samples as shown in Figure 8. The comparison with absorption coefficients derived from optical reflection and transmission measurements of $Cu(In,Ga)Se_2$ films made with comparable Ga concentrations is fairly good. Care must be used in the interpretation at small values of α derived from QE because of the reflected light from the Mo back contact creating additional optical absorption and minority carrier generation in the $Cu(In,Ga)Se_2$ (this would increase the calculated α above its true value).

It has been shown that the analysis of bi-facial quantum efficiency measurements can be a useful tool in determining the minority carrier collection properties of Cu(In,Ga)Se2 devices under actual operating conditions.

3. CdTe-based Solar Cells

3.1 Influence of Processing Conditions on Performance and Stability in Polycrystalline Thin-Film CdTe-based Solar Cells

3.1.1 Introduction

This section addresses three aspects of thin-film CdTe-based solar cells critical to performance and stability using a superstrate configuration: the role of the window layer on open circuit voltage; diffusion of CdS into the CdTe-based absorber layer during $CdCl_2$ treatment; and the role of the treatments used to fabricate back contacts. Section 3.2 describes the chemical and electrical characterization of the back contact in greater detail. Optimal performance is conventionally obtained by utilizing the thinnest CdS thickness possible while maintaining uniform coverage; this allows open circuit voltage to be maintained while maximizing short circuit current. For each CdTe/CdS fabrication technology under investigation, a certain degree of pinholes can exist in the CdS films, and the CdS is consumed during post-deposition thermal treatments. If a suitable TCO/window layer can be found, and if the CdS diffusion could be controlled, a more robust process with reduced $CdCl_2$ processing time could be developed. Finally, the post-deposition thermal treatments require oxygen, which oxidizes the CdTe surface, creating the need for a surface modification treatment before contact can be made. Optimal V_{oc} and FF are obtained when copper is reacted with the CdTe surface and is diffused into the CdTe layer. This paper presents data for physical vapor deposited cells demonstrating that a high resistance layer between conductive TCO can allow V_{oc} to be maintained as CdS thickness is reduced. Control of CdS diffusion is demonstrated by annealing the CdTe/CdS structure prior to $CdCl_2$ treatment or by using a $CdTe_{1-x}S_x$ alloy absorber layer in place of CdTe. The effects of contacting treatments on the current-voltage behavior and implications for stability are also presented.

3.1.2 Film Deposition and Device Fabrication

CdTe/CdS devices were fabricated in a superstrate configuration on glass coated with a transparent conductive oxide (TCO). Different bilayer TCO configurations were used to examine the effects of a high resistance interlayer between the TCO and CdS. Single layer indium-tin oxide (ITO) films 200 nm thick and 20 Ω/sq were used as superstrates for the bilayer structures. The low resistivity single layers were deposited by sputtering in flowing Ar/O_2 at 5 mTorr; the high resistivity second ITO layers were obtained by increasing the oxygen concentration. Bilayer structures using indium oxide (In_2O_3) films were formed by oxidation of elemental indium films deposited directly onto the low resistivity single layers. Bilayer tin oxide (SnO_2) superstrates were also evaluated using low resistivity SnO_2 made by Libby Owens Ford over-coated with a high resistivity SnO_2 layer at Golden Photon, Inc. The thickness and resistivity of the high-resistivity layers are shown in Table IV.

CdS films from 10 to 210 nm thick were evaporated onto the TCO surface at 220°C and 3 Å/s from 99.999% purity CdS powder. Prior to CdTe deposition the CdS/ITO/glass structures were treated in $CdCl_2$ vapor at 420˚C in air for 15 minutes to limit Te diffusion into CdS [27]. CdTe films were evaporated onto the treated CdS at 250°C and 40 Å/s from 99.999% purity CdTe

powder. For devices, the CdTe film thickness ranged from 4 to 5 μm. To examine the dependence of the CdS diffusion into the absorber layer during post-deposition processing, different absorber layers and different post-deposition treatments were employed. Absorber layers consisting of pure CdTe and uniform $CdTe_{1-x}S_x$ alloy with x = 0.05 were deposited by evaporation of CdTe and co-evaporation of CdTe and CdS powders, respectively [28]. Two post-deposition treatments were compared: $CdCl_2$:O_2:Ar treatment only and an anneal in Ar at 1 Torr at 600˚C for 4 minutes followed by $CdCl_2$ treatment [29]. $CdCl_2$:O_2:Ar treatments were carried out in a reactor configured to deliver fixed amount of $CdCl_2$ vapor at a partial pressure of 5-10 mTorr to the CdTe surface at different reaction temperatures, times, and oxygen concentrations.

Back contact to CdTe was formed by a surface modification treatment followed by reaction with Cu. The surface modification treatment consisted of sequential reactions with Br_2:CH_3OH, acidic $K_2Cr_2O_7$ solution, and aqueous N_2H_4. Reaction with Cu was carried out by evaporation of a Cu layer, followed by heat treatment at 200˚C in vacuum for 30 minutes, and then etching the structure in Br_2:CH_3OH solution to remove metallic Cu as described in Reference 30. To complete the devices, a current carrying conductor, such as carbon, was applied to the modified surface, followed by mechanical scribing to isolate each device.

Table IV. Transparent conductive oxide configurations and properties.

TCO Structure	Interlayer Thickness (nm)	Exposed Layer Resistivity (Ω-cm)
Single Layer ITO	0	4×10^{-4}
ITO/ITO	50	50
ITO/ITO	100	1
ITO/In_2O_3	120	>100
SnO_2/SnO_2	~100	>1

3.1.3 Materials and Device Measurements

The phase composition of the TCO surface layers and of the CdTe back surface at different stages in the processing sequence was determined from wide-angle glancing-incidence x-ray diffraction measurements made with a Philips Electronics X'PERT thin-film diffractometer using Cu-kα radiation at an incident beam angle of 1˚. Narrow-angle θ/2θ x-ray diffraction patterns of the (511) were obtained to determine the CdS uptake in the absorber during the treatment. To permit detection of the interfacial region, samples with absorber layers ~2 μm thick were utilized.

Cross-sectional transmission electron microscopy (TEM) with a Philips EM400T microscope was used to evaluate the crystal quality of individual grains and the integrity of the CdTe-CdS interface after the treatments. Samples were prepared by cutting slabs from the structure, mechanical polishing to 10 μm lateral thickness, followed by Ar ion-milling at 5 kV to electron transparency thicknesses using a Gatan Dual ion mill.

Device performance was characterized by current-voltage (J-V) measurements measured at 25˚C under AM 1.5 simulation at 100 mW/cm^2. Final CdS thicknesses in devices was determined

from quantum efficiency measurements at 400-450 nm and were corroborated by depth profilometry of the CdS layer after removal of the absorber layer.

3.1.4 Effect of the Transparent Conductive Oxide/CdS Window Layer Combination

Devices incorporating a high resistivity interlayer between the CdS and the current-carrying TCO layers exhibit enhanced V_{oc} for CdS < 100 nm. Figure 9 shows light and dark J-V data for devices from the same CdS and CdTe depositions but with single layer and bilayer sputtered ITO. The ITO interlayer was 100 nm thick, and the final CdS thickness in these devices was 70 nm ± 5 nm. The J-V behavior of the two samples is similar, but the sample with bilayer ITO exhibits 180 mv higher V_{oc}.

Similar results have been found for devices using other bilayer approaches as shown in Figure 10. For samples with d(CdS) < 140 nm, a fall-off in V_{oc} was obtained using single layer ITO superstrates. Compared to this trend, devices with a high resistance interlayer from 50 to 120 nm thick allow V_{oc} to be maintained. In Figure 10, two devices having SnO_2 bilayers (GPI SnO_2) with d(CdS) < 1 nm are shown; the sample with V_{oc} ~ 730 mV was fabricated with an initial CdS film < 40 nm thick, while the sample with V_{oc} ~ 550 mV had no CdS layer. This suggests that reaction of CdS with CdTe and/or the TCO are related to the V_{oc}-limiting mechanism. Also, utilization of a high resistivity interlayer relaxes the degree of processing tolerance with respect to CdS thickness.

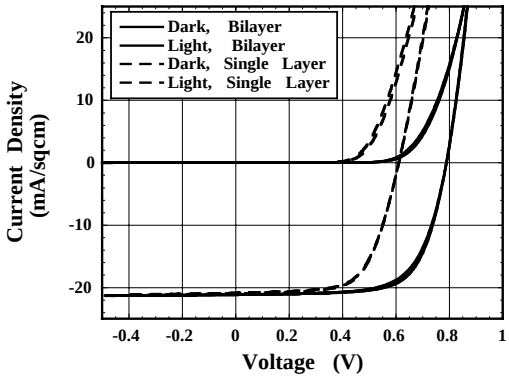


Figure 9. Dark and light J-V measurements of physical vapor deposited CdTe/CdS with single layer and bilayer ITO superstrates.

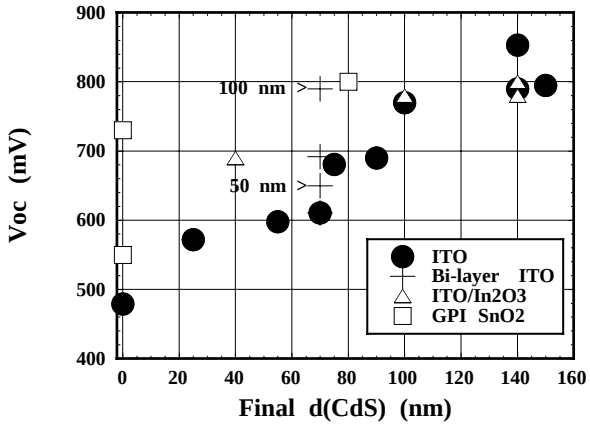


Figure 10. V_{oc} versus final CdS thickness in physical vapor deposited CdTe/CdS devices with different TCO structures.

3.1.5 CdS/CdTe Interaction

It has been shown that during $CdCl_2$ vapor treatment, the diffusion of CdS into the absorber layer proceeds faster than the diffusion of CdTe into the CdS and is enhanced by O_2 pressure, $CdCl_2$ pressure, and reaction temperature [31, 32]. Figure 11 shows the time dependence of CdS uptake by the absorber layer for physical vapor deposited CdTe/CdS/ITO/7059 structures at fixed $CdCl_2$ vapor pressure = 10 mTorr. CdS uptake is enhanced by both temperature and oxygen concentration. Reducing $CdCl_2$ processing time from 20 minutes to 1-2 minutes while maintaining baseline device performance by merely increasing temperature results in enhanced CdS uptake. Two solutions were found to overcome this problem: 1) anneal CdTe/CdS prior to $CdCl_2$ treatment to reduce grain boundary and other defect density and 2) utilize $CdTe_{1-x}S_x$ absorber layer with x near solubility limit of processing temperature [8]. Figure 12 shows x-ray diffraction (511) line profile of three cases *after* $CdCl_2$ treatment which illustrate this point. The broad doublet is typical of low-temperature ($T < 400^{\circ}C$) deposited CdTe/CdS structures after $CdCl_2$ treatment. The peak at 76.3˚ is typical of either low-temperature deposited CdTe films which have been annealed or of high-temperature deposited films ($T > 500^{\circ}C$). The peak near 76.8˚, near the solubility limit for CdS in CdTe at 420˚C, is for a $CdTe_{0.95}S_{0.05}$ absorber layer; no anneal was needed since the diffusion driving force was reduced by the composition of the absorber. TEM data showed that the anneal step reduced crystallographic defect density. Baseline device performance was achieved with either processing change, and the use of the anneal allowed a 10% device to be fabricated with a 2 minute $CdCl_2$ treatment at 460˚C. These innovations widen the processing window and should be applicable to all CdTe/CdS structures deposited at low temperature.

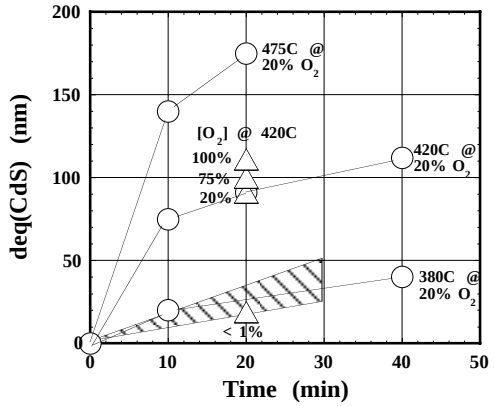


Figure 11. Equivalent CdS film thickness diffused into CdTe absorber layer versus $CdCl_2$:O_2:Ar vapor treatment time at constant $CdCl_2$ concentration. Triangular points are for treatments at different O_2 concentration. Hatched band indicates range of results for films treated at 420˚C with either $CdTe_{0.95}S_{0.05}$ absorber layer or CdTe absorber layer and 600˚C anneal prior to $CdCl_2$ treatment, resulting in similar CdS uptake.

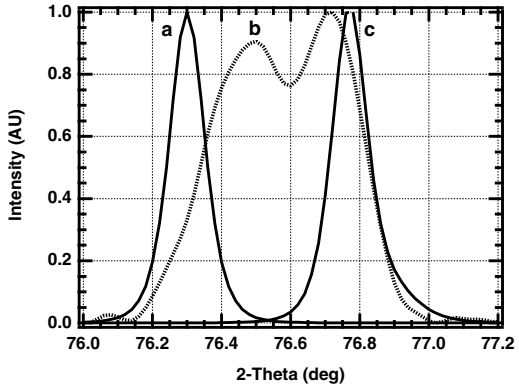


Figure 12. X-ray diffraction (511) line profiles after $CdCl_2$:O_2:Ar vapor treatment at 420˚C for 20 minutes: a) CdTe absorber layer with 600˚C anneal prior to $CdCl_2$ treatment; b) CdTe absorber layer with no anneal prior to $CdCl_2$ treatment; c) $CdTe_{0.95}S_{0.05}$ absorber layer with no anneal.

3.1.6 Contact to CdTe

Glancing incidence x-ray diffraction of the $CdTe_{1-x}S_x$ surface after $CdCl_2$:O_2:Ar treatment reveals the presence of CdO and $CdTeO_3$ phases. CdO forms as the by-product of the reaction:

$$CdCl_2\ (g) + O_2\ (g) + CdTe_{1-x}S_x\ (s) <=> (1-x)TeCl_2\ (g) + xSCl_2\ (g) + 2CdO\ (s),$$

$$\Delta G_{rxn}(400^{\circ}C) \sim -49 \text{ kcal/mol.} \qquad (14)$$

Glancing incidence x-ray diffraction scans further show that sequential reaction in acidic dichromate solution and hydrazine removes oxides and forms a Te residue. Ohmic electrical contact to $CdTe_{1-x}S_x$ is facilitated by delivery of Cu to the $CdTe_{1-x}S_x$ surface and an activation treatment. The treatment diffuses Cu into both bulk and grain boundary regions of the $CdTe_{1-x}S_x$

layer and completes the reaction between Cu and Te to form copper tellurides. The effects of the surface treatment and the relative quantity of Cu are seen in Figure 13. With no surface preparation or Cu deposition after $CdCl_2$ treatment, both dark and light behavior are dominated by blocking behavior. With only the dichromate and hydrazine treatment but no Cu deposition, contact behavior becomes less blocking, but V_{oc} and FF remain low. Deposition of 5 to 15 nm of Cu and subsequent reaction at 200˚C for 30 minutes reduces contact resistance further and increases V_{oc} and FF. We have found that for this treatment schedule, use of Cu > 40 nm causes shunting. It is thus expected that sustained thermal stressing of devices with even slight Cu excess will degrade the $CdTe_{1-x}S_x$/CdS junction. Glancing incidence x-ray diffraction of these reacted surfaces show phases of copper tellurides [10]. Ohmic and blocking behavior at room temperature were obtained when the surface was dominated by Cu_2Te and CuTe, respectively.

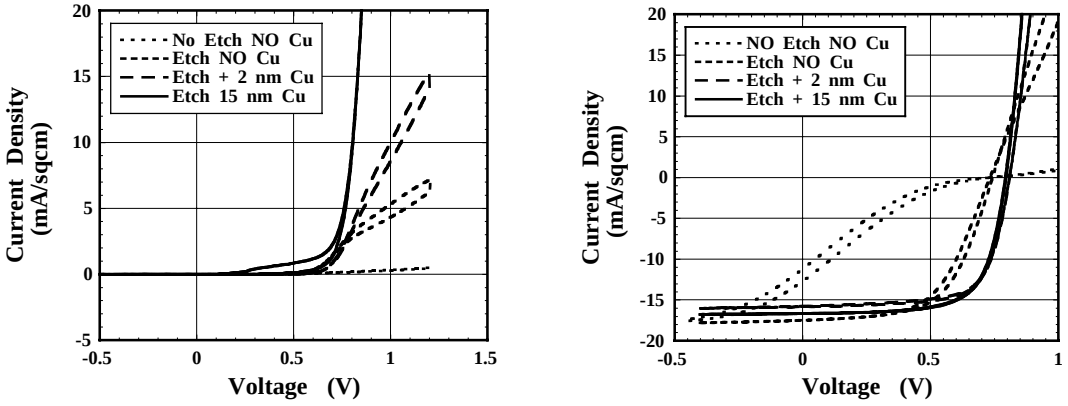


Figure 13. Dark (left) and light J-V measurements of CdTe/CdS with varying post-$CdCl_2$ processing.

3.1.7 Conclusions

Critical aspects of processing CdTe-based thin film solar cells have been addressed. The use of high resistivity interlayers between the transparent conductive oxide and the CdS allows high V_{oc} to be maintained as the CdS thickness is reduced. CdS-CdTe interdiffusion is reduced by either use of a short 600˚C anneal prior to $CdCl_2$ vapor treatment or by use of $CdTe_{1-x}S_x$ alloy absorber layers, which should facilitate reduction in $CdCl_2$ treatment time. Cu used in the contacting process dopes CdTe and forms a Cu_2Te surface layer. The chemical nature of back surface affects performance and stability.

3.2 Characterizing Contacts to p-Type CdTe in CdS/CdTe Solar Cells

3.2.1 Introduction

In superstrate CdTe-based thin film solar cells, the electrical behavior of the p-type CdTe contact depends upon the conductivity of the CdTe and the resulting band alignment between the CdTe and the contact material. The requirement of low contact resistance for optimal performance of the device means that the contact must provide a negligible barrier to majority carriers when operating at forward bias. In order to maintain a low resistance contact on superstrate CdS/CdTe

devices, it is necessary to control the electrical conductivity of the CdTe layer and its exposed surface. In practice, this is achieved by controlling post-deposition processing parameters such as heat treatment and chemical surface modification [33, 30]. The degree of post-deposition processing needed to attain the desired conductivity depends in part on the technique used to form the CdTe layer, but all cell making processes rely on formation of a p+ layer on the CdTe surface to form the primary contact to CdTe. Typically, Cu, excess Te, or combinations of these and other materials are used to facilitate contact formation. In earlier papers we described a contacting procedure that is applicable to CdTe made by several methods [30, 34]. The resulting CdTe contact can exhibit various degrees of leaky diode "blocking" behavior under different conditions: 1) at room temperature if insufficient Cu is used; 2) at lower temperatures; and 3) after stressing devices at V_{OC} and T ~ 100˚C [35]. In stress-degraded devices, removing the current-carrying contact, re-etching the surface, and re-applying a contact removes the leaky diode "blocking" behavior. Thus, this behavior can be attributed to the CdTe/contact interface. To gain additional information about the nature of the CdTe contact surface, glancing incidence x-ray diffraction measurements were made. Making measurements at each processing stage directly revealed the chemical effect of each processing step.

3.2.2 Experimental

Thin film CdS/CdTe films were deposited by thermal evaporation from high purity CdS and CdTe source powders in a superstrate configuration onto ITO-coated Corning 7059 glass as indicated in Figure 14.

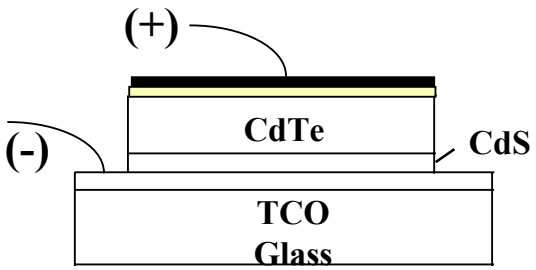


Figure 14. Cross-section schematic of CdS/CdTe solar cell. The gray band between the CdTe layer and the black current-carrying conductor represents the primary electrical contact to CdTe.

The CdS and CdTe thicknesses were 0.18 μm and 4 to 5 μm, respectively. Prior to contact processing, the structures were heat treated in a vapor mixture of $CdCl_2$ and O_2 [32]. The primary contact to the CdTe surface was prepared by a six-step wet chemical process (Table V).

At different stages of surface preparation, glancing incidence x-ray diffraction measurements were made at 1˚ incident beam angle with Cu-kα x-rays to determine the chemical phase composition of the contact region. At glancing incident beam angles of ~1˚, the sampling depth is ~100 nm.

Table V. Processing steps used after $CdCl_2$:O_2 heat treatment to form primary contact to p-type CdTe.

Contact Process
Reaction in Br_2:CH_3OH
Reaction in aqueous $K_2Cr_2O_7$:H_2SO_4
Reaction in aqueous N_2H_4
Evaporation of 15 nm Cu
Vacuum heat treatment at 200°C
Reaction in Br_2:CH_3OH

Following the last bromine-methanol reaction, Acheson 505SS carbon ink conductor was applied to the surface, and the area of the devices was defined by mechanical scribing [30]. Current-voltage (*J-V*) measurements were made in the dark and under Xe arc lamp illumination. Measurements at different temperatures allowed determination of the barrier heights of the main CdS/CdTe junction and the primary CdTe contact.

3.2.3 J-V Measurements and Analysis

The J-V behavior at various temperatures for a CdS/CdTe device made by physical vapor deposition with a carbon contact is shown in Figure 15. At room temperature and above, the slopes (dV/dJ) of the forward bias dark and light characteristics decrease monotonically with increasing voltage. At -50˚C, however, the dark and light forward bias J-V characteristics exhibit an inflection point ("blocking" behavior) in forward bias. Similar "blocking" behavior has been obtained at room temperature after thermal and electrical stressing [35] and for devices made without copper in the contacting process [30]. Finally, we have found that for stress-degraded devices, the "blocking" behavior can be eliminated by removing the original contact, re-etching the surface, and applying a new contact. All of this suggests the existence of a junction in the interface between CdTe and the current-carrying conductor whose properties depend critically on sample preparation and subsequent treatment.

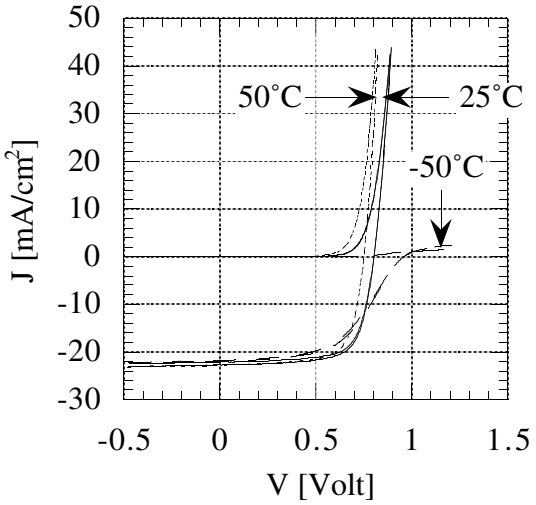


Figure 15. J-V data of a CdS/CdTe device under AM1.5G illumination and dark showing the effect of the contact at various temperatures.

The device is modeled with an equivalent circuit series connection of a temperature independent resistance (R_0), a leaky diode representing the contact (J_C) and a diode representing the main CdS/CdTe junction (J_J) (Figure 16).

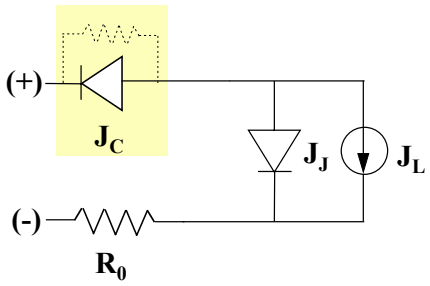


Figure 16. Equivalent circuit model with a temperature independent resistance (R_0), a leaky diode representing the contact (J_C) and a diode representing the main CdS/CdTe junction (J_J).

The primary CdTe/contact is shown with a shunt path to account for non-zero slope at far forward bias. To model circuit behavior near the device V_{oc}, however, we only consider the two diodes, the lumped resistor, and the current generator. This model assumes that the two diodes are electrically separate and that the back diode operates only as a dark diode.

In forward bias, near V_{oc} of the main junction, the total series resistance of the device is the sum of contributions from the lumped resistor, R_0, and the primary contact, R_C:

$$R_S = R_0 + R_C, \tag{15}$$

where the R_C contribution is due to the contact diode:

$$R_C = \frac{V_C}{J_C}. \tag{16}$$

The forward current through the equivalent circuit is limited by the contact diode current, J_C, and can be represented as:

$$J = -J_{00_C} e^{-\frac{\Phi_C}{kT}} \left(e^{\frac{qV_C}{A_C kT}} - 1 \right), \tag{17}$$

where the prefactor, J_{00C}, and exponent, $e^{-\Phi/kT}$, are the reverse saturation current of the contact diode, J_{0C}. For small voltage drops, $qV_C/A_CkT \ll 1$, Equation 17 reduces to:

$$J \approx \frac{qJ_{00_C}}{A_C kT} e^{-\frac{\Phi_C}{kT}}. \tag{18}$$

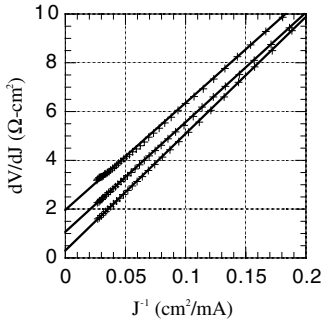
Substituting into Equation 15 and solving for R_C:

$$R_C = R_S - R_0 \approx \frac{A_C kT}{qJ_{00_C}} e^{\frac{\Phi_C}{kT}}. \quad (19)$$

The barrier height for the contact diode, F_C, was obtained from the Arrhenius slope, $\ln(R_C)$ versus q/kT. R_S was evaluated from measurements of the device forward bias slope, dV/dJ, at elevated temperatures:

$$\frac{dV}{dJ} = R_S + \frac{(A_J kT)}{q(J + J_L)}. \quad (20)$$

The temperature dependence of the dark forward bias slope, dV/dJ, is shown in Figure 17 for different measurement temperatures. At high temperature, $R_C \sim 0$, and $R_S \sim R_0$. Using the minimum R as R_0 (0.3 Ω-cm^2), the contact diode barrier height was determined using Equation 19 to be 0.33 eV (Figure 18).



T (°C)	R_s (Ω-cm^2)
10	1.95
25	1.05
80	0.28

Figure 17. dV/dJ derived from dark J-V measurements for a CdS/CdTe device showing the temperature dependence of R_s. From this data, the minimum value of R_s (0.3 -Ωcm^2) is taken as R_0.

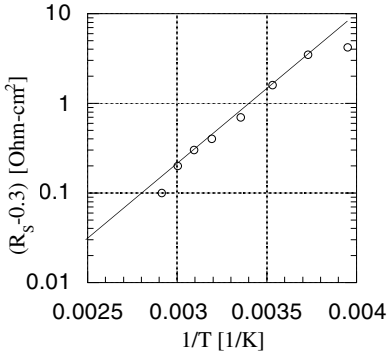


Figure 18. Temperature dependence of R_s with R_0 = 0.3 (Ω-cm^2) derived from dark J-V measurements for a CdS/CdTe device. This contact had a barrier height of 0.3 eV.

The barrier height, F_J, of the main diode was evaluated at 0K from V_{OC} versus T, since the contact diode, for a CdTe thickness of 4 μm, is in the dark:

$$V_{oc} = (A_J kT/q) Ln\left(\frac{J_{sc}}{J_{00_J}} e^{-\frac{\Phi_J}{A_J kT}}\right), \quad (21)$$

$$V_{oc} = \Phi_J + (A_J kT/q) Ln\left(\frac{J_{sc}}{J_{00_J}}\right). \quad (22)$$

The main junction barrier height was found to be ~1.4 eV (Figure 19). The linear behavior over this temperature range demonstrates that the J = 0 bias point of the entire device is not affected by the contact.

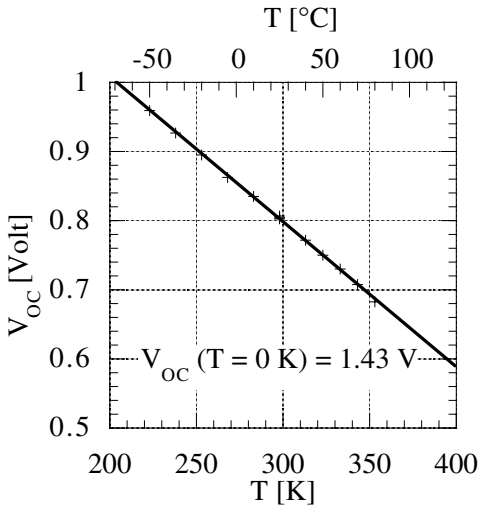


Figure 19. V_{oc} as a function of temperature for a CdS/CdTe device under AM1.5G illumination.

3.2.4 CdTe Contact Surface Analysis

In previous work, we speculated that the chemical process used to prepare the CdTe for application of a current-carrying conductor produced copper tellurides [30]. This has now been confirmed by direct detection of Cu_2Te and CuTe phases with glancing incidence x-ray diffraction. The correlation of the glancing incidence x-ray diffraction surface analysis with reaction products expected based on chemical free-energy calculations is described below. During $CdCl_2$:O_2 vapor heat treatment, CdTe reacts with $CdCl_2$ and O_2 resulting in production of CdO on the surface of the CdTe grains according to the reaction:

$$CdCl_2\ (g) + O_2\ (g) + CdTe\ (s) <=> TeCl_2\ (g) + 2CdO\ (s), \quad (23)$$

$$\Delta G_{rxn}(400^{\circ}C) = -49.33\ \text{kcal/mol}. \quad (24)$$

This system leads to the Guldberg and Waage expression of overall chemical equilibrium,

$$K_1 = [TeCl_2][CdO]^2/[CdCl_2][O_2][CdTe], \quad (25)$$

in which the quantity of CdO obtained will vary as the square root of O_2 concentration. It is necessary to remove the surface CdO to allow delivery of dopant to the near-surface CdTe and to facilitate formation of a low resistance contact. The CdO is removed by reaction with bromine, which also liberates free Te.

Reaction of CdTe and CdO in Br_2:CH_3OH are shown to be thermodynamically favored according to:

$$2CdO\ (s) + 2Br_2\ (l) <=> 2CdBr_2\ (s) + O_2\ (g), \quad (26)$$

$$\Delta G_{rxn}(25^{\circ}C) = -32.29\ \text{kcal/mol}, \quad (27)$$

and

$$CdTe\ (s) + Br_2\ (l) <=> CdBr_2\ (s) + Te\ (s), \quad (28)$$

$$\Delta G_{rxn}(25^{\circ}C) = -47.98\ \text{kcal/mol}. \quad (29)$$

The product $CdBr_2$ is soluble in methanol and water and is removed from the surface by agitation and rinsing. The reaction to form elemental Te from lattice-bound Te^{2-} is further described by the room temperature half-cell reactions at the surface:

$$Br_2\ (l) + 2e^- <=> 2Br^-,\ E^o = +1.065V, \quad (30)$$

$$Te^{2-}\ (s) <=> Te^o\ (s) + 2\ e^-,\ E^o = +0.92V. \quad (31)$$

Adding these reactions and potentials, the highly favored overall reaction is expected:

$$Br_2\ (l) + Te^{2-}\ (s) <=> 2\ Br^- + Te^o\ (s),\ E^o = +1.985V. \quad (32)$$

X-ray photoemission spectroscopic (XPS) analysis by Danaher, et. al. [36] on single crystal CdTe reacted in 0.01% (vol) Br_2:CH_3OH showed Cd-depletion at the surface, extending 3 nm into the surface. They determined an oxidation rate of free Te to be 0.02 nm/minute, according to the favored reaction:

$$Te\ (s) + O_2\ (g) <=> TeO_2\ (s), \quad (33)$$

$$\Delta G_{rxn}(25^{\circ}C) = -64.39\ \text{kcal/mol}. \quad (34)$$

The thin Te coating produced by etching in Br_2:CH_3OH is not extensive and oxidizes rapidly, diminishing the benefits for doping or contacting; the bromine step is therefore primarily used to eliminate CdO.

The reaction of CdTe in aqueous K_2CrO_4 produces TeO_2 according to:

$$2\ CrO_4^{2-} + Te\ (s) <=> CrO_3 + Cr^{6+} + TeO_2\ (s) \quad (35)$$

The addition of protons to the solution by addition of acid complicates the ionic makeup of the solution. At low pH, the primary effect is the reduction of the chromate ion to dichromate:

$$2\ CrO_4^{=} + 2\ H^+ <=> Cr_2O_7^{2-} + H_2O, \quad (36)$$

and the production of chromic acid:

$$CrO_4^{2-} + 2\ H^+ <=> H_2CrO_4. \quad (37)$$

Elemental Te is readily liberated from the CdTe lattice by electrolytic reaction with the chromate or hypochromous ion. The overall favored reactions and room temperature potentials are:

$$Cr_2O_7^{2-} + 14\ H^+ + 3\ Te^{2-} <=> 3\ Te^o + 2\ Cr^{3+} + 7\ H_2O, \ E^o = +2.07V, \quad (38)$$

$$HCrO_4^- + 7\ H^+ + Te^{2-} <=> Te^o + Cr^{3+} + 4\ H_2O, \ E^o = +2.115V. \quad (39)$$

XPS and studies by Danaher , et al. [36] on single crystal CdTe reacted in aqueous K_2CrO_4 and in $K_2Cr_2O_7$:H_2SO_4 solution confirmed this chemistry, indicating Cd-depleted surface in all cases, with TeO_2 on the surface reacted with aqueous K_2CrO_4 and elemental Te on the surface reacted with 1:1 $K_2Cr_2O_7$:H_2SO_4. Mixed Te:TeO_2 was obtained on samples reacted with lower acid concentrations. Secondary ion mass spectroscopic depth profiles of reacted CdTe/CdS/ITO films further indicated that Cr penetrated the CdTe film but did not accumulate within the CdS/ITO films [36].

As a final step in producing a Te-enriched surface, reaction in hydrazine solution is carried out. Reactions with TeO_2 powder and 98:2 N_2H_4:H_2O solution at 25-40˚C released significant quantities of gas and changed the solution color from clear to faint purple. Similar results were obtained when etching CdTe films after reaction with $K_2Cr_2O_7$:H_2SO_4. These observations are consistent with reduction of TeO_2:

$$TeO_2\ (s) + N_2H_4\ (l) <=> Te\ (s) + 2\ H_2O\ (l) + N_2\ (g), \quad (40)$$

$$\Delta G_{rxn}(40^\circ C) = -85.0\ \text{kcal/mol}. \quad (41)$$

Direct reaction of CdTe with N_2H_4 to produce either elemental Cd or Te is not thermodynamically favored. Glancing incidence x-ray diffraction measurements of CdTe/CdS/ITO thin films confirm the formation of elemental Te after the entire reaction process as shown in Figure 20 (bottom).

Thus, reaction in acidic dichromate solution liberates additional Te but also forms TeO_2, depending on the solution pH. Reaction in hydrazine reduces TeO_2 to Te. Deposition and *in situ* heat treatment of this surface with elemental Cu diffuses some Cu into CdTe and leads to production of copper tellurides:

$$Te\ (s) + 2\ Cu\ (s) <=> Cu_2Te\ (s), \quad (42)$$

$$\Delta G_{rxn}(200^\circ C) = -12.13\ \text{kcal/mol}, \quad (43)$$

and

$$Te\ (s) + Cu\ (s) <=> CuTe\ (s), \quad (44)$$

$$\Delta G_{rxn}(200^\circ C) = -6.47\ \text{kcal/mol}. \quad (45)$$

The equilibrium T-x phase diagram for the Cu-Te system shows the possible phases obtained over the full range of relative quantities of Cu and Te [37]. The possible equilibrium phase fields are Cu + Cu_2Te, $Cu_{2-x}Te$, $Cu_{2-x}Te$ + Cu_3Te_2, and Cu_3Te_2 + CuTe, depending on the relative quantities of Cu and Te. Figure 20 (middle) shows that for excess Cu, the heat treatment produces Cu_2Te.

Figure 20 (top) shows that reaction with bromine removed excess Cu and resulted in both Cu_2Te and CuTe surface phases in an as-yet undetermined configuration. The favored reactions for this are:

$$Cu\ (s) + Br_2\ (l) <=> CuBr\ (s), \tag{46}$$

$$\Delta G_{rxn}(25^{\circ}C) = -29.01\ \text{kcal/mol}, \tag{47}$$

$$CdTe\ (s) + 2\ Cu\ (s) + Br_2\ (l) <=> Cu_2Te\ (s) + CdBr_2\ (s), \tag{48}$$

$$\Delta G_{rxn}(25^{\circ}C) = -50.82\ \text{kcal/mol}, \tag{49}$$

and

$$CdTe\ (s) + Cu\ (s) + Br_2\ (l) <=> CuTe\ (s) + CdBr_2\ (s), \tag{50}$$

$$\Delta G_{rxn}(25^{\circ}C) = -54.24\ \text{kcal/mol}. \tag{51}$$

In both reactions, the bromide products are soluble in methanol and water and are thus removed by agitation or rinsing. Preliminary experiments show that increasing the proportion of cupric to cuprous tellurides in the final surface increases the non-ohmic contact behavior.

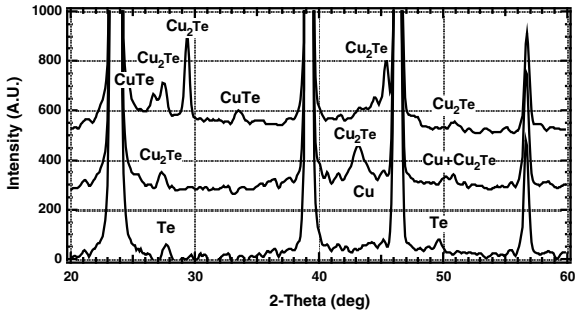


Figure 20. Glancing incidence X-ray diffraction patterns of the CdTe surface after three contact treatment steps: (bottom) after hydrazine reaction; (middle) after Cu deposition and vacuum heat treatment; and (top) after bromine reaction.

3.2.5 Conclusions

CdS/CdTe solar cells have been analyzed to model the behavior of the CdS/CdTe junction and CdTe contact. The analysis was applied to devices fabricated by physical vapor deposition with carbon contacts and showed that the main junction and contact are electrically separate with barrier heights of 1.4 and 0.3 eV, respectively. The contact barrier height is attributable to a junction between CdTe and copper tellurides detected at the contact surface. It is expected that this information, coupled with further characterization of the contact region, will lead to

improvements in contact performance as well as a better understanding of contact behavior under different thermal, electrical, and illumination stresses.

4. a-Si:H-based Solar Cells

4.1 Preparation and Characterization of Micro-Crystalline Hydrogenated Silicon Carbide p-Layers

4.1.1 Introduction

The p-layer is critical to a-Si solar cell performance since the p-i junction is the dominant junction in the p-i-n solar cell [38]. One of the most significant developments in a-Si solar cell technology was the incorporation of C in the a-Si p-layer by the group at Osaka University in the early 1980's [39]. The a-Si:C p-layer leads to increased quantum efficiency (QE) at short wavelengths due to its higher transmission. Considerable effort has been made in the past 15 years to improve the a-Si:C p-layer properties [40].

Alternatively, there has been considerable effort focused on changing the structure of the p-layer from amorphous to "microcrystalline" (μc). These μc layers are typically inhomogeneous with a mix of a-Si or a-Si:C with c-Si crystallites of several tens of nanometers. The grain size, fraction crystallinity, and conductivity depend strongly on extrinsic variables such as the thickness and substrate [41, 42]. Independent of deposition method or substrate, it is found that increased hydrogen dilution (H_2/SiH_4 ~100-200) and RF power are required to produce μc films.

Microcrystalline p-layers have been incorporated into superstrate [43] and substrate [44] type of solar cells without substantially improving device performance. The problem lies first on the two phase nature of these p-layers resulting in devices having two p-i junctions in parallel. In addition, c-Si has lower bandgap than what one would like to see in a window layer. The challenge regarding μc p-layers is to develop a process that results in single phase SiC films of high conductivity, which is compatible with deposition on transparent conductive oxides (TCO).

Several groups have attempted to deposit μc-SiC using conditions based on those giving μc-Si p-layers. Growth of SiC films by standard RF PECVD [45, 46], photo-CVD [47] and ECR CVD [48, 49] has been investigated. With the exception of Reference 48 where a mixture of c-Si and c-SiC was obtained, all other groups report that their films consist of c-Si crystallites surrounded by a-Si:C material; i.e., they found no evidence of SiC structure.

4.1.2 Experiment

Films were deposited in an RF(13.56 MHz) PECVD system having an electrode area of 119 cm^2, on 7059 glass substrates from mixtures of SiH_4, CH_4, H_2 with B_2H_6 and $B(CH_3)_3$ (TMB) as dopant gases. Total pressure and substrate temperatures were kept constant at 1 Torr and 175°C respectively. Experimental variables were dopant gas, CH_4 and H_2 gas flows normalized to the sum of SiH_4 and CH_4 flows, and the power.

Co-planar conductivity vs. temperature, optical spectrophotometry and micro-Raman spectroscopy were used to determine optoelectronic properties and the structure of the films. Structurally, the films were characterized by their crystalline volume fraction, X_c, computed by the formula [50, 51],

$$X_c = \sum I_{c-Si} \Big/ \left(\sum I_{c-Si} + 0.9 \times I_{a-Si} \right) \tag{52}$$

where the intensities are the integrated intensities of the TO bands obtained from the baseline corrected deconvolution of the Raman spectrum as illustrated in Figure 21 for a film consisting of a-Si and c-Si phases.

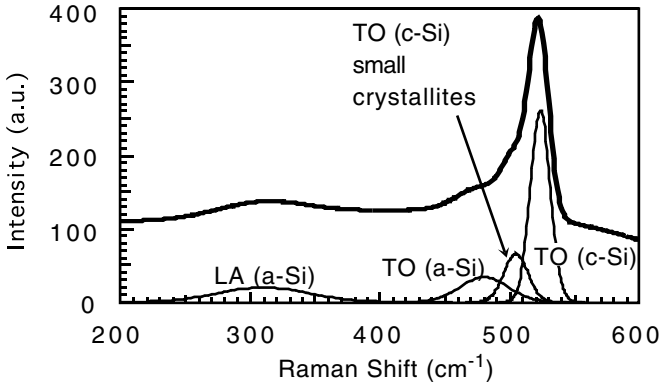


Figure 21. Raman spectrum of a typical a-Si/c-Se film deconvoluted to its gaussian components.

4.1.3 Comparing Effects of B_2H_6 and $B(CH_3)_3$

The p-layers were deposited under conditions previously determined to yield high conductivity μc-Si n-layers. These layers were deposited without any CH_4 to compare the doping effectiveness of B_2H_6 and $B(CH_3)_3$. Table VI gives the conditions and critical material parameters where E_a is the activation energy and σ_d the dark conductivity. Since B_2H_6 has twice as many B atoms per unit volume compared to $B(CH_3)_3$, the normalized flow values listed under B_2H_6 are twice the actual flow. This way normalized flow values, in either case, represent B atom delivery into the reaction zone.

Table VI. Deposition conditions and characteristics of μc-Si films with different doping gases.

Normalized Flow			Power	Thickness	E_a	σ_d	X_c
B_2H_6	TMB	H_2	(W)	(μm)	(eV)	(S/cm)	(%)
0		100	50	0.11	0.38	$5x10^{-6}$	85
0.02		100	50	0.20	0.04	1.2	87
0.03		100	50	0.24	0.03	1.3	52
	0.01	100	50	0.17	0.11	0.02	71
	0.02	100	50	0.18	0.07	0.03	53

Compared to B_2H_6, doping with $B(CH_3)_3$ lowered the conductivity by a factor of 40, increased the activation energy by 0.03 eV, and reduced the fraction of crystallinity from 87% to 53%. The much greater amorphous component for the film doped with $B(CH_3)_3$ may be due to C containing species in the gas phase suppressing nucleation as is reported for CH_4 [45]. We note that only one group reports high conductivity μc-Si layers with $B(CH_3)_3$ dopant [42]. All other groups use either B_2H_6 or BF_3. In view of the fact that TMB suppresses crystallinity more than B_2H_6, for the rest of the present investigation only B_2H_6 was used as the dopant source.

4.1.4 Effect of CH_4 on Crystallinity

In order to determine the effect of CH_4 on the crystallinity of the films a series of undoped films were deposited at different normalized CH_4 flow keeping all other parameters constant, including SiH_4 partial pressure P_s. Again, these deposition parameters are the ones that yielded high crystalline fraction for non-carbon containing films. Table VII gives the deposition conditions and critical material parameters of the films. The data indicates the steep decline of the c-Si fraction with the increasing amount of CH_4 in the gas phase.

Table VII. Deposition conditions and characteristics of films with different normalized CH_4 flows.

Normalized Flow		Power	P_s	Thickness	E_a	σ_d	X_c
CH_4	H_2	(W)	(mT)	(μm)	(eV)	(S/cm)	(%)
0	100	50	9.9	0.11	0.38	$5x10^{-6}$	85
0.33	100	50	9.9	0.33	0.67	$3x10^{-10}$	38
0.43	100	50	9.8	0.34	0.75	$2.5x10^{-12}$	0
0.5	100	50	9.8	0.36	0.82	$2.1x10^{-13}$	3

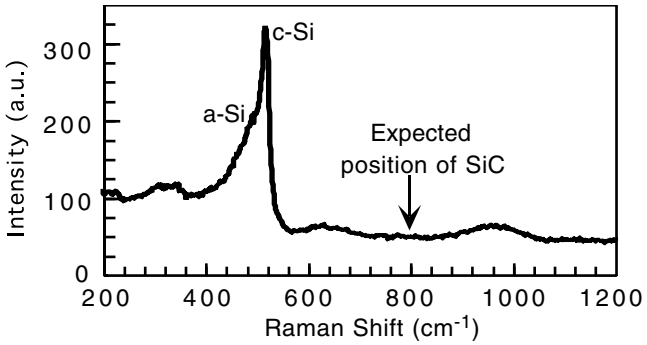


Figure 22. Raman spectrum of a μc-Si film deposited with CH_4 normalized flow of 0.33.

Raman spectra of these films showed only the presence of c-Si and a-Si phases, as can be seen in a typical spectrum in Figure 22. No carbon containing species, such as SiC, were identified in these samples. This observation leads us to conclude that all the carbon in the film is located within the amorphous phase.

4.1.5 Effect of Hydrogen Dilution

The effect of H_2 dilution on the properties of the B-doped C containing films were investigated in a series of runs where normalized H_2 flow was progressively increased. During these runs normalized flows of CH_4, B_2H_6 and power were kept constant at 0.33, 0.02 and 50 W levels. Analysis of the Raman spectra of the films showed, as before, the presence of c-Si and a-Si phases only. The change of c-Si volume fraction in the films as a function normalized H_2 flow is plotted in Figure 23 (left) along with the variation of the SiH_4 partial pressure. The crystalline fraction increases strongly with H_2 dilution while SiH_4 partial pressure decreases, as would be expected. At the present time it was not possible to decouple H_2 dilution and SiH_4 partial

pressure in our reactor. Therefore, even though a large increase in the c-Si volume fraction accompanies increases in the H_2 dilution, this variation cannot uniquely ascribe to H_2 dilution alone because of the significant variation in the SiH_4 partial pressure.

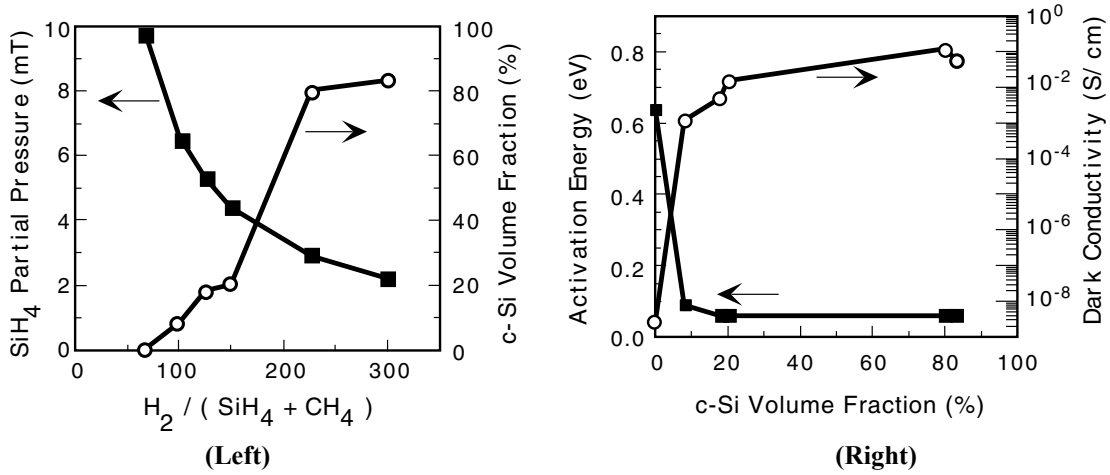


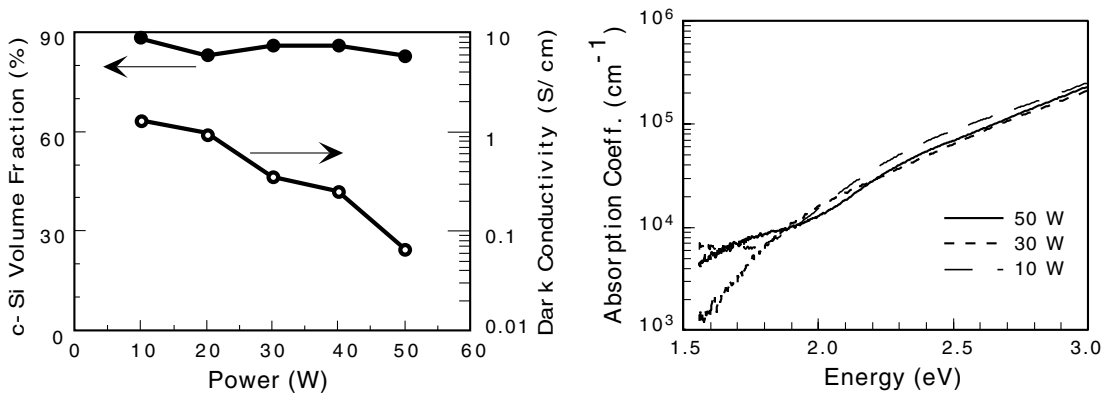
Figure 23. Variation of c-Si fraction and SiH_4 partial pressure with H_2 dilution (left); conductivity and activation energy as a function of c-Si fraction (right).

Room temperature in-plane conductivity and the activation energy of the films as a function of the c-Si volume fraction are shown in Figure 23 (right). The data indicates that c-Si regions begin to form a connected network at a volume fraction less than 10% and control in-plane electrical transport thereafter.

4.1.6 Effect of RF Power

The effect of RF power was investigated in the range of 10 to 50W, corresponding to power density range from 84 to 420 mW/cm^2. For this set of experiments normalized flows of H_2, CH_4, B_2H_6 and SiH_4 partial pressure were kept constant at 300, 0.33, 0.02 and 2.2 mT levels. Raman spectra showed that, as before, only c-Si and a-Si phases are present in the films. The activation energies were measured to be around 0.05 eV for all the films, which indicates that in-plane c-Si phase controls in-plane electrical transport.

Figure 24 (left), where room temperature dark conductivity and the c-Si volume fraction is plotted against discharge power, shows that for SiH_4 partial pressure of 2.2 mT, crystallinity is independent of power while conductivity decreases with increasing power. This decrease in conductivity cannot be explained with the available data.



(Left) **(Right)**

Figure 24. c-Si volume fraction and dark conductivity as a function of discharge power (left); absorption coefficient as a function of energy at three different discharge power levels (right).

Optical analysis of the films is displayed in Figure 24 (right) in the form of absorption coefficient vs. energy. Within experimental errors absorption at high energies is independent of power, suggesting that the amount of carbon in the amorphous phase is also independent of the discharge power.

4.1.7 Conclusions

It has been demonstrated that high conductivity p-layers having high c-Si volume fraction (>85%) can be deposited on glass at low power density (84 mW/cm^2) which is compatible with deposition on TCO substrates for device fabrication.

Proper and quantitative interpretation of H_2 dilution experiments requires depositions under constant SiH_4 partial pressure.

For normalized CH_4 flow of ≤ 0.5 microcrystalline films consist of c-Si and carbon containing a-Si phases.

It has been shown also that at low SiH_4 partial pressures c-Si volume fraction and optical absorption are independent of discharge power.

4.2 Characterization of TCO/P Contact Resistance and Change in TCO Resistance in a-Si Solar Cells

4.2.1 Introduction

Transparent conductive oxides (TCO) are critical to the optical and electrical performance of a-Si based solar cells. This is especially true for superstrate a-Si p-i-n solar cells that are deposited on a glass/TCO substrate. Optically, the TCO must have high transparency and provide scattering to enhance light trapping. Electrically, the TCO must have low lateral sheet resistance since there are no grids and low contact resistance with the p-layer. The TCO is subjected to all processing steps including H-rich plasmas during the p-layer deposition which can degrade its

optical transparency [52, 53]. The TCO must be robust, inert to subsequent chemical and thermal device processing [54] and also must be able to be laser scribed with high yield [55]. Presently, textured fluorine doped SnO_2 is the standard TCO for commercial applications [56].

Minimizing the resistance between the p-layer and TCO of superstrate p-i-n a-Si devices and modules is a critical issue for utilizing new TCO materials like ZnO and new p-layers like μc-SiC or μc-SiO. Compared to SnO_2, ZnO typically gives higher short circuit density (J_{SC}) due to lower absorption losses but poorer electrical performance [55, 57] commonly attributed to the ZnO/p interface, forming a non-ohmic contact. Various schemes to improve the ZnO/p electrical contact have been discussed [58]. However, characterization of the TCO/p interface is difficult since it is in series with the dominant p-i-n junction.

We have developed a method to characterize the TCO/p contact based on the work of Shafarman and Phillips [59]. This method requires having a two adjacent TCO regions. A device is biased to have standard current flow through its TCO/p contact and TCO region while the voltage is measured on the adjacent TCO pad which is electrically "floating." The second pad is thus a voltage sensing contact giving internal access to the potential in the biased device. An additional benefit to this technique is that the SnO_2 sheet resistance in a completed device structure is also obtained.

4.2.2 Sample Fabrication

The substrates studied here were textured SnO_2-coated glass made by Asahi Glass (Type U), AFG, or Solarex. The devices were fabricated at Solarex. The SnO_2 on the 3x3 inch square pieces was laser scribed to create long parallel strips approximately 8-10 mm wide and 76 mm (3") long. Then, single junction a-Si p-i-n layers were deposited by PECVD. The p-layers were a-SiC:H. A row of six individual devices were fabricated on each SnO_2 strip by depositing a ZnO/Al back contact (5x5 mm^2) mm through a mask on the n-layer. A low resistance contact to the SnO_2 strip was made with Ag paste that was baked at 200°C.

4.2.3 Analysis

A top view and side view of the resulting structure is shown in Figure 25. The two SnO_2 strips of width W, with Ag-paste contacts labeled A and B, each have a row of square devices. The current in cells 1, 2, 3, etc. travels in the SnO_2 a distance L from each device to the SnO_2 contact A. The series resistance of the SnO_2 between the device and the contact is

$$R_{TCO} = R_{SH} \times (L/W) \qquad (53)$$

where R_{SH} is the sheet resistance of the SnO_2. As L increases, the series resistance of the TCO between the device and its SnO_2 contact increases. Assuming each device is identical, and its TCO/p contact is identical, this increase in R_{TCO} will be the only difference between devices in the same row.

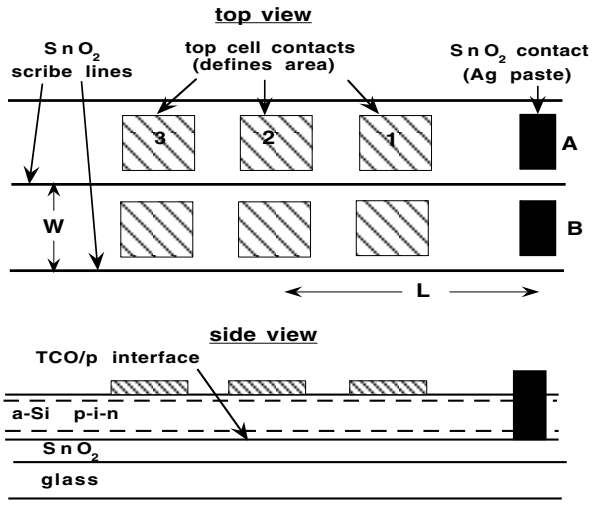


Figure 25. Top view and side view of row of a-Si devices (1-2-3) on scribed SnO_2 strips with contacts labeled A and B.

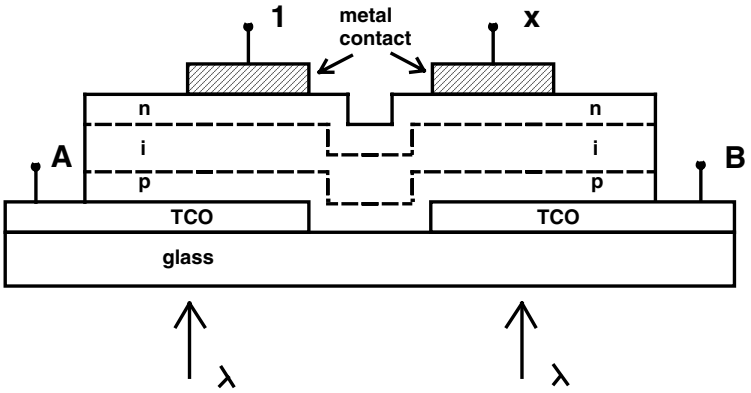


Figure 26. Cross-section view looking down SnO_2 strips A and B. Current flow is established in p-i-n cell 1 between 1 and A while voltage is measured between 1 and A, 1 and B, or A and B. SnO_2 strip B is floating at some potential as the p-layer over strip A.

The three different measurement configurations will be discussed in reference to Figure 26 which shows a cross-sectional view looking down the two SnO_2 strips having contacts A and B. For example, assume that cell 1 in the row of devices labeled 1-2-3 in Figure Figure 25 is to be characterized. For all three measurements, it is biased such that the *current flow* is always between the cell's back contact (1) and the strip's TCO contact (A) as in a standard device JV test. The difference between the 3 measurement configurations is where the *voltage* is measured. In a standard JV measurement, the voltage V_{1A} is measured between the same two contacts where the current is flowing. This voltage V_{1A} includes potential across the p-i-n junction, the TCO/p contact and voltage dropped across the SnO_2 series resistance. When the voltage is instead measured across 1 and B or across A and B, there is no current flow through B so it is

floating at the same potential as the p-layer contacting it, i.e., the p-layer over strip A. The SnO_2 strip B is used as a voltage probe giving access to the internal voltage of devices on strip A. Thus, the voltage measured across device 1 and B (V_{1B}) is only the potential *across* the p-i-n junction of a-Si device 1. It excludes the voltage dropped across TCO/p contact and TCO series resistance. Measuring the voltage across adjacent TCO strips (V_{AB}) gives *only* the voltage dropped across TCO/p contact and TCO series resistance since strip B is floating at the same potential as the p-layer above strip A.

We chose to analyze the different JV data in terms of resistances. The three components of resistance and their relation to the three different voltage measurements are given in Equations 54-56. The three dominant resistances are the junction dynamic resistance R_J , the TCO/p contact resistance R_{TCO}/p, and the series resistance through the TCO R_{TCO}, as defined in Equation 53. The subscripts 1A, 1B, and AB represent voltage measured between nodes 1 and A, 1 and B or A and B as defined in Figure 26. We assume that the other contact resistances, such as between the cell back contact and the n-layer and between the SnO_2 and Ag contact, are negligible.

$$R_{1A} = dV_{1A}/dJ = R_J + R_{TCO/p} + R_{TCO} \quad (54)$$

$$R_{1B} = dV_{1B}/dJ = R_J \quad (55)$$

$$R_{AB} = dV_{AB}/dJ = R_{TCO/p} + R_{TCO} \quad (56)$$

$$R_J = dV/dJ = (AkT/q)/(J + J_{sc}) \quad (57)$$

A critical assumption is that TCO strip B is floating at the same potential as the p-layer over strip A. If this is correct, Equations 54-56 predict that the difference in resistance between cases 1A and 1B should be the same as that measured in case AB. This resistance, R_{AB}, should be the sum of the TCO/p contact and the TCO sheet resistance. From Equation 53, R_{AB} should be linear against L/W with a slope of R_{TCO} and an intercept of $R_{TCO/p}$. Thus, measuring the three resistances on a series of devices on the same strip with increasing L/W should allow determination of $R_{TCO/p}$ and R_{TCO} . Hence, Equations 54-56 show two *independent* ways to obtain R_{AB}. This allows verification of the assumptions and the measurements.

4.2.4 Results

Figure 27 shows JV curves for all three cases of voltage measurement on one device (#8090-4C-1) which was on Asahi SnO_2. Normal solar cell JV curves result when the V_{1A} or V_{1B} is measured while V_{AB} gives a linear JV curve through the origin. This linear JV relation indicates the TCO/p contact is ohmic according to Equation 56. For purposes of analysis, we determine values of the resistances defined in Equations 54-56 at V_{OC}. Thus, for the case where V is measured across 1 and B, R_{OC} is dV_{1B}/dJ at V_{OC}. Values of V_{oc}, FF and R_{OC} are listed in Table VIII. Note that the V_{OC} is the same between configurations 1A and 1B, as expected since the p-i-n junction determines V_{OC}, but the FF increases in configuration 1B since it excludes the TCO series resistance. V_{OC} is zero in configuration V_{AB} as expected from Equation 56. (Some devices we have measured on other TCO materials have exhibited small values of V_{OC}~20-40 mV in configuration V_{AB}, indicating a photovoltage was developed at the TCO/p contact. These devices had inferior V_{oc} and FF when measured in the standard configuration.)

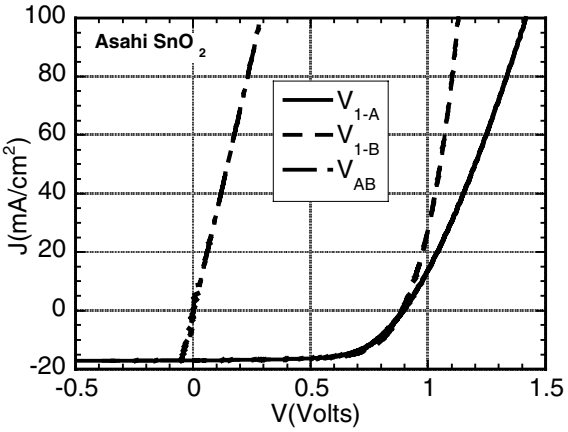


Figure 27. JV curves under illumination for a device (cell 1) with three voltage measurement configurations. Parameters given in Table VIII.

Table VIII. FF, resistance at V_{oc}, and V_{oc} for the three curves in Figure 27 obtained from three-voltage measurement configurations on the same device.

test voltage configuration	FF (%)	R_{OC} (Ω-cm^2)	V_{OC} (V)
cell 1 and A	64	8.8	0.89
cell 1 and B	68	6.1	0.89
A and B	0	2.9	0

Figure 28 shows linear JV behavior for voltages measured across AB for three devices on the same strip of TCO having different L/W. Table Table IX shows values of resistance calculated from both methods. The two resistances increase with L/W as expected, and the FF measured in standard configuration (V_{CELL-A}) decreases as L/W increases as expected. Note the close agreement in Table Table IX between resistances determined independently.

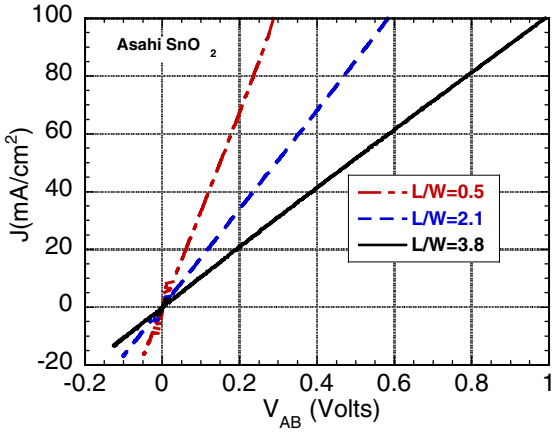


Figure 28. JV measurements for three devices with varying L/W on the same TCO strip A. Voltage was measured across the adjacent strips A and B.

Table IX. Resistance and FF for three devices with increasing L/W. $R(V_{AB})$ determined from slopes of lines in Figure 28. ΔR_{OC} determined from difference of $R(V_{CELL-A})$ and $R(V_{CELL-B})$ at V_{oc}.

L/W	$R(V_{AB})$ (Ω-cm^2)	ΔR_{OC} (Ω-cm^2)	$FF(V_{CELL-A})$ (%)
0.5	2.9	2.7	64
2.1	5.8	6.0	60
3.5	9.5	10	56

Figure 29 shows the two resistances plotted against L/W for devices on the same strip of Asahi SnO_2. ΔR_{OC} is the difference in R_{OC} for JV measured as V_{CELL-A} and V_{CELL-B} while $R(V_{AB})$ is the resistance obtained directly from the slope of V_{AB} as in Figure 28. Clearly, they are the same, verifying Equations 54-56 that the difference in resistance between $R(V_{CELL-A})$ and $R(V_{CELL-B})$ is the same as $R(V_{AB})$, i.e., the TCO sheet resistance and TCO/p contact resistances. From the slope, R_{SH} is ~8 Ω/sq and from the intercept, $R_{TCO/p}$ is 2 Ω-cm^2.

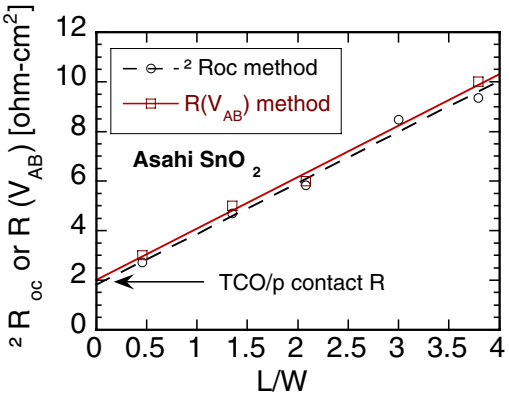


Figure 29. Resistance calculated from two methods vs L/W for row of cells on Asahi SnO_2. The slope is the SnO_2 sheet resistance and the intercept is the TCO/p contact resistance.

Table X. TCO sheet resistance before and after a-Si deposition and TCO/p contact resistance for three types of SnO_2. R_{SH} before deposition obtained from 4 point probe measurements.

TCO	R_{SH} (Ω/sq) before a-Si	R_{SH} (Ω/sq) after a-Si	$R_{TCO/p}$ Ω-cm^2)
Solarex	~12	9	2.5
Asahi	~12	8	2.0
AFG	~13	9	2.5

Table X shows results from the 3 brands of SnO_2 studied. It indicates the SnO_2 sheet resistance is lower after a-Si deposition, with the largest change being for the Asahi SnO_2. This decrease in SnO_2 sheet resistance is consistent with results from devices deposited at IEC on unscribed 1 inch squares of Asahi TCO. A tab-to-tab SnO_2 sheet resistance of 8-9 Ω/sq is typically found after fabrication of a device while the sheet resistance is 13-14 Ω/sq before deposition. The Asahi group has reported a decrease in SnO_2 resistivity of the same amount (from 12 to 8 Ω/sq) with mild H_2 plasma treatments at 200°C due to increased mobility without any loss in optical transmission [60]. Our results from Table X are consistent with these values.

Table X indicates a TCO/p contact resistance of approximately 2 Ω-cm^2 for all three SnO_2 materials. This value also includes any fixed contact or bulk parasitic resistances not accounted for in Equations 54-56. However, values of ~1-2 Ω-cm^2 are reported by others [58, 61] using special test structures (not p-i-n devices) which confirms that the values in Table X are representative of the TCO/p contact.

4.2.5 Conclusions

A new procedure has been presented to determine the TCO sheet resistance and TCO/p contact resistance in operating TCO/p-i-n superstrate devices. Devices must be fabricated on scribed

TCO regions. Two independent methods give very close agreement, verifying the assumptions and analysis. Three brands of SnO_2 were studied here. Very similar SnO_2/p contact resistances were found. The sheet resistance of the Asahi brand SnO_2 decreased ~50% with a-Si processing. This is consistent with reports of others. We conclude that this technique can be helpful in evaluating factors that affect the TCO/p contact resistance, such use of new TCO materials or p-layer processing. In particular, it should be useful in solving the ZnO/p contact problem and evaluating the effect of microcrystalline p-layers.

5. Abstract

This final report describes results achieved under a 20-month NREL subcontract to develop and understand thin film solar cell technology associated to $CuInSe_2$ and related alloys, a-Si and its alloys and CdTe. Modules based on all these thin films are promising candidates to meet DOE long-range efficiency, reliability and manufacturing cost goals. The critical issues being addressed under this program are intended to provide the science and engineering basis for the development of viable commercial processes and to improve module performance. The generic research issues addressed are: 1) quantitative analysis of processing steps to provide information for efficient commercial scale equipment design and operation; 2) device characterization relating the device performance to materials properties and process conditions; 3) development of alloy materials with different bandgaps to allow improved device structures for stability and compatibility with module design; 4) development and improved window/heterojunction layers and contacts to improve device performance and reliability; and 5) evaluation of cell stability with respect to device structure and module encapsulation.

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13. ABSTRACT *(Maximum 200 words)*
This final report describes results achieved under a 20-month NREL subcontract to develop and understand thin-film solar cell technology associated to $CuInSe_2$ and related alloys, a-Si and its alloys, and CdTe. Modules based on all these thin films are promising candidates to meet DOE's long-range efficiency, reliability and manufacturing cost goals. The critical issues being addressed under this program are intended to provide the science and engineering basis for the development of viable commercial processes and to improve module performance. The generic research issues addressed are: 1) quantitative analysis of processing steps to provide information for efficient commercial-scale equipment design and operation; 2) device characterization relating the device performance to materials properties and process conditions; 3) development of alloy materials with different bandgaps to allow improved device structures for stability and compatibility with module design; 4) development and improved window/heterojunction layers and contacts to improve device performance and reliability; and 5) evaluation of cell stability with respect to device structure and module encapsulation.

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