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Novel CdTe Cell Fabrication Process with Potential for Low Cost and High Throughput

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Abstract

There are several production disadvantages inherent in the conventional SnO_2/CdS/CdTe manufacturing processes. In this paper, we report a novel manufacturing process for fabrication of polycrystalline Cd_2SnO_4/Zn_2SnO_4/CdS/CdTe thin-film solar cells that yielded a CdS/CdTe device with an NREL-confirmed efficiency of 14.0%. This process addresses undesirable manufacturing issues such as time-consuming and expensive heat-up and cool-down processes and generation of large amounts of liquid waste. CdTe cells prepared by this process have good performance, good uniformity, and excellent reproducibility. These results, coupled with the improved process manufacturability, can draw significant industrial interest.

Introdution

Cadmium telluride has been recognized as a promising photovoltaic material for thin-film solar cells because of its near-optimum bandgap of ~1.45 eV and its high direct-absorption coefficient. Commercial-scale modules with efficiencies of 6%-10% have been produced by several CdTe deposition techniques. However, performance and reproducibility of the CdTe modules have been limited by the conventional SnO_2/CdS/CdTe device structure used for many years. For example, higher short-circuit current density (J_{sc}) can be achieved by reducing the CdS thickness in CdTe cells. However, reducing the CdS thickness can adversely impact device open-circuit voltage (V_{oc}) and fill factor (FF). Hence, a thicker CdS layer has to be used in most CdTe module manufacturing processes, which results in low J_{sc} (~18 mA/cm^2). In addition, there are several undesirable production disadvantages in the conventional CdTe module manufacturing processes (see Figure 1). For example, the transparent conductive oxide (TCO) films are typically deposited at high temperatures using chemical-vapor deposition (CVD) or spray techniques. The CdS window layer is deposited at lower temperatures using chemical-bath deposition (CBD) or at high temperature using close-spaced sublimation (CSS) or CVD techniques.

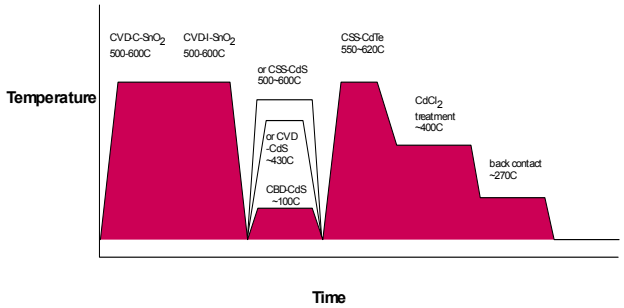

Figure 1. Conventional CdTe device manufacturing processes.

The high-temperature deposition process requires time-consuming and expensive heat-up and cool-down process segments. However, the treatment of a large amounts of liquid waste solution generated in wet processes can increase the manufacturing costs. Therefore, it is necessary to develop a more manufacturing-friendly process for fabricating CdTe modules. In this paper, we report a novel manufacturing process for fabricating CdTe solar cells with a modified device structure.

New Manufacturing Process

Figure 2 shows the new CdTe device manufacturing process. Compared to the conventional manufacturing processes, there are several new aspects in this CdTe device manufacturing process. First, the modified Cd_2SnO_4/Zn_2SnO_4/CdS/CdTe device structure developed at NREL has been used in the new process. In the modified device structure, the Cd_2SnO_4 (CTO) film replaces the conventional SnO_2 TCO film as a front-contact layer, and a Zn_2SnO_4 (ZTO) film is integrated into the device as a buffer layer. The device performance and reproducibility can be improved significantly by using the modified device structure. Second, the first three layers (including CTO TCO layer, ZTO buffer layer, and CdS window layer) are prepared by the same deposition technique – RF magnetron sputtering at room temperature. Third, the new process has only one heat-up segment in the entire device fabrication process. The recrystallization of the first three layers and the interdiffusion at the three interfaces (including the CTO/ZTO, ZTO/CdS, and CdS/CdTe interfaces) were completed during CdTe deposition by the CSS technique.

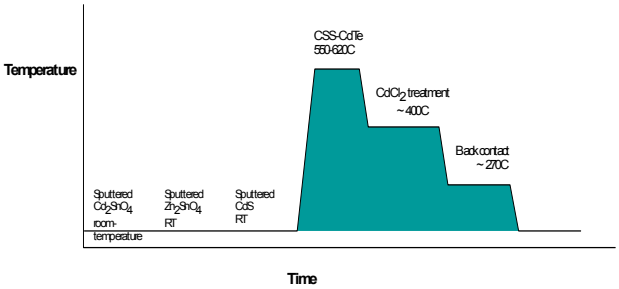

Figure 2. Novel CdTe device manufacturing processes.

Experimental

In this new process, the first three layers (CTO, ZTO, and CdS) were deposited at room temperature by the same RF magnetron sputtering technique. The CTO and ZTO layers were prepared in pure oxygen using commercial hot-pressed oxide targets, and the CdS film was deposited in pure Ar. The CdTe layer was deposited by the CSS technique at a substrate temperatures of 570°C-625°C for 3 minutes. Samples then received a vapor $CdCl_2$ treatment at 400°C-420°C for 15 minutes. Several techniques were used for

material and interface characterization, including Hall effect measurement, visible/near-UV spectrophotometry, X-ray diffraction (XRD), X-ray photoemission spectroscopy (XPS), and transmissiom electron microscopy (TEM). The standard current-voltage (I-V) curves, absolute external and internal quantum efficiencies, time-resolved photoluminescence, saturation dark-current density, and device diode factor have been measured for device performance analysis.

Results

In this process, the first three layers (CTO, ZTO, and CdS) were deposited at room temperature. Hence, all three as-grown films have an amorphous structure and very poor electrical and optical properties. After CdTe deposition at 570□C-625□C for 3 minutes, the three films were changed significantly in material structure, and in electrical and optical properties. We have done much work to understand these changes for the three materials. For example, the as-grown CTO film has an amorphous structure, very high resistivity (>25 Ω cm), and a low bandgap (~2.6 eV). After CdTe deposition at 620□C for 3 minutes, the CTO film structure changed to a spinel polycrystalline structure, and the material properties improved significantly. The post-heat-treated CTO film has a bulk resistivity (~$2.3x10^{-4}$ Ω cm) more than 5 orders of magnitude lower than the as-grown CTO film, and has a higher bandgap (~3.1 eV) and good transmission. We also investigated the interdiffusion among the four layers. For example, XPS and SIMS results show that the interdiffusion occurs at both the CTO/ZTO interface and at the ZTO/CdS interface. This feature can be used to improve device performance and reproducibility.

We have fabricated a Cd_2SnO_4/Zn_2SnO_4/CdS/CdTe solar cell with an NREL-confirmed efficiency of 14.0% (V_{oc} = 841.1 mV, J_{sc} = 22.28 mA/cm^2, fill factor = 74.95%) by this new process (see Figure 3). We believe that this is the highest NREL-confirmed efficiency ever reported for any thin-film solar cell with both the TCO and the CdS layer deposited at room temperature.

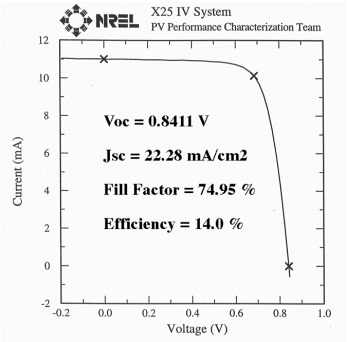

Figure 3. I-V curve of a Cd_2SnO_4/Zn_2SnO_4/CdS/CdTe cell prepared by the new process.

Our device results also demonstrated that CdTe cells prepared by this process have good uniformity and reproducibility, which is desirable for scaling-up a process. Table 1 shows the I-V data of four cells prepared from one substrate. We believe that this excellent device uniformity is from both the CSS and RF sputtering techniques. The good uniformity of devices can help reduce the efficiency gap between the small-area cells and the modules. Preliminary results of device reliability accelerated testing indicate that the CdTe cells prepared by the new process have similar behavior with NREL base-line CdTe cells and no extra degradation from the simplified process. The device was stressed at 100°C and in light of 2 suns, and the acceleration factor is 500-1000.

Table 1. Uniformity of CdTe cells prepared by the new process.

Device #	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
W331-A	840	22.9	73.3	14.1
W331-B	838	22.5	73.2	13.8
W331-C	835	23.3	72.9	14.2
W331-D	835	23.3	71.5	13.9

Potential Benefits from the New Process

1. This process can significantly reduce the thermal budget, because the first three layers are deposited at room temperature and the entire process has only one heat-up segment.
2. This process can significantly reduce the process time, thus increasing the throughput. Because the first three layers are deposited at room temperature, therefore no time is required for substrate heat-up and cool-down. In addition, because the first three layers are prepared by the same RF sputtering, thus no time is required for substrate loading and unloading.
3. This process can provide high yield, because all layers are prepared by two compatible deposition techniques: CSS and RF sputtering. Substrates can stay in vacuum through the entire process, and devices have very clean interfaces. In addition, devices prepared by the new process have no adhesion problems due to integrating the ZTO buffer layer.
4. This process can produce high-performance CdTe cells with good uniformity, good reproducibility, and acceptable device stability.

Conclusions

We have developed a low-cost manufacturing friendly process with the potential of high throughput for fabricating CdTe solar cells. CdTe cells prepared by this process have good performance, good uniformity, acceptable device stability, and excellent reproducibility. These results, coupled with the improved process manufacturability, will draw significant industrial interest. We also demonstrated the highest NREL-confirmed efficiency (14.0%) ever reported for any thin-film solar cell with both the TCO and the CdS layer deposited at room temperature.

Aknowledgments

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