June 2000 • NREL/SR-520-28597

Subcontractor Report

Commercialization of CIS-Based Thin-Film PV

Phase I Annual Technical Report August 1998—August 1999

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National Renewable Energy Laboratory

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Preface

Siemens Solar Industries (SSI) has pursued the research and development of $CuInSe_2$-based thin film PV technology since 1980 [1]. At the start of subcontract activities with NREL, SSI had demonstrated a 14.1% efficient 3.4 cm^2 active-area cell, unencapsulated integrated modules with aperture efficiencies of 11.2% on 940 cm^2 and 9.1% on 3900 cm^2, and an encapsulated module with 8.7% efficiency on 3883 cm^2 (verified by NREL).

SSI began a 3-year, 3 phase cost-shared subcontract (No. ZN-1-19019-5) on May 1, 1991 with the overall project goal of fabricating a large area, stable, 12.5% aperture efficient encapsulated CIS module by scaleable, low-cost techniques on inexpensive substrates. Subcontract accomplishments were facilitated by addressing module reproducibility using small area test devices and min-modules, and statistical process control disciplines were adopted to rigorously quantify process reproducibility. SSI addressed uniformity and reproducibility of absorber formation, interactions of the substrate with the absorber, and performance losses near interconnects. Subcontract accomplishments included demonstration of encapsulated module efficiencies that were at that time the highest reported mini-module efficiencies for any thin film technology (encapsulated 12.8% efficient mini-module on 68.9 cm^2 and an NREL-verified 12.7% efficient unencapsulated circuit on 69 cm^2 with a prismatic cover), demonstration of a champion large area (3860 cm^2) encapsulated module efficiency of 10.3% (verified by NREL) that was the first thin film module of its size to exceed the 10% efficiency level, and delivery to NREL of a one kilowatt array of large area (~3890 cm^2) approximately 30 watt modules [2].

From September 1995 through December 1998 SSI participated in a 3-year, 3 phase cost-shared TFPPP subcontract (No. ZAF-5-14142-03). The primary objective of this subcontract was to establish reliable high-throughput, high-yield thin film deposition processes in order to make CIS a viable option for the next generation of photovoltaics. Outdoor testing, accelerated environmental testing, and packaging development progressed throughout all phases of this subcontract. During Phase 1, SSI rigorously demonstrating process reproducibility and yield for a 10x10-cm monolithically interconnected "mini-module" baseline process and demonstrated a 13.6% aperture area efficient mini-module (verified by NREL). During Phase 2, SSI demonstrated the need to replace an existing large area reactor with a reactor based on a more direct scale-up of the baseline reactor, built a new large area reactor, and demonstrated comparable performance for the mini-modules baseline and 28x30-cm circuit plates. SSI developed products and prototype large area modules using a new package designed to integrate small circuit plates into larger modules. A one kilowatt array of $Cu(In,Ga)(S,Se)_2$ modules was delivered to NREL replacing a previously installed array based on an older absorber formation technology without sulfur incorporated in the absorber ($Cu(In,Ga)Se_2$). This array demonstrated significant improvements in efficiency and the temperature coefficient for power. SSI introduced two new 5-watt (ST5) and 10-watt (ST10) CIS-based products designed for use in 12 V systems, and NREL confirmed a new world-record efficiency of 11.1% on a SSI large area (3665 cm^2) module. During subcontract Phase 3, substrate size was scaled from ~30x30 cm to ~30x120 cm and good process control was demonstrated with an average efficiency of 10.8%. Commercial product samples were delivered to NREL and a second set of ~30x120 cm modules (32 modules totaling ~1.2 kW) were delivered to the NREL Outdoor Test Facility. The NREL measured average efficiency at standard test conditions of 11.4% was at that time the highest large area efficiency for any thin-film technology and NREL confirmed a world-record 11.8% large area (3651 cm^2) efficiency for the champion module [3].

The primary objectives of this subcontract are to scale up substrate size and to scale up production capacity of the baseline SSI CIS-based module process while introducing CIS-based products. The primary goals of this subcontract are to scale the substrate size from approximately 900 cm^2 (1 ft^2) to

approximately 4000 cm^2 by the middle of the Phase II, and to achieve pilot production rates of 500 kW per year by the end of Phase III. Deliverables for the subcontract include CIS-based products and representative modules delivered to the NREL Module Testing Team for outdoor testing and evaluation. SSI will continue mid-term and longer-term thin-film R&D with the goals of:

- Assuring future product competitiveness
- Improving module performance
- Reducing cost per watt
- Assuring product reliability

This document reports on progress toward these objectives and goals through approximately the first year of this three year subcontract; October 1998 through September 1999.

Acknowledgments

Siemens Solar Industries wishes to acknowledge the contributions of the following people and organizations.

The Siemens Solar Industries CIS Team:
G. Aledia, J. Bauer, V. Bell, R. Dearmore, M. Dietrich, S. Dingding, M. Eclevia, G. Fernandez, O. Frausto, R. Gay (Program Manager), C. Köble, A. Ramos, U. Rühle, J. Schmitzberger, D. Tarrant (Principal Investigator), R. Wieting, D. Willett
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National Institute for Environmental Health Sciences
Showa Shell Seikyu, K.K.
Siemens Solar GmbH
Siemens AG
Washington State University

Summary

Compared to traditional wafer-based crystalline silicon technologies, monolithic integration of thin film technologies can lead to products of comparable performance but with significant manufacturing advantages [1]: lower consumption of direct and indirect materials, fewer processing steps, easier automation. Monolithic integration is required to achieve these advantages since this eliminates multiple process steps and handling operations during formation of the absorber and during module assembly. The basic module elements for all thin-film technologies (alloys of amorphous silicon, cadmium telluride and CIS) are the same; the module elements are a circuit-glass/cover-glass laminate, a frame, and a junction box. The basic circuit elements are also very similar; they each have a base electrode, an absorber, a junction, a top electrode and three patterning steps for monolithic integration. While the details of these module elements or equivalent module elements differ, the basic cost structures are the same on an area-related basis. Since the cost per unit area is the same, the cost per watt is inversely proportional to the module efficiency. CIS cells and monolithically integrated modules have demonstrated the highest efficiencies of any candidate thin-film technologies; therefore, CIS is expected to have the lowest manufacturing cost/watt.

The primary objectives of the SSI "Commercialization of CIS-Based Thin-Film PV" subcontract are to scale-up substrate size and to increase production capacity of the baseline CIS module process while introducing CIS-based products. An additional mid- to longer-term objective is to advance CIS based thin-film technology thereby assuring future product competitiveness by improving module performance, cost per watt produced, and reliability. The foundation of the SSI's approach to process scale-up, process optimization, and demonstration of product durability is the application of design of experiment and statistical process control methodologies. These combined objectives are pursued to fabricate efficient and stable thin-film modules made by scaleable, manufacturable, low-cost techniques. SSI milestones for this subcontract are to:

- Scale from a substrate size of approximately 900 cm^2 to a substrate size of approximately 4000 cm^2 (4 ft^2) by the middle of the second phase of this subcontract. The criteria for achievement of this milestone is a 4000 cm^2 circuit plate process that has been adopted for SSI commercial activities and is reproducible as determined by statistical process control criteria.
- Achieve a pilot production rate 500 kW per year by the end of subcontract

During this subcontract period SSI introduced two new CIS products to the SSI ST family of products including an approximately 1x4 ft, 40Wp module. Also, process data for the production of circuit plates for the CIS family of products demonstrates improved efficiency and exhibits generally good control for extended periods. These combined results met the first subcontract milestone and SSI delivered product samples as deliverables that are larger and of higher efficiency than originally defined for this subcontract phase.

Capacity has been increased while also increasing the average efficiency of 1x4 ft circuit plates from 10.8% to 11.2%. Similarly, yield improvements have been made by implementing improvements in processes and manufacturing protocols. No one major process improvement is responsible for the demonstrated increase in throughput and average efficiency accomplished while simultaneously increasing capacity. Instead, advancements during this subcontract phase are due to continuous improvement of all process. Process development has improved adhesion, decreased breakage, addressed control of raw materials, and decreased failures associated with patterning. In addition to process development aimed at improving efficiency and continual yield improvements, development of manufacturing coordination systems has been critical for successful scale-up.

The durability and reliability of the ST family of CIS thin-film products is backed by a 5 year warrantee and during this subcontract period FM and UL approval was obtained for the ST series of products. Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules have undergone testing for over eleven years.

SSI capabilities are leveraged as a Technology Partner participating in NREL team oriented TFPPP activities to address near-term to longer-term R&D topics. SSI's participation in Team activities is focused primarily on understanding the fundamental mechanisms responsible for transient effects in CIGS-based devices with the objective of eliminating or minimizing their impact.

SSI introduced ST5 (5 Wp) and ST10 (10 Wp) products during the previous subcontract. During this subcontract period, R&D Magazine recognized the significance of this major milestone in the development of photovoltaics by awarding the prestigious R&D 100 Award to the SSI family of CIS modules. This family of modules includes two new larger area CIS products introduced during this subcontract period; the ST20, 20 Wp and ST40 40Wp modules. NREL confirmed a world-record 12.1% conversion efficiency large area (3651 cm^2) CIS module.

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Introduction

Overview

Multinary $Cu(In,Ga)(Se,S)_2$ absorbers (CIS-based absorbers) are promising candidates for reducing the cost of photovoltaics well below the cost of crystalline silicon. CIS champion solar cells have exceeded 18% efficiency for devices fabricated at NREL [4]. Small area, fully integrated modules exceeding 13% in efficiency have been demonstrated by several groups [5]. Long-term outdoor stability has been demonstrated at NREL by ~30x30 cm and ~30x120 cm SSI modules which have been in field testing for as long as eleven years. Projections based on current processing indicate production costs well below the cost of crystalline silicon [5].

Compared to traditional wafer-based crystalline silicon technologies, new thin film technologies yield products of comparable performance but with significant advantages in manufacturing [5]:

- Lower consumption of direct and indirect materials
- Fewer processing steps
- Easier automation

Lower consumption of direct and indirect materials results in part from the thin-film structure for the semiconductor used to collect solar energy. All three of these manufacturing advantages are in part due to an integrated, monolithic circuit design illustrated in Figure 1. Monolithic integration eliminates multiple process steps that are otherwise required to handle individual wafers and assemble individual solar cells into the final product.

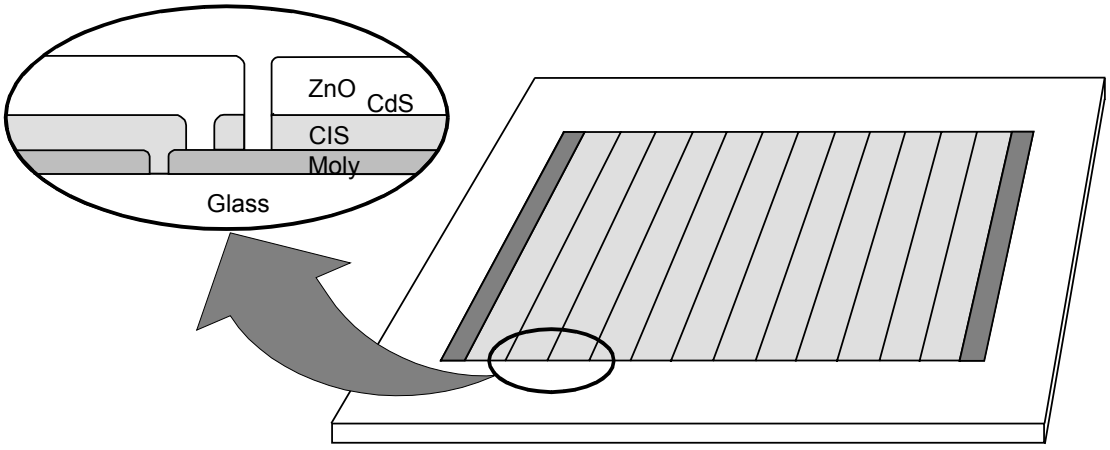


Figure 1. Structure of SSI's monolithically integrated thin-film circuits.

A number of thin film photovoltaic technologies have been developed as alternatives to the traditional solar cells based on crystalline silicon wafers [5]. Those technologies with the greatest potential to significantly reduce manufacturing costs are based on alloys of amorphous silicon (a-Si), cadmium

telluride (CdTe), CIS, and film silicon (Si-film). These photovoltaic thin film technologies have similar manufacturing costs per unit area since all share common elements of design and construction:

- Deposition of typically three layers on a suitable substrate – window/electrode, absorber, and back electrode
- Patterning to create monolithically integrated circuit plates
- Encapsulation to construct modules

Cost per watt is a more appropriate figure of merit than cost per unit area [5]. All thin film technologies have similar manufacturing costs per unit area since they all use similar deposition, patterning, and encapsulation processes. About half of the total module cost – material, labor, and overhead – originates in the encapsulation scheme which is for the most part independent of the thin film technology. Costs for alternative encapsulation schemes are typically similar or even higher. The average efficiency of large, ~30x120 cm modules in pilot production at Siemens Solar is approximately 11%. This performance is comparable to many modules based on crystalline silicon, and is substantially better than the performance reported for competing thin-film technologies. The lowest cost per peak watt will result from the technology with the highest efficiency, CIS technology, since most thin film technologies have similar cost per unit area.

SSI CIS Process

Most terrestrial photovoltaic products today are designed to charge a 12-volt battery, however the output voltage of an individual solar cell is typically about 0.5 volts. Wafer-based technologies build up the voltage by connecting individual solar cells in series. In contrast, CIS circuits are fabricated monolithically (Figure 1); the interconnection is accomplished as part of the processing sequence to form the solar cell by alternately depositing a layer in the cell structure and patterning the layer using laser or mechanical scribing.

The structure of a SSI CIS solar cell is shown in Figure 2. The full process to form CIS circuit plates, including monolithic integration, is outlined in Figure 3. This process starts with ordinary sodalime window glass, which is cleaned and prepared for the deposition of the thin films. A molybdenum (Mo) base electrode is sputtered onto the substrate. This is followed by the first patterning step (referred to as "P1") required to create monolithically integrated circuit plates – laser scribing to cut an isolation scribe in the Mo electrode. Copper and indium precursors to CIS formation are then deposited by sputtering. CIS formation is accomplished by heating the precursors in H_2Se and H_2S to form the CIS absorber. This deposition of copper and indium precursors followed by reaction to form CIS is often referred to as the two-stage process. A very thin coating of cadmium sulfide (CdS) is deposited by chemical bath deposition (CBD). This layer is often referred to as a "buffer layer." A second patterning step (P2) is performed by mechanical scribing through the CIS absorber to the Mo substrate thereby forming an interconnect via. A transparent contact is made by chemical vapor deposition (CVD) of zinc oxide (ZnO). This layer is often referred to as a "window layer" or a transparent conducting oxide (TCO). Simultaneously, ZnO is deposited on the exposed part of the Mo substrate in the interconnect via and thereby connects the Mo and ZnO electrodes of adjacent cells. A third and final patterning step (P3) is performed by mechanical scribing through the ZnO and CIS absorber to isolate adjacent cells.

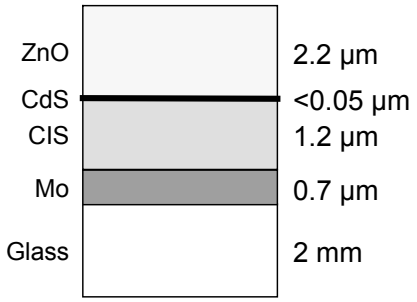


Figure 2. Structure of SSI's CIS cell structure.

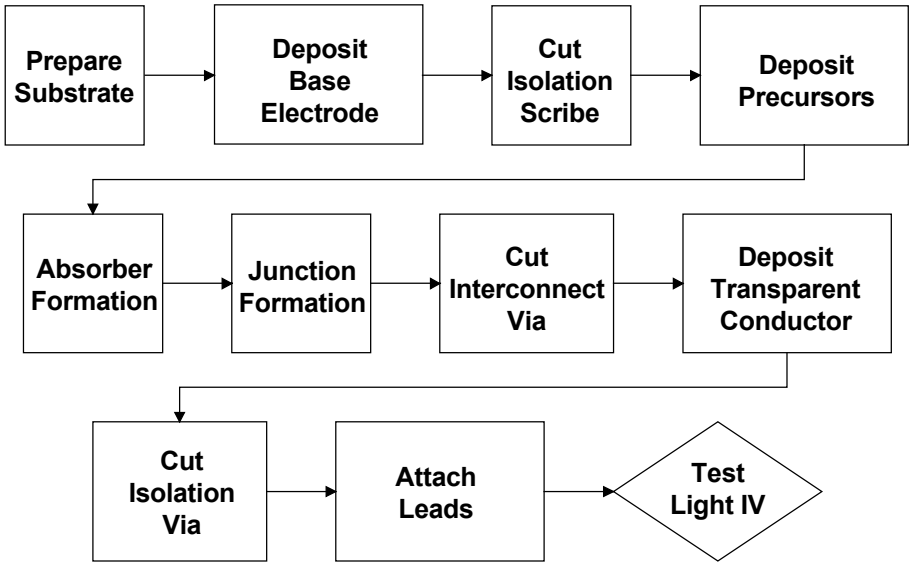


Figure 3. SSI CIS Circuit Processing Sequence.

The CIS-based absorber referred to in this report is composed of the ternary compound $CuInSe_2$ combined with sulfur and gallium to form the multinary compound $Cu(In,Ga)(S,Se)_2$. Gallium and sulfur are not uniformly distributed throughout the absorber but the concentrations are graded; hence, this structure is referred to as a "graded absorber." The graded absorber structure is a graded $Cu(In,Ga)(Se,S)_2$ multinary with higher sulfur concentration at the front and back and higher Ga concentration at the back. Elemental profiles typical of the SSI graded absorber structures are presented in Figure 4. Efficiency, voltage, and adhesion improvements have been reported for the SSI graded absorber structure [2, 6, 7].

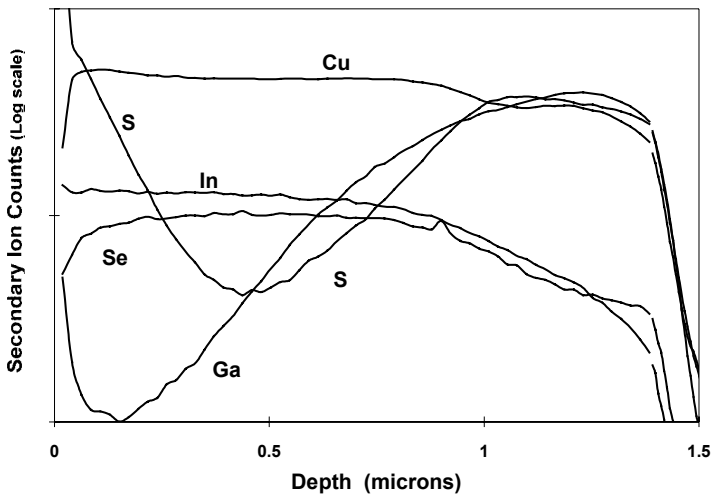


Figure 4. Typical elemental profile for the SSI graded absorber (SIMS from NREL).

Figure 5 illustrates the module configuration used for prototypes and ST products during this subcontract period [3]. EVA is used to laminate circuit plates to a tempered cover glass and a Tedlar/polyester/Al/Tedlar (TPAT) backsheet provides a hermetic seal. Aluminum extrusions are used to build frames for the modules. In addition to providing a hermetic seal, the combination of the TPAT backsheet and the offset between the circuit plate and the frame provides electrical isolation from the frame.

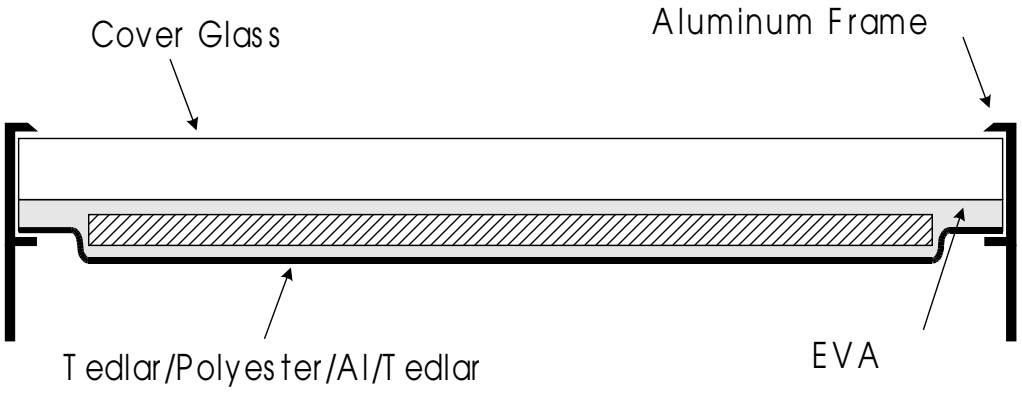


Figure 5. Single circuit plate module configuration with a TPAT backsheet.

SSI's R&D Approach

From the industrial perspective, the full process sequence anticipated for use in large-scale production must be mastered and rigorously demonstrated. The SSI research approach is composed of two main elements:

- Experimentation and development using device structures that exercise all aspects of large area module production [8]

- Application of statistical process control (SPC) as the discipline to rigorously quantify process reproducibility, and application of statistical methods such as analysis of variation (ANOVA) to rigorously quantify experimental results [9, 10].

Process predictability is a prerequisite for commercialization of thin-film PV since product performance ratings, yields and costs must be known before committing to produce products. Also, process predictability is essential for proper interpretation of process development efforts since experimental results may be ambiguous or misleading if compared to an unpredictable baseline process. SSI has adopted SPC methodologies because SPC was developed to rigorously quantify process reproducibility and process capability; the essence of SPC is predictability. Equally significantly, SPC provides the measure of systematic progress as processes are developed and communication of this progress is typically best expressed in the language of the SPC discipline [11]. For example, process characterization results are demonstrated to be "statistically significant" based on knowledge of process repeatability measured using the SPC discipline, and confidence in the appropriate interpretation of experimental results is gained through application of statistical methods such as ANOVA.

Subcontract Activities and Milestones

The primary work of this subcontract is to advance module fabrication processes by progressively scaling substrate size and capacity for the SSI baseline CIS circuit-plate process. While scaling up the baseline process SSI is pursuing understanding of the impact of circuit plate and module fabrication processes on device performance and module reliability. Understanding and optimization of the these processes is based on the application of DOE and SPC methodologies to identify dominant process issues and address process specific topics. Five subcontract activities have been defined to support this work:

Substrate Size Scale-up – The primary emphasis for this activity is to progressively scale substrate size from approximately 900 cm^2 (1 ft^2) approximately 4000 cm^2 (4 ft^2).

Capacity Scale-up - The technical base supporting manufacturability will be advanced as the production capacity is increased to about 500 kW/yr.

Product Durability - SSI will continue package development and qualification in parallel with substrate size and capacity scale up.

Environment, Safety and Health (ES&H) - SSI will continue internal programs and collaborative efforts such as with the TFPPP ES&H team to safely produce CIS-based devices and modules and to explore technical approaches for removing and recycling module components.

Process Improvements – This task emphasizes advancement of the technical base supporting manufacturing as SSI scales up substrate size and capacity. SSI capabilities are leveraged as a Technology Partner participating in NREL team oriented TFPPP activities to address near-term to longer-term R&D topics.

Milestones

SSI milestones for this subcontract are to:

- Scale from a substrate size of approximately 900 cm^2 to a substrate size of approximately 4000 cm^2 (4 ft^2) by the middle of the second phase of this subcontract. The criteria for achievement of this milestone is a 4000 cm^2 circuit plate process that has been adopted for SSI commercial activities and is reproducible as determined by statistical process control criteria.
- Achieve a pilot production rate of 500 kW per year by the end of this subcontract

Deliverables

The following deliverables have been defined for each phase of this subcontract.

Phase I

D1. End of the 12th month: Deliver ten (10) 900-cm^2 (1-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10%.

D2. End of the 12th month: Deliver ten (10) 900-cm^2 (1-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10% for the NREL Module Testing Team.

Phase II

D3. End of the 24th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10%.

D4. End of the 24th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10% for the NREL Module Testing Team.

Phase III

D5. End of the 36th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 12%.

D6. End of the 36th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 12% for the NREL Module Testing Team.

Technical Review

Large Area Circuit Fabrication

Circuit Plate Statistics

Progress on this subcontract phase will be discussed by comparison with circuit plate statistics from the early portion of this subcontract combined with the later part of the previous TFPPP subcontract (Figure 6, Figure 7). During that time frame (January through November 1998), about 1300 ~30x120 cm circuit plates were produced including 18% that were dedicated to experiments [3, 12].

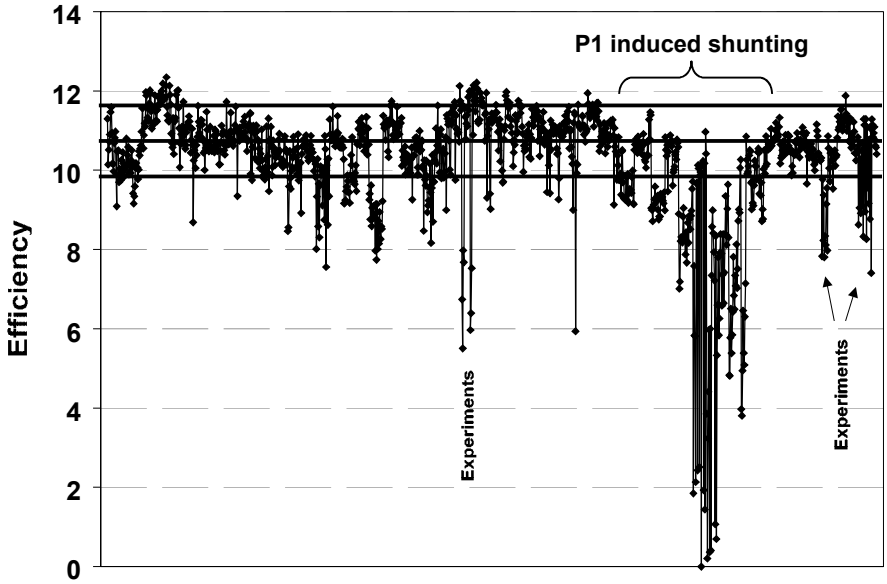


Figure 6. CIS Circuits Produced January through November 1998 (abscissa – module identifier).

The process data exhibits generally good control for extended periods with an average efficiency of 10.8% based on a Gaussian fit to the main portion of the distribution. Periodic shifts in the short-term average efficiency between about 10.25 and 11.25 are determined by shifts in V_{oc} and FF resulting from batch-to-batch variability in precursor or base electrode preparation. Similarly, periodic shunting along the laser scribed pattern lines in the Mo base electrode results from batch-to-batch variability in base electrode preparation.

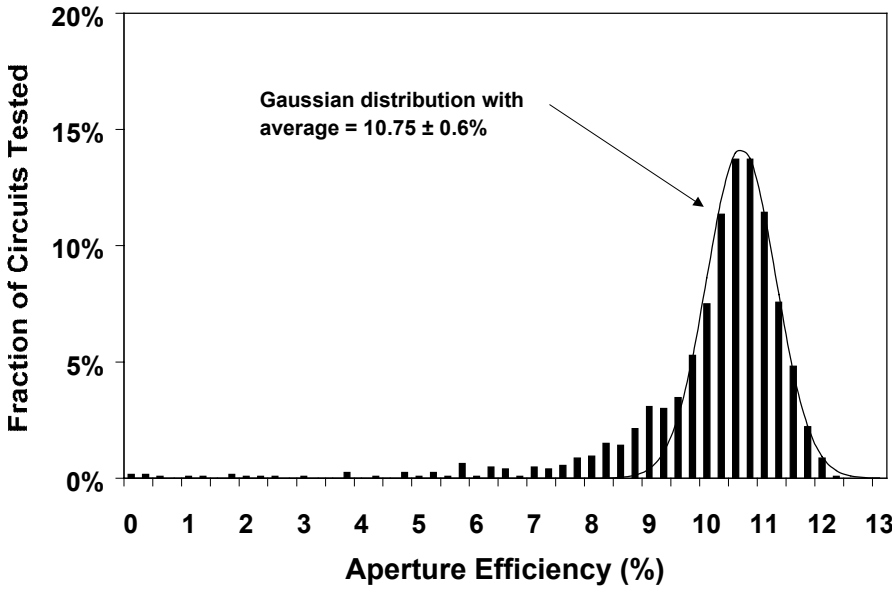


Figure 7. CIS Circuit Efficiency Distribution - January through November 1998.

Similar data representative of this subcontract period is presented in Figure 8 and Figure 9. The timeframe corresponds with the SSI fiscal year (October 1998 through September 1999) and there is some overlap with the previous charts. An average efficiency of 11.2% is demonstrated for 3,030 circuit plates.

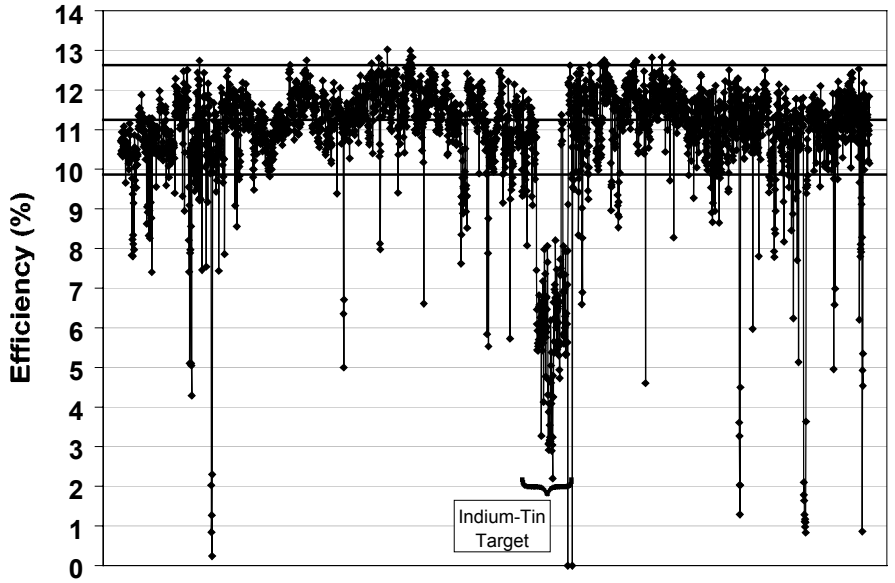


Figure 8. CIS Circuits Produced October 1998 through September 1999 (abscissa – module identifier).

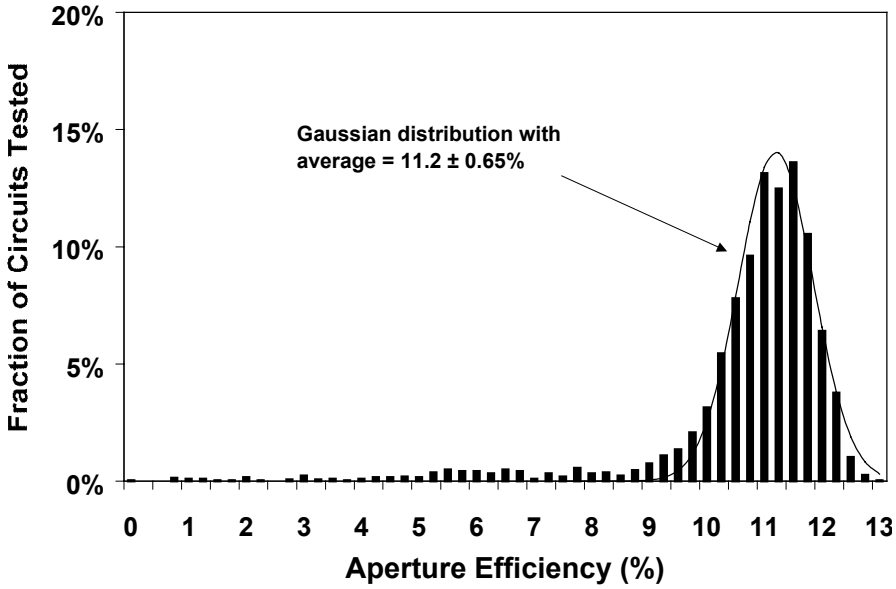


Figure 9. CIS Circuit Efficiency Distribution - October 1998 through September 1999 (abscissa – module identifier).

During this subcontract period the process data again exhibits generally good control for extended periods. The average efficiency based on a Gaussian fit to the main portion of the distribution has increased from 10.8% to 11.2% in part due to better consistency and in part due to changes in the reaction process. Small periodic shifts in the short-term average efficiency continue and are determined by shifts in V_{oc} and FF resulting from batch-to-batch variability in precursor or base electrode preparation. Process development has eliminated or greatly reduced periodic shunting along the laser scribed pattern lines. With the exception of identified special causes for irregular performance such as bad raw materials (discussed below), 87% of the circuit plates are above 10% efficiency.

No one major process improvement is responsible for the demonstrated increase in throughput and average efficiency accomplished while simultaneously increasing volume. Instead, advancements during this subcontract phase are due to continuous improvement of all process. Scale up and process improvement efforts during this subcontract phase include the following:

- Large area absorber formation process capacity was increased in existing equipment.
- SPC techniques were applied to all aspects of the process. SPC techniques led to the characterization and improvement of electrical and mechanical yields related to breakage, peeling, substrate preparation, operator errors, warped substrates, and equipment malfunctions.
- All process diagnostic techniques were continually reviewed for adequacy, improved, and updated to accommodate increased capacity.
- Particular attention was paid to improving yield by proper handling between process steps. This included definition of maximum allowable times between process steps and attention to manual handling and transport.
- Process time was decreased, increasing the throughput of the reaction process by demonstrating the viability of removing circuit plates from the reactor at a higher temperature.

- Studies of the interdependence of Mo thin-film properties and laser processing led to improved laser scribe quality and consistency.
- Experience led to improved inspection to identify and avoid using warped substrates.
- Improved adhesion was obtained by alterations in the absorber formation process.
- An approximately 5% increase in V_{oc} accompanied by a similar decrease in Jsc was achieved through absorber formation process changes.
- The increase in V_{oc} combined with module optimization modeling led to decreasing the number of cells in a module from 50 cells to 42. This resulted in making CIS product current/voltage characteristics similar to typical Si products, decreased active area losses due to patterning, and decreased changes in efficiency with temperature.

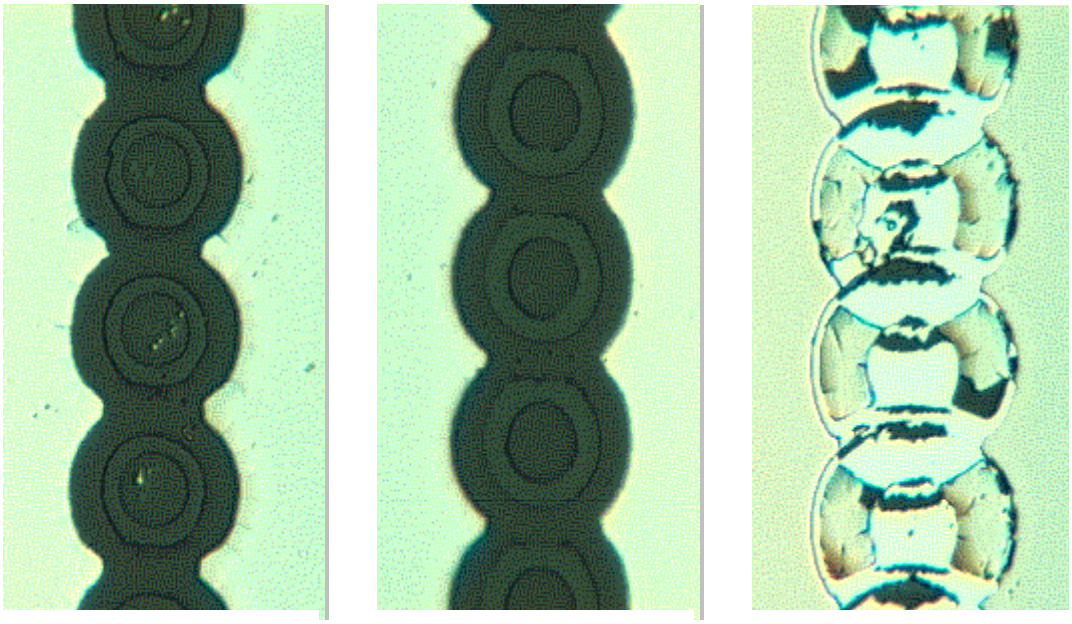
Process Development Examples

Examples of subcontract work that both did and did not lead to implemented improvements in the baseline process will be discussed in more detail.

A major loss in production was caused by a serious quality lapse by the H_2Se supplier. Instead of H_2Se, the supplier delivered a cylinder, and subsequently yet another cylinder, of a gas with a much higher vapor pressure. This triggered overpressure relief valves, contaminated gas lines, interrupted production, and resulted in a general interruption of ongoing development activities. In addition to being a process issue, this overpressure of gas lines is a potential safety issue. As part of SSI's efforts to promote safe operations throughout the photovoltaics community, SSI communicated results and insights regarding this incident to the photovoltaics community through the leaders of the TFPPP ES&H Team, Paul Moskowitz. and Vasilis Fthenakis.

Production losses due the wrong process gas do not appear on the charts for circuit plate statistics since safety systems prohibited even attempting absorber formation. However, a major loss of circuit plates due to a similar problem with new materials is annotated in Figure 8. An indium-tin target was supplied instead of an indium target. Poor circuit performance resulted from this inadvertent test of changes in the relative concentrations of precursors and the addition of tin. These events introduced materials with extreme differences from specified materials and illustrated the vigilance required in obtaining the proper materials to achieve high yield.

Shunting along laser P1 scribes has sporadically caused poor performance particularly during the previous subcontract. During this subcontract period, studies of the interdependence of Mo properties and laser processing led to improved laser scribe quality and consistency. An experiment to determine if laser scribing of Mo is affected by a background of O_2 during Mo deposition is an example of these studies. Mo was sputtered with no O_2 (baseline) and with O_2 flowing at 1% and 10% of the Argon flow. Figure 10 illustrates that visual appearance is not dramatically affected by 1% O_2 but is distinctly affected by 10% O_2 - the Mo deposited with 10% O_2 is not completely removed. A similar trend was observed for mini-module performance. Performance differences between baseline and a 1% partial pressure of O_2 were not statistically significant for the relatively small number of devices processed. The modules made with Mo deposited with a 10% O_2 background could not be tested since the modules did not have complete P1 scribes.



Baseline **1% O_2** **10% O_2**

Figure 10. The dependence of Mo scribe appearance on background O_2 during Mo deposition.

As an example of subcontract activities that did not lead to improvements in the baseline process, an etching technology used in the printed circuit board industry was tested as an alternative to laser scribing. The goals of this study were to demonstrate the process, compare shunting along P1 for laser ("L-P1") and etched ("E-P1") patterning, and demonstrate simultaneous processing of P1 and a wide Mo free border. The Mo free boarder would be one step for one possible class of alternative module encapsulation configurations. The E-P1 process was tested in the full module fabrication process and physical features unique to the E-P1 process were analyzed with the help of NREL resources. Smaller than typical circuit plates (~30x30 cm) were used to accommodate the available equipment.

The visual appearance of E-P1 scribes motivated analysis of scribe features. A very thin transparent and insulating layer remains within some etched P1 scribes. Also, a narrow strip is present at the edge of all lines that appears to be similar to the thin layer. Rick Matson (NREL) supplied SEM micrographs of E-P1 scribe features (Figure 11) and Amy Swartzlander (NREL) supplied Auger and XPS analysis. Features are numbered as follows in the SEM:

1	- Mo
2, 3, 5, 6	- thin transparent layer
4	- center of the E-P1 scribe

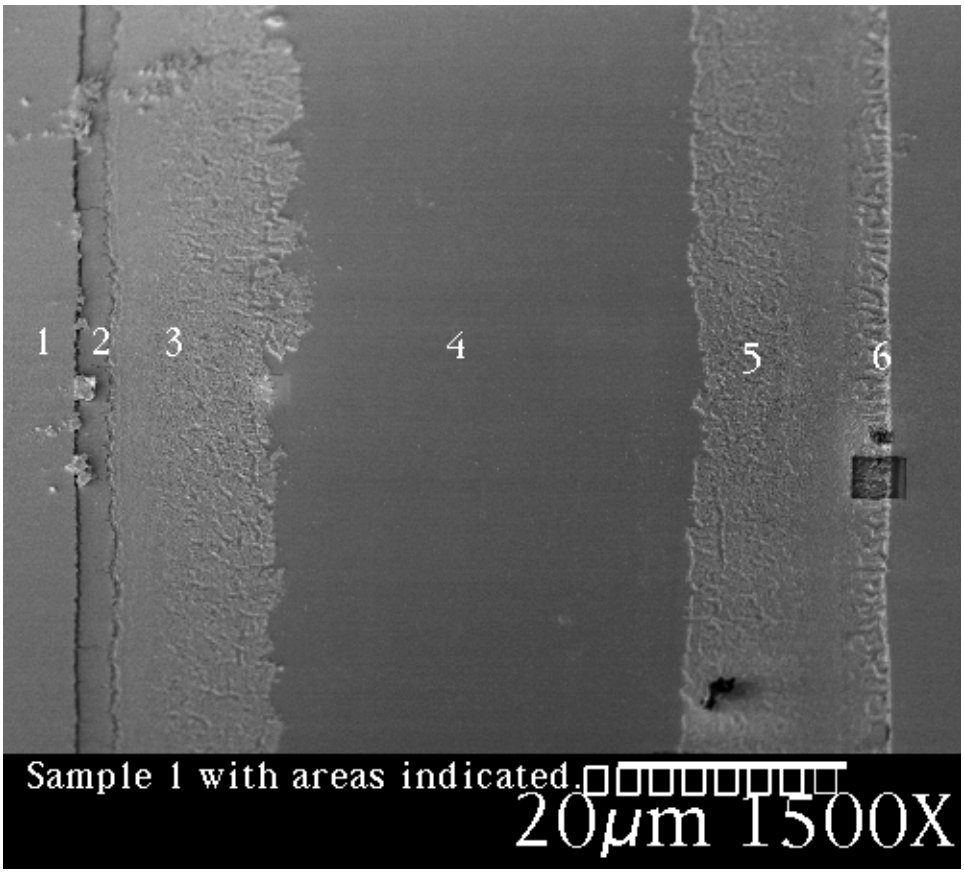


Figure 11. NREL supplied SEM of an etched P1 isolation via.

Auger analysis was complicated by sample charging; however, charging was less of a problem for area 2 than areas 3 through 5 since area 2 is close to the Mo. The following elements were identified for the areas labeled 1 and 2 on the numbered SEM.

Area 1; On the Mo	Mo, C, O
Area 2; On the transparent insulator	Mo, C, O, Ca, N, Fe

NREL also used XPS analysis however the dimensions of the probe beam are larger than the scribe width. Table 1 summarizes the results:

Table 1. XPS analysis of an etched Mo isolation scribe (percent concentration).

Analysis Area	C	O	Mo	Na	Ca	Si	S
Mo	57	25	16	1	1	0	0
Scribe including some Mo	60	23	12	1	trace	2	1

Module performance results are summarized in the following module power chart (Figure 12). Two circuits with particularly low performance were eliminated from the E-P1 data set (open data markers). The distribution of power for circuit plates with L-P1 is ~4 points better than the distribution for E-P1 and the difference is statistically significant. Differences in FF explain the majority of this difference. No definite but several possible causes for the low performance, including the analyzed narrow strip at the edge of all lines, were determined by observing circuit plates. It is assumed that elimination of these relatively small differences would be possible with in-house process development. The potential advantage of an E-P1 process for reducing sporadic shunting along P1 was not demonstrated since poor adhesion along P1 was not observed for either process during the time frame of this experiment. This alternative to isolation scribes produced with a laser was not adopted due to simultaneous improvements in the laser P1 and commercialization issues for the process.

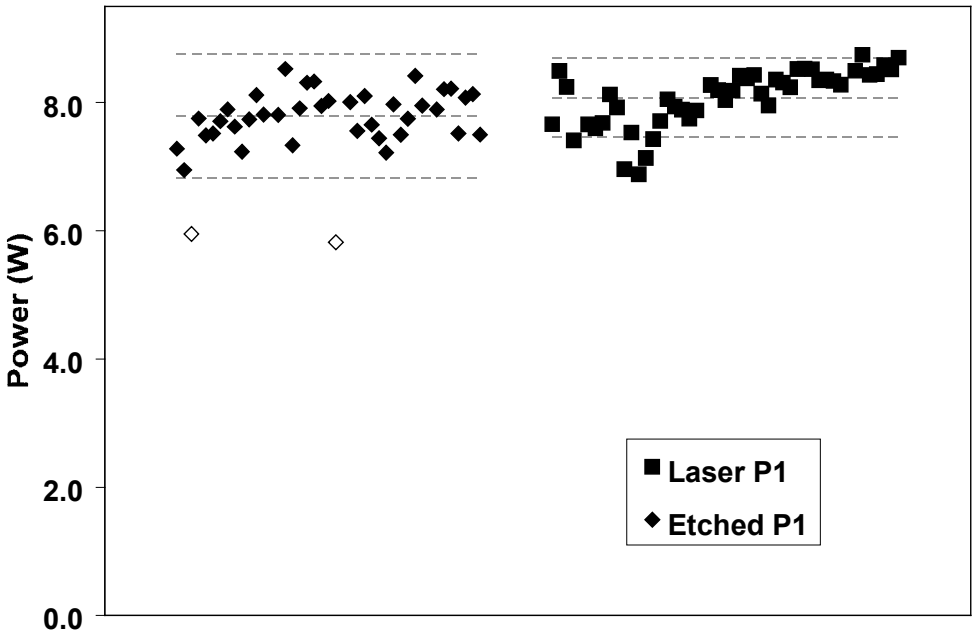


Figure 12. Module performance for laser and etched Mo patterning (abscissa – module identifier).

Process development related to Mo deposition and the absorber formation process is another example of collaborations between NREL and SSI. SIMS and AES analysis support from Sally Asher and Amy Swartzlander indicates that representative samples processed in both a large area reactor and a small area reactor exhibit minimal differences in the elemental profiles of the major constituents (Cu, Ga, In, S, Se) for a factor of two difference in the Mo thickness. With the exception of features that are assumed to be anomalous, the samples also exhibit minimal differences in the elemental profiles of the minor constituents. If observed differences by a factor of two to three in sodium and potassium are significant, the differences correlate with the reactors rather than the Mo thickness. The SIMS data set indicates anomalously high O_2 in one sample; however, the Auger data indicates that this high value is still below 1 to 2 atomic percent. The SIMS data also indicates a high Ca concentration in one sample. However, this signal is probably the result of contamination after formation of the absorber since the Ca profiles for all other samples but this sample exhibit structure in the Ca profile that parallels structure for other elements

in the graded absorber. Results of this collaboration resulted in support for decisions regarding implementation of process variations.

National CIS R&D Team Participation

The dependence of transient effects on circuit fabrication process have been examined in collaboration with NREL TFPPP Teams and as studies at SSI extending results from Team activities. The NREL TFPPP "Transient Effects Group" is composed of representatives from industry, NREL and universities (Joe delCueto, NREL; Joe Cuiffi. Pennsylvania State University; Keith Emery, NREL; Pam Johnson, Colorado State University, Larry Olsen, WSU; James Phillips, University of Delaware; Kannan Ramanathan, NREL; James Sites, Colorado State University; Dale Tarrant, Siemens Solar Industries; Hong Zhu, Penn State University).

SSI's participation in Team activities is focused primarily on understanding the fundamental mechanisms responsible for transient effects in CIGS-based devices with the objective of eliminating or minimizing their impact. Buffer layer technology is directly related to transient effects and alternative buffer layer approaches are also of particular interest for process scale-up. Therefore, team objectives also include defining improved buffer layer processes. Summarizing results for all of the extensive team activities is not attempted in this report since the expertise for most team activities resides with the team members. Instead, the following joint NREL/SSI experiment is discussed as an example of team work where SSI has had major involvement in sample preparation and data analysis.

Collaborative studies with Kannan Ramanathan (NREL) explored buffer and window layer options with emphasis on the impact of these layers on transient effects. Additional long term objectives of these studies were to improve understanding of the basic roles of the buffer and window layers, and to define a Cd free buffer layer process with minimal transients. In general, long term experiments are not necessarily limited to CBD, "dry," CVD or any particular deposition method; however, these initial experiments concentrated on existing deposition methods at NREL and SSI. The following will discuss studies to explore differences between CdS and ZnO deposited by NREL and SSI on SSI absorbers. Process variations included:

- SSI baseline CdS & ZnO
    - Standard processing time frame and environmental exposures during processing
    - SSI baseline held at SSI - interrupted processing to parallel the processing at NREL
    - SSI baseline shipped to NREL and back to SSI
- NREL baseline CdS & sputtered ZnO
- NREL CdS and SSI ZnO
- NREL CdS & thin sputtered ZnO combined with SSI ZnO

Process variations were tested using SSI mini-modules and small area NREL test structures (0.43 cm^2). Processing at SSI employed baseline processing with the exception of interruptions for shipping. The sputtered ZnO depositions at NREL were a standard NREL process. CdS deposition at NREL required modification of their standard procedures to allow processing 10x10 cm substrates. Relatively long storage times in N_2 occurred while waiting for processing at NREL and while waiting for the redevelopment of a 10x10 lamination process in new equipment at SSI.

Figure 13 and Table 2 summarize the data for circuit plates and cell. Circuit plate data is a measurement after two minutes of exposure and 1 sun illumination in a solar simulator. Poor circuit plate performance

and nominal cell performance for the NREL ZnO without the addition of SSI ZnO is not significant since this is simply due to a sheet resistance that is higher than appropriate for circuit plates.

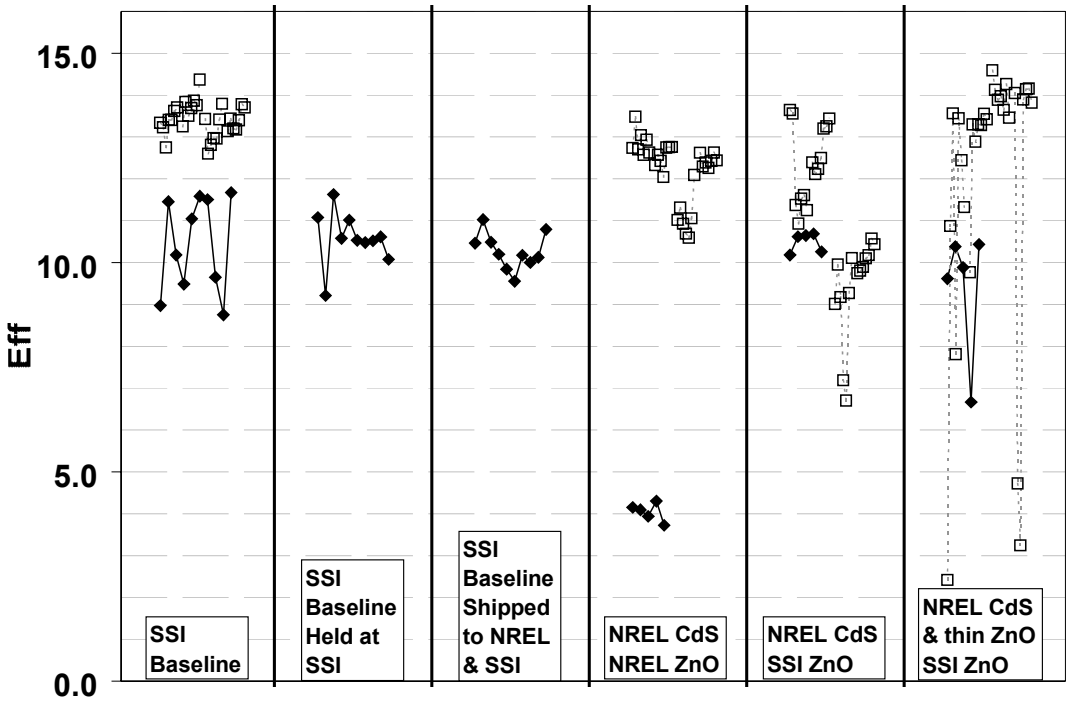


Figure 13. NREL/SSI buffer and window layer comparisons
Eff for circuit plates (♦, two minutes measurements) and cells ( ) .

Table 2. Statistical analysis of SSI circuit plates (two minutes measurements) and NREL cells.

Circuit Plate and Cell Measurements

Average, Standard Deviation, P-value

Mini-modules

Description	Group	Eff.		V_{oc}		J_{sc}		FF	
		Avg.	Dev. p -%	Avg.	Dev. p -%	Avg.	Dev. p -%	Avg.	Dev. p -%
SSI Baseline	**1**	**10.4**	1.2 68	**0.51**	0.02 **0**	**34.6**	0.4 **0**	**0.59**	0.1 12
SSI Baseline held at SSI	**2**	**10.6**	0.6 23	**0.49**	0.01 29	**34.5**	0.9 3	**0.62**	0.0 91
SSI Baseline shipped to NREL	**3**	**10.3**	0.4 100	**0.49**	0.01 100	**33.8**	0.6 100	**0.62**	0.0 100
NREL Baseline CdS & ZnO	**4**	**4.0**	0.2 **0**	**0.53**	0.01 **0**	**23.2**	1.1 **0**	**0.33**	0.0 **0**
NREL CdS / SSI ZnO	**5**	**10.5**	0.2 25	**0.52**	0.01 **0**	**32.5**	0.6 1	**0.62**	0.0 95
NREL CdS & thin ZnO / SSI ZnO	**6**	**9.4**	1.6 28	**0.50**	0.03 55	**33.0**	0.4 1	**0.57**	0.1 16

NREL Cells

Description	Group	Eff.		V_{oc}		J_{sc}		FF	
		Avg.	Dev. p -%	Avg.	Dev. p -%	Avg.	Dev. p -%	Avg.	Dev. p -%
SSI Baseline	**1N**	**13.4**	0.4 100	**0.54**	0.01 100	**34.8**	0.9 100	**0.72**	0.01 100
SSI Baseline held at SSI	2								
SSI Baseline shipped to NREL	3								
NREL Baseline CdS & ZnO	**4N**	**12.2**	0.8 **0**	**0.56**	0.01 **0**	**32.3**	1.1 **0**	**0.68**	0.02 **0**
NREL CdS / SSI ZnO	**5N**	**10.9**	1.8 **0**	**0.54**	0.01 **0**	**32.8**	0.8 **0**	**0.61**	0.09 **0**
NREL CdS & thin ZnO / SSI ZnO	**6N**	**12.0**	3.4 4	**0.52**	0.07 41	**34.0**	0.6 **0**	**0.66**	0.14 3

Table 2 summarizes the data in terms of average parameters, standard deviations, and T-test results. T-test results are rounded so that only entries that round to 0% probability indicate significant differences at the 95% confidence level. For circuit plates, the SSI baseline process which was shipped to NREL is chosen as the reference group (p = 100%). For NREL cells, the immediately processed SSI baseline is the reference group. The following summarizes the results for circuit plates and cells:

- There is a statistically significant but small (3 to 5 points in Voc and Jsc) difference between immediately processed SSI baseline circuits and those shipped to NREL and returned for SSI baseline processing (the reference group). The differences may be related to differences between CdS/ZnO processing groups at SSI or differences in storage time.

- Statistically significant differences are demonstrated between the Voc for the circuit plate reference group and the circuit plates with NREL CdS & SSI ZnO. This difference in Voc would not have been significant with a different choice for the reference group (the immediately processed SSI baseline circuits). However, also considering the T-tests for NREL cells indicates that there are significant differences between Voc and Jsc for CdS from NREL and SSI. NREL CdS yields a slightly higher Voc (2 to 5 points) and lower Jsc (2 to 7 points).

- The other entries in Table 2 indicating statistically significant differences between groups (typically Voc and Jsc entries) are related to high variability or small group size rather than physically significant observations.

Transient effect information for the process variations was obtained for circuit plates before lamination, after lamination, after a 12 day outdoor exposure, and after exposure to 85°C for 44 hours. For each of these states, data was obtained by taking multiple measurements during a two-minute exposure (~1.5, 5, 12, 30, and 120 sec.) in a constant light source solar simulator. As an example of this data, Figure 14 is a chart of FF data after exposure to 85°C for 44 hours ("dry dark heat") where the sequential measurements for each circuit are connected as illustrated to the right of the chart. Differences in transient effects for the process variations were compared for each state using a T-tests for differences in the change in device parameters over the two minute exposure, and differences in the slope calculated by linear regression of FF versus the log of the exposure time [3, 13, 14]. Process variation dependent transient effect differences without a consistent trend are observed before lamination, after lamination, and after a 12 day outdoor exposure. However, there was no statistically significant process dependence after the exposure to 85°C for 44 hours (Figure 14). T-test based comparisons for a relatively small data sets also indicated that there is no difference in transient effects for NREL sputtered ZnO and CVD ZnO.

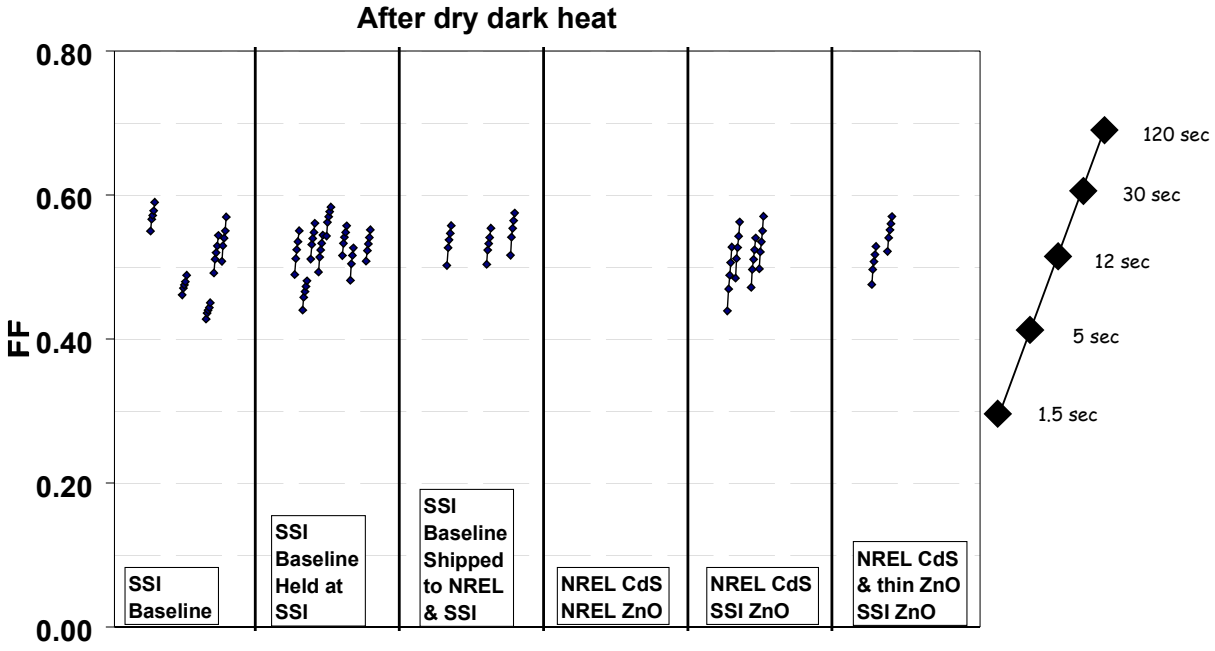


Figure 14. FF for mini-modules after a thermal stress.
(Multiple measurements over the two-minute test are connected for each circuit.).

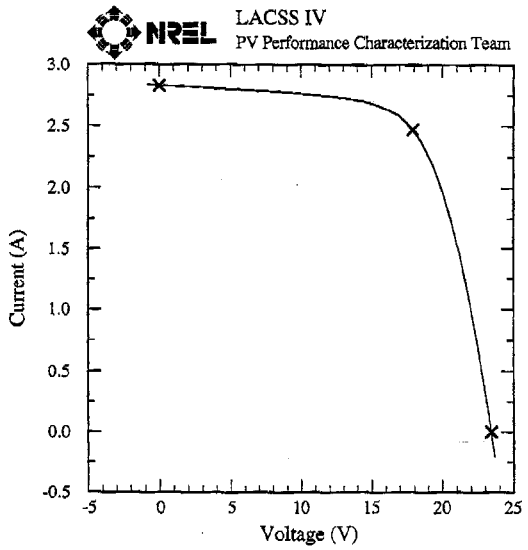
New Product and Deliverables

SSI introduced ST5 (5 Wp) and ST10 (10 Wp) products during the previous subcontract. During this subcontract period, R&D Magazine recognized the significance of this major milestone in the development of photovoltaics by awarding the prestigious R&D 100 Award to the SSI family of CIS modules. This award is shared by the California Energy Commission, NREL and SSI [15].

Also during this subcontract period, SSI announced the availability of two new CIS products. Larger area modules expand the power range of CIS products available from SSI – ST20 (20 Wp) and ST40 (initially rated at 38 Wp and then rerated as 40Wp). A photo of the expanded product line appears in Figure 15. These four products are fabricated from circuit plates that are processed through all device formation processes in an ~1x4 ft. format. The 1x4 ft. circuit plates are laminated as ST40 modules or cut to smaller sizes to form ~30x70 cm ST20, ~30x36 cm ST10, or ~30x18 cm ST5 products.

Figure 15. SSI's CIS thin-film module products.

NREL confirmed a world-record 12.1 percent conversion efficiency for a large area (3651 cm^2) CIS module.



	Module	per Cell	
Eff	12.1		%
Voc	23.4	0.558	V
Isc	2.8		A
Jsc		32.5	mA/cm^2
FF	66.9		%
Area	3651	86.9	cm^2

Figure 16. World-record 12.1 percent conversion efficiency large area CIS module.

The following deliverables were due for this subcontract phase:

- D1. End of the 12th month: Deliver ten (10) 900-cm^2 (1-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10%.
- D2. End of the 12th month: Deliver ten (10) 900-cm^2 (1-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10% for the NREL Module Testing Team.

These specifications for commercial modules as deliverables are most closely matched by the 10-Watt ST10 and the 5-Watt ST5 modules which were introduced in 1998. However, activities during this subcontract period led to the availability of commercial products larger than anticipated at the time the deliverables were defined. As agreed to by the NREL Technical Monitor, SSI delivered the following samples of larger area product as the D1 and D2 deliverables:

- Four 20-Watt "ST20" modules
- Four 40-Watt "ST40" modules

Product Durability

SSI completed the necessary engineering investigations and obtained FM and UL approval for the ST series of products. The durability and reliability of the ST family of CIS thin-film products is backed by a 5 year warrantee.

NREL supports SSI through long term testing of arrays and individual modules at the NREL Outdoor Test Facility (OTF). SSI has supplied modules of increasing size and efficiency for testing since 1988. The measurements in Figure 17 were made by bringing the modules indoors, performing the measurements under standard test conditions using a pulsed solar simulator, and then returning the modules to their outdoor test location. Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules have undergone testing for over eleven years.

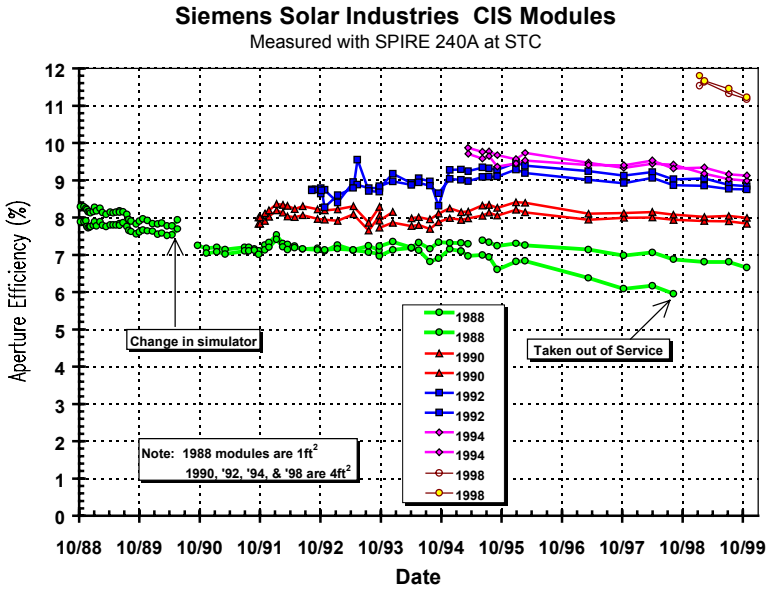


Figure 17. Long term outdoor stability measurements at the NREL OTF made using a pulsed solar simulator.

NREL measurements for long term stability testing include both measurements made using a pulsed solar simulator and measurements made outdoors near standard test conditions. The data in Figure 17 was obtained using a pulsed solar simulator and might be interpreted as showing performance variation with time. However, the effects of voltage bias history and light bias history for these modules that exhibit transient effects confound the interpretation of data particularly for pulsed solar simulators (3]. Parallel data made outdoors near standard test conditions is presented in Figure 18 and indicates much less variation in performance with time for all modules tested.

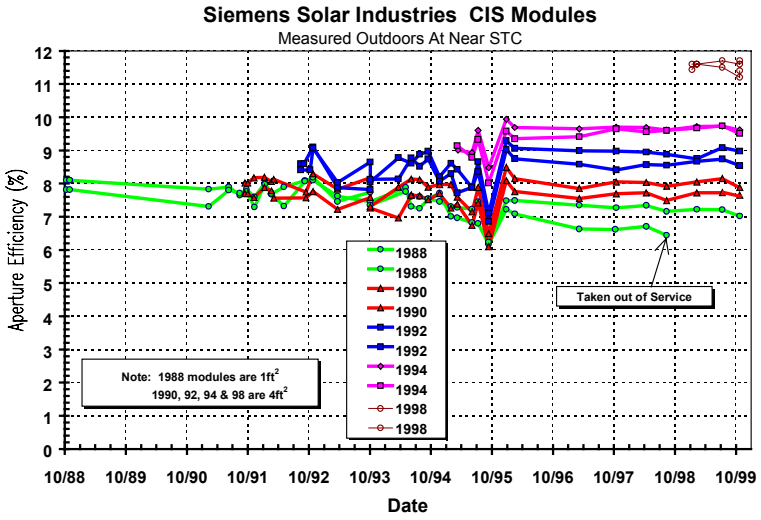


Figure 18. Long term outdoor stability measurements at the NREL OTF made outdoors near standard test conditions.

SSI has supplied modules to the NREL OTF for three 1kW arrays. In each case, a newer generations of modules has been used to replaced older designs using the same test site. The third 1kW array of modules was installed on November 17, 1998, and data acquisition started on November 18, 1998. The system is comprised of 28 modules with an average efficiency of 11.4% at STC. The aperture area of each module is 0.3651m^2 and of the total array is 10.223 m^2. The array is fixed at a 40° tilt aligned true south and is connected to a resistive load through 3 maximum power trackers. Figure 19 summarizes performance over 9-months of operation through June 30, 1999 for data restricted to between 950-1050 W/m^2. The array remains stable and has an average power normalized to standard test conditions of 1028 W.

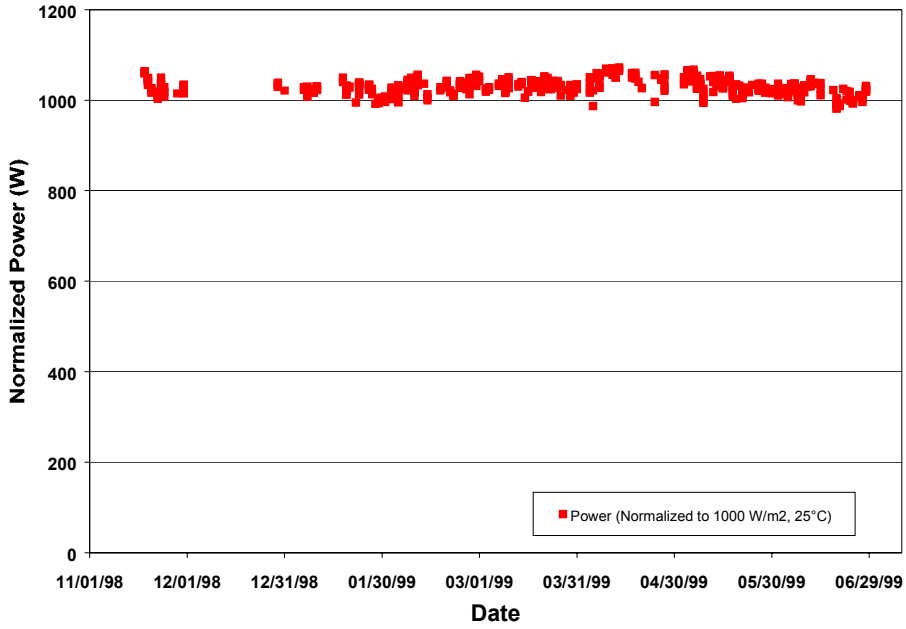


Figure 19. Temperature corrected power vs. time for the third 1kW array delivered to the NREL OTF in 1998.

Conclusions

Outstanding progress toward achieving NREL/DOE goals was achieved during this subcontract:

- SSI introduced two new CIS products to the SSI ST family of products including an approximately 1x4 ft, 40Wp module.
- Process data for the production of circuit plates for the CIS family of products demonstrates improved efficiency and exhibits generally good control for extended periods.
- The first subcontract milestone and the deliverables for this subcontract phase were met by delivering product samples that are larger and of higher efficiency than originally promised for this subcontract phase.
- Capacity has been increased while also increasing the average efficiency of 1x4 ft circuit plates from 10.8% to 11.2%.
- Yield improvements have been made by implementing improvements in processes and manufacturing protocols.
- FM and UL approval was obtained for the ST series of products.
- Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules have undergone testing for over eleven years.
- SSI is addressing near-term and longer-term R&D topics through SSI's participation in NREL CIS National Team activities.
- NREL confirmed a world-record 12.1% conversion efficiency large area (3651 cm^2) CIS module.
- R&D Magazine awarded the prestigious R&D 100 Award to SSI, NREL, and the CEC for the SSI family of CIS modules.

CIS has demonstrated the prerequisites for a commitment to large scale commercialization – high efficiency, long-term outdoor stability, and attractive cost projections. Remaining R&D challenges are to scale the processes to even larger areas, to reach higher production capacity, to demonstrate in-service durability over even longer times, and to advance the fundamental understanding of CIS-based materials and devices with the goal of further efficiency improvements for future products.

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15. The ST product development was supported in part by NREL as part of the Thin Film Photovoltaic Partnership Program through the US Department of Energy, and by a cooperative agreement with the State of California Energy Commission in support of the US Department of Energy's Commercialization Ventures Program.

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13. ABSTRACT *(Maximum 200 words)*

Outstanding progress toward reaching NREL/DOE goals was achieved during this subcontract:

- Siemens Solar Industries (SSI) introduced two new CIS products to the SSI ST family of products, including an approximately 1-ft × 4-ft, 40-Wp module.
- Process data for the production of circuit plates for the CIS family of products demonstrates improved efficiency and exhibits generally good control for extended periods.
- The first subcontract milestone and the deliverables for this subcontract phase were met by delivering product samples that are larger and of higher efficiency than originally promised for this subcontract phase.
- Capacity has been increased while also increasing the average efficiency of 1-ft × 4-ft circuit plates from 10.8% to 11.2%.
- Yield improvements have been made by implementing improvements in processes and manufacturing protocols.
- FM and UL approval was obtained for the ST series of products.
- Long-term outdoor stability has been demonstrated at NREL, where ~30-cm × 30-cm and ~30-cm × 120-cm modules have undergone testing for more than 11 years.
- SSI is addressing near-term and longer-term R&D topics through SSI's participation in NREL CIS National Team activities.
- NREL confirmed a world-record 12.1% conversion efficiency large-area (3651 cm^2) CIS module.
- R&D Magazine awarded the prestigious R&D 100 Award to SSI, NREL, and the California Energy Commission for the SSI family of CIS modules.

CIS has demonstrated the prerequisites for a commitment to large-scale commercialization – high efficiency, long-term outdoor stability, and attractive cost projections. Remaining R&D challenges are to: scale the processes to even larger areas, reach higher production capacity, demonstrate in-service durability over even longer times, and advance the fundamental understanding of CIS-based materials and devices, with the goal of further efficiency improvements for future products.

14. SUBJECT TERMS
photovoltaics ; CIS-based thin films ; monolithically integrated thin-film circuits ; outdoor testing ; module performance ; product reliability ; large-area circuit fabrication

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