September 2000 • NREL/SR-520-28710

Subcontractor Report

Apollo® Thin Film Process Development

Phase 2 Technical Report
May 1999–April 2000

D.W. Cunningham and D.E. Skinner
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Fairfield, California

National Renewable Energy Laboratory

1617 Cole Boulevard
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Introduction

The following report highlights achievements and progress in the Apollo® CdTe technology over the second phase of BP Solarex's PV Partnership program (ZAK-7-17619-27) at Fairfield, CA. In this report, the results are presented and discussed from the following areas:

CdS and CdTe optimization. In this section, semiconductor properties, optical properties and device optimization are discussed. Crystallographic characteristics were determined under collaborative work with the Institute of Energy Conversion, (University of Delaware) and NREL. In addition to this, module performance results are presented to illustrate the efficiency improvements gained as a result of this work.

Reliability and testing. In this section, both indoor stress testing and outdoor long term test systems are described. Detailed design, set up and initial results are presented.

Health, Safety and Environment. Three main sections described in this section are optimization of waste treatment systems at the Fairfield plant, reclaimed cadmium metal recycling and closed loop/zero discharge studies.

CONTENTS

TABLES

FIGURES

1.0 TASK 1: CdS AND CdTe OPTIMIZATION

Introduction

During Phase 2 of BP's thin film partnership project, the Apollo® team focused on the intrinsic properties of the electroless CdS and electrodeposited CdTe films. The film properties were investigated using various analytical methods to determine electrical, optical as well as morphological characteristics, in particular, how they changed at various stages of processing. This work lead to increased collaboration with CdTe teams in organizations such as Institute of Energy Conversion, University of Delaware (IEC, UOD) and NREL. Collaboration with both groups lead to a greater understanding of the mechanisms that contribute to the performance of the Apollo® devices and enabled the team to further optimize films.
Task 1 results will be presented relating to plating uniformity of CdTe, optical loss analysis within the film as well as morphological and crystallographic features of the semiconductors.

1.1 Cross Plate Uniformity:

In this section, cross plate uniformity is quantified in terms of electrical performance. This work was done primarily to determine the effect of substrate resistivity on uniformity as a prerequisite to large area plating, in particular to establish the limit for 24" wide, 0.94m^2, substrates. The work described here was performed on a 14", 10Ω/sq. substrate coated 900Å CdS and 1.8µm CdTe. The CdTe plate was cut down into 15cm wide strips in order to determine the cross plate performance uniformity. The cuts were made at 90^o to the laser cuts so that the integrity of the cells could be maintained. In doing this, the cells (area,15cm^2) could be measured individually and the cross plate performance could be obtained. In the electrochemical deposition of CdTe the width of the substrate is limited by the conductivity of the tin oxide layer. If a substantial voltage drop is observed across the plate, between the metal contacts, then this can affect the deposition stoichiometry of the CdTe. High (negative versus a cadmium reference electrode) potentials will encourage a cadmium rich deposit, while low potentials will encourage a tellurium rich deposit. The following graphs show the performance of the individual cells across the 14" dimension of the test plate.

Figure 1. through 4. illustrates the effect of CdTe uniformity for various electrical parameters across the plate. The cell number notation relates to individual cells of 10mm wide. The 10mm dimension is defined by the cell to cell separation of two laser scribe sets (one set equates to 3 separated scribes and defines the wasted width). For a normal Apollo® 14" x 61" module, the laser scribes run parallel to the 61" length. Cell 1 relates to the first cell on the left hand side of the module looking at the "sunny side" of the glass. Cell 32 relates to the last cell on the right hand side of the plate. There are 32 series connected cells with one cell sacrificed as a negative contact, this leaves 31 active cells. The cells were measured using a simple computer controlled addressable current/voltage source. Light level was set to 100mWcm^{-2} using a CdTe reference cell.

Figure 1. Efficiency Across the Apollo® plate

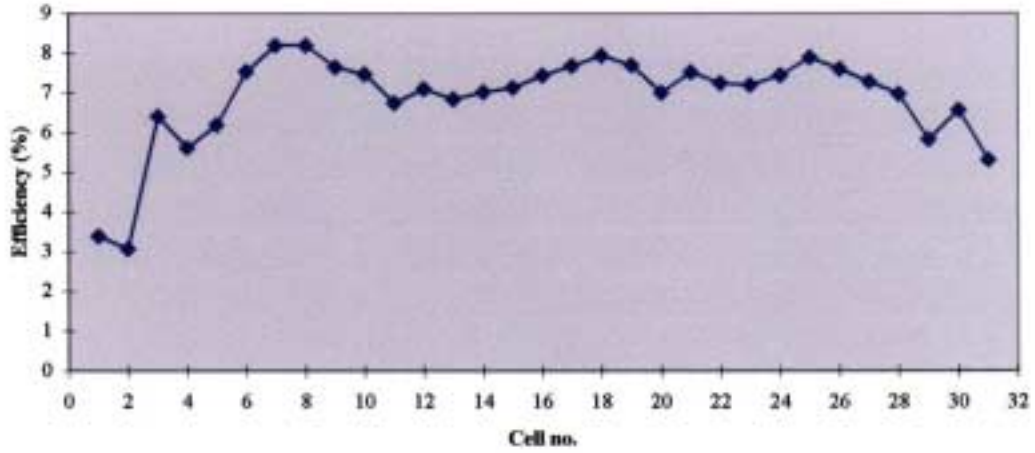


Figure 2. Voc Across the Apollo® plate

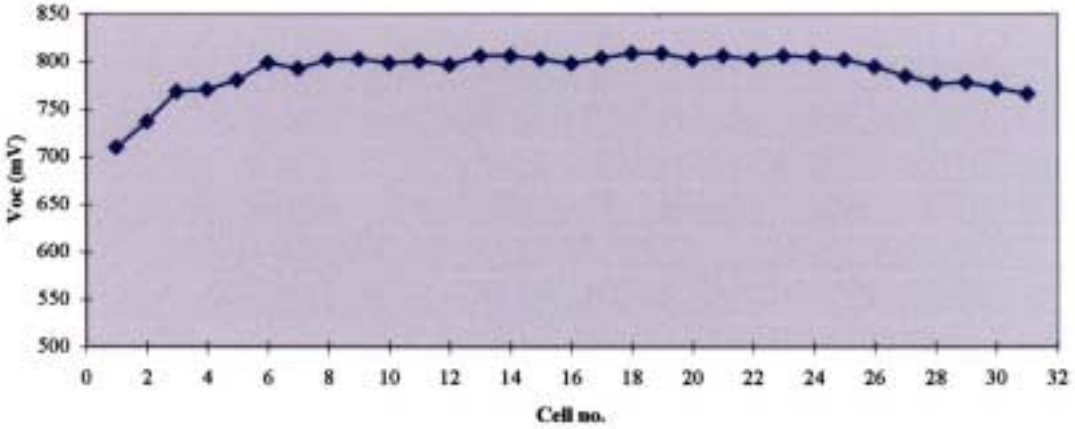


Figure 3. FF Variation Across the Apollo® plate

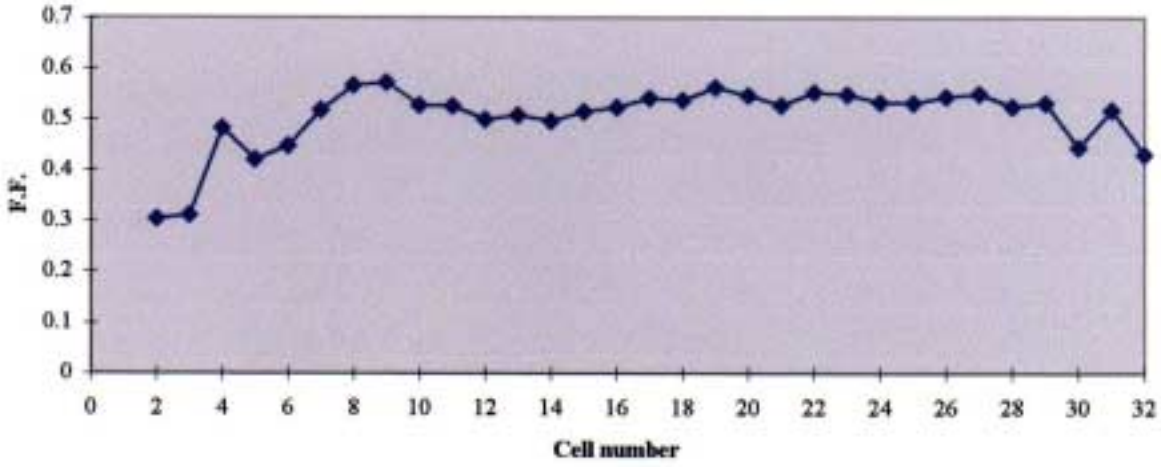
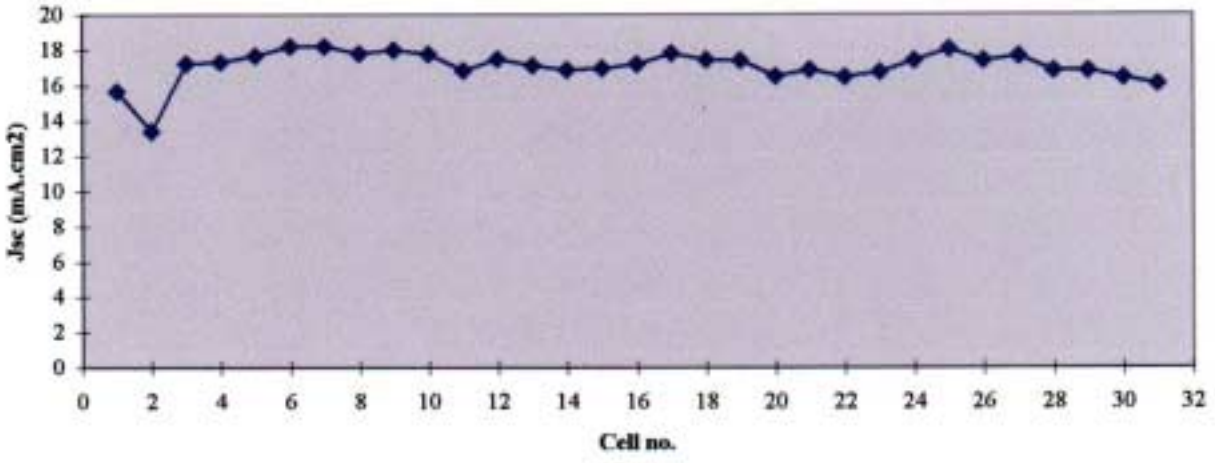


Figure 4. Jsc Across the Apollo® plate



It can be seen from the above graphs that the performance of the edge cells drops off considerably. The performance increases within the first two cells from the edge. All three electrical parameters decrease at the edge cells, however the largest contribution is from fill factor. The low fill factor was due to a combined increased series resistance and decreased parallel resistance. This is indicative of poorer quality material at the edges with reduced recrystallisation of the as deposited CdTe. X ray analysis confirmed this showing a larger abundance of <220> crystals in the center region post air anneal versus the edge region which retained a high proportion of the as deposited <111> crystal orientation.

The result indicated that in order for wider substrates to be electroplated successfully with good uniformity, a lower sheet resistivity would be required. It was estimated that sheet resistivities in the region of 8Ω/sq. would be required to maintain good composition uniformity across a 24" substrate.

1.2 CdS Optimization and Optical Loss Analysis

As part of the Apollo® team effort on semiconductor optimization, work has focused on characterization of the CdS/CdTe crystal structure at various stages of the process. BP has worked with IEC (University of Delaware) and the CdTe group at NREL in order to determine the physical properties of the films. Various techniques were incorporated including AFM and XRD as well as QE and electrical measurements. The data obtained from this work were used to optimize the semiconductor recrystallisation steps and heat treatments. One important study that was undertaken was an optical loss analysis of the finished device. The aim of this work was to identify the loss mechanism in the device and then prioritize for largest potential gain and compatibility with the existing process. The following section describes the work performed on standard CdS / CdTe cells

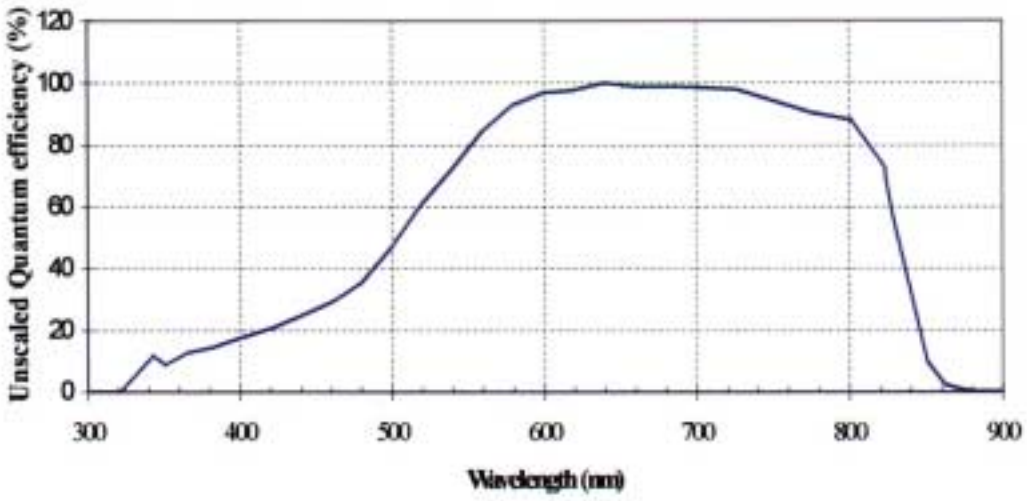
1.2.1 Device Loss Analysis:

Quantum efficiency measurements and a loss analysis were carried out on typical CdS and CdTe films. The CdS thickness was 1050Å and the CdTe thickness was 1.8microns. These films were deposited on standard TCO substrates with a sheet resistance of 10Ω/sq. Loss analysis was carried out at IEC (UOD) and module spectral response was measured by K Emery of NREL. The light and voltage bias conditions for the QE measurements were as follows.

Voltage Bias	16.20 V
Light Bias region area	16.00 cm2
Light Bias Density	0.587 mA/cm2

The spectral response for the Apollo® mini-module measured at NREL is shown in Figure 5.

Figure 5. Apollo® Mini-module QE



The mini module dimension was 645cm^2 and had a glass tedlar configuration. This size and construction was chosen especially for the QE work and is not standard for BP Solar's Apollo® product. Electrical connection was such that a single cell or the whole module could be measured independently if required.
The module electrical parameters that correspond to the above QE are shown in Table 1.

Table 1. Mini-module Electrical Characteristics

Voc	25.45 V (0.795V/cell)
Jsc	16.60 mA.cm^{-2}
FF	0.64
Efficiency	8.62%

1.2.2 Intepretation of the Module QE

The low Jsc is due to losses in the 400nm to 600nm wavelength range. This can be accounted for in terms of CdS absorption and band gap narrowing due to Te/CdS intermixing at the hetero-junction interface.

A complete loss analysis study was conducted by B McCandless of IEC (UOD) that lead to the following individual break down for specified wavelength ranges. The results are shown in Table 2:

Table 2. Summary of Loss Analysis

Loss mechanism	**Wavelength range** (nm)	**Integrated Photocurrent** ($mA.cm^{-2}$)
TCO/glass absorption	300-860	4.0
CdS absorption	300-490	3.0
Cell reflection	300-860	1.3
"Red" carrier collection	650-860	1.0
CdS/Te absorption	490-600	0.8
Unabsorbed red carriers	820-860	0.2

Some of the losses described above are avoidable but inevitable for a cost effective production process. For instance, $5mA.cm^{-2}$ of Jsc is lost due to TCO/ glass absorption and cell reflection. The TCO/glass absorption could be reduced by moving to 1mm thick borosilicate glass instead of float line, 3mm soda lime glass. Equally, the 10Ω/sq. (approx. resistivity $6x10^{-4}$ Ω.cm.) fluorine doped tin oxide could have a higher transmission by using other more transparent oxides. However, from a commercial point of view it is felt that gains in these areas, while technically possible, will increase the total cost of the product or reduce the robustness of the final device. Reduction of CdS thickness will reduce the absorption in the 300nm to 490nm range and increase Jsc accordingly. Jsc's as high as $19.0mA.cm^{-2}$ have been demonstrated with CdS thickness of 690nm to 700nm. However, this typically is accompanied by a loss in Voc and FF for the device. It has been shown by other groups ([1]) that highly resistive buffer layers can be incorporated between the TCO and the window layer to inhibit shunting through pinholes in thin CdS. Utilizing a thin, highly resistive tin oxide or zinc doped tin oxide buffer layer in conjunction with thin CdS has been used successfully to maintain Voc and fill factor while obtaining beneficial increases in Jsc. This could be one route to decreasing the losses from CdS absorption but as yet, there is little or no data on how compatible an electrochemical CdTe process is with a highly resistive buffer layer. Table 3 show results of electrical analysis performed on chemical bath deposition CdS produced at Fairfield. This data was generated by T. Gessert's group at NREL.

[1] National CdTe Team Meeting, Denver, 1998.

Table 3. CdS Electrical Properties

CdS ELECTRICAL PROPERTIES	
Sheet resistance	7.00E+09 ohm/sq.
Resistivity	7.00E+04 ohm.cm.
Mobility	2.86 $cm^2/V.s$
Doping density	-3.12E+13 $/cm^3$

Electrochemical deposition of CdTe on CdS is easily performed at BP Solar. The resistivity of the CdS film is $7x10^4$ ohm.cm. Therefore, it is hoped that the addition of a 1000Å, 1 to 10 ohm.cm. resistive film will not affect the plating potential required to control the deposit stoichiometry. Tests will be carried out to determine this.

Another area of considerable loss is in "red" carrier collection and absorption (total potential gain $1.2mA.cm^2$). Grain size for electrodeposited CdTe is small. Typically, CdTe grains average at 0.3 microns that is normal for low temperature processes. Increasing this grain size will reduce the grain boundary to grain size ratio and improve carrier lifetime and collection. This is an area the BP Solar team will continue to investigate.

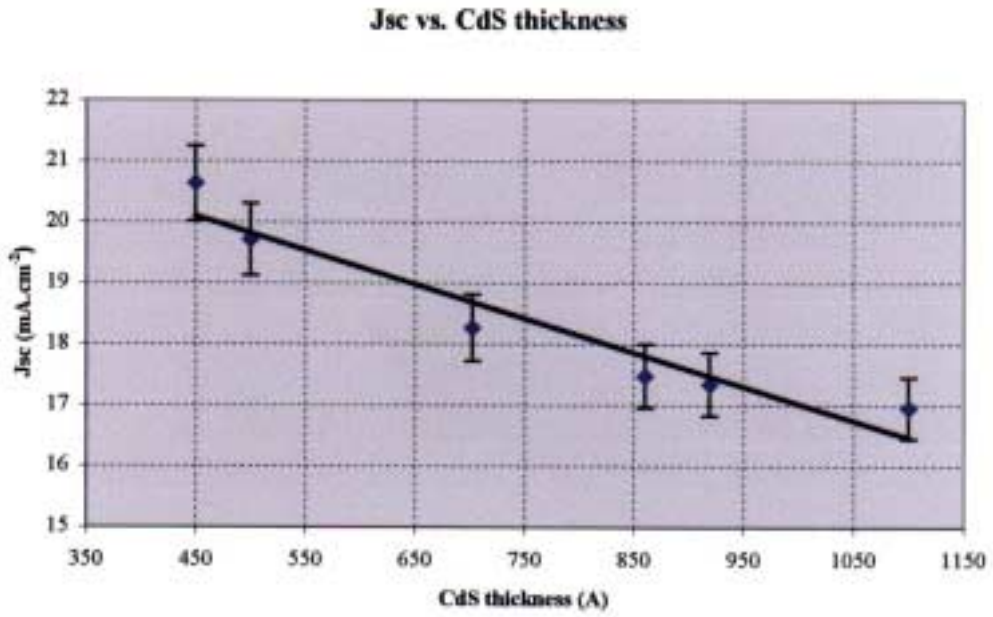
In summary, the loss analysis has helped focus efforts in areas that will increase device performance through Jsc increases. If a Jsc of $20mA.cm^{-2}$ is used as a target for $0.55m^2$ and $0.94m^2$ modules, then if the Voc and fill factor illustrated in Table 1 are maintained, then module aperture area efficiencies greater than 10% will be realized.

1.2.3 Optimization CdS Window Layer Thickness

A study was performed to determine the relationship of Jsc with CdS thickness to follow on from the optical loss analysis described in the previous section. The loss analysis had shown that between 3 to 4 $mA.cm^{-2}$ could be gained from optimization of the CdS properties. The majority of the gain coming from a reduction in the CdS thickness.

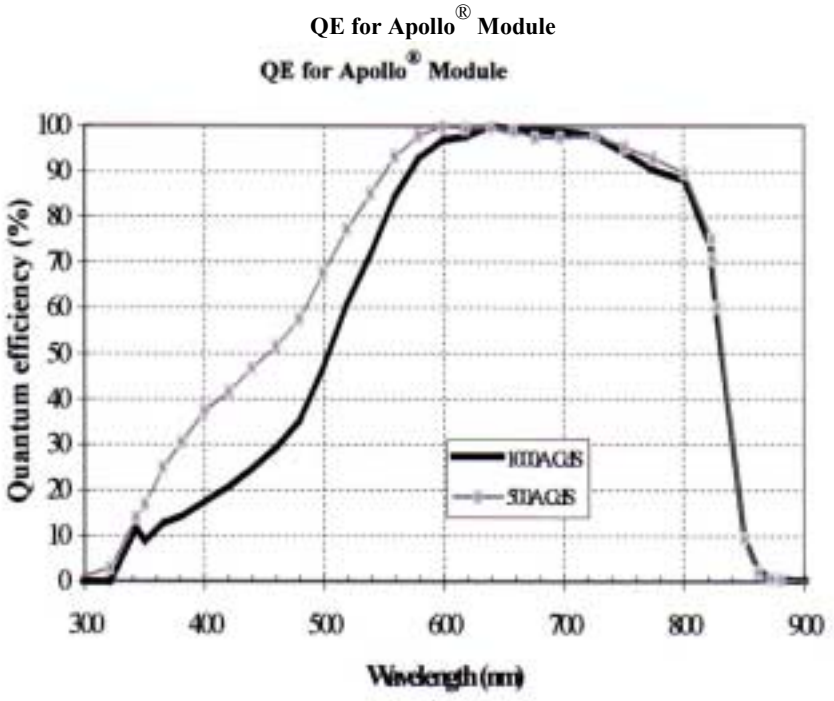
The loss analysis had been performed on a mini module that had a 1050Å thick CdS film which gave a corresponding 16.6 $mA.cm^{-2}$ Jsc. CdS films were made using a modified chemical bath deposition process which gave thickness as low as 450Å. Figure 6 shows the relationship of CdS thickness with Jsc as the film is reduced and glass substrate, CdTe and back contact films remain constant. From these devices, quantum efficiency measurements were obtained to ascertain the effect on the blue response on reducing the window layer.

Figure 6. Jsc vs. CdS Thickness



Quantum efficiency (QE) is a good technique for determining the wavelength dependent response for solar cells. Quantum efficiency also helps resolve the spatial response through the device. Knowing the band gap and absorption coefficients of the window and absorber layers, a loss analysis can be performed to determine which semiconductors are limiting performance. The QE shown in Figure 7 shows the response for Apollo® devices made with different thickness' of CdS window layer. The standard process incorporates a 1000Å CdS layer, which limits the blue response of the device. At 400nm and 500nm, the QE values are 17% and 50% respectively for the standard device. This wavelength range has been shown to be greatly influenced by CdS absorption. Typical Jsc values associated with a 1000Å CdS film are in range of 17mA.cm^{-2}. The QE for devices containing a 500Å and 1000Å window layers are compared in Figure 7. Clearly, there is an improved blue response for the thinner window layer. At 400nm and 500nm, QE values of 38% and 69% were measured respectively with essentially no change in the regions relating to the bulk absorber (>600nm). The Jsc values for these devices were in the range of 20.0mA.cm^{-2}, indicating more than 20% increase over the thicker window layer. We believe this is a significant achievement as these Jsc values are currently unprecedented for a commercial size modules. Later in the report, the effect of improved blue response on device results will be discussed in more detail.

Figure 7. QE for Reduced CdS Window Layer vs. Standard Thickness



1.3 CdTe Morphology

1.3.1 Cross Plate Uniformity

In Section 1.1 there was a clear edge to center effect with lower performance in the first 3 to 4 cm. It was believed that these variations were due to crystallographic differences within the deposited CdTe film. In order to determine this, X-ray diffraction (XRD) studies were performed on the CdTe film. The back contact was removed from the material so that crystal orientation could be determined and matched directly to the cell electrical results. The study focused on two CdTe orientations in particular, <111> and <220>. As deposited, CdTe has an abundance of <111> orientation grains. A heat treatment in air at 450C induces recrystallization and the <111> grain diminishes as the <220> orientation increases.

The analysis showed that the poorer performing edge material had a low <220>/<111> ratio indicating a high predominance of <111> grains post heat treatment. Table 4 shows a low <220>/<111> ratio for cells 2 and 32 (edge cells) while cell number 6 and 26 shows a predominance of <220> grains post heat treatment. Cells 6 and 26 are representative of mid plate cells.

Table 4. Orientation Ratio for CdTe, Edge to Center

<220> / <111> ratio data for CdTe.	
Cell #	Ratio
2	0.03
6	1.48
26	1.21
32	0.21

An edge to center performance variation has been shown for the electro-deposited CdTe material. This has been mainly due to low fill factor and Voc. XRD studies has shown that the lower performance material has a lack of <220> orientation grains, post heat treatment. Further studies will focus on the cause of the lower performing material and how recrystallization can be enhanced in those regions.

1.3.2 Morphology of Center Plate CdTe Material

In order to understand the crystallographic detail samples were sent to external laboratories (NREL and IEC) for analysis and quantification of the changes in morphology at various stages of the CdTe process. Of particular interest was the form of the CdTe directly after electrodeposition and after subsequent heat treatments. Typically, low temperature depositions of CdTe such as electrochemical, physical vapor deposition, and sputtering afford small grain structures (<1μm). There is a considerable amount of strain incorporated in these films as deposited and the crystal structure has a predominant <111> orientation. Strain relief, is one of the aspects seen in the CdTe film after a 450C anneal in air, as is a change in orientation of the crystal unit cell. As well as the orientation change, grain growth can also occur when the heat treatment is performed in the presence of chloride. In the electrochemical deposition of CdTe, chloride can be incorporated in the film during the plating process. Initial results confirm that chloride additions can also be performed post deposition, commensurate with other CdTe films.

The two techniques used to investigate the crystal structure were atomic force microscopy (AFM) and X-ray diffraction (XRD). The following data illustrates some of the typical structures seen for the Apollo® films.

Figure 8. **AFM of as Deposited CdTe**

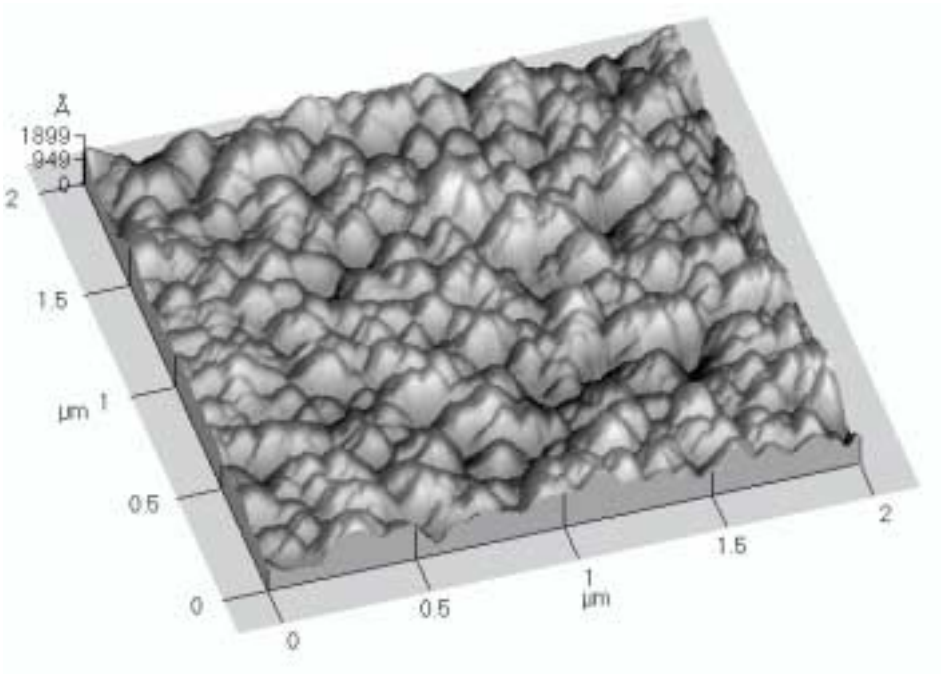


Figure 9. XRD of as Deposited CdTe Film

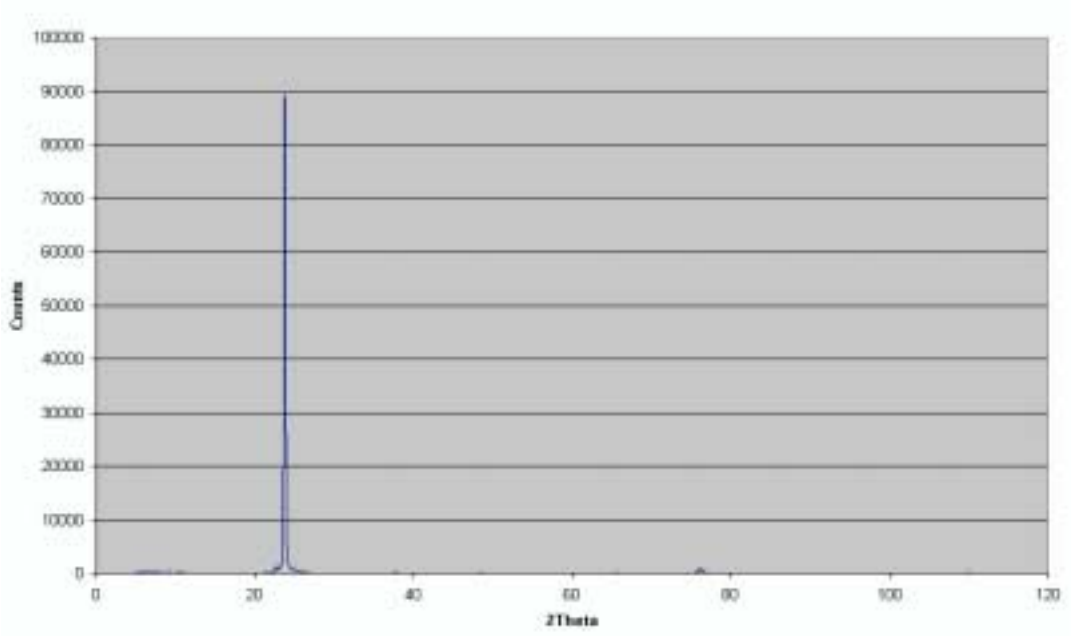


Figure 10. AFM of CdTe Post Air Anneal

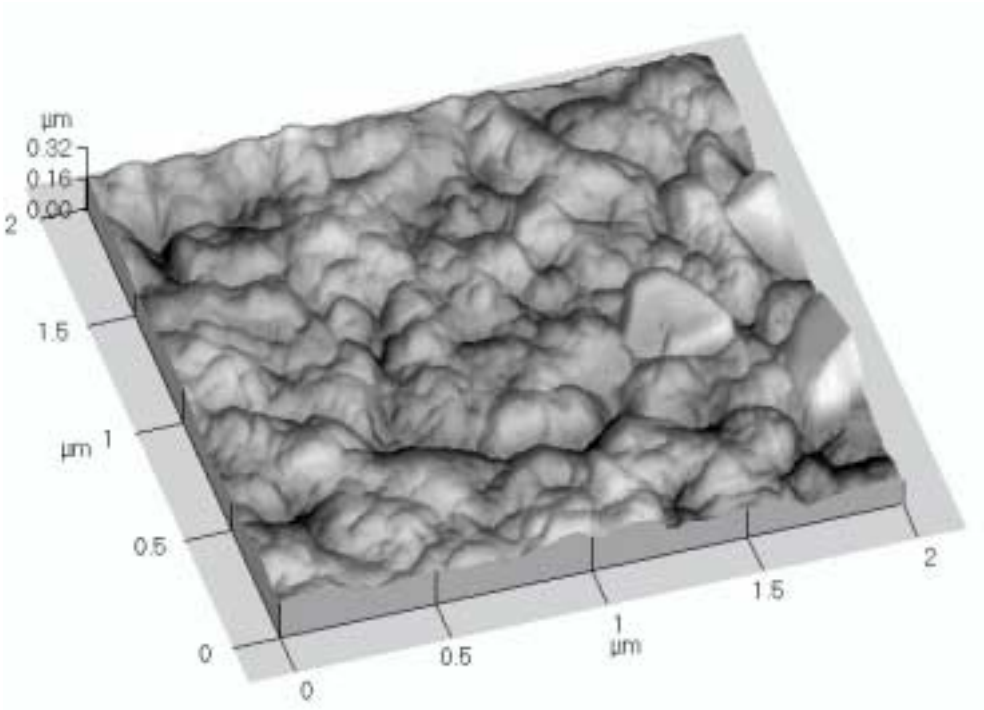


Figure 11. XRD of CdTe Post Air Anneal

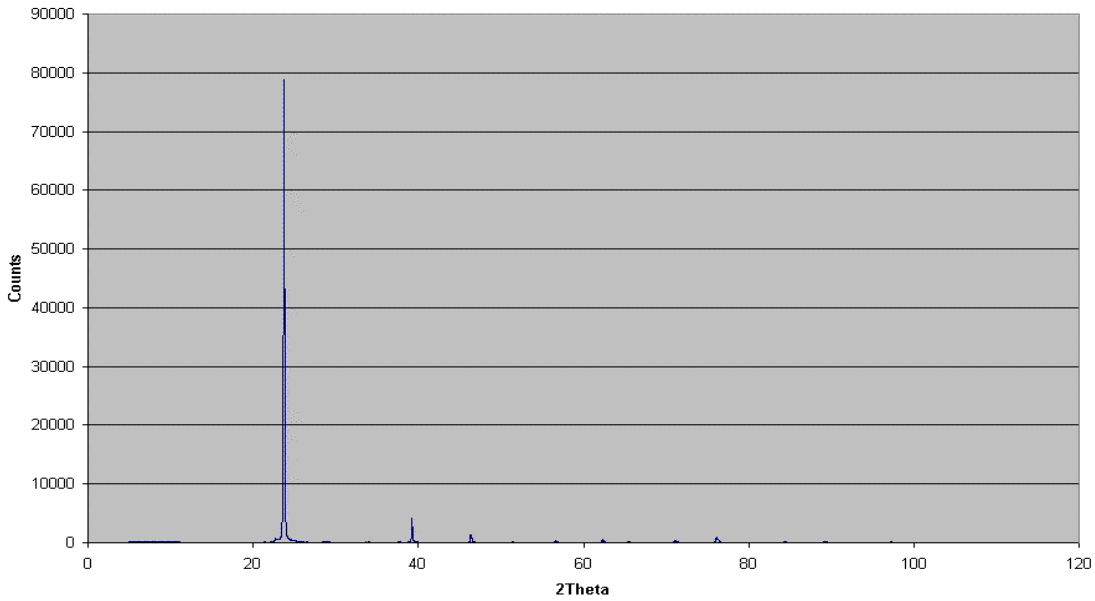


Figure 8 shows the grain structure for as deposited CdTe. The typical grain size is between 0.1μm and 0.2μm. Some grains exhibit faceted faces, which indicate that grain sizes could be smaller than 0.1μm. The XRD data in Figure 9 shows that the grain orientation at this stage was predominantly <111> as normally seen for films at this stage.

Figure 10 shows grain formation after heat treatment in air at 450C. Some grain growth and coalescing of the grain facets was observed. Also, the maximum grain dimension had increased to about 0.4μm from 0.2μm.

The XRD results for this film shown in Figure 11, shows some increase in <220> orientation at 39°, Theta.

This data indicates that, while some gain growth occurred, it was not substantial and that the grain structure is held or pinned in some way. This is also confirmed by only slight growth in <220> orientation.

1.4 Device Results

1.4.1 0.55m^2 Module Performance

Four 0.55m^2 modules were sent to NREL as deliverables during Q2. The deliverable criterion for Phase 1 was for an active efficiency greater than 8% on a 14" x 61" module.

Table 5 shown below summarizes the results from measurements made at NREL. Spire 240A and outdoor measurements are shown for each module.

Table 5. 0.55m^2 Module Measurements Made at NREL

Module Number	Test System	Voc (V)	Isc (A)	FF (%)	Pmax (W)	Cell Eff. (%)
92030034	Spire 240A	24.7	2.53	0.61	38.2	8.1%
92030034	Outdoors	24.7	2.55	0.63	40.0	8.4%
92030041	Spire 240A	24.4	2.62	0.60	38.2	8.1%
92030041	Outdoors	24.5	2.63	0.63	40.4	8.5%
92030055	Spire 240A	24.8	2.57	0.60	38.4	8.1%
92030055	Outdoors	24.8	2.61	0.62	40.0	8.4%
92080115	Spire 240A	24.6	2.57	0.62	39.5	8.3%
92080115	Outdoors	23.5	2.60	0.62	38.2	8.0%

The cell (aperture) efficiency was calculated from the active area of each cell. The total active area was 153cm^2 per cell with 31 cells in series connection. This gave a total active (aperture) area of 0.474m^2. All modules satisfied the deliverable criteria of >8.0% for Phase 1 of BP Solar's Thin Film PV Partnership program. Two modules were returned to BP Solar to be used as reference modules for performance testing.

1.4.2 Electrical Performance of Reduced Window Layer Devices

The potential benefits of a reduced window layer were discussed in the previous section. The optical improvement in reducing the window layer thickness from 1000Å to 500Å is seen as an increase in blue response in the 400nm to 500nm range. The relationship of increase in Jsc with reduced CdS layer was also shown earlier. It was found that on reducing the CdS layer significantly below 500Å that a loss in Voc and fill factor occurred. This is commensurate with increased shunting from micro pinholes in the CdS layer. One method to reduce the effect of this layer may be to introduce a high resistivity buffer layer between the CdS and conducting oxide film. As mentioned before, this is not fully proven in the electrochemical deposition process used at Fairfield, especially when considering the sensitivity to potential drop that this system has.

A series of devices were made using a CdS film at 500Å. Some typical values for devices incorporating the reduced window layer are shown below in Table 6.

Table 6. Electrical Performance of Reduced Window Layer Modules

VOC (V)	VOC/CELL (V)	ISC (A)	JSC (mA.cm^{-2})	PMAX (W)	FF	EFFICIENCY
26.46	0.827	3.19	21.0	54.3	0.64	11.1
26.57	0.830	3.18	20.9	53.3	0.63	10.9
26.22	0.819	3.08	20.3	51.1	0.63	10.5
25.96	0.811	3.09	20.3	50.0	0.62	10.3
26.26	0.820	3.05	20.1	49.0	0.61	10.1
25.89	0.809	3.03	19.9	47.3	0.60	9.7
25.78	0.806	3.02	19.9	46.0	0.59	9.4

Comparing the results with those using the standard process, the main difference in the performance can be seen as an increase in Jsc. The difference in Voc is due to the alternative process modules containing 32 series connected cells instead of 31 as in the standard process cells. The increase in Isc relates to a Jsc change from an average of 17mA.cm-2 for the standard modules (1000Å CdS), compared to 20.3mA.cm-2 for reduced window layer modules. This gain is inline with the gain predicted by the loss analysis.

Figure 12. Efficiency Histogram for Reduced Window Layer

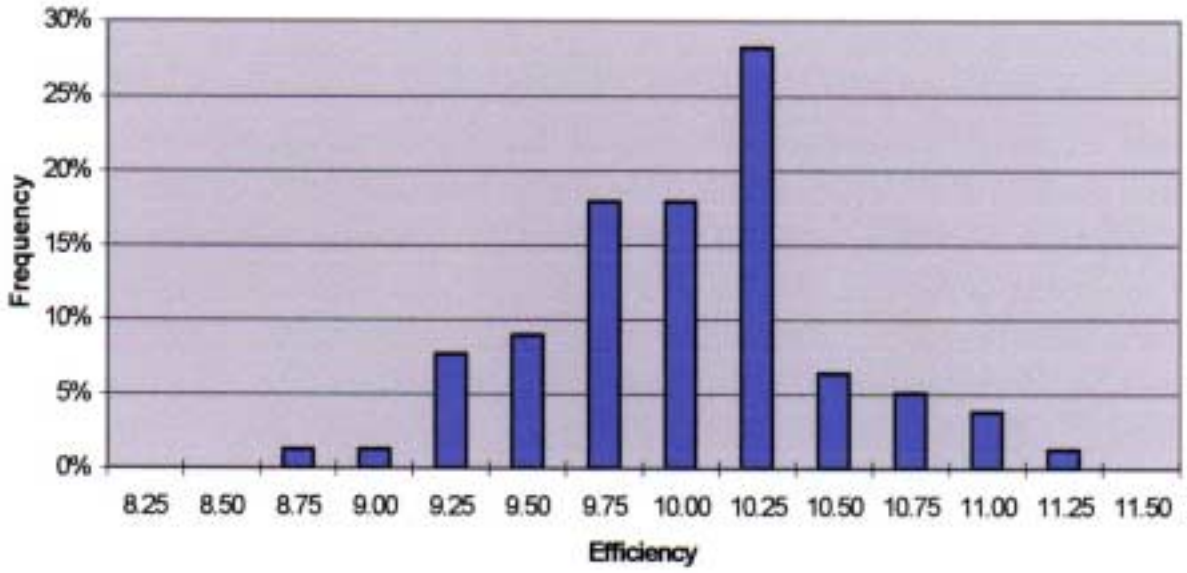


Table 7. Statistics for Alternative Process Run

	Voc (V)	Voc/cell (V)	Isc (A)	Jsc cal (mA.cm^{-2})	Pmax (W)	Vmp (V)	Imp (A)	FF	Rs.cm2 (ohm.cm^{-2})	Eff. (%)
Average	26.09	0.815	3.09	20.3	48.4	18.45	2.62	0.599	10.7	9.9
Max	26.57	0.830	3.43	22.5	54.3	19.48	2.82	0.642	18.1	11.1
Min	24.91	0.779	2.97	19.5	42.0	16.30	2.44	0.528	7.6	8.6
Stdev	0.31	0.010	0.08	0.5	2.4	0.52	0.08	0.021	1.2	0.5

The data in Table 7 shows the distribution efficiencies for four production runs using the reduced window layer process. A maximum efficiency of 11.1% was measured in this distribution with an average of 9.9%. In Figure 12, even with a reduced CdS layer, a very good Voc and fill factor were maintained. From the histogram, it can be seen that the efficiency mode is approximately 10.25%. This indicates the capability for an optimized process should give an average efficiency higher than 9.9%, as recorded above, once process defects have been removed.

1.5 Large Area Module Development

Considerable effort was placed on large area development during this phase. One of the challenges for electroplating large areas is how to overcome potential drop within the conductive transparent oxide (CTO). While potential drops in the connections to the plate are minimal, potential drops in the CTO between the connections can be substantial. If a substantial potential drop occurs in the CTO, then CdTe stoichiometry will vary, favoring Te rich or Cd rich CdTe deposits, depending on the extent of the drop within the plate.

The technical team at BP Solar worked with suppliers to obtain CTO films with sheet resistance below 10Ω/.sq. in order to reduce potential drop in the 61" x 24" ($0.94m^2$) plate. Initial results were encouraging, and films were obtained with good compositional uniformity. Some of the first plates were fully processed without cutting down to smaller sizes. The results indicated good robustness of the process towards large area scale up. The performance of two of the plates was verified at NREL and the results are summarized in Table 8.

Table 8. $0.94m^2$ Module Measurements Made at NREL

Module Number	Test System	Voc (V)	Isc (A)	FF (%)	Pmax (W)	Cell Eff. (%)
92440041	Spire 240A	44.92	2.476	.607	67.53	7.8
92440041	Outdoors	45.00	2.466	.623	69.08	7.9
92030054	Spire 240A	45.08	2.503	.615	69.43	8.0
92030054	Outdoors	45.19	2.477	.646	72.23	8.3

The electrical configuration of these modules consisted of 57 cells in series. The cell area was $152.3cm^2$ giving an active are of $0.868m^2$ and a total module area of $0.944m^2$. All these dimension measurements, together with the electrical measurements were confirmed by NREL.

Initial results (Table 9) using the reduced window layer process on large area were also encouraging. The results below show typical values for $0.94m^2$ modules incorporating a 500Å CdS film. Compared to the 14" wide substrate Voc and Jsc are only marginally lower for the 24" substrate. Jsc is probably lower due to increased light absorption in the thicker conducting oxide for <10Ω/□ substrates required for large area deposition. The fill factor was considerably higher for the large area plates. This improvement comes from the lower sheet resistivity substrate.

Table 9. 0.94m^2 Module Results with Reduced Window Layer

Module Number	Voc (V)	Voc/cell (V)	Isc (A)	Jsc (mA.cm^{-2})	Rs.cm^{-2} (Ω.cm^{-2})	Pmax (W)	FF	Eff. (%)
01010001	46.17	0.810	3.07	20.18	8.08	89.6	0.632	10.3
01010012	46.62	0.818	3.02	19.85	8.17	89.6	0.636	10.3
01010018	46.32	0.813	3.00	19.73	7.54	90.3	0.649	10.4
01010019	46.52	0.816	3.03	19.89	7.60	91.0	0.646	10.5
01010021	46.28	0.812	3.00	19.72	7.63	90.0	0.647	10.3
01010023	46.57	0.817	2.97	19.48	7.66	89.7	0.649	10.3
01010025	46.18	0.810	3.04	19.96	6.24	89.7	0.640	10.3
01190016	45.30	0.795	3.05	20.03	8.25	86.4	0.626	9.9
01190022	46.52	0.816	3.03	19.90	7.84	88.6	0.629	10.2
01190025	46.06	0.808	3.10	20.34	9.20	87.8	0.616	10.1
Average	**46.25**	**0.811**	**3.03**	**19.91**	**7.82**	**89.26**	**0.637**	**10.3**

Four modules were sent to NREL for measurement confirmation. These modules were also to be used as primary references by the Apollo® team at Fairfield. NREL measured one of the modules as having an aperture efficiency of 10.6% with a power of 91.5W. At the time of this report, this is the highest power monolithic thin film module measured at NREL and supercedes the 72.2W record held by the Apollo® group last year.

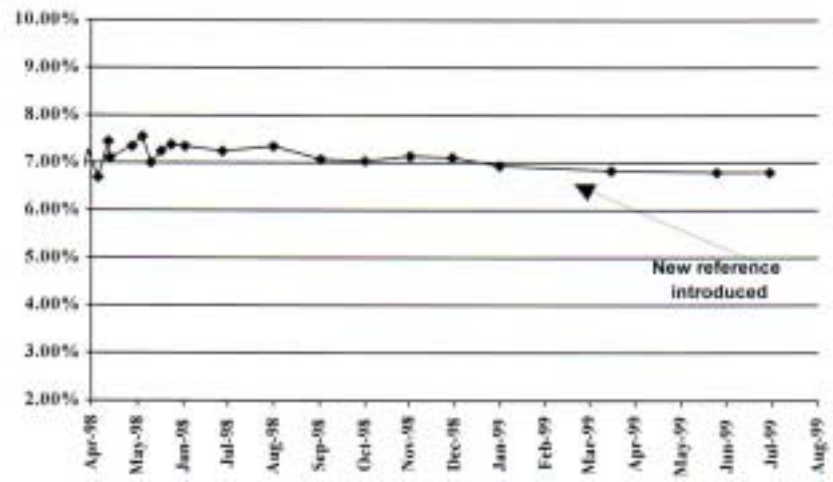
2.0 TASK 3: RELIABILITY AND MODULE TESTING

2.1 Outdoor Testing

Figure 13. Apollo® Grid Connected Array Layout

The Apollo® CdTe modules made in April 1998 last year have been on continual test outside for 16 months (Figure 14). The modules still show good stability. The drop seen in February 1999 was in fact due to a reference re-calibration (NREL measurement). The modules used on this small array are some of the very first articles made at Fairfield. They have subsequently made way for newer module varients and more flexible systems that allow for easier and more comprehensive, in situ data acquisition. In this section of Task 3, those new outdoor systems (Figure 13) will be discussed.

Figure 14. Apollo® Module Stability at Fairfield



During quarter 2 of phase 2, the BP Solar engineering staff replaced the original 14" x 48" engineering modules on the grid connected system with 14" x 61" samples. A total of 48 of the larger modules were installed on the system. The average power of the new modules was 35W (STC) and therefore, the STC rating for the array becomes 1.68kW. The new modules were connected in the same series/parallel configuration except that there are 4 groups of 12 modules instead of 6 groups of 12. The DC output from the modules (Vmax and Imax) will be logged on a regular basis as before. The reason for the reduced module number was due to the structure wind loading capacity, which would be exceeded if the same number of larger units were installed.

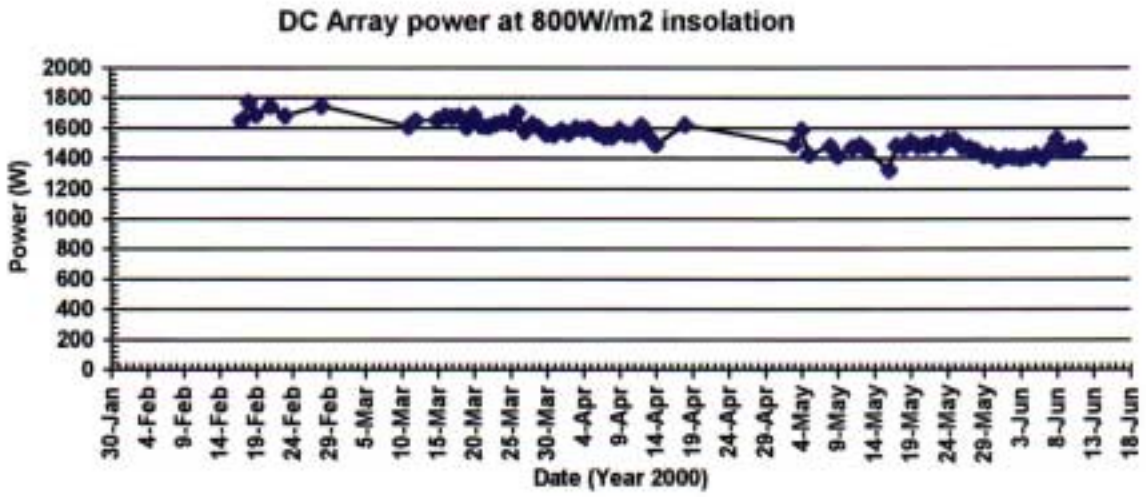
In Figure 15, the new loading configuration can be seen. The retrofitted array is in the background of the picture.

Figure 15. Retro Fitted 1.68kW Array and 2.23kW Array. (Powers STC)

In January 2000, a new array was commissioned on the grounds of the Fairfield facility. The array incorporates 60, 0.55m^2 Apollo® modules with an average STC performance of 38W each (foreground array in Figure 14 & 15). This would give an equivalent array output of 2.28 kW (DC STC) assuming no system/inverter losses. The array is connected to an Omnion 2200 inverter. There are 3 sub arrays of 20 series connected modules. The inverter is bi-polar and a center tap is made between the 10th and 11th module. Each group of 20 modules is connected in parallel and before input is made to the inverter. The DC outputs of the sub arrays are monitored using shunt resistors to determine load current while DC load voltage is measured directly across each sub array. The readings are recorded in a shared data acquisition system (DAS). The DAS is shared with the 1st ground mounted system installed in 1999. The 1st system (shown in the background of Figure 14 & 15) was retrofitted with 48, 0.55m^2 Apollo® modules in October 1999 after the original 14" x 48" engineering prototypes were removed. The 0.55m^2 modules are a

truer representation of production devices. Both systems are monitored every two minutes.
Some of the initial data from the newest array is shown in Figure 16.

Figure 16. Output of Omnion 2200 Array



On first appearance it looks as though there was a reduction in performance over the first 5 months of operation. In order to isolate system, module and/or temperature effects, the bottom row of 20 modules was removed and measured internally on a Spire 240A simulator. The results and comparison with pre installation values are shown in the Table 10 below.

Table 10. Array String Indoor Measurements

SPIRE 240A MEASUREMENTS FOR STRING 1.							
Date		**Isc**	**Voc**	**Rs**	**PMax**	**FF**	**Eff**
1/12/00	average	2.71	25.2	2.99	38.4	0.561	7.87
6/12/00	average	2.71	25.2	2.38	39.0	0.570	7.97
Change	average	0%	0%	-21%	1%	2%	1%

It can be seen that the internal measurements indicate no change in module perfromance over the last 5 months of operation under load. The modules have been reinstalled and a similar comparison will be made once per quarter.

2.2 Internal Light Soaking.

Two new internal light soak stations have been constructed. The light soak stations were constructed to hold five, 0.94m^2 modules per unit. The modules can be held at Voc, Isc or Pmax. The Pmax is set using a simple variable resistor with the load current and load voltage displayed, real time, via a computer interface. The modules are forced cooled in air using a central fan. The lamps are 2kW metal halide and there are 4 lamps per unit. The temperature is monitored for each module and the light intensity is measured for uniformity using a 142cm^2 silicon cell. The overall average intensity for each of the five positions is measured by a CdTe reference module (Ref. module calibrated at NREL OTF). Typical light intensity and temperature ranges are shown in Table 11.

Table 11. Light Soak Insolation and Temperature

Light Soak Intensity And Module Temperature		
Intensity	800W.m^{-2}	+/- 5%
Temperature	50C	+/- 5C

The electrical parameters for Apollo® modules at various stress conditions are shown in Figures 17 through 19 Typically, each light soak station has one position that is left on for extended stress testing. A result for extended light soak is shown in Figure 20

Figure 17. Light Soak: Jsc at Various Stress Conditions

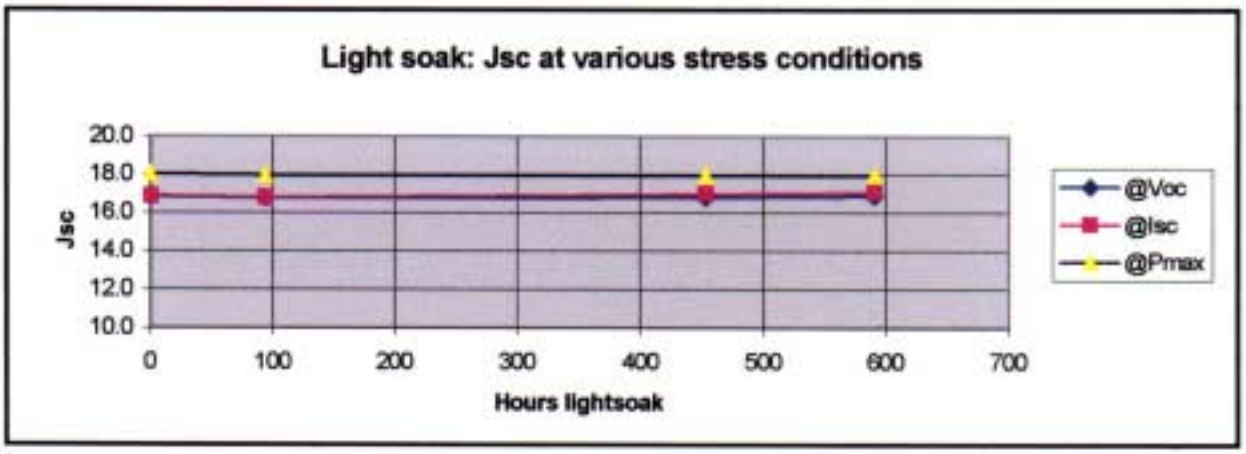


Figure 18. Light Soak: Voc at Various Stress Conditions

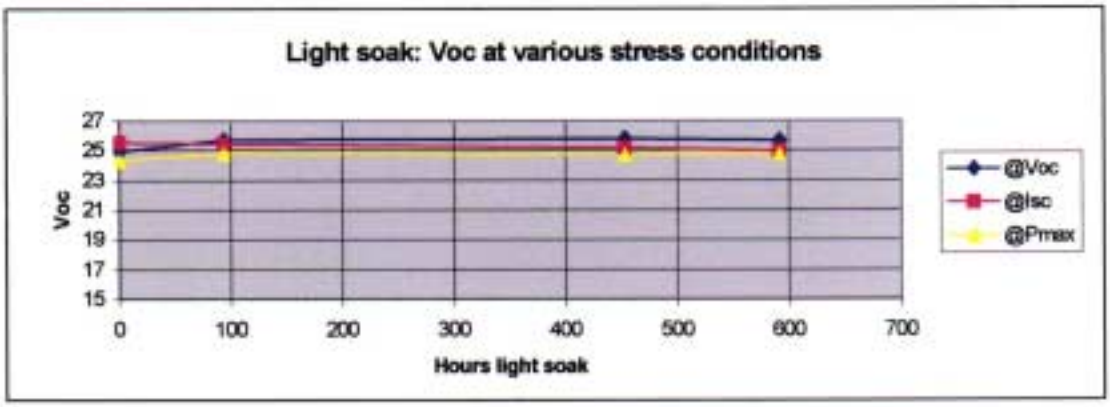
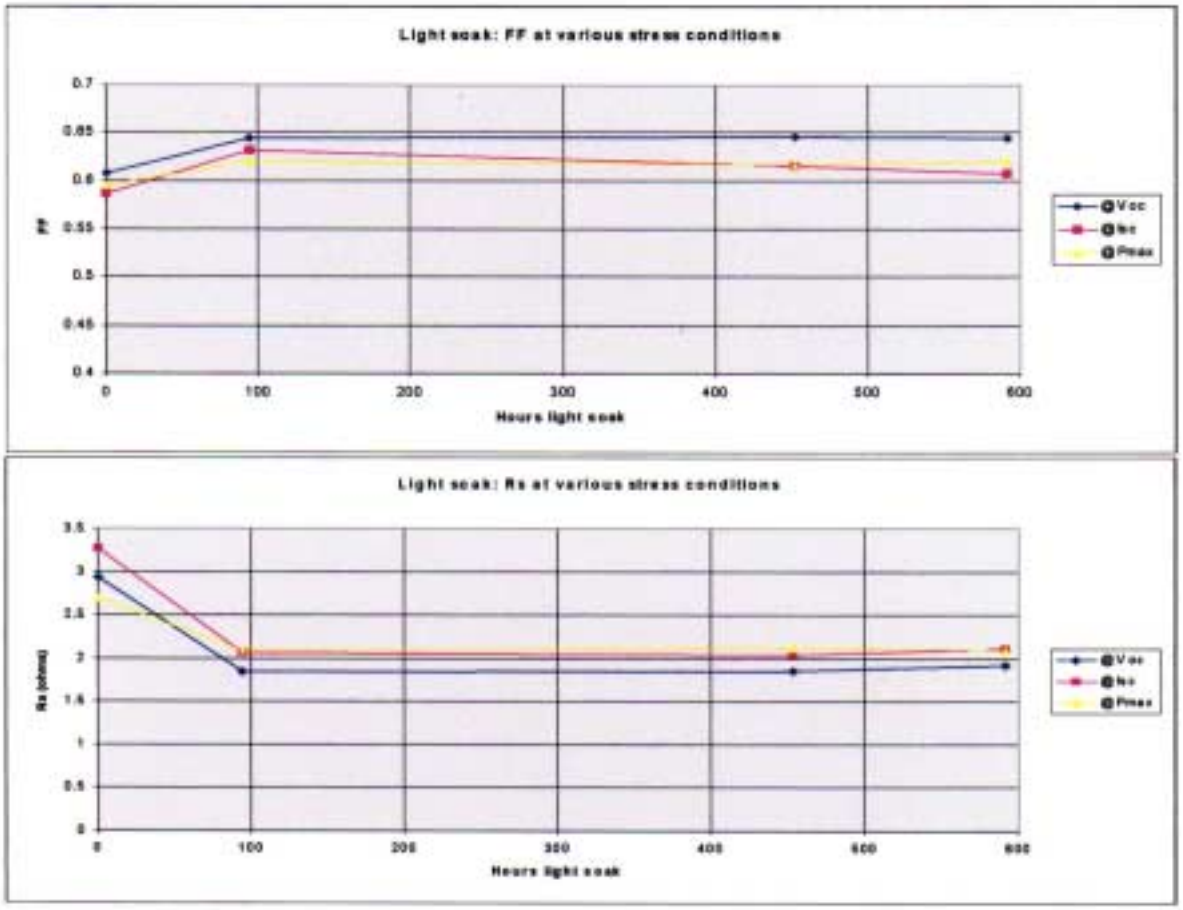


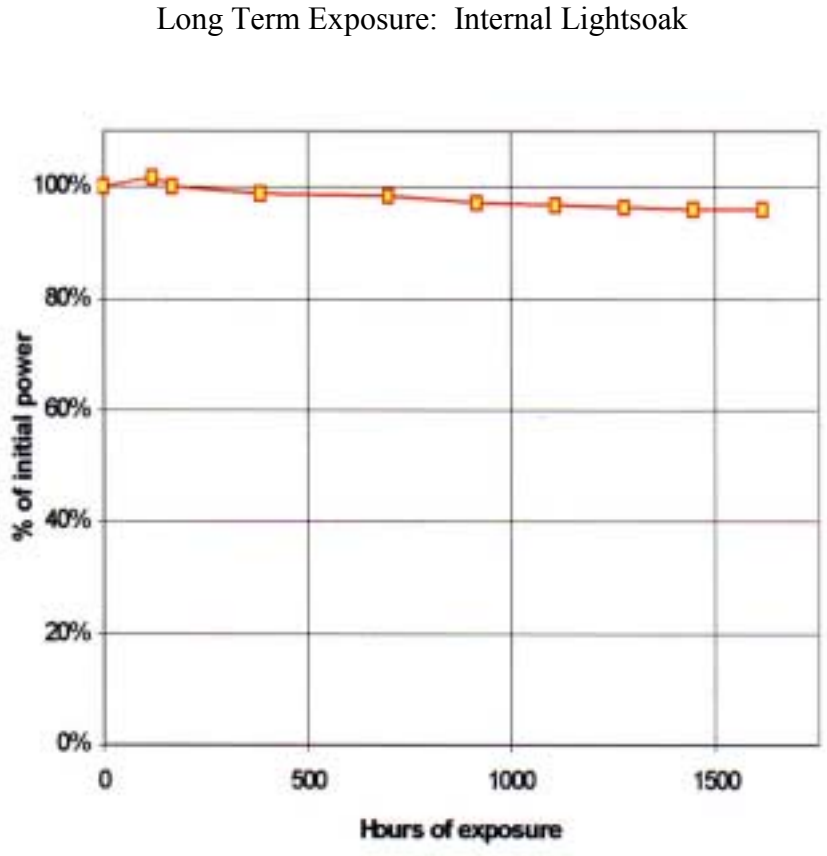
Figure 19. Light Soak: Effect on Fill Factor and Rs. at Various Load Conditions



Figures 17 through 19 shows very similar performance for modules under light soak at Voc, Isc and Pmax stress conditions. Module Isc and Voc show good stability at each condition. Fill factor also behaves in a similar fashion at each condition. However, in this case there is a decrease in the module series resistance in the first 100 hours that produced an increase in fill factor by about 5%. This effect is maintained throughout the light soak period. It is believed that this effect is evidence of the existence of traps within the absorber layer. These traps are passivated by carriers once the module is illuminated. More work will be carried out to characterize this phenomenon.

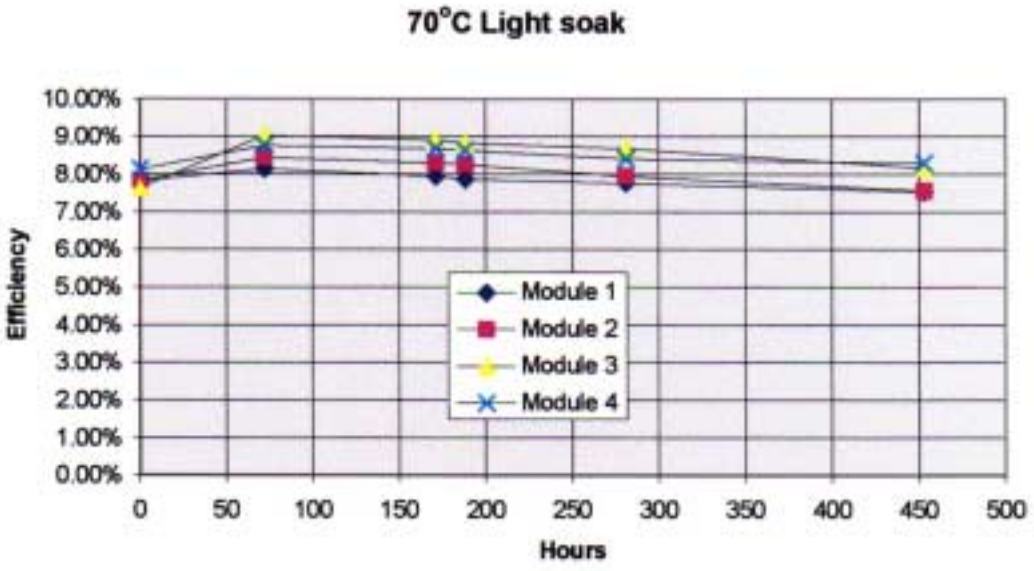
Long term exposure (>1500 hours continuous) as shows good stability with less than a 4% change over this period (Figure 20).

Figure 20. **Internal Light Soak: Long Term Exposure**



A new light soak station has been built so that higher intensities and temperatures can be applied during stress tests. It is capable of light soaking four modules simultaneously and will have the capability of exposing 0.94m^2 modules to temperatures of up to 100^{o}C for sustained periods at intensities of over 1 sun. Preliminary results of modules stressed at 70^{o}C (20^{o}C higher than standard temperatures) gave the following results.

Figure 21. Efficiency vs. Hours Lightsoak



The graph shows some stabilization of the modules in the 400 to 500 hour range after an initial increase. As at the lower temperatures (50°C), the increase occurs within the first 100 hours and is due to a reduced series and improved fill factor.

3.0 TASK 4: HEALTH, SAFETY, AND ENVIRONMENTAL (HSE) ACTIVITIES

3.1 Optimization of Waste Treatment Systems

Pretreatment of liquids generated from the production of cadmium telluride photovoltaic modules is not an option rather an economic and environmental necessity. Pretreatment of liquids generated on-site allow the facility to remove or reduce the cadmium concentration and adjust pH into ranges that can easily be handled by Publicly Owned Treatment Works, POTW, meeting all federal, state, and local waste discharge requirements and significantly lowering the disposal costs of liquid wastes.

Focus has been placed on two primary tasks:

1) Improving the reliability, optimization, of the existing cadmium pretreatment equipment, specifically the cadmium scavenger and cadmium electrowinning systems.
2) Research recycling options associated with the existing waste treatment equipment and systems, i.e. recycling of electrowinned cadmium and recovery of the effluent discharged from the cadmium scavenger/electrowinning system.

Studies on the ion exchange resin system used to extract Cd ions from wastewater have identified a tendency for Cd particulates to foul treated wastewater. The following describes various efforts put in place to remove the Cd particulates. By replacing the original filters with higher efficiency units the performance was improved as follows.
The cadmium scavenger system was originally equipped with 2 pairs of 25 micron bag filters which were later replaced with 1 micron bag filters; particle fouling continued. A particle distribution studies indicated the mean particle size to be composed of approximately 75% 0.75 micron material. A system of prefilters, a combination of 1 micron bag filters and 0.5 micron cartridge filters, were installed upstream of cadmium scavenger system. The combination of prefilters and changes in the primary filters increased the operational life of the lead ion exchange bed from 2-3, 500 gallon batches of cadmium sulfide, CdS, solutions to 30 - 50, 500 gallon batches of CdS solutions. Cadmium loading on the lead resin beds now exceeds the manufacturer's expectations, 31 lbs. estimated by Original Equipment Manufacturer, OEM, versus 50 lbs. actual.

The cadmium pretreatment system was designed to have both the scavenger (ion exchange) system and the electrowinner work in tandem. The electrowinner would remove cadmium from sulfuric acid solution used in the regeneration process of the scavenger system. The sulfuric acid could then be reused or neutralized and discharged through the scavenger system. Each time the excess sulfuric acid solutions were neutralized and discharged through the scavenger system, the scavenger system would experience problems similar to those noted in the previous paragraphs and another regeneration cycle was needed to restore the scavenger system to full operation. Suspended particulate cadmium from the electrowinner was apparently fouling the scavenger. A series of 2 - 1 micron bag filters were installed to filter both 1000 gallon batches of electrowinned sulfuric acid solutions prior to discharge through the scavenger system. This significantly improved the electrowinner operation and eliminated scavenger systems problems associated reprocessing the excess electrowinned sulfuric acid solution.

Experiments with stainless steel cathodes in the electrowinner instead of copper cathodes are in process to improve the quality of electrowinned cadmium thus making it more attractive for recycling, i.e. minimizing the copper contamination.

3.2 Cadmium Metal Recycling or Disposal

The existing BP Solar cadmium scavenger/electrowinning system produces a liquid stream meeting Federal, State, and Local discharge requirements. As a by product, the system also produces solid cadmium. Each scavenger regeneration/electrowinning cycle produces between 30 and 60 pounds of solid cadmium at full capacity. To date there has been insufficient quantities of the electrowinned cadmium to warrant disposal or recycling. Investigations into recycling or disposal of solid cadmium have begun utilizing previous NREL and International Cadmium Development Association, ICDA (a consortium of cadmium producers, reprocessors, and users) data.

Preliminary Analytical Characterization of Electrowinned Cadmium:

Cadmium (Cd)	60 - 95 %,	wt./wt.
Moisture, as Water (H_2O)	5 - 35 %,	wt./wt.
Copper (Cu)	1 %,	wt./wt.
Iron (Fe)	0.05 %,	wt./wt.
Lead (Pb)	No Analysis	
Zinc (Zn)	0.05 %,	wt./wt.

Experiments with stainless steel cathodes in the electrowinner, instead of the OEM specified, copper cathodes are in process to improve the quality and handling characteristics of the electrowinned cadmium. Electrowinned cadmium, according to the OEM, does not adhere to the stainless steel cathode material, making removal of the cadmium easier, extending the useful of the cathode, and reducing the copper contamination. Moreover, using stainless cathodes will eliminate copper and make the Cd metal amenable for conversion in CdTe precursor salts.

Traditional cadmium reclaimer/recyclers such as NiCd battery reprocessors, which reprocess material either back as NiCd feed stock or into steel smelting, appear uninterested in electrowinned cadmium. Alternate outlets such as raw materials suppliers (process chemicals) and primary metal processors, lead and zinc smelters, have been researched and investigated. Chemical (process chemical) raw materials suppliers appear to require a high purity cadmium source, 99% Cadmium or better, for production of process chemical such as cadmium oxide, cadmium sulfate, etc. Primary metal producers, such as lead and zinc smelters, are capable of handling and refining electrowinned cadmium, as characterized above, since cadmium is a by-product and/or process waste from the mining and smelting operation.

Using the March 11-12, 1992 Brookhaven National Laboratory, Department of Applied Sciences Workshop Report "Recycling of Cadmium and Selenium from Photovoltaic Modules and Manufacturing Wastes" as a reference, discussions have been held with Dr. V. M. Fthenakis, of Brookhaven National Laboratories regarding recycling options for solid cadmium. Dr. Fthenakis provided additional references for previous NREL projects, and contacts within International Cadmium Development Association (ICDA).

3.3 Liquid Processes --- Closed Loop / Zero Discharge Studies

BP Solarex, Fairfield, CA utilizes a unique cadmium telluride deposition in the production of its PV modules. Substantial quantities of liquids are used and treated on-site. Investigations into various aspects of "Closed Loop and/or Zero Discharge processes have begun. The following describes some of the issues.

Waste Streams originating from BP Solar's Panel manufacturing operations are composed predominantly of three (3) components:

1) Dissolved cadmium from the semiconductor deposition operation.
2) Rinse waters containing trace levels of dissolved cadmium.
3) Soluble organics from down stream process.

The existing BP Solar waste treatment system is capable of treating (reducing) dissolved cadmium from approximately 200 mg/l to <0.030mg/l. The existing system is sensitive to particulate fouling from suspended sub-micron cadmium and fouling from organics. To eliminate fouling of the existing waste treatment system, a system of pre-filters, capable of macro and sub-micron filtration, was installed upstream. After a review of applicable treatment processes, two vendors were selected for further technology evaluation.

The first vendor, U.S. Filters, offers a wide range of treatment systems, from simple filtration to multi-step combination systems that are readily integrated with existing equipment. The second, HydroTech Environmental System, HTES, offers a novel technology solution that has the potential to simplify and reduce the number of needed treatment systems.

Both vendors were sent representative samples from the BP Solar deposition operations, rinse waters operations, and back contact application process. Characteristics of the samples have been established through previous analysis. The goals of the treatability studies were:

1) Review the recyclability of water from the existing RO/DI System
2) Produce liquids dischargeable under the terms of the local sewer agreement and conditions.
3) Further the treatment capabilities of the existing system.
4) Substantially reduced in volume to facilitate economical off-site treatment and disposal.
5) Economically treat or dispose of waste waters.

US Filter, a company with a proven history of design, manufacture, and operation of waste treatment systems, returned proposals for two process systems:

1) A cleanable membrane filtration system to reduce the quantity of particulate cadmium sulfide discharged to the scavenger system.
2) A chemical precipitation/cleanable membrane filtration system for removal of organic residue and gross cadmium contamination.

US Filters was further requested to provide additional information relevant to the proposed systems, i.e. projected annual operation expenses for each proposed system, maintenance schedules, equipment footprint, cost proposal for an on-site pilot system, and analytical data for tests performed. The proposed systems appear relatively inexpensive and utilize proven technologies.

HydroTech Environmental Systems, HTES, a manufacturer's representative for companies producing novel waste treatment technologies, returned a single proposal for a high shear vibrating membrane system, which could accommodate a combined waste stream laden with both organic and particulate residues. Laboratory results, from test solution, indicated excellent removal or reductions of organic and particulate residues. HTES maintains the proposed system could function as a stand-alone unit. HTES was asked to propose a system, which would work in conjunction with existing waste treatments and produce a higher concentration ratio. Additional tests were performed, indicating that the original system could be reduced in size and the membrane pore size increased, yielding a financially more attractive system.

Treated wastewater samples from each of the prospective vendors were returned to BP Solar and then sent to a certified waste water laboratory for further analysis. Requested test parameters were total cadmium concentration (as Cd), chemical oxygen demand (COD), Total Suspended Solids (TSS), Total Organic Carbon (TOC), Conductivity, EPA Method 625 (Semivolatile Organic Compounds), and EPA Method 624 (Volatile Organic Compounds).

Both systems mentioned above are capable of working in conjunction with the existing treatment system, substantially increase on-site treatment capabilities, and reduce the quantity of waste sent for off-site treatment or disposal. A review of technologies used, analytical results, and economic feasibility is currently in progress and will determine which vendor's technology to test in pilot scale. Once a best technology is determined, a pilot line system will be set up in the Fairfield plant.

Summary.

The results presented in this Phase 2 report have shown considerable progress in advancing the Apollo® technologies fundamental understanding. This understanding has lead to a significant increase in device performance. Module performances in both the $0.55m^2$ and $0.94m^2$ sizes have been confirmed during Phase 2 at 10.8% and 10.6% respectively. In the latter case, the power of the monolithic module was 91.5W. At the time of this report, this is a record power for any monolithic thin film module.
During Phase 3, work will continue to increase the understanding and knowledge base for the large area modules. In particular, mechanisms to increase device performance will continue to be investigated.

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• 13. ABSTRACT *(Maximum 200 words)*. In this report, the results are presented and discussed from the following areas: *CdS and CdTe optimization*. In this section, semiconductor properties, optical properties and device optimization are discussed. Crystallographic characteristics were determined under collaborative work with the Institute of Energy Conversion, (University of Delaware) and NREL. In addition to this, module performance results are presented to illustrate the efficiency improvements gained as a result of this research. R*eliability and testing.* In this section, both indoor stress testing and outdoor long term test systems are described. Detailed design, set up and initial results are presented. *Health, Safety and Environment.* Three main sections described in this section are on handling of waste treatment systems at the Fairfield plant, reclaimed cadmium metal recycling and closed loop/zero discharge studies.

14. SUBJECT TERMS
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