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Subcontractor Report

Technology Support for High-Throughput Processing of Thin-Film CdTe PV Modules

Annual Technical Report, Phase II
1 April 1999—31 March 2000

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First Solar, L.L.C.
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National Renewable Energy Laboratory

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Table of Contents

Abstract

Results and conclusions from Phase II of a three year subcontract are presented. The subcontract, entitled "Technology Support for High-Throughput Processing of Thin-Film CdTe PV Modules," is First Solar's portion of the Thin-Film Photovoltaic Partnership Program. The research effort of this subcontract is divided into four areas of effort: 1) process and equipment development, 2) efficiency improvement, 3) characterization and analysis, and 4) environmental, health, and safety.

As part of the process and equipment development effort, a new semiconductor deposition system with a throughput of 3 m^2/min was completed, and a production line in a new 75,000 ft^2 facility was started and is near completion. With the near-term plan of 8%-efficient modules, this system and production line will have a capacity of 80 MW_p/year for CdS/CdTe plates and 20 MW_p/year for finished modules. As part of pilot-production and process improvement during Phase II, over 12,500 plates (each 0.72 m^2) were coated with CdS/CdTe films; this is 4 times the total number produced prior to the start of this contract.

Process development efforts were aided by the development of large-area characterization techniques. Advances in large-area techniques this reporting period include improvement of spatial mapping of CdS, progress towards spatial mapping of CdTe, and addition of in-situ measurement of CdS film thickness and substrate temperature. Using spatial mapping of a representative film from the new deposition system it was determined that the standard deviation of the CdS film thickness was 1.3% in the down-web direction and 7% in the cross-web direction. Using a 13-point per plate measurement of a sampling of plates from the new deposition system it was determined that the average CdTe film thickness was 3.78±0.46 μm and that the average standard deviation within plates was 0.44±0.16 μm. These values are better than expected for this phase in the start-up of a new system, but additional improvement in the cross-web direction for both CdS and CdTe will be pursued in order to improve module performance.

Progress was also made in large-area vapor-$CdCl_2$ treatment and in laser scribing. Heat-treatment profiles were verified for the module-scale vapor-$CdCl_2$ system and vapor-delivery issues were identified. A new laser-scribing technique that provides linear scribing speeds up to 3 m/s was developed which allows all of the scribing for a scribe set to be done for a module in less than 1 minute with one laser, thus improving system uptime and decreasing costs relative to the previous multi-laser approach.

As part of the efficiency-improvement task, research was done on cells and modules with thin CdS and buffer layers as way to increase photocurrent with no loss in the other photovoltaic characteristics. New chemistries for atmospheric-pressure chemical vapor deposition (APCVD) of buffer layers were developed, APVCD systems were built for 100 cm^2 and 7200 cm^2 substrates, and process parameters were explored. Cells with APCVD buffer layers and thin CdS on standard commercially-available

TCO-coated soda-lime glass substrates were produced with NREL-verified efficiencies as high as 13.2%. Modules with APCVD buffer layers and thin-CdS from the new production deposition system were produced (after the end of this reporting period, but as part of a deliverable for this reporting period) with aperture efficiency up to 9.6% (unconfirmed).

Other efforts as part of the efficiency-improvement task included exploration of the effect of ambient during vapor-$CdCl_2$ treatment, characterization of module-scale non-uniformity, module problem diagnosis, and improvement and use of a large-area sputter system and a small-area VTD system.

A number of activities were part of the characterization and analysis task, including:

- A new admittance spectroscopy system, with a range of 0.001 Hz to 100 kHz, was developed and used to characterize cells.
- A new spectral-response system was developed and used.
- Planar electron-beam induced current (EBIC) was used to characterize intra-grain vs. grain-boundary regions of cells and cell non-uniformity.
- Energy-dispersive spectroscopy (EDS) capabilities were upgraded.
- Low-temperature photoluminescence (PL) was used to investigate the electronic states of impurities in CdTe films and cells.
- The effect of back contacts on cell open-circuit voltage was investigated, and micro-non-uniformity (grain-boundaries or point defects) was proposed as the cause of large suppression of open-circuit voltage in some cells.
- Given the potential importance of micro- and macro-non-uniformity, the effect of non-uniformity was modeled, and an analytical solution based on the mean-field approximation was developed.
- An analytical solution to shunt-screening in cells was developed and verified.
- Scribe contact resistance was characterized.
- Performance of modules under non-standard conditions was investigated.
- Advances were made in accelerated-testing capabilities, included the construction of a new environmentally-controlled light soak station, the development of a new high-acceleration-factor laser-light soak test, and the development of planar EBIC as a very-high acceleration-factor screening test.
- Field stability to a period of greater than 5 years was verified with further analysis of the array at NREL.
- Light soak and other accelerated tests were used to investigate the stability of alternative processes at First Solar and for National CdTe Team members' contacts on First Solar substrates.
- Failure mechanism research continued with some information presented on temperature and contact effects.

As part of the environmental, health, and safety task, the methanol-based $CdCl_2$ process was replaced with aqueous-$CdCl_2$. This change enabled the retention of a "De Minimus" level of emissions for the manufacturing plant, so no permitting is required.

Acknowledgements

Principal Investigators: Doug Rose, Rick Powell
Program Manager: Gary Dorer

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Introduction

This report is the second annual report for a subcontract originally awarded to Solar Cells, Inc. (SCI) in 1998. In February 1999, SCI and True North Partners, LLC of Phoenix, Arizona jointly formed First Solar, LLC. First Solar assumed all activities of SCI, including the research described in this report.

First Solar has been the leading developer of high-speed, thin-film deposition techniques for CdTe photovoltaic modules. Using a proprietary vapor-transport deposition technique the semiconductor films for a 0.72 m^2 module can be deposited in less than 15 seconds. First Solar has also developed reasonably high-throughput processes for the remainder of the steps required to make finished modules and has been producing modules in various levels of pilot production for 6 years. Modules with power output up to 60.5 W under standard measurement conditions have been produced (area of 0.72 m^2) and field stability has been demonstrated.

The basic process First Solar currently uses is as follows: 60 cm x 120 cm SnO_2:F-coated soda-lime glass plates are first edge seamed to eliminate sharp edges and prevent breakage during processing. After washing, ~0.3 μm CdS and then ~3.5 μm CdTe are deposited on the plate at ~1 μm/s using vapor-transport deposition (VTD). After a $CdCl_2$ anneal and CdTe surface modification, contact metals are sputter-deposited then annealed. Laser scribing is used to turn the filmed plate into a monolithically integrated submodule. A module is then made by placing a film of ethylene vinyl acetate (EVA) on the back side of the submodule and then encapsulating with a back sheet of glass. At this time, small cells (1.1 cm^2) from production plates have efficiencies of ~10%, which result in 0.72 m^2 modules with total-area efficiencies of approximately 7%.

The goal of the Thin-Film Photovoltaic Partnership program is to advance the state-of-the-art of large-scale thin-film module fabrication. The subcontract awarded to First Solar as part of the program leverages First Solar's extensive knowledge and equipment base to achieve that goal. The subcontract is divided into four areas of effort: i) process and equipment development, ii) efficiency improvement, iii) characterization and analysis, and iv) environmental, health, and safety. During Phase II, First Solar made progress in all four areas.

This report is organized in the same manner as the task description of the subcontract, with the exceptions that Task 3.5 of the statement of work (Research VTD chamber design) is reported in section 2.3.2 of this report, and Task 3.6 (buffer-layer research) is reported in section 2.1.1.

1. Equipment, Process, and Fabrication Development

1.1 High-throughput Deposition System Development ("100 MW coater")

A high-throughput semiconductor deposition system was completed during Phase II, with the coating technology for the system developed under the Thin-Film Photovoltaic Partnership program. The system has a 1.2 m (4 ft) web width and a line speed of approximately 2.5 m/min. The high line speed is made possible by the high growth rate achieved with Vapor Transport Deposition (VTD) -- the ~3.5 μm-thick CdTe film is grown at ~1 μm/sec. High-speed-index load locks enable continuous glass flow into the deposition region, thus achieving the target throughput of four 0.72 m^2 plates/min. If run at this throughput for three 40-hr shifts/week, the system would produce 1.5 million CdS/CdTe-coated plates per year. If these plates were finished into 10%-efficient modules with a 93% combined uptime and yield, the PV production would be 100 MW_p/year. The system, which is normally referred to as the production coater in this report, is shown in Figure 1.1 (with the load/glass-seaming robots, conveyor, and glass washer in the foreground).

Figure 1.1. High-speed CdS/CdTe deposition system with 3 m^2/min throughput.

The system consists of an entrance load-lock, a glass heating section, a deposition section, an exit load-lock, and a cooling section. The cylindrical geometry of the glass heating and deposition sections is suitable both to support the atmospheric pressure load and to form an excellent radiation cavity to achieve uniform glass temperature. Multiple heating zones allow adjustment of cross-web glass temperature. Glass sheets

are supported and moved throughout the system using ceramic rolls that are tangentially driven by a flat chain.

Multiple, redundant coating subsystems are located within the deposition section of the furnace. Injected source material is vaporized, the vapors distributed, and the inert carrier gas exhausted in each coating subsystem. One distributor is used to form the CdS layer and one to form the CdTe layer.

Critical to production operation is raw material utilization and equipment up-time. To a large degree, these are coupled in the system, since whatever material is not deposited condenses on cooler components and filters and eventually requires cleaning. Fortunately the components that directly control the coating itself, the vaporizer and distributor, generally remain clean, as they are the hottest components. Uniformity and utilization issues are discussed in section 1.5 of this report. In-line diagnostics in the system are discussed in section 1.4.2.

The first CdS/CdTe coatings were made with the system in February. The first CdS/CdTe-coated plate from the system yielded cells of up to 11% efficiency after light soaking. Additional results from use of the system will be discussed in sections 1.3, 1.5, and 2.4.3.

1.2 Manufacturing Facility and Production Line Development

A 75,000 ft^2 manufacturing facility and module production line were developed during this reporting period, primarily with internal and PVMaT funding. However, R&D support of the development was funded under this contract, and the production line will be instrumental in the fulfillment of this contract's Phase III objectives. Ground was broken for the manufacturing facility in July 1999 in Perrysburg Township, OH. Equipment placement began in December, with all deposition equipment and approximately half of the module finishing equipment installed by March 2000. The equipment has been designed and constructed to handle the post-CdTe-deposition processes at one plate per minute. The plan is to establish production at this level (20 MW/yr for 8%-efficient modules) with the ability to quickly add finishing capacity in increments on site or at other locations.

1.3 Pilot-production Experience and Deposition-equipment Improvement

In parallel with the development of the production coater and production line as described above, efforts continued on the improvement and use of the pilot-production deposition system and pilot-production line. This work included ongoing problem diagnosis and machine upgrades. For example, in January, coating problems were traced to feed-line vacuum leaks -- repair of the leaks resolved the problems. Ramp-up of pilot-production volumes continued as a way to learn about the process and make product for evaluation purposes. In the 42 months prior to Phase I of this contract, the average CdS/CdTe production was only ~80 plates/month. During Phase I the average was ~550 plates/month, and during Phase II the average was ~1050 plates/month. Production by

month during Phase II is shown in Figure 1.2. Note the transition to the production coater in March 2000.

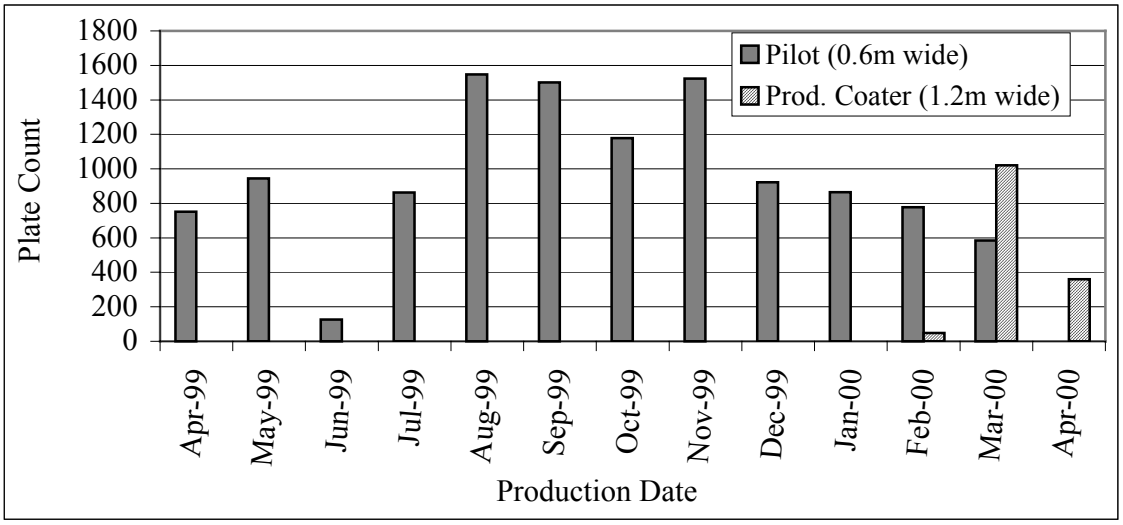


Figure 1.2. CdS/CdTe plate production per month during Phase II.

1.4 Diagnostics

New automated measurement systems and techniques were developed to provide in-line information and spatial mapping of film characteristics. Each area will be briefly described in the following sections. Examples of resulting data will be presented in the subsequent sections describing process development. Small-area characterization development is described in section 3.

1.4.1 Off-line Measurements

Construction began on two new spatial mapping characterization systems. Like the previously-built system described in the Phase I report[1], these systems will be able to characterize full size (0.6 m x 1.2 m) plates. The systems use the same basic approach as the system developed last year; namely, fixed-position excitation/detector pairs with X-Y movement of the plate enabling high-density mapping of several important quantities.

Among the improvements to the two systems are: i) improvements in the CdS thickness measurement, and ii) addition of CdTe thickness measurement capability. The CdS thickness will be measured by the optical absorption of a gallium nitride quantum-well LED with improved detection electronics so that calibration before each scan is not required. CdTe thickness mapping capability was added by the addition of a 808 nm 5 mW laser with thermo-electric cooling of the diode to prevent mode hopping and a DSP lock-in to improve signal acquisition. Mock-ups of the CdS and CdTe measurement systems show excellent results.

1.4.2 On-line Measurements

The Production coater has over 80 channels of temperature, pressure, position and speed control, continuous residual gas analysis, a scanning infrared imaging system, and an internal laser absorption system to measure CdS thickness.

Infrared radiation emitted from the SnO_2-coated glass surface is detected by an imaging system located between the heating chamber and the deposition chamber. The emitted radiation passes through a ZnSe vacuum window. A spinning mirror sequentially reflects radiation from across the web towards a single detector. The imaging system creates a 2-dimensional map of the glass surface temperature. After correcting for some spurious internal reflections, glass temperature uniformity has been measured to be ±10ºC on the 60 cm x 120 cm substrates.

Since the CdS layer is soon buried by the lower bandgap CdTe, CdS thickness detection is best done *in-situ* at deposition temperature. Therefore, an array of fixed-position green lasers and paired detectors have been installed in the deposition system to infer CdS thickness based on optical absorption. Fortuitously, the decrease in CdS bandgap with temperature is sufficient to allow the use of small, readily available, stable solid-state 532 nm lasers.

1.5 Deposition Development

Efforts to improve deposition characteristics (e.g., film uniformity, plate-to-plate consistency, and material utilization) proceeded on the 60-cm-web pilot-production system for most of Phase II and then were continued on the 120-cm-web production coater.

1.5.1 Uniformity

Uniformity of performance over the area of the 60 cm x 120 cm module is critical for high performance modules. Uniformity of film thickness is an important indication of uniformity of performance because film thickness can directly affect performance (e.g., thinner CdS can result in increased J_{sc} but lower V_{oc} and changes in CdTe thickness could result in differences in performance after the $CdCl_2$ anneal) and because film thickness can be an indication of other area-dependent variables which could affect performance (e.g., deposition temperature and species-flux during growth).

One of the methods of investigating film uniformity is to take thickness profiles or maps on a sampling of plates. This method is particularly useful for determining the effect of process changes on uniformity. Figure 1.3 shows the thickness of the CdS for a variety of thickness films made on the 60-cm-web pilot-production system and the 120-cm-web production coater. Each curve is a function of cross-web position and is an average of 3 measurements in the down-web direction.

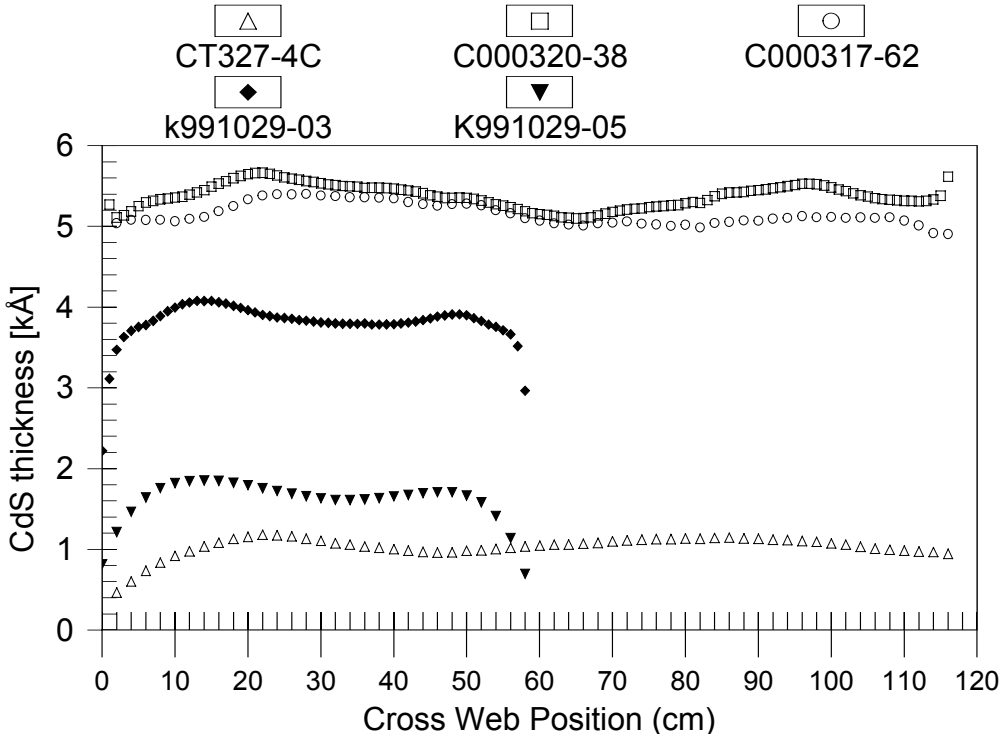


Figure 1.3. Comparison of average cross-web thickness profiles for CdS films made in the production system (open symbols) and the pilot equipment (solid symbols).

Instead of averaging the three down-web position measurements as was done for the previous figure, plotting the three curves separately shows the high down-web uniformity of the process, as can be seen in Figure 1.4. For the plate shown, the standard deviation was 0.004 and 0.023 μm in the down-web and cross-web directions, respectively (1.3% down-web and 7% cross-web).

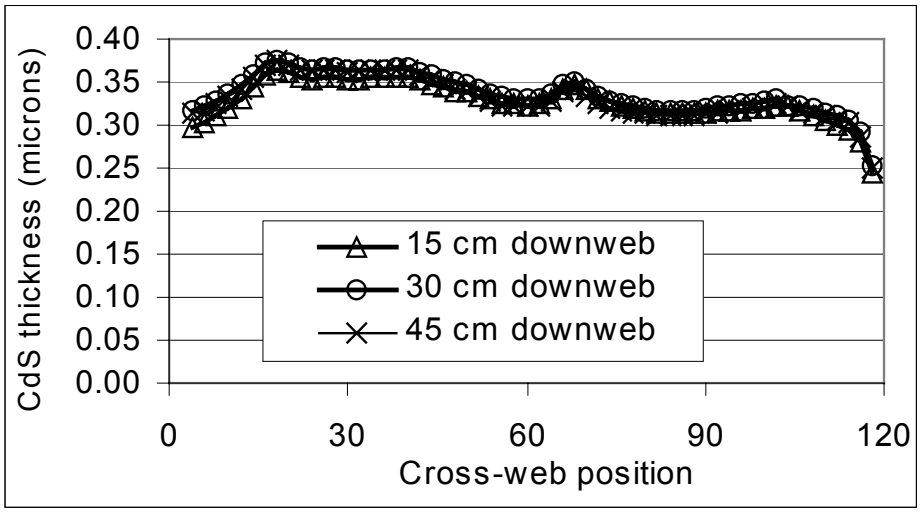


Figure 1.4. CdS thickness as a function of cross-web position for three different down-web positions for a film made with the production coater.

Another method of investigating CdS film uniformity is to take in situ measurements. Figure 1.5 shows the down-web thickness of CdS as deduced by the optical technique described in section 1.4.2.

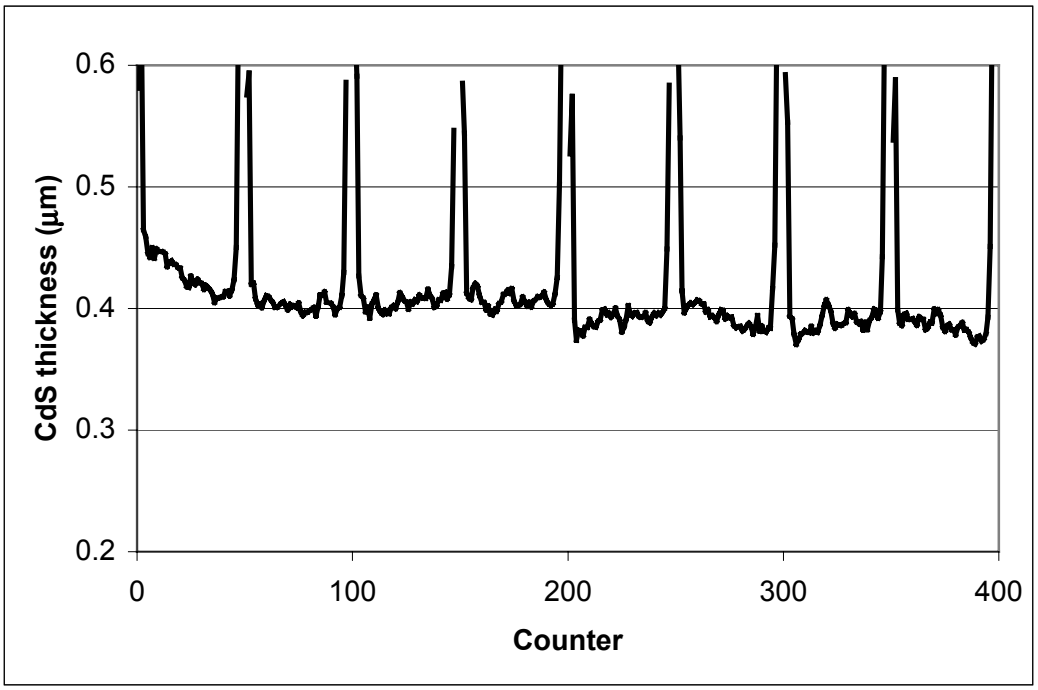
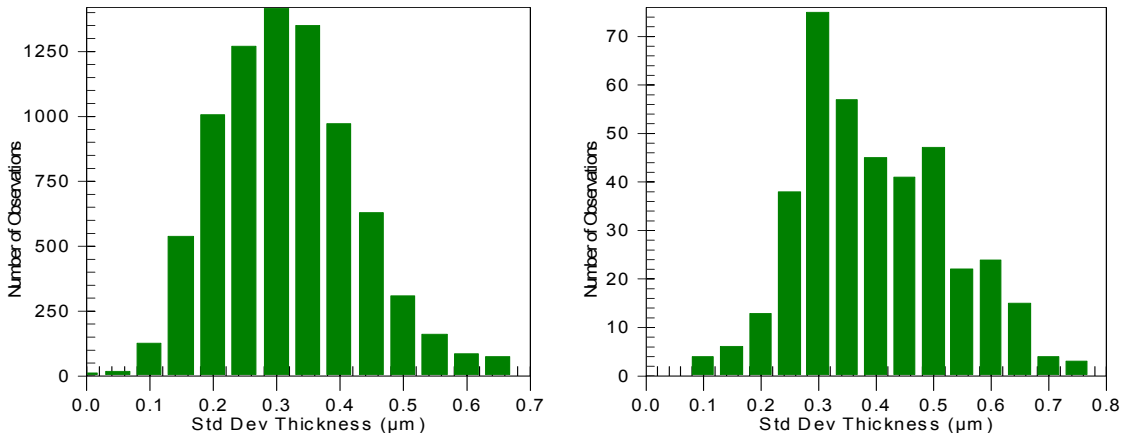


Figure 1.5. CdS film thickness as determined by in-situ optical absorption sensors. Sharp up-turns are detection of coating on backside of glass at leading and trailing edges of plates.

Still another method of investigating film uniformity is to take a number of point measurements within plates which can be used to determine the standard deviation of film thickness within each plate for a large number of plates. This method is used to present the uniformity of thickness of the CdTe layer. Figure 1.6a is a histogram of the standard deviations of the CdTe thickness from 13-point per plate measurements for plates from the 60-cm-web pilot production system. The average of the standard deviations is 0.358 µm, which is ~10% of the average thickness. Figure 1.6b is a histogram of the standard deviations of the CdTe thickness for plates from the 120-cm-web production coater. The average of the standard deviations is 0.44 µm, which is higher than that for the pilot production system. Two factors contributed to this increased standard deviation: first, the data was taken during the start-up phase of the production coater, and second, the data for the production coater is weighted toward non-standard plates (for the pilot system all plates were measured, while for the production coater only a sampling, on average 1 per 80, plates is measured with all "dial-in" and problem-investigation plates being measured).



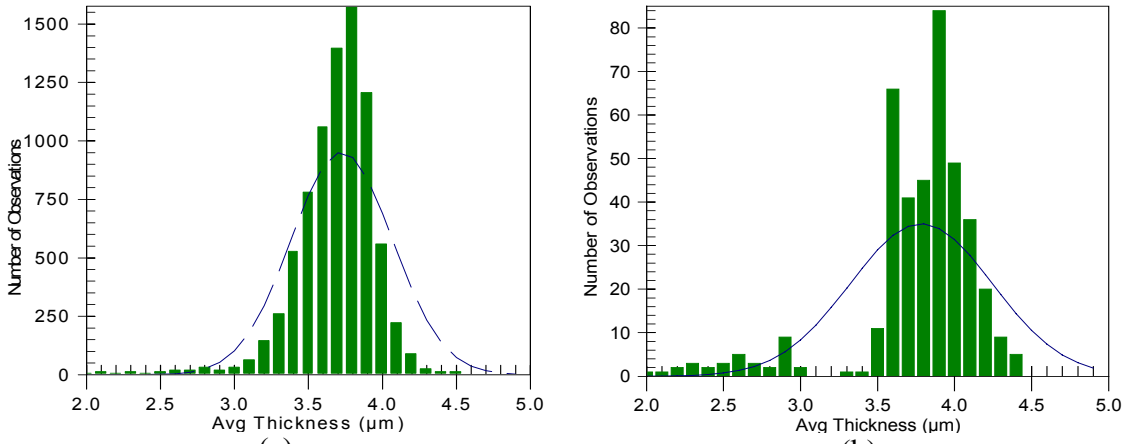
(a) (b)

Figure 1.6. Histogram of standard deviation of CdTe thickness within plates. (a) Plates from pilot-production system deposition (0.358±0.170 µm); (b) Plates from production coater (0.44±0.16 µm).

Metrics of film uniformity other than film thickness, for example film morphology, were also investigated. A series of experiments in the pilot-production system showed that one type of CdS edge banding was feed-related. As a result of these experiments, modifications were made to the distributors to improve deposition uniformity.

1.5.2 Consistency

Plate-to-plate consistency of film thickness is another metric of deposition quality. The CdTe thickness of all plates produced on the 60-cm-web pilot-production system was measured with the beta-backscatter technique with a grid of 13 points per plate. A histogram of plates produced during Phase II is shown in Figure 1.7a.



(a) (b)

Figure 1.7. Histogram of average CdTe thickness per plate with measurement by beta-backscatter technique with a grid of 13 points per plate. (a) Data taken from plates made on the pilot equipment (3.73±0.34 µm); (b) Data from sampling (~1 per 80) of plates from the production coater (3.78µm ±0.46).

In February 2000 the first CdTe films were deposited with the new production coater. Plates were measured only on a sampling basis, on average about 1 every 80, with a higher sampling done during the "dial-in" phase after a process-parameter change. A histogram was made for all of the plate measurements for the production coater and thus includes the "dial-in" plates and experiments designed to produce thinner CdTe. Despite the inclusion of all the data including the non-standard plates, this histogram, shown as Figure 1.7b, still shows encouraging results with a plate-to-plate standard deviation of 12%. In Phase III a systematic study is planned to determine the plate-to-plate consistency.

1.5.3 Utilization

Increasing semiconductor utilization is a way to reduce direct material costs and system-cleaning costs. The latest calculations for continuous-stream CdS utilization indicate 34% for the pilot-production system and 50% for the production coater. Calculations for CdTe utilization indicate 72% for the pilot-production system and 67% for the production coater. The values for the production coater are actual output divided by input, while for the pilot-production system estimates were made for a continuous flow using the intermittent-flow data -- this may account for the slight drop in CdTe utilization on the production coater relative to the pilot system. The cause for the increase in CdS utilization is not known at this time.

The CdTe utilization, at 67%, is encouraging relative to some other deposition technologies, but is short of our goal of 90%. Loss mechanisms, such as "web-edge overspray" and re-sublimation have been identified, but efforts to reduce these losses have been subordinated during the start-up phase of the production coater. Additional work on utilization is planned after the system parameter space has been more fully explored.

1.5.4 Pinholes

The Phase I report included a description of CdTe pinholes that were prevalent along the outer edges of plates. In Phase II we confirmed that these CdTe pinholes were the result of large CdS particulates (at later stages of processing the CdS particulates would get knocked off, leaving behind the CdTe pinholes). Tests also indicated that the CdS particulates were the result of homogenous nucleation. The flow dynamics of the production coater are such that CdS particulate, and thus CdTe pinhole, formation is no longer a problem.

1.6 Large-area Vapor-$CdCl_2$ System

A pilot-production vapor-$CdCl_2$ system with a 60-cm-web and a throughput of one module every 3 minutes was constructed in Phase I. During Phase II, the mechanical and heating aspects of the system were verified by successfully using the system to heat-treat plates that had received a spray with wet-$CdCl_2$. The trial was so successful that the system was commandeered for pilot-production in this spray/anneal mode. Later attempts to run the system as intended with $CdCl_2$ vapor generators or open boats resulted in inadequate treatment of plates. Subsequent modifications to provide a more confined space for the vapor gave indications of better treatment, but possible machine life/uptime

problems. By this time, the urgency for a vapor-$CdCl_2$ system was removed by the success of the aqueous $CdCl_2$-treatement approach (see section 4.2) since the vapor-$CdCl_2$ system was no longer needed to achieve the goal of a no-emissions plant. However, since vapor-$CdCl_2$ results in a more uniform treatment and a more pristine CdTe surface, it is expected to be capable of providing a higher performance product and be more suited to production and will thus continue to be investigated with the intention of being available for future manufacturing capacity additions. The system has been moved to the First Solar Technology Center for this work in Phase III.

1.7 Interconnect Process Development

To make a monolithically-connected module, laser scribing is used to turn the filmed plate into 116 series-connected cells. As shown in Figure 1.8, scribe-1 isolates the front contact of the cells, scribe-2 enables the series connection to the next cell, and scribe-3 isolates the back contact of the cells. In pilot-production, laser scribing of modules was done with two multi-beam laser systems at ~5 min/module. New concepts were thus needed to reach the goal of 1 plate/min throughput with low capital costs.

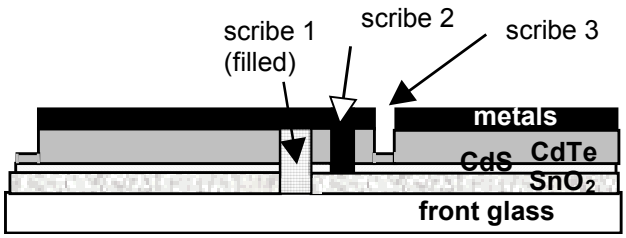


Figure 1.8. Monolithic integration with laser scribing.

In Phase I, one concept explored was the use of a large number of fixed lasers. In Phase II, a new concept was explored and developed that will allow all of the scribing of a scribe set to be done with one system with one laser in less than a minute. The use of just one laser has the advantages of lower initial cost and higher system up-time compared to the previous concepts.

Technology support of this new concept was done under this contract, with machine development by PVMaT and internal funds. The approach provides an increase in scribing accuracy, linear scribing speeds up to 3 m/s (an order of magnitude increase), and at least a 50% reduction of capital costs.

2. Efficiency Improvement

Improvement of module conversion efficiency has tremendous leverage in decreasing total system "per Watt" costs. As a result, several projects were pursued with the intent of improving module efficiencies. In addition to the work described below, considerable work described elsewhere in this report was part of the effort to improve efficiencies (for example the diagnostics of section 1.4, the deposition development of section 1.5, and the characterization of section 3.1).

2.1 Buffer Layer and Thin CdS

The short-circuit current for an ideal solar cell with a direct bandgap of 1.45 eV is ~30.6 mA/cm^2. The typical J_{sc} of our current-production cell of only ~18 mA/cm^2 thus stands out as an opportunity for significant improvement in cell efficiency. The low J_{sc} is the result of absorption of photons with energy greater than 2.4 eV in the ~3000Å-thick CdS layer, with no collection of these photogenerated carriers. Thinning of the VTD CdS layer results in increased J_{sc}, but low V_{oc}. The incorporation of a thin high-resistivity layer, commonly called a buffer layer, between the conductive front contact (SnO_2:F) and the CdS has been shown to allow thinning of CdS without loss of V_{oc} [2] [3]. Efforts to develop a high-throughput process for a buffer layer are discussed in the next section with device results using the layer and thin CdS in section 2.1.2.

2.1.1 Buffer-layer Development

In Phase II the majority of our efforts in buffer-layer development were focused on exploring atmospheric-pressure chemical vapor deposition (APCVD). While we have had some success with a sputtered buffer layer in devices with thin CdS, the very low cost of APCVD makes it more attractive for high-volume production if the necessary properties of the layer can be obtained.

A description of the equipment built for this APCVD work is given in sections 2.5.3 and 2.5.4. A description of the criterion for screening for new APCVD chemical systems was given in a paper submitted to the Spring MRS Conference in San Francisco, CA (D. Giolando, *et al.*). Briefly, the ideal chemical system for high-volume production would have the following characteristics:

- Volatility - should be at least 10 mm Hg vapor pressure to achieve growth rates of 100 to 2000 Å/s.
- Reactivity - should give fast growth rate at the substrate with no pre-reactions
- Cost - low cost and ease of preparation lowers product cost and ensures adequate supply of the chemicals.
- Toxicity - systems with low toxicity and lack of other characteristics that would require safety efforts are preferred and should be investigated first.
- Waste treatment - Ease of treatment important; preferable if the waste product can be converted back into the reagent.
- Patentable - Ownership of the chemical systems ensures access.

From a screening process using the above criteria, new chemistries were identified and tested on 100 cm^2 and then 7200 cm^2 substrates. Ranges of film properties were identified that gave superior device performance. Several potentially novel features of the deposition process, including new chemistries, have been identified and patent applications are in process.

In parallel with the in-house effort to develop an APCVD capability for the buffer layer, we have also explored the capability of outside vendors to make buffer layers. The first batch from one vendor was found to be outside the range of electrical properties needed and the first batch from another vendor was found to be unstable at cell processing temperatures.

2.1.2 Thin-CdS Devices

Buffer-layer films made on 100 cm^2 substrates were used to make small-area cells, and films on full-size plates (7200 cm^2) were used to make both cells and modules. The results were used to identify the important film characteristics. The function of the buffer layer is to allow thinning of the CdS in order to increase J_{sc} without loss in other I-V parameters (primarily V_{oc}, but also FF). This function was verified through the use of controls. For example, one batch of control samples with thin CdS but no buffer layer had an average efficiency of 6.7%, while cells with a doped buffer layer had an average efficiency of 12.5%.

High efficiency cells have been achieved using the APCVD buffer layer and thin CdS. A cell with a standard 3 mm-thick sodalime-glass substrate, commercially-available TCO, and an APCVD buffer layer was made, given a 7 day light soak (~800 W/m^2, 65°C), and then measured at NREL to be 13.2% efficient (V_{oc} of 0.821V, J_{sc} of 23.0 mA/cm^2, FF of 70.06%). The spectral response of a similar high-efficiency cell and a standard production cell is shown in Figure 2-1. As can be seen in the figure, the buffer/thin-CdS cell has significant response in the wavelengths that would normally be lost in absorption in the CdS (350-500 nm).

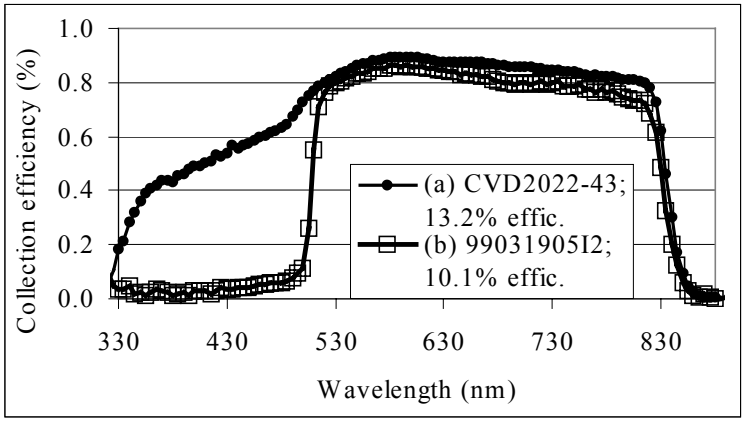


Figure 2-1. Spectral response of (a) standard production cell and (b) cell with APCVD buffer layer and thin CdS.

Modules were also made with buffer layers and thin CdS. Details are given in section 2.4.3.

2.2 Improved TCOs

First Solar currently uses TEC 15 substrates from Libby-0wens-Ford (LOF). The work described in section 2.1.1 (and the equipment section of 2.5) may also lead to improvements in the APCVD of conductive layers for TCOs. Advances in this area might be provided to glass/TCO vendors or might be used in-house for TCO films. New TCO layers developed at NREL and other glass/TCO vendors were also evaluated for suitability in our process.

2.3 Small-area Experiments

2.3.1 Vapor-$CdCl_2$ Treatment

Because in-line vapor processes can provide more uniform treatment and a more pristine surface compared to wet-$CdCl_2$ treatment, they present an opportunity for improved module performance. In Phase II the small-area vapor-$CdCl_2$ system (which was described in the Phase I report) was used to explore the effect of treatment ambient. Different gasses were injected into the treatment chamber at 7.5 sccm. The results were multi-cell average efficiency of 10.91% for dry air, 10.69% for nitrogen, 10.68% for room air, 10.74% for wetted nitrogen, 10.45% for wetted dry air, 10.25% for 50% oxygen, and 10.20% for 100% oxygen. More remarkably, the light soak behavior of the cells $CdCl_2$ treated with injection of wetted (room-temperature saturated) air was dramatically different -- the cells dropped from 10.45% to 6.8% with 1 day of light soak then came back to 8.7% with 14 days of light soak. The interaction of vapor-$CdCl_2$ treatment ambient and light soak behavior of cells will be explored further in Phase III.

2.3.2 Small-area VTD

The small-area vapor-transport deposition system was used to discover that higher substrate temperature can result in improved CdS uniformity. As a result of this work, a 13.5% (unconfirmed) efficient cell on standard TEC 15 glass (with no buffer layer) was achieved. Research also progressed on doping of the CdTe during deposition. Cells of ~9% have been achieved with no post-deposition doping.

2.4 Large-area Experiments

2.4.1 Module Uniformity

Non-uniformity of performance harms the total performance of any solar cell or module (modeling of the effect of non-uniformity is discussed in section 3.1.7). Even if the all the areas of a module are the same efficiency, if there are variations in the solar cell parameters (V_{oc}, J_{sc}, FF) as a function of location, then the total performance will be lower than the average of the areas due to the series/parallel connection of a module (i.e., the 116 cells of the module all have to carry the same current and the area within a given

cell is ideally equipotential). Improvement of uniformity is thus a path to improved module performance.

Efforts to improve coating uniformity were discussed in section 1.5.1. Efforts to improve processing uniformity have been a central theme in the design and construction of the new manufacturing line discussed in section 1.2. In this section we discuss data from two modules that were cut up into 72 minimodules each. First, a low-efficiency module from the pilot-production coater (9/10/99 deposition date) was characterized and was found to be highly non-uniform as shown in Table 2-1. Second, one of the early plates from the new production coater (3/24/00 deposition date) was characterized in the same manner and was found to be much more uniform, as shown in the same table.

Table 2-1. I-V parameters of 72 minimodules from 9/99 and 3/00 plates:

	Substandard module from pilot line			Module from production coater		
Mini-module parameter	Average	Standard deviation	Relative std dev.	Average	Standard deviation	Relative std dev.
Efficiency (%)	5.6	1.6	29%	7.0	0.5	7%
V_{oc} (mV)	752	82	11%	809	14	2%
J_{sc} (mA/cm^2)	17.8	0.8	4%	18.9	0.4	2%
Fill Factor (%)	44	7.8	18%	50.1	3.0	6%

In phase III we plan to do spatial characterization with an automated system that will provide up to 7200 data points for a module.

2.4.2 Module Diagnosis

Another path to improving average efficiency of modules is to diagnose problems that occur. Significant effort was expended in this manner for modules from the pilot-production line. One of the primary problems identified was poor laser scribing from the old multi-laser approach. These problems included poor electrical isolation across scribe 3 caused by occasional metal bridging and melting down the sides of the scribe, poor isolation across scribe 1 at the side-edges of module caused by incomplete scribing, high series resistance in the metal over scribe-1 caused by metal cracking, and high series resistance of scribe 2 caused by improper-depth scribing.

While most of these problems are expected to be eliminated with the transition to the new laser approach in the production line (see section 1.7), improvement of the pilot-line process from module diagnosis resulted in better module performance and thus an opportunity to identify other performance-limiting problems before scaling to large volumes on the new production line. Protocols for module diagnosis were also improved and are expected to be useful for the production line.

2.4.3 Modules

Twelve modules were fabricated and shipped to NREL. For nine of the modules, the addition of a APCVD buffer layer in between the front contact and a thin CdS layer

(see section 2.1) resulted in increased J_{sc} without loss in V_{oc} or FF. Three of the twelve modules were chosen from standard production to show contrast with the thin-CdS modules and to show progress with the standard process. All of the modules were made on the production coater and new manufacturing line and had aperture areas of approximately 6477 cm^2. While the modules were completed after the Phase II reporting period, the information is included in this report because the modules were a Phase II contract requirement. The unconfirmed I-V parameters of the modules are shown in Table 2-2.

Table 2-2. Unconfirmed I-V parameters of 12 modules delivered to NREL.

	Aperture efficiency	Total-area efficiency	V_{oc} (per cell)	J_{sc} (mA/cm^2)	FF	V_{mp} (module)
Average of thin-CdS set	9.12	8.20	0.797	21.9	57.1	64.2
Average of standard set	8.35	7.54	0.799	19.6	58.2	64.5
Average of all	8.93	8.03	0.798	21.3	57.4	64.3
Champion of thin-CdS set	9.59	8.58	0.805	22.2	58.6	64.1
Champion of standard set	8.43	7.60	0.803	19.6	58.6	65.1

2.5 Research Equipment Development

2.5.1 Large-area Sputter Deposition System

The large-area multi-cathode sputtering system was completed. This system, which is capable of depositing films on 60cm x 120 plates, was built to enable TCO, buffer-layer, and back-contact research on the module-size scale. Problems that were overcome, such as system leaks and power dissipation difficulties, were discussed in quarterly reports. The system has excellent uniformity (< 10% variation in thickness and resistivity) and base pressure (3 x 10^{-6} torr).

2.5.2 Small-area VTD System

System upgrade and research continued with the small vapor-transport deposition system. A more robust stainless steel exhaust manifold was installed, but concerns about flaking from the oxidized stainless led to the replacement with a ceramic manifold. A period of non-standard deposition-behavior, characterized by low cell short circuit currents and unplanned sublimation of CdTe from an internal surface within the system, provided some information about non-optimum CdS/CdTe junction formation.

2.5.3 Small-area APCVD Systems

To screen potential chemical systems a small APCVD reactor using SiC fiber substrates was built. The reactor uses laboratory-glass components and was inexpensive to construct and easy to clean. Two other systems were built to investigate deposition on glass substrates. These systems can accommodate 10 cm x 10 cm glass substrates and were used to investigate deposition, resultant film, and device characteristics. The systems use stainless steel chambers with the glass substrate heated by a ceramic block.

Chemical precursors are carried into a mixing manifold, which is a double-wall tube with heated air passed through the outer tube for temperature control. Additional details of the designs for these systems were included in a paper submitted by Dean Giolando, *et al.*, to the Spring 2000 MRS meeting in San Francisco, CA.

2.5.4 Large-area APCVD System

In parallel with the effort to develop new deposition chemistries and process parameters for the APCVD of buffer layers that was described in section 2.1, we have proceeded with the development of a pilot-production system capable of depositing the buffer layer on a 60-cm wide web (Figure 2-2). While this system is limited to a speed of 1.8 m/min, the process is suitable for a glass line speed of 12 m/min. The system has resulted in cells with unconfirmed efficiencies as high as 13.8% and was used to produce the buffer layer for the modules described in section 2.4.3.

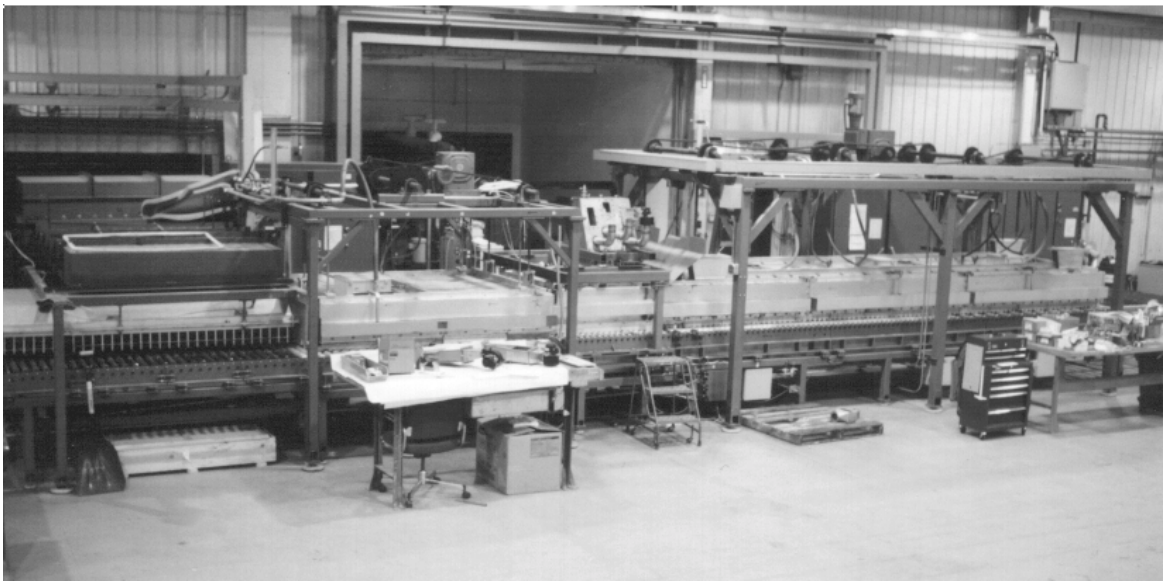


Figure 2-2. APCVD system for module-scale buffer-layer deposition.

3. Characterization and Analysis

3.1 Characterization of Films and Devices

3.1.1 Spectral Response

A grating-monochromater-based quantum efficiency (QE) system was designed, assembled, and used to characterize cells. The system provides high-resolution measurement of the spectral response of solar cells, with scans normally done over the range of 320 to 1000 nm. An example of output from the system was shown previously in Figure 2.1.

3.1.2 C-V and C-F Characterization

A new admittance (capacitance, C, and conductance, G) measurement system was developed and used. The system measures admittance as a function of voltage (V) and frequency (F). The system is designed to provide information on the doping profiles and trap density of CdTe solar cells.

In a typical admittance measurement system a small ac voltage signal is applied across the device and the real and imaginary part of the resulting current signal is measured. A synchronous detector is used to detect the complex current., which can be converted to C and G respectively by knowing the frequency and magnitude of the excitation signal. To have a linear response, the excitation voltage must be small (normally ~5 mV because it must be smaller than kT/q, which is ~25 mV at room temperature). Since the impedance of a capacitor is inversely proportional to the frequency, at low frequencies the current signal would thus be very small. Additionally in a device with low shunt resistance, the phase angle ($\tan^{-1}$[imaginary/real]) would be so small that the imaginary part, and hence the capacitance, cannot be resolved. Because of this problem, most commercial systems are limited to high frequency (>10 kHz) excitation. This prevents characterization of deep trap states that may be present in CdTe devices. Fortunately, due to recent advances in digital signal processing (DSP), lock-in amplifiers are now available with very good low frequency performance. One of these new DSPs, a Stanford Research 830, was used for the new system. Additionally, a custom electronic circuit was built to condition the input and output signals. The system is capable of accurate admittance measurements in the range of 0.001 Hz to 100 kHz. Due to the high phase accuracy, the system is capable of accurate capacitance measurements even when the phase angle is as low as 0.2 degrees (with earlier analog circuitry it was not possible to resolve the capacitance accurately if the phase angle was less than ~5 degrees). Calibration measurements are taken before each experimental data point to further increase accuracy and a windows interface was created using Visual Basic for ease of use.

A series of CF measurements were performed using the new system on CdTe-based devices with different dopants in the CdTe film. The range of measurements, 0.1 Hz to 100 kHz, is much larger than typically reported in literature, and provides information related to deep trap states. Measurements of devices indicate that C-F and G-F curves are similar in shape to cases where a continuous distribution of defects is assumed to exist

around the Fermi level. An abstract on admittance spectroscopy results was submitted for the IEEE Photovoltaic Specialists Conference (D. Grecu, *et al.*)

3.1.3 Electron-beam Induced Current (EBIC)

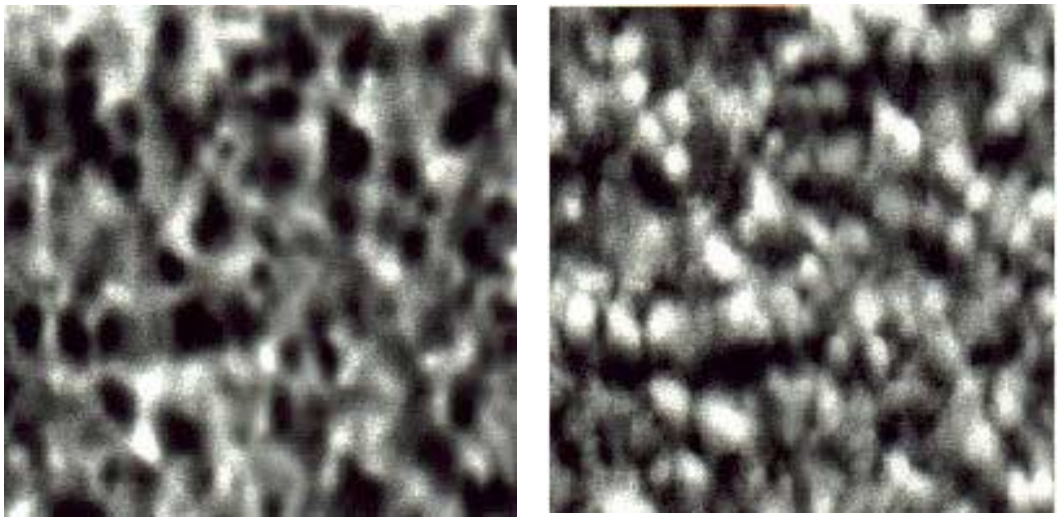
Electron-beam induced effects are known to give valuable information about the physics of defects in semiconductors. Electron beams with energies of 10 – 30 keV and currents between 0.01 and 10 nA, available in electron microscopes, do not produce much heating and are not energetic enough to cause atomic displacements. However, in semiconductor materials, electron-beams can lead to electron-hole pair generation rates up to 10^5 higher than light (AM 1.5). This reporting period, planar EBIC, with the electron beam incident on the back contact of cells, was used to characterize grain boundaries, as will be discussed here, and was used to investigate cell non-uniformity and cell degradation kinetics (discussed in sections 3.1.7 and 3.2.1.2).

The electron beam generates electron-hole pairs in a localized teardrop-shaped region whose position and size inside the device depend on the electron energy. The distance from the back contact to the center of the generation region varies monotonically with that energy up to 5.1 μm at 30 keV. The beam scans an area A of a given size (ranging from 0.5 μm^2 to 13,200 μm^2 in our experiments) and the generation region follows the beam adiabatically. The time, t, that the beam spends on a given local spot decreases with A,

$$t = \frac{\sigma}{A} t_s << t_s , \qquad (3.1.3\text{-}1)$$

where $\sigma << A$ is the generation region area, t_s is the measured scanning time. In our experiments we measured EBIC as a function of scan time t_s, area A, electron energy E, and beam current I_e.

We compared the secondary electron image to the EBIC image and found grain-boundary regions to be more effective current collectors than the intra-grain material (Figure 3-1). The two images when superimposed produce a uniform black appearance. They are complimentary to each other as a negative to the photographic image. The ratio of the grain boundary to intra-grain EBIC intensity can be as large as 100 (different etches changed the EBIC image and the ratio of intra-grain to grain-boundary EBIC intensities.). Galloway, Edwards, and Durose [4] reported a similar effect for CdTe cells.



(a) (b)

Figure 3-1. EBIC image (a) in comparison with the secondary electron image (b). Bright spots in the EBIC map correspond to the grain boundary regions where EBIC is a maximum. E-beam parameters: I_e=1.30 nA, E=25 keV, A=530 μm^2.

We explain the increased collection at the grain boundaries by the presence of built-in electric fields that effectively separate non-equilibrium electron and holes and thus suppress their recombination. We note that the parameters of such fields (the amplitude and the screening length) depend on local impurity (defect) concentration and thus fluctuate between different grain boundary regions. The corresponding recombination barrier fluctuations make the recombination parameter fluctuate exponentially between different grain boundary regions. This non-uniformity is discussed further in section 3.1.7; it may also be the cause for the observed variations in degradation kinetics between different spots on the same sample as discussed in section 3.2.1.2.

3.1.4 SEM/EDS

A significant upgrade was made to First Solar's SEM/EDS system. The computer and data acquisition capabilities were upgraded and the EDS (energy dispersive spectroscopy) system was repaired and improved to cover light-element detection.

3.1.5 Photoluminescence Studies

In cooperation with the University of Toledo, photoluminescence (PL) was used to investigate the electronic states of impurities in CdTe films and cells. Details beyond those given below were included in a paper by D. Grecu, *et al.* submitted to the Journal of Applied Physics, which was accepted for publication.

Additional confirmation of the assignment of the PL lines and further insight into the nature of the Cu complexes was provided by examining the PL spectra of samples annealed in Cd and Te overpressures. Figure 3-2 illustrates the PL signal from pure and Cu-doped CdTe samples annealed in Cd and Te overpressures. The PL spectra for the Cu-free samples (Fig. 3-2a) are very similar for the two different anneal atmospheres

with a much stronger 1.55eV DAP transition for the Te-annealed sample, consistent with the D-V_{Cd} assignment.

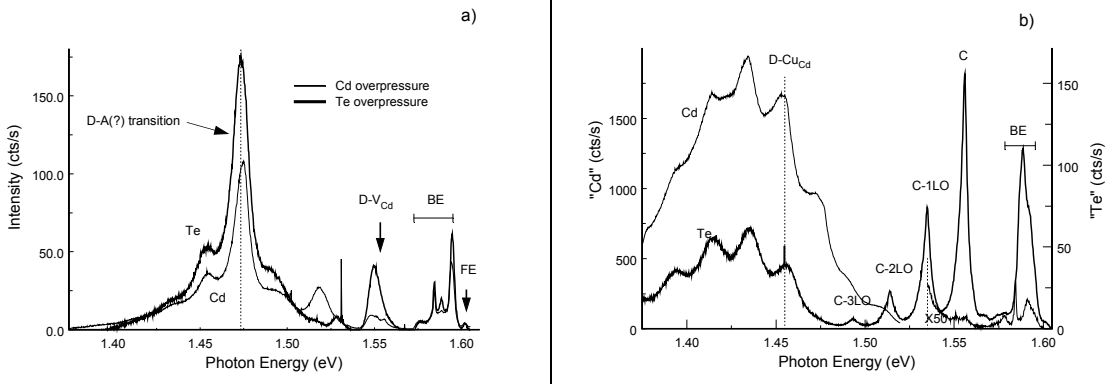


Figure 3-2. PL spectra of single crystal CdTe annealed in Cd and Te overpressures. a) no Cu, b) Cu-doped.

The PL spectra of the Cu-doped samples are markedly different depending on the anneal atmosphere (Figure 3-2b). The Cd-annealed sample is characterized by a very strong deep "defect" band (1.4 –1.5 eV) relative to the excitonic region while the spectrum of the Te-annealed sample is dominated by the "complex" transition, C at 1.555 eV. Both samples show a DAP transition at 1.45 eV, indicating the formation of Cu_{Cd} states. This is consistent with results reported by Shaw [5] who suggests that Cu diffusion is independent of the anneal atmosphere (similar diffusion was obtained by annealing in Cd and Te rich overpressures). The proposed diffusion mechanism that would explain this behavior [5] is the formation of Cu-V_{Cd} pairs at the surface, which acts as an infinite source of Cd vacancies, followed by the diffusion of these pairs. The "defect" region for both the samples without Cu (Figure 3-2a) is dominated by a DAP transition at 1.47eV. The origin of this transition is uncertain: Onodera and Taguchi [6] attributed it to the recombination of the excitons bound to a localized center; however, Meyer *et al.*[7] ascribe it to a donor→A-center transition.

While transitions related to Cu_{Cd} states are observed for both types of samples, the 1.555eV "complex" transition (C) is observed only for the sample with an increased number of Cd vacancies (annealed in Te overpressure). Based on this observation we propose that the 1.555eV transition is due to Cu_i-V_{Cd} states rather than Cu_i-Cu_{Cd} or Cu_{Cd}-Cd_i.

Annealing the samples in a Cd or Te overpressure had a dramatic influence on the Cu-related aging behavior. We observe that samples annealed with Cu in a Cd overpressure show a substantially amplified PL degradation when compared with similar samples annealed in a Te overpressure as illustrated in Figure 3-3. For the Cd-annealed sample the amplitude of the bound-exciton region of the spectrum drops by a factor of 2-3 and shifts towards higher energies. This shift is due to the drop in intensity of the 1.59 eV exciton-bound to Cu_{Cd} relative to bound-exciton transitions at

higher energies. In addition, the 1.45 eV DAP band exhibits a drop of 6000 times. In contrast, the Te-annealed sample exhibits a relatively constant overall luminescence signal although it is much weaker than for the fresh Cd-annealed sample. We observe a shift of 5 meV towards higher energies in the 1.555eV line and its phonon replicas after the 90 hours illumination, which is presumably due to changes in the Cu-V_{Cd} complexes.

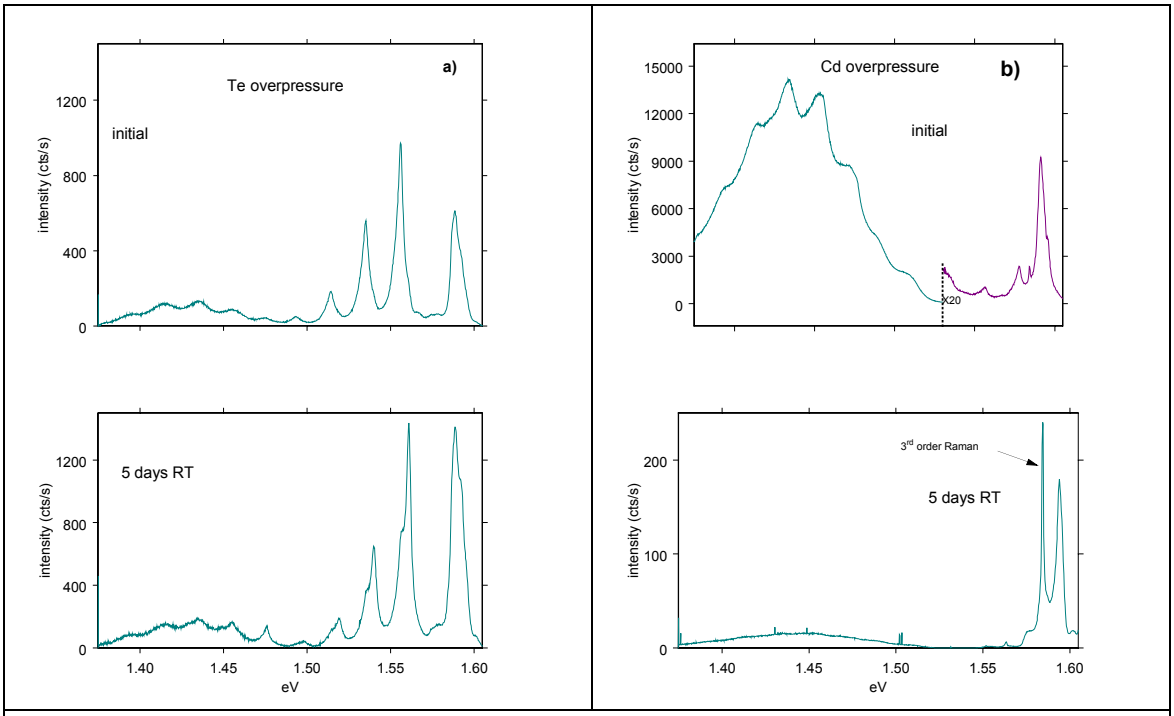


Figure 3-3: Changes in PL in Cd and Te annealed, Cu-doped samples following 90 hours illumination at room temperature

The decrease of the Cu_{Cd} related PL transitions in samples annealed in a Cd overpressure compared to their stability in samples annealed in a Te overpressure indicates the important role played by the Cd vacancies in "stabilizing" Cu atoms in the CdTe lattice. We suggest that, while Cu_{Cd} states are likely to dissociate at a similar rate regardless of the density of Cd vacancies, a diffusing Cu_i^+ ion has a higher probability to recombine with a new V_{Cd}^- in the sample with an increased number of Cd vacancies. In the absence of the Cd vacancies, Cu ions are more likely to precipitate or otherwise participate in the formation of non-radiative recombination centers.

3.1.6 Back Contact Effect on Open Circuit Voltage–Micro-non-uniformity?

In the Phase I report we discussed the effect of copper on devices, namely, that the addition of Cu in the back contact followed by an anneal improves the V_{oc}, not just the series resistance, of devices. This year we continued research in this area to try to understand how different layers or processes at the back contact can influence V_{oc} (the influence of the back contact extends far beyond whether or not Cu is introduced). In order to aid team members' attempts to build conceptual and numerical models for CdTe device operation, we presented data at the National CdTe

Team meeting showing an extreme example of a back contact effect. The example presented was for two cells made from the same CdS/CdTe plate -- one cell processed with the normal back contact procedure and one cell with the same procedure except that the interfacial layer (IFL)/surface treatment between the CdTe and the back contact metals was omitted. The current-density vs. voltage (J-V) curves of these two cells are shown in Figure 3-4.

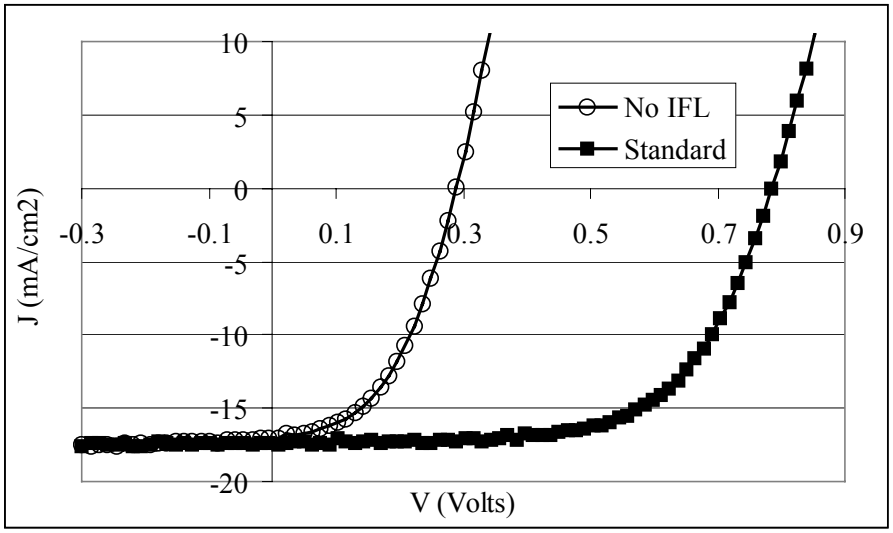


Figure 3-4. J-V plots of two cells from same CdS/CdTe substrate illustrating effect of back contact on Voc. "No IFL" cell is identical to "standard" cell except that the normal interfacial layer between the CdTe and the back contact metals is omitted.

Also presented was information on the V_{oc} and quasi-surface photovoltage (SPV) of these two cells with and without the back metal layers. The SPV technique, which was described in greater detail in our Phase I report, consists of measurement with a high-impedance electrometer and a graphite pad in contact with the back surface with illumination from the front side. For measurement "without the back metal layers", the layers were removed by mechanical force after bonding a metal post to the back layer. The results were as follows: the standard cell had a V_{oc} of ~800 mV with the metals and an SPV of ~800 mV with the metals removed. The "No IFL" cell had a V_{oc} of ~300 mV with the metals and an SPV of ~800 mV with the metals removed. *Thus, the lack of the IFL in the back contact processing only suppressed the voltage of the device when the metal layers were on the device.*

This startling result is not the only report of strong effects from back contacts or back contact processes. For example, Tim Gessert reported to the National Team that the use or absence of ion-beam milling in his sputtered-ZnTe contact process can affect the V_{oc} by hundreds of mV. These results have large implications for conceptual models of device operation -- for any model to be valid, it must be able to be consistent with a suppression of up to 500mV from the back contact with and without visible roll-over of the J-V curve.

At the October and January team meetings we presented a list of conceptual models. Since supporting evidence exists for more than one model, it is possible that back contact processes can influence device V_{oc} by more than one mechanism. For instance, dopants have been shown to diffuse from the back contacts into the CdS and CdTe [8] and would thus affect V_{oc} via modification of the junction, but this mechanism alone would likely be insufficient to explain the V_{oc} vs. SPV results of the cells discussed above. Modification of a barrier at the back contact would affect V_{oc} if there were minority carriers available at the back contact (by local generation or diffusion) to form a photovoltage opposing the main diode, but since strong V_{oc} effects can be seen even in thick devices it is likely that this mechanism could not produce the full magnitude of the shifts seen experimentally. A dipole effect was proposed by another team member, but we are not aware of how this can be added to the conceptual and numerical models currently in-use to test the theory.

To explain the large changes we were left with two models, both of which involve more than 1-dimensional device operation. First, the back contact processes could change the Fermi-level in the grain boundaries and thus somehow influence the effective carrier concentration in the CdTe grains near the junction or otherwise effect junction properties. This would be consistent with the observation by Levi, *et al.* [9] that Te at the back of CdTe devices changes the high-injection photoluminescence at the front of the device. Second, the back contact processes could alter the influence of micro-non-uniformities which suppress V_{oc}. Both of these models would be consistent with the elimination of the V_{oc} suppression with the removal of the laterally-conductive back metal layers. Modeling for the effect of non-uniformity shows that the 500 mV suppression of V_{oc} can be easily achieved -- this modeling is discussed in the next section.

3.1.7 Cell and Module Uniformity

As discussed in the previous section (3.1.6), micro-non-uniformity could be the explanation of large (>500mV) suppression of V_{oc} in non-standard-process devices. It thus could be a prime determinant of variation in V_{oc} in normal cells. And as discussed in sections 1.5.1 and 2.4.1, non-uniformity on the macro-scale is clearly important and has room for improvement. This reporting period significant strides were made in the modeling and understanding of the effects of non-uniformity.

A simple illustration of the potential impact of non-uniformity is numerical modeling that shows the effect of a “bad diode” in a cell. The results of the numerical analysis show that even a small bad area can greatly lower the V_{oc} without appreciably affecting J_{sc} or the shape of the IV curve -- this is experimentally what is seen in the “no-IFL” cell of Figure 3-4. The numerical analysis was done by finite difference assuming a 1 cm^2 cell with a 0.2 cm separation to the busbar which surrounds the cell and a sheet resistance of the TCO of 10 Ω/□. For the "normal cell", the dark-current coefficient, j_o, is 7.72e-11 A/cm^2 on the full area of cell. For the "with bad diode" cell, j_o, is the same as for the normal cell except for a small area (2.5% of the total area) with j_o = 100,000 times the nominal. For both cells the diode ideality factor, A, is assumed to be 2.03, kT is 0.025854 eV, and the photocurrent, j_L, is 0.023 A/cm^2. Plots of the J-V curves from this numerical analysis are shown in Figure 3-5.

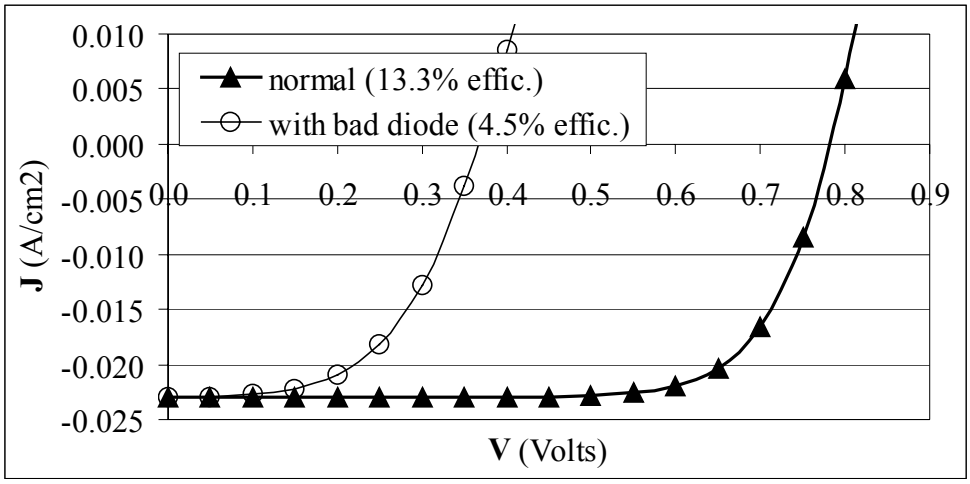


Figure 3-5. Calculated (by finite-difference model) J-Vs for two cells. For "normal cell", j_o=7.72e-11 A/cm^2 on full area of cell. For "with bad diode" cell, j_o is same as for normal cell except for small spot (2.5% of the area) with j_o = 100,000 times the nominal.

More advanced mathematical treatments and experimental evidence of non-uniformity were also developed this reporting period. One experimental observation of non-uniformity in polycrystalline PV thin film devices came from electron beam induced current (EBIC) measurements (see section 3.1.3 for a description of the technique). Shown in Figure 3-6 is the EBIC measured at five spots 200 µm apart along a straight line in a CdTe/CdS polycrystalline cell. Since EBIC is proportional to the carrier collection efficiency, we conclude that the latter fluctuates between different spots in the device.

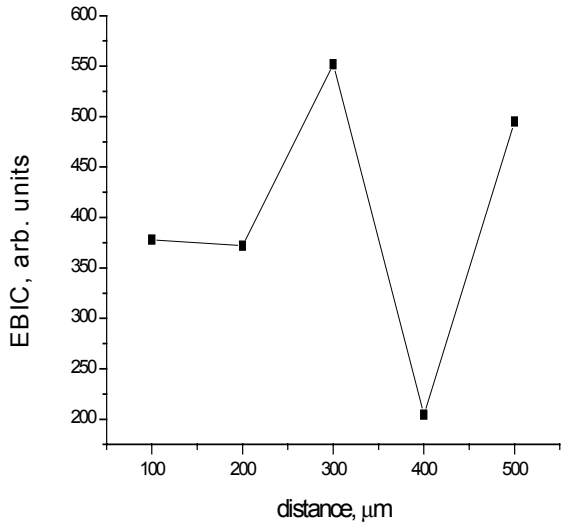


Figure 3-6. EBIC variations in a CdTe/CdS PV cell; electron beam scan area 530 µm^2, energy 20kV, and current 1 nA.

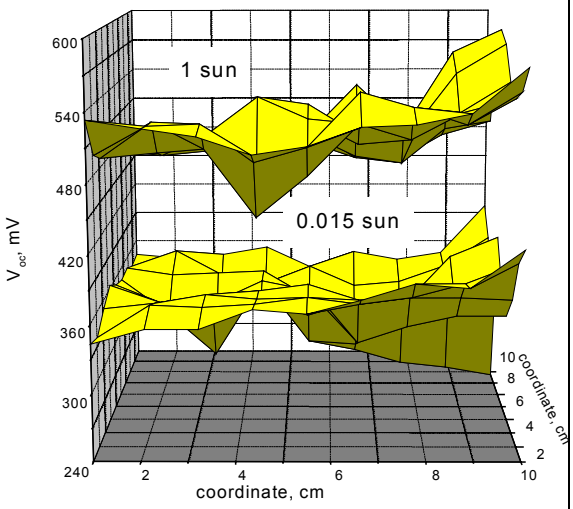


Fig. 3-7. Open-circuit potential variations in the back wall plane of CdTe/CdS cell with intentionally-low V_{oc}.

Other experimental support for non-uniformity in cells includes the following:

1) Laser scans from thin-film polycrystalline modules (optical beam induced currents, OBIC) show the same effect. OBIC spatial variations are maximum at forward bias near the open-circuit regime [10] and depend on material treatments [11].
2) The temperature field in an illuminated open-circuit cell is non-uniform. To visualize this effect we used thermal paper at the back wall of a CdTe/CdS cell whose front wall (CdS side) was illuminated. We found rare (of the order of one per 100 cm^2) hot spots of ~1mm size that were not associated with pinholes or other SEM visible defects.
3) The electric potential in un-biased cells is non-uniform. Direct measurements were made at 81 spots 1 cm apart in the back wall of CdTe/CdS cell whose front wall was illuminated. A thin (100Å) metal film was deposited on the back wall. Because of its high sheet resistance (ρ~170 Ω/□), local regions in the cell were effectively screened of each other. The characteristic screening length $(kT/e\rho j)^{1/2}$ (see Eq. 3.1.7-6) below) depends on the light intensity via the electric current density *j* and is estimated as 1 cm for low light (~0.01 sun), and 1mm for high light (1sun) conditions. The distributions in Figure 3-7 correspond to a sample that received intentionally poor back contact treatment (we are able to significantly improve uniformity by optimizing the back contact).
4) Other groups results, including those reported at the National CdTe Team meetings.

Given the potential importance of non-uniformity in thin-film PV devices, an effort was made to advance understanding in this subject. This reporting period a new approach to closed-form analysis of the problem was developed. Beyond the text below, additional details were included in a paper submitted to the IEEE Photovoltaic Specialists Conference (V. Karpov, *et al.*).

To take into account variations in local properties we treat polycrystalline PV film as a system of random micro-diodes in parallel. Each diode has a diameter *l*. An important feature of the model is that one of its electrodes mimics the TCO and has a finite sheet resistance. The micro-diodes generate the current

$$j = j_0\left\{\exp\left[\frac{e(\varphi - v)}{kT}\right] - 1\right\} \qquad (3.1.7\text{-}1)$$

per area, where φ is the electric potential, v is the local open circuit voltage, e is the electron charge, T is the temperature, and k is the Boltzmann's constant. In our model v is a random quantity varying between different points in the film (Figure 3-8) and is characterized by its probability distribution g(v*)*.

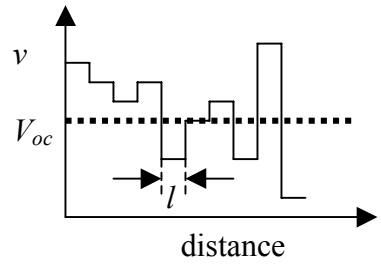


Figure 3-8. Spatial variations in micro-diode open circuit voltage v and the effective macroscopic open circuit voltage V_{oc}.

Because the micro-diodes are not equivalent, there are electric currents circulating in the system. This makes the measured open circuit voltage V_{oc} different from the simple average over the local v's. To solve the above problem we develop the effective medium approximation (also referred to as the self-consistent approximation or the mean-field approximation in the physics of disordered systems and phase transitions). The effective medium sought is an imaginary homogeneous system that effectively represents the non-homogeneous system under consideration.

To determine the effective medium parameters we start with a single foreign diode embedded into a uniform effective medium consisting of identical diodes of an open-circuit voltage V_{oc} each. The voltage drop V across the foreign diode is a function of its bare open-circuit voltage v and V_{oc},

$$V = f(v, V_{oc}). \tag{3.1.7-2}$$

This function is specified in what follows. Given the latter function, we consider an arbitrary random diode in the original non-uniform system and approximate its surroundings by the uniform effective medium. This approximation and corresponding Eq. (3.1.7-2) must be valid for any of the random diodes. The self-consistency dictates that, as averaged over all such diodes, the voltage V in the equation is equal to the effective-medium open circuit voltage,

$$V_{oc} = \int dv g(v) f(v, V_{oc}). \tag{3.1.7-3}$$

The effective medium parameter V_{oc} is found as a solution to the latter equation. In other words, instead of averaging insulated micro-diode open-circuit voltages, the effective medium theory self-consistently averages the voltages of micro-diodes interacting with the effective medium.

To implement the above approach one need to specify the probability distribution in Eq. (3.1.7-3) and the function f in Eq. (3.1.7-2). We used the simplest (uniform) probability distribution,

$$g(v) = (v_{\max} - v_{\min})^{-1}. \tag{3.1.7-4}$$

Solving the problem of one foreign diode embedded into homogeneous array gives

$$f \approx \begin{cases} V_{oc} \quad \text{for} \quad v > V_{oc} - \dfrac{2kT}{e}\ln\left(\dfrac{L}{l}\right) \\ v + 2\dfrac{kT}{e}\ln\left(\dfrac{L}{l}\right) \quad \text{otherwise.} \end{cases}, \tag{3.1.7-5}$$

Here L is the characteristic correlation length, over which the presence of a foreign diode affects the electric potential distribution in the system. L is described by the equation

$$L = \sqrt{\frac{2kT}{j_0 \rho e}\ln\left(\frac{L}{l}\right)} \quad . \tag{3.1.7-6}$$

Eq. (3.1.7-5) was derived assuming relative fluctuations in individual diode currents j_0 to be small as compared to $(L/l)^2$.

Note that, in spite of its cumbersome form, Eq. (3.1.7-5) has a simple physical meaning. A large-v micro-diode ($v>V_{oc}$) generates effective forward bias applied to the surrounding medium. This causes strong forward currents screening the perturbation over a small distance and exponentially suppressing its amplitude, hence $f \approx V_{oc}$. A small-v micro-diode ($v<V_{oc}$) finds itself under forward bias. The voltage across it increases by δV, so that to accommodate the reverse currents generated by $(L/l)^2$ stronger diodes in the correlated are of the radius $L>>l$,

$$\exp\left(\frac{e\delta V}{kT}\right) = \left(\frac{L}{l}\right)^2 .$$

Eq. (3.1.7-6) states that the voltage difference balances the drop due to the sheet resistance, that is

$$\delta V = \rho j_0 L^2 .$$

Here j_0 is understood as the average over individual micro-diode currents. The latter two equations constitute a simplified derivation of Eqs. (3.1.7-5) and (3.1.7-6).

Substituting (3.1.7-4) and (3.1.7-5) into Eq. (3.1.7-3) yields

$$V_{oc} = \min\left\{ v_{\min} + 2\frac{kT}{e}\ln\left(\frac{L}{l}\right), v_{\max} \right\}. \tag{3.1.7-7}$$

From our EBIC measurements we can estimate the characteristic non-uniformity scale l~0.2mm. Then using the parameters of our samples we get from Eq. (3.1.7-4) the screening length L ~4mm.

One phenomenon associated with weak diodes is hot spots. Because the current generated in the area L^2 is forced through much smaller weak diode area $l^2 << L^2$, there is a high local heat density, corresponding to the power $P=j_0 L^2 V_{oc}$. Thermal conductivity diffuses this power over the system and thus determines the hot spot characteristic radius. We performed the standard thermal analysis of the temperature distribution caused by a cylindrical heat source across the film in contact with the glassy substrate. Far from the source thermal diffusion occurs through the glass substrate. The local temperature increase δT and the hot spot characteristic radius λ were found to be

$$\delta T = \frac{V_{oc} j_0 L^2}{2h\kappa} \text{ and } \lambda = \sqrt{\frac{\kappa}{\mathrm{K}} Hh} . \quad (3.1.7\text{-}8)$$

Here κ and K are the film and substrate thermal conductivities respectively; h and H are their thicknesses. Using our sample parameters gives $\delta T \sim 10^{o}$C and $\lambda \sim 1$mm.

When the correlated area L^2 contains many identical weak diodes, they all shunt the currents generated in the area. Since the heat is liberated in many diodes, it is less localized and causes less temperature increase, as compared to the case of a single weak diode. Hence, the hottest spots in the system correspond to configurations where there is only one weakest diode in the correlated area. The concentration of such spots can be estimated from the Poisson's distribution,

$$N = \frac{1}{L^2} \exp\left(-\frac{L^2}{l^2} \frac{eT}{v_{\max} - v_{\min}} \right) \quad (3.1.7\text{-}9)$$

We applied this result to the hot spots observed in our samples. By putting $L/l=20$ and $N \sim 0.01\text{cm}^{-2}$, we estimated from Eq. (3.1.7-9) v_{max}-v_{min}=0.6eV, which is qualitatively consistent with our direct measurements of electric voltage distribution in Figure 3-7.

3.1.8 Shunt Screening

An area of investigation closely related to the issue of non-uniformity (which was discussed in the previous section) is the effect of shunts on the performance of cells. This reporting period a closed-form solution was developed that enables calculation of the area affected by a point-perturbation such as a shunt. In addition to providing a useful tool for analysis of cells with shunts, the solution has the important implication that the voltage (V) applied to a cell by attaching two electrodes is not the voltage seen by all parts of the cell and that the effect of the deviation from the uniform-voltage assumption is governed by the same screening relationship as shunts. Thus the measured I-V characteristics of the cell will depend on the relationship between the cell size (l) and the screening length (L), being markedly different for the cases of small ($l<<L$) and large ($l>>L$) cells. Because L is voltage dependent, the standard interpretation of the PV cell I-V characteristics needs to be revised.

The simplest model for a shunt in a PV cell consists of a one-dimensional array of elemental diode in parallel with a resistor *(R)*. One electrode of the cell mimics the TCO and has a finite resistance per length *(ρ)*. L is the distance from the point perturbation

(the point where R exists instead of a diode) to the point where $V \cong V_{oc}$. Each diode is described by the classical equation, so that the current per length in the circuit, j is equal to $j_o(\exp(q\varphi/kT)-1)-j_L$ where e is the electron charge, φ is the electric potential, k is the Boltzmann's constant, and j_0 and j_L are the thermal and photo-generated currents. The open-circuit voltage (V_{oc}) is defined as the potential that results with $j = 0$.

For a finite resistance shunt, R, the potential drop across the shunt, V_R, can be related to the screening length via the loss current that flows through the shunt as follows:

$$L = \sqrt{\frac{2V_{oc}}{(j_L + j_0)\rho}} \equiv L_O \quad \text{(for R=0)} \tag{3.1.8-1}$$

$$L = L_0\sqrt{1-\frac{V_R}{V_{oc}}}, \quad \text{and } \frac{V_R}{V_{oc}} = \frac{r^2}{2}\left(\sqrt{1+\frac{4}{r^2}}-1\right), \; r \equiv \frac{R}{L_0\rho} \tag{3.1.8-2}$$

The I-V characteristics of this system are:

$$I = \frac{\delta V}{R_{eff}}, \quad R_{eff} = \rho L, \tag{3.1.8-3}$$

where δV is the voltage drop across the system and the effective resistance R_{eff} is determined by the region of the screening length L where the current is collected.

For $V<V_{oc}$, the solution is:

$$\delta V = V_{oc} - V, \; L = L_0\sqrt{\frac{V_{oc}-V}{V_{oc}}}, \quad \text{and } I = -\sqrt{\frac{j_L(V_{oc}-V)}{\rho}} \tag{3.1.8-4}$$

For $V>>V_{oc}$, the thermal generation dominates the current. Thus j_L in the above result must be replaced by $j_0 \exp(V/kT) \approx j_L \exp[(V - V_{oc})/kT]$ which for $\delta V = V - V_{oc}$, gives:

$$L = L_0\sqrt{\frac{V-V_{oc}}{V_{oc}}}\exp\left(\frac{V_{oc}-V}{2kT}\right), \text{and } I = \sqrt{\frac{(V-V_{oc})j_L}{\rho}}\exp\left(\frac{V-V_{oc}}{2kT}\right) \tag{3.1.8-5}$$

And for $V_{oc} - \varphi > T$ and $x < L$ the coordinate dependence of the electric potential is:

$$\varphi \approx V_{oc} - (V_{oc} - V_R)\left(1-\frac{x}{L}\right)^2 \tag{3.1.8-6}$$

Equation 3.1.8-6 was verified by a finite difference numerical model of a cell with a point-shunt as shown in Figure 3-9. It was also verified with a physical cell (a fixed-resistor shunt at the end of the linear-scribed cell) as shown in Figure 3-10.

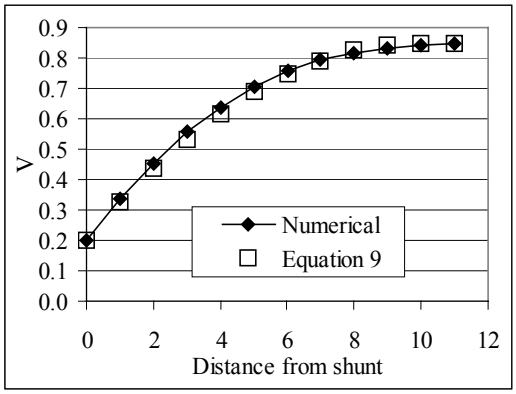


Figure 3-9. Equation 3.1.8-6 compared to FD numerical solution (for J_{sc} of 0.017A/cm^2, J_s of 2e-10, n of 1.8, T of 300K, ρ of 1, and R of 1.5).

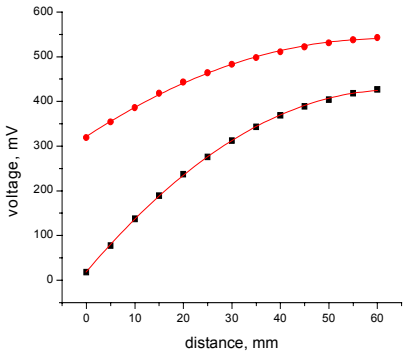


Figure 3-10. Two examples of experimental verification of equation 3.1.8-6.

Some of the consequences of the analytical solution to shunt-screening discussed above are as follows:

1. The I-V of a large cell will differ from that of a small cell. If a cell is larger than the characteristic screening length, the I-V will show the effect of the series resistance of the TCO which classical I-V analysis could misinterpret as rollover and higher diode quality factor. This may explain the diode-quality factors of greater than 2 that are determined for many thin-film cells by the classical approach. Note that the classical analysis, which assumes the cell bias to be uniform across the cell, is able to predict a lower slope of the I-V caused by the series resistance of the TCO by using a lumped-parameter series resistance, but this lumped-parameter approach does not include the voltage-dependent nature of the screening and thus does not correctly predict the shape of the I-V curve.
2. The transition from small- to large-cell regimes is dependent on the illumination. For dark conditions j_L is replaced by j_o in the formula for determination of the characteristic length; this can increase the screening length by a factor of 3000 and thus shift the I-V to the standard-diode equations of the small-cell regime. Again, the classical approach is able to show a simplified effect with a lumped-parameter series and shunt resistance, but the voltage-dependent nature of the screening is not reflected.
3. A high resistance "buffer layer", which is often included in high efficiency cells (see section 2.1.1), is shown to protect V_{oc} by greatly reducing the impact of micro-shunts.

3.1.9 Scribe Contact Resistance

Contact resistance measurements were made using a test pattern made by laser scribing (with 25 μm scribe width). The contact resistance of the standard IFL/metal to the TCO was found to be only 0.00025 Ωcm^2, which would result in minimal modules losses (only ~1.6% of the loss from lateral transport resistance of the TCO). In contrast, the contact resistance of an alternative IFL to the TCO was found to be high enough to significantly

affect module performance and would thus require scribing after the IFL is deposited. The contact resistance of the metal to CdS on TCO was found to be 0.0022 Ωcm^2, which would result in ~14% of the loss of TCO lateral resistance.

3.1.10 Performance of Modules under Non-standard Conditions

Modules are typically measured under standard conditions, which are defined as 25ºC module temperature and a normal incidence of 1000 W/m^2 with an AM1.5 global spectrum. In the field, conditions can deviate significantly from these standard conditions. A paper study and some experiments were done in response to reports from the field that First Solar modules were doing very well relative to other technologies in non-standard conditions such as high temperature, low light, and end-of-day conditions.

The reports of good high-temperature performance were found to be consistent with the small temperature coefficient that is theoretically predicted for CdTe solar cells and is normally found experimentally. The most recently obtained value of the temperature coefficient for maximum power was -0.06%/C for the First Solar 10 kW array at PVUSA (calculation courtesy of Tim Townsend, Endecon). This compares very favorably to crystalline silicon modules which typically have a coefficient between -0.35%/C and -0.55%/C. However, there has been considerable variation in the experimental values obtained for modules and arrays produced at SCI/First Solar over the years. As recounted in last year's report, the temperature coefficients for the maximum power was found to be on average -0.15%/C using seven different modules/arrays and/or calculation methods, but the standard deviation of 0.15%/C shows that there is considerable variation either in the products or the measurement methods.

In order to gain insight into favorable end-of-day performance, experiments and modeling were done. Measurement of a cell with illumination angle varying from 0 to 90 degrees showed very little dependence of the conversion efficiency on the angle of incidence, thus providing benefits for end-of-day conditions in non-tracking arrays. A lack of drop in performance with deviations from the standard-condition spectrum is due to the fact that the modules are single junction. Good performance under non-uniform illumination was suspected to be the result of distributed-shunt resistance inherent in the thin-film modules.

Finally, a review of studies that investigated module rating procedures revealed that the CdTe modules used in the studies overall rated better under non-standard conditions than most technologies (often on the order of 5-10% over the range conditions investigated), but there was variation depending on the study. For instance, in a report by Marion, et. al [12] the CdTe module studied had a 15% higher relative output at 50°C compared to the c-Si module, while in Whitaker and J.D. Newmiller [13] the output was only 3% higher. We look forward to the higher reproducibility of the new manufacturing line and the improvement of module energy rating procedures to more definitively show the performance advantages of CdTe modules in non-standard conditions.

3.1.11 External Characterization Results

Several groups, including NREL, the Institute of Energy Conversion, Colorado School of Mines, and Colorado State University, have provided characterization to aid in our effort to understand the operation of CdS/CdTe cells. Below are some of the results of that characterization.

3.1.11.1 CdS Characterization

Dr. Helio Moutinho of NREL used AFM to characterize SnO_2/glass, CdS/SnO_2/glass, and annealed-CdS/SnO_2/glass substrates. It was determined that CdS grain size was generally larger than the underlying SnO_2 grain size, but the SnO_2 could still influence CdS grain growth. Figure 3-11 and 3-12 show representative images for the TEC 15 substrates.

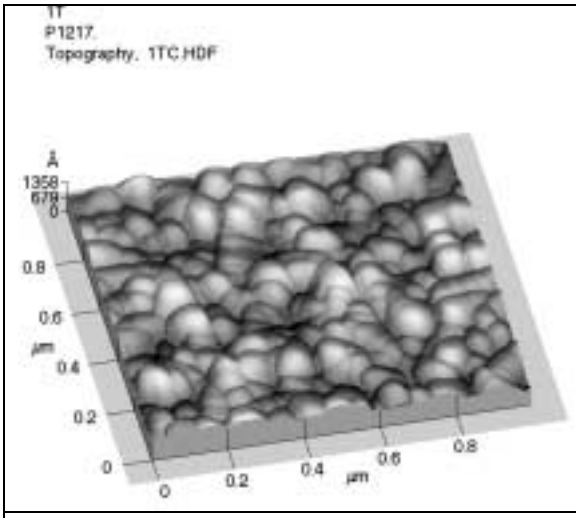


Figure 3-11. TEC 15 SnO_2

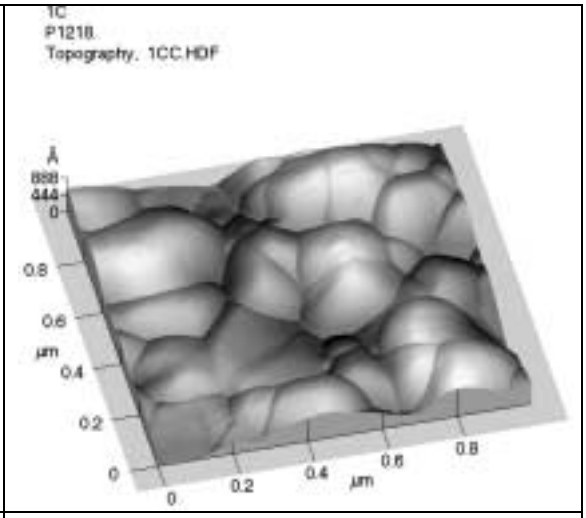


Figure 3-12. CdS on TEC 15 SnO_2

Some results of our analysis of the images provided by Dr. Moutinho for a variety of substrates is summarized in Table 3-1.

Table 3-1. Estimates of average grain size and pinhole count for SnO_2, CdS/SnO_2, and annealed CdS/SnO_2 films based on images from Dr. Helio Moutinho of NREL.

	Average Grain Size (µm)			Pinholes (#/µm^2)		
Substrate Type	SnO_2 only	CdS on SnO_2	Annealed CdS/SnO_2	SnO_2 only	CdS on SnO_2	Annealed CdS/SnO_2
Ultrasonic-cleaned TEC 15	0.08	0.18	0.18	1.4	1.1	0.9
Scrubbed TEC 15	0.09	0.19	0.21	0.1	0.3	0.3
Ultrasonic-cleaned Asahi	0.26	0.27	0.26	0	0.4	0.4
Ultrasonic-cleaned TEC 8	0.23	0.25	0.24	0	0.4	0.4

Dr. Moutinho also performed XRD on these same samples. From the XRD scans of samples from the ultrasonically-cleaned TEC 15 batch we concluded that no peaks were found that were not identified as SnO_2 and CdS (41-1049), with the possible exception of a small peak at 80.6° on one sample. From scans of annealed CdS/SnO_2 substrates of the

other types (scrubbed TEC 15, Asahi, and TEC 8) it was concluded that all peaks were identifiable as SnO_2 and hexagonal CdS.

3.1.11.2 Small-spot OBIC

Jason Hiltner and Jim Sites of CSU provided results of their small-spot induced-current characterization of two of our cells. Using a 20 μm spot and a 1 μm spot, the cells we sent showed remarkably uniform photocurrent (maximum decrease was 4% for the 1 μm spot size). While this would seem to counter the conclusions regarding cell non-uniformity in section 3.1.7, the cells analyzed had relatively high efficiency while non-uniformity might only be a significant factor in lower efficiency cells; also the short-circuit current measurement of the small-spot OBIC may not be very sensitive to non-uniformities which influence V_{oc} more than J_{sc}. To test these conclusions, cells with lower performance will be sent for the characterization in Phase III.

3.2 Reliability Verification and Improvement

3.2.1 Accelerated-test and Measurement-systems Development

To the extent that they can be correlated with field performance, accelerated-life tests (ALTs) are necessary to be able to set warranties and to be able to make process changes with confidence. However, even without proven correlation, ALTs can be valuable because i) a failure mechanism in an ALT that is not currently seen in the field could be a problem later if some unknown protector is lost, ii) improved performance of cells in ALTs could lead to cost savings by reducing encapsulation or other requirements otherwise needed to protect performance, and iii) the fact that something changes in cells with ALTs (including improvement in performance in some cases) is an important "window" into cell operation and could thus lead to better conceptual and numerical models and higher performance.

3.2.1.1 Light-soak Equipment Development

A new environmentally-controlled light soak was designed and constructed. The system gives the ability to light soak up to 60 samples (10 cm x 10 cm each) at controlled temperatures (from ~50ºC to ~110ºC) with a controlled ambient (air or nitrogen). Temperature control is performed via gas heating and cooling -- heating is done with in-line coil heaters and cooling is done via heat exchangers connected to a chiller unit. The system is shown in Figure 3-13.

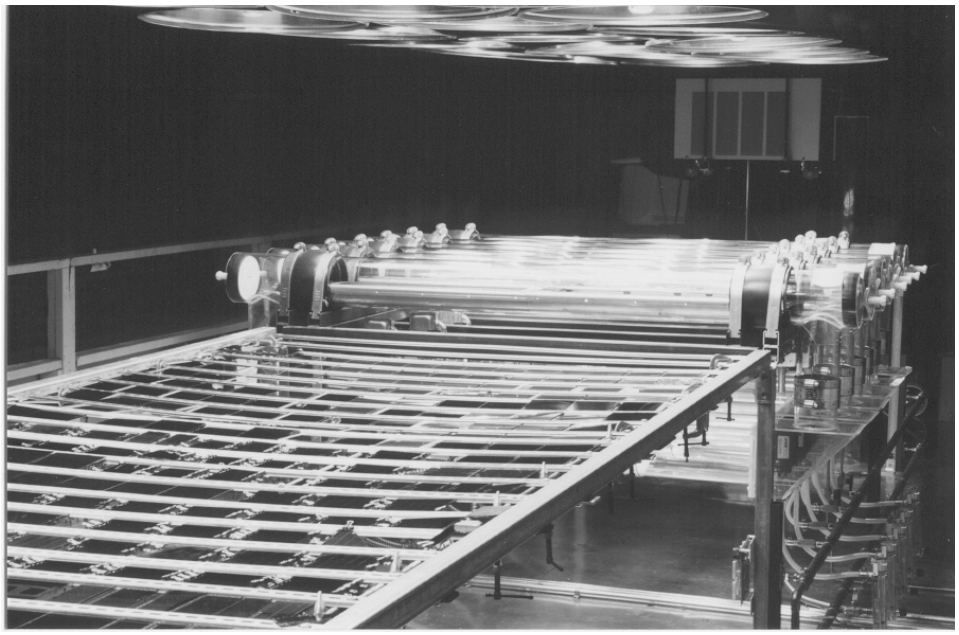


Figure 3-13. Environmentally-controlled light-soak station.

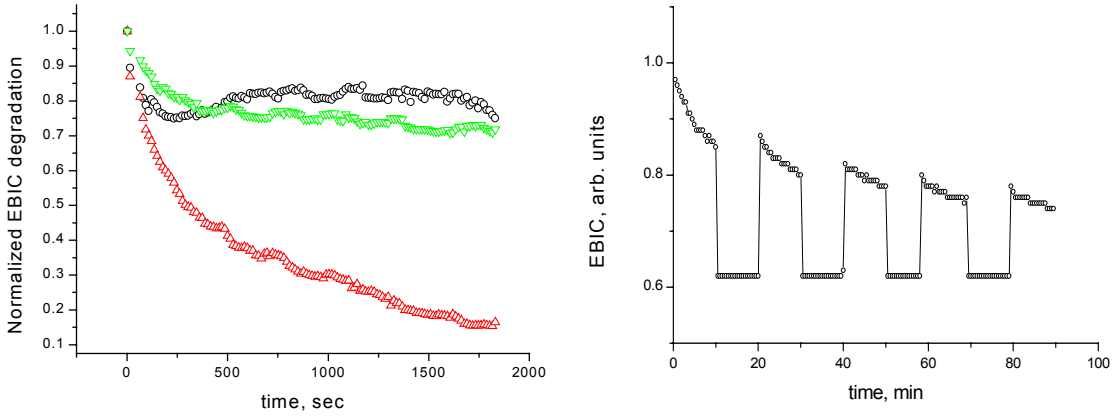
3.2.1.2 Laser-light Soak Technique and System Development

Laser illumination of small cells was explored as a potential high-acceleration-factor ALT. A first attempt used a small multi-line argon laser, but it was found to produce only about 50 sun illumination of a 0.87 mm^2 cell, and due to the multi-band nature of the laser (488-514nm), only about 30% of the light contributed to the photovoltaic effect. In order to get much higher intensity, a 808 nm IR diode laser system capable of producing over 200 mW was constructed. By focusing the laser on a 0.87 mm^2 cell, an illumination of ~130 suns is achieved, but considering that almost all of the photons are absorbed in the active portion of the cell, an illumination of ~400X is achieved compared to 1 sun intensity with an AM1.5 spectrum. Preliminary results indicate that 1 day laser-soak may give similar degradation to 56 days of 65°C light soak. While much work is still needed, this result is encouraging because laser-light soak might provide a very-high acceleration test for at least one failure mode.

3.2.1.3 EBIC Accelerated-test Development

Planar EBIC (Electron-beam-induced current) was also explored as a high-acceleration factor screening test. The EBIC technique was described in section 3.1.3 along with non-time-dependent results. In section 3.1.7 some EBIC results were used in support of modeling of non-uniformity. Some of the results and implications of electron-beam induced degradation will be discussed in this section, with additional details in a paper submitted (and accepted for publication) to the *Journal of Applied Physics* (R. Harju, *et al.*).

In general, the EBIC signal exhibits considerable variability between different spots on the same sample and between samples of different recipes. Figure 3-14a shows a typical observed EBIC decay measured in three samples of different recipes, two of them showing a remarkable stability. To maximize the observed effects in this study we concentrate on the least stable recipes.



(a) (b)

Figure 3-14. EBIC decay for (a) 3 different samples with different processing parameters, and (b) for one sample showing partial reversibility.

To study the reversibility of the e-beam induced degradation we used a time-modulated e-beam. When the beam is turned off the current drops a certain value with any transient effects appear to have time constants less than 1 minute. As can be observed in Figure 3-14b, the EBIC decay is partly reversible.

Our phenomenological model relates the above-described phenomena to changes in the semiconductor absorber layer. We assume that the observed decay of the EBIC signal reflects changes in the charged-carrier concentration caused by e-beam induced defects. We postulate that new defects appear in response to extra carriers (electrons and/or holes). The same mechanism of defect creation may be responsible for the phenomenon of self-compensation that makes it impossible (or very hard) to dope the materials under consideration. Indeed, because there is no difference between the charge carriers brought into the system by radiation and doping, the latter will trigger defect creation as well. In the simplest approximation the defect generation rate dN/dt is taken to be linear in the charge carrier concentration n:

$$\frac{dN}{dt} = \alpha n - \beta N \qquad (3.2.1.2\text{-}2)$$

Here the last term represent the process of defect annihilation; α and β are material parameters that are in general temperature dependent and may be also impurity dependent. Because the electron kinetics is relatively fast (as compared to that of the defects) we write the corresponding balance equation in the quasi-stationary approximation:

$$G - \gamma N n = 0 \qquad (3.2.1.2\text{-}3)$$

where G is the electron-hole generation rate and γ is the recombination constant. We have chosen here the recombination rate to be linear in electron concentration, which is a typical case in semiconductors.

The solution to Eqs. (2) and (3) can be obtained in a closed form. When the time is relatively short ($\beta t << 1$) the equation for n simplifies to the form

$$n = const + \frac{G}{\gamma N_0}\frac{1}{\sqrt{1+t/\tau}},\ \tau \equiv \frac{1}{2\beta}\frac{N_0^2}{N_\infty^2 - N_0^2} \qquad (3.2.1.2\text{-}4)$$

where N_∞ is the limiting concentration of defects after infinitely long exposure to irradiation, and N_0 is the initial concentration of these defects. Eq. (4) is convenient for fitting the experimental results. In the case of considerable changes the characteristic decay time τ is shorter by the factor of $(N_0/N_\infty)^2 << 1$ than the annealing time $1/\beta$. Therefore Eq. (6) can describe a strong change in concentration ($t/\tau >> 1$) in the domain of its applicability $\beta t << 1$, that is far from saturation. Note that in addition to defect accumulation the above equations describe defect annealing, which formally corresponds to the case of $N_0 > N_\infty$, reflecting the situation when radiation is decreased or stopped.
Most of the data on EBIC decay versus time can be surprisingly well approximated by the temporal dependence in Eq. (4). Fitting various curves gave characteristic true (under the beam) decay time τ ranging from 0.3 to 3s.

3.2.1.4 Simulator Improvements

High-volume manufacturing and high-quality monitoring of module performance require repeatable and accurate solar simulators. This reporting period we began procurement of two new solar simulators for production (one for submodules and one for encapsulated modules) and one simulator with advanced filtering and class-A uniformity. The technical support for the procurement specification was done under the subject contract. The production systems have been delivered and are undergoing final modifications for integration in the manufacturing line.

All three simulators use continuous-illumination xenon-lamps and can accommodate 60 cm x 120 cm modules. The decision to use continuous simulators was driven in part by the observation (reported in detail in our first quarterly report of Phase II) that the modules that we delivered to NREL last year measured on average 6% lower on a pulsed simulator than a continuous simulator and outdoor measurements (6.96% on Spire pulsed, 7.42% on NREL Spectrolab continuous, 7.4-7.5% on NREL outdoor system, and 7.26% on old First Solar continuous). The inaccurate readings from the pulsed simulator are likely the result of trap-states in the semiconductor layers. Pre-illumination or an extended-pulse simulator would likely solve this measurement problem, but continuous illumination was chosen as the highest-confidence approach for a fast scale-up to high-volume manufacturing.

3.2.2 Documentation of Reliability of Devices, Modules, and Arrays

3.2.2.1 Field Performance

Last year we reported that the 1 kW array mounted at NREL provided the best documentation of the reliability of modules that had been manufactured by Solar Cells,

Inc. (First Solar). The array, which consists of 24 modules installed in March 1995, is maximum-power tracked and is closely monitored. During this reporting period we received data from NREL staff indicating some drop in system performance. However, measurements taken in August 2000 showed that the modules are performing slightly better now when they were installed. Analysis is being done by NREL staff to determine if the drop at the system level was the result of an inverter malfunction.

Since the data obtained in August 2000 is the best documentation of reliability, it is included here even though it was obtained during Phase III of the contract. Measurements taken by NREL staff are shown in Table 3-2.

Table 3-2. Performance of modules made by SCI in the 1 kW array at NREL.

	3/15/95 Spire	3/23/95 SOMS	4/1/95 SOMS	6/95 SOMS	8/7/00 Spire	8/8/00 SOMS
Average efficiency of all modules (# *modules measured*)	6.95 *(all)*	*7.09 (17)*	*7.07 (19)*	*7.02 (8)*	7.17 *(all)*	7.29 *(all)*
Change compared to 3/15/95:	0%	*2%*	*2%*	*1%*	3%	5%
Standard Deviation of efficiency:	0.47	0.20	0.25	0.39	0.54	0.63
Avg. for modules measured 3/23/95:	6.86	7.11	7.12		7.06	7.15
Avg. for modules measured 6/95:	6.75		6.96	7.01		7.12

Between the time of installation and the measurement on 8/7/00, one module was replaced due to accidental breakage (module ID#15225, which was measured to be 6.85% efficient by SOMS in April 1995, had the back glass broken by impact -- it was replaced by module ID#12504, which was measured to be 6.96% efficient on 8/7/00). As can be seen in the table above, simulator and spectrally-corrected outdoor measurements show the average efficiency of the modules to be ~3% higher than when the modules were fielded over 5 years ago. Seven of the 24 modules did measure lower in 2000 than in 1995, with the largest drop being 9% and the average drop of the 7 being 4%. Despite these changes, mismatch in the strings of the array was essentially unchanged. We consider the results for this array significant because it demonstrates, with a high degree of measurement confidence, field stability for a period of over 5 years.

3.2.2.2 Accelerated Life Tests

The IV measurements for the second round of stability tests for the CdTe National Team were completed. The purpose was to determine ALT behavior of cells made with various back contact schemes (by several Team members) on First Solar CdTe substrates. A total of 451 cells were stressed, with the number of cells stressed at stress conditions shown in Table 3-3. "OC" refers to open-circuit-bias light soak with the cell temperature and ambient specified. "R" refers to light soak with a resistive load so that the bias is somewhat near the maximum power point. "SC" refers to light soak with a short circuit bias. "Dark" refers to stress in the dark (no bias applied). All light soak was done under metal-halide lights with approximately 0.7 suns intensity. The duration of the stress was 56 days which was then followed by 7 days rest (25ºC dark) before final measurement.

Table 3-3. Number of cells stressed at each stress condition (e.g., 135 cells light soaked at open-circuit bias in an air ambient with a cell temperature of 65°C).

	Light soak with __ bias:			
Cell temp., ambient	OC	R	SC	Dark
65°C, air	135	28	27	31
100°C, air	33	24	22	30
65°C, N_2	17	9	9	0
100°C, N_2	24	15	12	35

The results for each type of cell, as an average of all stress condition, are shown in Table 3-4. "CSM" refers to cells made at Colorado School of Mines, "IEC" refers to cells made at the Institute of Energy Conversion with "0.3Cu" referring to 30% of the normal Cu level in their contact, "USF" refers to cells made at the University of South Florida, and "UT" refers to cells made at the University of Toledo. Note that none of the cells included in the table were made with First Solar contacts. The results for each stress condition, as an average of all cell types, are shown in Table 3-5.

Table 3-4. Results by cell type (average of all stress conditions). (Note: R_{oc} is the resistance at open circuit which is ≈ the series resistance, and R_{sc} is the resistance at short circuit which is ≈ the shunt resistance).

	Efficiency			V_{oc}			% Change in___:			
Cells from:	Start	End	%Δ	Start	End	%Δ	J_{sc}	FF	R_{oc}	R_{sc}
CSM	7.7	5.9	-21	818	783	-4	-6	-14	148	-26
IEC (0.3Cu)	7.6	5.7	-24	789	725	-8	-7	-11	101	-18
IEC (Cu)	8.6	5.9	-30	806	732	-9	-9	-17	84	-57
USF (Wet-$CdCl_2$)	9.2	4.8	-46	815	607	-25	-5	-29	79	-58
USF (Vapor $CdCl_2$)	9.7	6.3	-35	827	646	-22	-2	-23	72	-5
USF (ZnTe)	8.7	6.7	-22	813	749	-8	-4	-13	48	-7
UT (ZnTe:N/ Au)	7.0	5.6	-19	727	664	-8	-2	-10	20	-46
UT (ZnTe:N/ Ni)	7.4	6.8	-8	694	668	-4	0	-4	91	-54
Average of these	8.2	6.0	-26	786	697	-11	-4	-15	80	-34

Table 3-5. Results by stress type (average of all cell types)

	% Change in Effic.					% Change in V_{oc}					% Change J_{sc}				
Stress:	OC	R	SC	D	Avg	OC	R	SC	D	Avg	OC	R	SC	D	Avg
65°C air	-38	-23	-17	-10	**-22**	-14	-7	-6	-2	**-7**	-8	-4	-3	-1	**-4**
100°C air	-42	-34	-23	-12	**-28**	-19	-15	-7	-2	**-11**	-6	-5	-6	-1	**-4**
65°C N_2	-19	-10	-16		**-15**	-6	-3	-4		**-4**	-5	-5	-8		**-6**
100°C N_2	-39	-29	-18	-10	**-24**	-19	-19	-7	-3	**-12**	-3	-2	-1	2	**-1**
Average	**-35**	**-24**	**-19**	**-11**	**-22**	**-15**	**-11**	**-6**	**-2**	**-9**	**-5**	**-4**	**-4**	**0**	**-4**
	% Change in FF					% Change in R_{oc}					% Change in R_{sc}				
65°C air	-24	-15	-10	-8	**-14**	191	82	45	38	**89**	-60	-28	-13	-15	**-29**
100°C air	-26	-21	-14	-9	**-18**	199	103	76	65	**111**	-57	-24	-19	-35	**-34**
65°C N_2	-9	-3	-4		**-6**	47	17	17		**27**	-49	5	-9		**-17**
100°C N_2	-25	-16	-12	-8	**-15**	88	42	24	50	**51**	-60	-6	25	-16	**-14**
Average	**-21**	**-14**	**-10**	**-8**	**-13**	**131**	**61**	**41**	**51**	**69**	**-57**	**-13**	**-4**	**-22**	**-24**

The results of table 3-5 show that, on average, the severity of stress from most to least was OC-light soak, R-load-light soak, SC-light soak, and dark oven. It can also be seen that stress in nitrogen gave only slightly less degradation than stress in air and that stress at 100°C resulted in ~50% more degradation than stress at 65°C. The results by temperature and cell type are given in Table 3-6. The variation gives an indication of the high dispersion of results that was seen for most sample sets.

Table 3-6. Ratio of degradation under 100°C stress to degradation under 65°C stress for each cell type (degradation of efficiency under OC-light-soak-stress at 65°C and 100°C shown in first two columns for reference).

	Efficiency						V_{oc}			
	OC stress			R	SC	Dark	OC	R	SC	Dark
	65°C	100°C	Ratio	Ratio	Ratio	Ratio	Ratio	Ratio	Ratio	Ratio
CSM	-63%	-27%	0.4	0.8	0.3	0.7	1.2	3.3	1.8	3.9
IEC 0.3Cu	-34%	-43%	1.2	1.7	3.1	1.1	1.0	0.8	3.5	1.5
IEC Cu	-49%	-43%	0.9	1.5	2.6	0.7	0.9	2.8	1.6	0.2
USF wet	-63%	-77%	1.2	1.4	1.5	3.4	1.6	1.9	0.6	0.9
USF Vapor	-58%	-71%	1.2	2.5	2.0	3.1	1.3	6.1	0.6	5.2
USF ZnTe	-25%	-34%	1.4	7.2			1.9	-12		
UT (ZnTe:N/ Au)	-29%	-36%	1.3	1.2	0.9	0.3	2.7	1.3	1.5	6.0
UT (ZnTe:N/ Ni)	-11%	-10%	0.9	1.1	0.6	-0.2	3.6	2.2	1.7	0.2
Average of these	-41%	-43%	1.1	2.2	1.6	1.3	1.8	0.8	1.6	2.6

In addition to the stress tests done for the National CdTe Team reported above, other accelerated tests were done to investigate input variables that influence stability and to investigate failure mechanisms that might be stimulated under accelerated testing. For example, light soak of aqueous-$CdCl_2$ and methanol-$CdCl_2$-treated samples was done to verify that the change to aqueous-$CdCl_2$ would not decrease the stability of products (see section 4.2.1 for information on the benefits of the aqueous process). In one experiment, minimodules (48 cm^2 aperture area) from aqueous- and methanol-$CdCl_2$ treated submodules were light soaked. Over the 14 minimodules of each type, the initial efficiency was 7.54% and 7.44% for the aqueous- and methanol-treated samples, respectively. After 56 days of continuous 65ºC light soak with a resistive load, the efficiency change was +9% and +5% for the aqueous- and methanol-treated samples, respectively. After 56 days of continuous 65ºC light soak at open circuit the efficiency change was -4% and -14% for the aqueous- and methanol-treated samples, respectively. Light soak for 56 days at 100ºC at open circuit showed no difference between the two treatments (-9% for both).

Light soak of modules further confirmed that the aqueous-$CdCl_2$ could result in good accelerated-test performance. Figure 3-15 is a plot of the performance of two aqueous-$CdCl_2$-treated modules in light soak (module temperature ~65C) for a period of ~8 weeks.

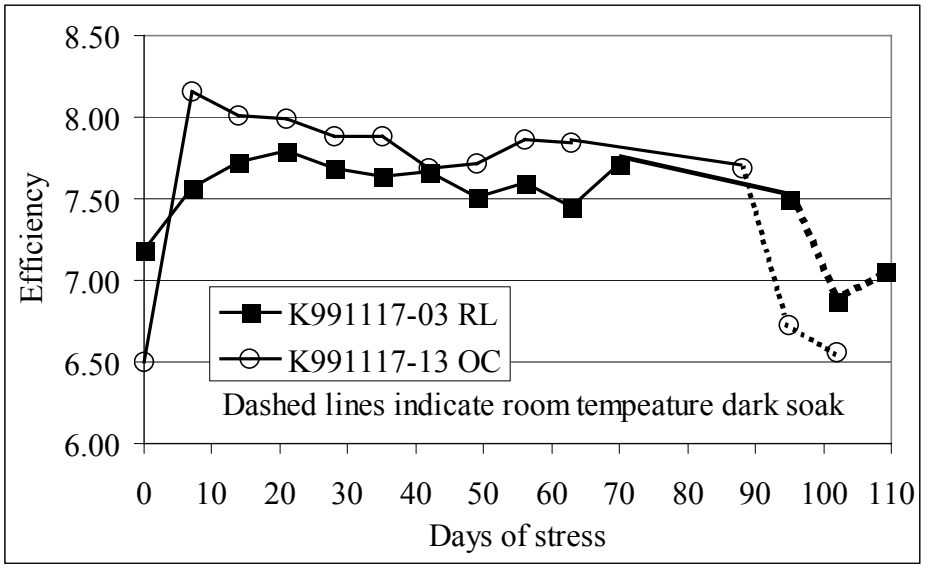


Figure 3-15. Module efficiency vs. days of stress for 2 modules in light soak at ~65ºC. One module (OC) was in light soak with an open-circuit bias. One module (RL) had a resistive load which placed the bias somewhere near the maximum power point during light soak.

3.2.3 Failure-mechanism Research and Mitigation

In both outdoor data and light-soak tests there are examples of cells and modules that have received very long term exposure with no degradation or even with improvement of performance; thus, it is clear that degradation processes in our devices can be avoided -- one of our key objectives is to determine the degradation modes and mechanisms so that we can insure that the stability will be excellent every time.

Several items in the characterization section of this report (3.1) are targeting to understanding device performance, which includes how cells operate and what might change with stress. Additional work includes the following.

3.2.3.1 Temperature Effects

An experiment was conducted to separate the effects of heat and light on cell degradation (separating failure modes is important for the testing of simple analytical models and the development of failure-acceleration factors). Cells that were known to be susceptible to degradation were light soaked at 65°C and 0°C and were placed in the dark at 65°C and 0°C. The results indicated that heat alone can result in an increase in the cell series resistance (presumably from an increase in the back contact resistance) while the combination of heat and light is necessary for appreciable degradation of the open circuit voltage. Additional information on the effect of temperature during light soak emerged from several other experiments, including the National CdTe Team set and the $CdCl_2$ set which were discussed in section 3.2.2.2.

3.2.3.2 Process Variable Identification

Screening and optimization experiments have indicated that process-variables in the $CdCl_2$ and back-contact steps can affect device stability. For the $CdCl_2$ process there was lower light-soak stability for treatments significantly below or above the optimum temperature range. For the back contact process, several variables have been identified that influence short-term light-soak performance.

3.2.3.3 Contact Research

Because contact formulation has been identified as the most important variable in First Solar cell stability, and because alteration of contact formulation could potentially raise module efficiency and lower production costs, alternative contacts were investigated. Work continued on the all-dry, sputtered-IFL contact briefly discussed in the Phase I report which has shown excellent stability, even under open circuit, high-temperature light soak.

4. Environmental, Health, and Safety

4.1 General Program

Work on the general EH&S program was primarily supported by internal and PVMaT funds. Success of the program continued in this phase with no additional emissions predicted over the extremely low levels described in last year's annual report (which was at the "De Minimus" level that did not require permitting). Additionally, cadmium medical monitoring of First Solar employees has continued to show that the ES&H protocols are effective for employee protection. Details were written in a paper to be presented at the IEEE Photovoltaic Specialists Conference (J. Bohland, *et al.*).

4.2 Process and Equipment Improvements

4.2.1 Aqueous $CdCl_2$

In Phase I, the organic emissions from the existing wet-$CdCl_2$ process were identified as the only emissions from the new plant that would require permitting if the process was scaled to high-volume manufacturing. $CdCl_2$-in-water was thus investigated as an alternative to the existing $CdCl_2$-in-methanol process as a way to reduce emissions and achieve the goal of a "zero emissions" plant. Due to the higher solubility of $CdCl_2$ in water compared to methanol and the lower-wetting acting of the aqueous solution, some modifications of the application approach were required. Before the modifications were made, the aqueous process could result in less-uniform and less consistent products. After the change to a spray/roll process with lower volume of application, which is now used in the manufacturing line, tests showed that the aqueous process was, if anything, slightly superior in performance to the old process. The largest controlled-run comparison of modules resulted in 0.2% (absolute) higher efficiency for the aqueous process. Light soak tests on aqueous- and $CdCl_2$-treated samples also showed, if anything, slightly better performance of the aqueous process, as discussed in section 3.2.2.2.

4.2.2 Edge Delete

Part of module finishing involves the removal of the outer ~1cm of films to prevent edge shunting and moisture ingress in encapsulated modules. In Phase I we reported improvements to a sand-blasting technique that resulted in improved operator safety and a reduction of hazardous waste. We also reported that a grinding-wheel edge delete can be used in place of the sand-blasting with a further reduction in waste and improvement in module quality. In Phase II it was determined that a fine diamond wheel can provide a clean and precise edge delete without the clogging problems found with 3M composite wheels. The project was transferred to the engineering group and commercial grinding-wheel systems were ordered. At this time, problems maintaining the correct force on the wheel have delayed introduction into production. The sandblast technique that was improved in Phase I will continue to be used until the mechanical problems of the system can be resolved.

Summary and Plans

Principle achievements during Phase II include the following:

- Completed a new semiconductor deposition system with a throughput of four plates per minute (each 0.72 m^2) and neared completion of a module-finishing line with a throughput of one 0.72 m^2 module/min.
- Produced over 12,500 CdS/CdTe-coated plates as part of pilot production.
- Transferred pilot production to the new deposition system, including the gathering of data on film characteristics. Spatial mapping of CdS thickness of a plate from the new coater showed a standard deviation of only 1.3% in the down-web direction and 7% in cross-web direction.
- Verified heat-treatment profiles and identified vapor delivery issues for module-sized vapor-$CdCl_2$ system.
- Developed a new laser-scribing technique that provides linear scribing speeds of 3 m/s, thus enabling the scribing for a scribe set to be done at one plate/min with one laser, thus reducing system downtime and costs compared to a multi-laser approach.
- Made significant progress towards high-efficiency modules made with buffer layers and thin CdS, specifically: i) identified and tested novel precursors for buffer films, ii) designed and built small-scale and module-scale equipment for atmospheric-pressure chemical-vapor deposition (APCVD) of buffer layers, and iii) made cells with NREL-verified efficiency as high as 13.2% on commercially-available SnO_2-coated float glass by incorporating new APCVD buffer layer.
- Increased capabilities in characterization (spectral response, EDS, and temperature-dependent CV/CF over the range 0.001 Hz - 100 kHz), accelerated-testing (EBIC, laser, and environmentally-controlled light soak), and in-situ monitoring (substrate temperature and CdS thickness).
- Made significant progress in characterization and modeling, including i) proposed micro-non-uniformity as the cause of large suppression of V_{oc} in some cells, ii) modeled the effect of non-uniformity and developed an analytical solution based on the mean-field approximation and an analytical solution to shunt screening, iii) used PL to ascertain electronic states of Cu in CdTe films and cells, and iv) characterized contact resistance, grain boundaries, and other cell and module properties
- Verified field stability to a period > 5 years with further analysis NREL array.
- Completed 2nd round of accelerated life tests, including tests of alternative processes at First Solar and cells by National CdTe Team members.
- Replaced methanol-based $CdCl_2$ step with an aqueous based process and thereby retained “De Minimus” emissions rating for the new production facility.

Plans for Phase III include the following:

- Explore process parameters for new production coater and production line and thereby improve product uniformity and reproducibility.
- Advance understanding of device operation through characterization and analysis.
- Provide modules with alternative contacts and variations in other process parameters for field testing.
- Demonstrate additional gains in module efficiency through improved uniformity of processes in concert with thin CdS and a buffer layer.

Glossary of Abbreviations

ALT	Accelerated life test
APVCD	Atmospheric-pressure chemical-vapor deposition
C	Capacitance
Cd_i	Interstitial cadmium
Cu_{Cd}	Copper on a cadmium site
Cu_i	Interstitial copper
DAP	Donor-acceptor pair
DSP	Digital signal processor
EBIC	Electron beam induced current
EDS	Energy dispersive spectroscopy
EVA	Ethylene vinyl acetate
F	Frequency
FD	Finite difference (numerical solution)
FF	Fill factor
FSEC	Florida Solar Energy Center
G	Conductance
IFL	Interfacial layer
I-V	Current-Voltage measurement
J_{sc}	Short circuit current
LED	Light emitting diode
LOF	Libbey-Owens Ford
MW_p	Peak megawatts (at standard conditions) of PV produced
NREL	National Renewable Energy Laboratory
OBIC	Optical beam induced current
OC	Open circuit (bias during stress)
PL	Photoluminescence
PV	Photovoltaics
PVMaT	Photovoltaic Manufacturing Technology Program
PVUSA	Photovoltaics for Utility Scale Applications program
RL	Resistive load (bias during stress - near maximum power point)
R_{oc}	Resistance at open circuit (~series resistance)
R_{sc}	Resistance at short circuit (~shunt resistance)
SC	Short circuit (bias during stress)
SIMS	Secondary-ion mass spectroscopy
SnO_2:F	Flourine-doped tin oxide
TCO	Transparent conducting oxide
V	Voltage
V_{Cd}	Cadmium vacancy
V_{oc}	Open circuit voltage
VTD	Vapor transport deposition

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13. ABSTRACT *(Maximum 200 words)*
Results and conclusions from Phase II of a three-year subcontract are presented. The subcontract, entitled "Technology Support for High-Throughput Processing of Thin-Film CdTe PV Modules," is First Solar's portion of the Thin-Film Photovoltaic Partnership Program. The research effort of this subcontract is divided into four areas of effort: 1) process and equipment development, 2) efficiency improvement, 3) characterization and analysis, and 4) environmental, health, and safety. As part of the process and equipment development effort, a new semiconductor deposition system with a throughput of 3 m^2/min was completed, and a production line in a new 75,000 ft^2 facility was started and is near completion. As part of the efficiency-improvement task, research was done on cells and modules with thin CdS and buffer layers as way to increase photocurrent with no loss in the other photovoltaic characteristics. A number of activities were part of the characterization and analysis task, including developing a new admittance spectroscopy system, with a range of 0.001 Hz to 100 kHz, to characterize cells. As part of the environmental, health, and safety task, the methanol-based $CdCl_2$ process was replaced with aqueous-$CdCl_2$. This change enabled the retention of a "De Minimus" level of emissions for the manufacturing plant, so no permitting is required.

14. SUBJECT TERMS
photovoltaics; PV modules; high-throughput processing; thin-film CdTe; process and equipment development; efficiency improvement; characterization and analysis; environmental health and safety; semiconductor deposition system; CdS ; $CdCl_2$

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