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Subcontractor Report

PVMaT Cost Reductions in the EFG High-Volume PV Manufacturing Line

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August 1998–December 2000

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Billerica, Massachusetts

National Renewable Energy Laboratory

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Summary

The PVMaT 5A2 program at ASE Americas is a three year program, which addresses topics in development of manufacturing systems, low cost processing approaches, and flexible manufacturing methods. The three-year objectives are as follows:

- Implementation of computer aided manufacturing systems, including Statistical Process Control, to aid in electrical and mechanical yield improvements of 10%
- Development and implementation of ISO 9000 and ISO 14000
- Deployment of wafer production from large diameter (up to 1 m) EFG cylinders and wafer thicknesses down to 95 microns
- Development of low damage, high yield laser cutting methods for thin wafers
- Cell designs for >15% cell efficiencies on 100 micron thick EFG wafers
- Development of Rapid Thermal Anneal processing for thin high efficiency EFG cells
- Deployment of flexible manufacturing methods for diversification in wafer size and module design

In the second year of this program, the significant accomplishments in each of three tasks which cover these areas are as follows:

Task 4 - Manufacturing Systems: Statistical Process Control (SPC) charting has been introduced in a number of places in the ASE Americas' manufacturing line, including measurement of laser power, spreading resistance, and interconnect bond strength Design of Experiment matrices have continued on various process steps in the cell line to optimize AR coating and metal firing conditions, writing of Documentation and Statistical sections of ISO 9000 procedures have been more than 80% completed, and a Gap Analysis for ISO14000 has been carried out. Cell efficiency has continued to improve.

Task 5 - Low Cost Processes: Solar cells of 13% efficiency and with thicknesses down to 150 μm have been made on 6 cm x 6 cm area wafers cut from 50 cm diameter EFG cylinders. A new non-acid based etching process has been developed and is being introduced into manufacturing, it will strengthen the wafer and reduce silicon acid etching load and waste products. Initial trials of the high speed CO_2 laser were not satisfactory in manufacturing and we are evaluating possibilities of obtaining alternate CO_2 lasers. We have completed evaluation of lasers for cutting of thin wafers with reduced levels of damage and have selected a candidate for manufacturing line trials. We are using a model developed for heat transfer to help in design of new hot zones for reducing stress in thin EFG tubes, and are starting to implement new diagnostic techniques for monitoring wafer properties to assist in this task. We have worked with Georgia Tech to optimize bulk EFG material lifetimes with Rapid Thermal Processing (RTP).

Task 6 - Flexible Manufacturing: Manufacturing of 10 cm x 15 cm EFG wafers has been brought up to full capacity. We have completed preliminary testing of an improved encapsulant with superior transmission and better lamination characteristics and are making plans to evaluate it in full scale manufacturing. We have extended our studies of field performance of modules to the AC module.

1. Introduction - PVMaT 5A2 Program Overview

We give here an overview of the progress made in the first year of a three-year PVMaT 5A2 program at ASE Americas. ASE Americas is currently engaged in a rapid scale-up of EFG PV manufacturing capacity. Wafer, cell and module capacity has grown fourfold in three years, from less than 1 MW/yr in 1994 to 4 MW/yr in 1997, and 8 MW of EFG wafer production furnaces were added in 1998. Current output is the equivalent to the manufacture of about 8 million 10 cm x 10 cm wafers annually. The EFG wafer manufacturing line has diversified so that both this previously standard area wafer and a larger 10 cm x 15 cm area wafer are now being produced. Building and infrastructure facilities are additionally completed to allow EFG wafer expansion to an annual capacity of 20 MW/yr. Planning has started for a further expansion of 8 MW to be completed in 2001. This rapid scale-up of EFG PV technology poses a number of technical and organizational challenges; we propose to attack the most essential of these challenges under PVMaT 5A2.

Technology improvements developed under PVMaT 2A (1992-1994) and PVMaT 4A2 (1995-98) were of critical importance in supporting the scale-up to commercial production. In the PVMaT 5A2 program at ASE Americas, we propose a multi-faceted technology development effort, which is aimed at implementing manufacturing line improvements to keep EFG PV products as low-cost PV leaders. We plan to introduce and integrate design, materials and processing improvements related to all major cost elements of the EFG PV module. These elements include new generations of EFG material growth processes and laser cutting technology, more efficient cell processing, and reduced cost module construction strategies, which match the key growing PV market applications. Under PVMaT 4A2, we demonstrated and developed EFG PV technology improvements in wafer manufacture aimed at better silicon feedstock utilization, improved purification for graphite to help raise solar cell efficiencies, longer EFG wafer furnace run-time approaches, and optimized laser cutting technology. In cell manufacturing, we installed data gathering and information tracking capabilities to support and allow demonstration and testing of Statistical Process Control (SPC) methodology, and demonstrated a low cost and environmentally advantageous glass etch process which dramatically reduces fluorine ion effluents. New module designs were developed and improved manufacturing methods were introduced. These have led to new product concepts. Advanced encapsulation technologies were evaluated for improving manufacturing yield and enhancing product field performance and lifetime.

In PVMaT 5A2, we will implement advances developed previously while we expand our manufacturing line. The higher capacity leverages the incremental advances and substantially enhances the competitiveness of EFG PV products. Specific tasks include implementation and utilization of SPC, and establishing a supporting system for data collection and documentation for processes (ISO 9000) and safety (ISO 14000), to cope with the large increase in manufacturing volume (Manufacturing Systems - Task 1). We plan to develop a new thin wafer technology using EFG cylinders, that have the potential to dramatically reduce the cost of EFG PV and x-Si PV products (Low Cost Processes - Task 2). We also will develop and introduce methods to cope with increased manufacturing process diversity – both in wafers and in modules – which will allow intermediate product (wafer and cell) and module field performance tracking to be used to improve manufacturing processes (Flexible Manufacturing - Task 6). These elements are considered to be cornerstones for capturing the full cost and technical improvements of EFG PV, and assure well-controlled, high-yield, high-volume production.

2. Task Objectives and Work in Progress

2.1 Task 4 - Manufacturing Systems

This task addresses efficient manufacturing management systems essential to achieving high-yields at high production volumes. We propose to implement process feedback, statistical process control, documentation procedures and ISO 14000 Certification. These manufacturing management systems improvements are absolutely essential to efficient, cost-effective manufacturing, and this task is a core activity of our PVMaT 5A2 work plan. The goal in pursuing these manufacturing management improvements is to incrementally lower costs, reduce waste and increase production output, and to lay a solid foundation for more substantial improvements made possible by implementation of the above-mentioned technology enhancements in high-volume production. Examples of such an infrastructure are statistical process control, total preventative maintenance, product quality enhancement, and industrial ecology.

Subtask 4.1 - Mechanical Yield Loss In the first year of the program, we focussed on improvement of cell efficiency in the EFG cell manufacturing line [1]. We achieved our program goal of demonstrating a 10% reduction in electrical yield losses by raising the cell efficiency in the manufacturing line to above 14%. This is discussed further in Subtask 4.2 below on SPC. This year we have initiated several programs to improve the mechanical yield and reach our program target of a 10 % reduction in losses in this area. One area of this is the development, testing and optimization of a plasma etch process for removing edge damage in wafers. It is reported under Subtask 5.1 below.

Year 2 Accomplishments In the electrical testing area, improvements in reliability and throughput were implemented in cell test equipment. The timing controls of the tester were reprogrammed to speed up the test cycle per cell by 10% and remove a bottleneck in throughput in this area. In the process, we were also able to correct some wiring deficiencies, which were resulting in test failures and fill factor measurement inconsistencies. Some of the improvements, including Fill Factor increases, sheet rho and metalization firing optimizations, are graphed in Figure 1 from Deliverable D-2.2.4, which shows a normalized plot of electrical yield from the start of the PVMaT 5A2 program.

Exploratory programs were started to develop new diagnostic equipment for various steps in the manufacturing line both to help R&D and also to assist the manufacturing operation. Two areas of diagnostics involve techniques already well understood and tested, which require the development of designs and manufacture of robust equipment for the manufacturing line. These are the fracture twist test in use in R&D at ASE Americas already for many years, and the pull strength test for solder bonds. In addition, there are a number of other pressing needs for diagnostic equipment, which will be pursued. We have already previously reported on efforts to qualify a diagnostic technique for residual stress measurements to help in crystal growth optimization. We have started to look at additional diagnostic tools both to help in SPC work and in development of low stress octagon and cylinder EFG systems. More specifically:

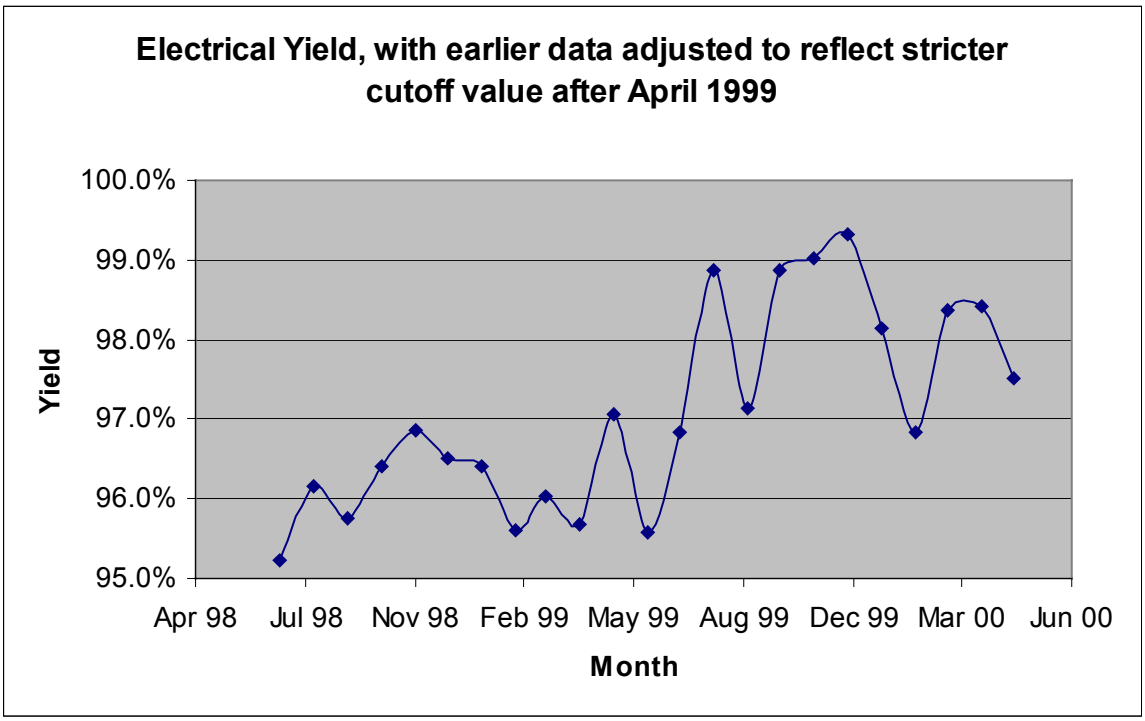

Figure 1. Plot of electrical yield since the start of the PVMaT 5A2 project

1. ***Crack detection*** Cracks may develop at any time during the processing from laser cutting on through to module lamination. Most often they do not extend more than a few mm or cm from a wafer edge or lead to fracture of the wafer or cell, but remain a potential source of failure further along in processing where the add-on costs increase. Under a lower-tier subcontract at the University of South Florida the resonance ultrasonic technique for crack detection will be investigated. We would like to have manufacturing diagnostics for crack detection at several points in the line: after laser cutting, during the cell processing, and in the interconnect and module areas. This may require more than one approach.
2. ***Flatness measurement – "buckle" monitor*** We have installed and are operating a set of capacitance sensors in the crystal growth furnace to provide traces of the surface profile of the growing tube. The flatness measurement reflects the extent of the stress acting on the tube during growth, and these sensors can measure deviations from flatness with a sensitivity of about 25 microns. By getting real time data on the deviations from flatness, we hope to be able to develop a feedback loop to temperature settings in the furnace so that we can attempt to correlate changes in operating conditions or furnace hot zone configuration to temperature fields and stress. We are also developing an on-line Fast Fourier Transform (FFT) capability in real time, and have contracted this problem to consultants.
3. ***Residual stress*** This is primarily needed to assist in stress reduction in crystal growth. Under a lower-tier subcontract at the University of South Florida, equipment was constructed and methods developed to provide maps of IR response of the wafers indicating areas of high strain. An example of a study of stress dependence on octagon (wafer) wall thickness is shown in Figure 2. In the crystal growth process, it is expected that the dislocation densities and residual stress will increase as the thickness of the tube wall decreases for a given external growth environment. This method of IR polariscopy had been evaluated for the tube because the temperature gradients driving the stress increase with decreasing crystal thickness. The IR polariscopy method also has been compared with other methods of stress

measurement and with dislocation mapping studies. Although the feasibility of using this technique on for measuring stress in EFG wafers is proven, additional work needs to be done to make IR polariscopy a practical diagnostic method for wafer analysis.

4. ***Photoluminescence lifetime mapping*** We have continued to explore the potential of room temperature photoluminescence (RTPL) as an on-line quality control tool. A measurement system has been installed at ASE Americas, and we are studying the behavior of defect bands that may be useful for reliable and fast identification of bulk quality of the University of South Florida. More details of this work are found in ref. [2].

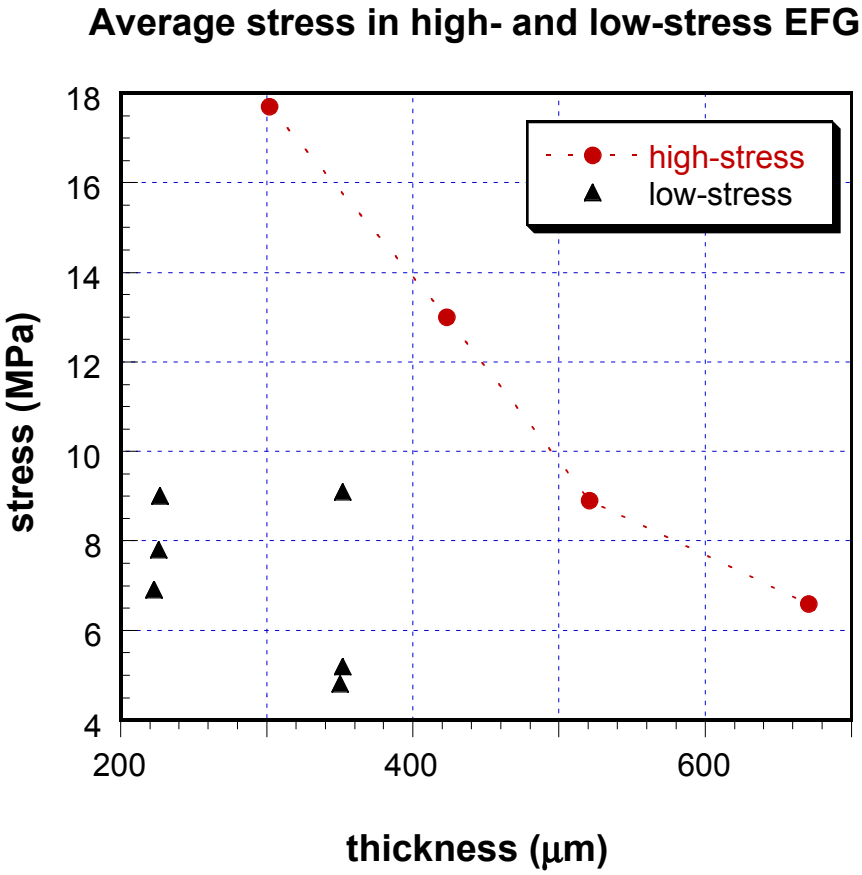

Figure 2. Residual stress as a function of EFG wafer thickness measured by IR polariscopy (Figure courtesy of S. Ostapenko, University of South Florida)

As described further in Subtask 5.2 below, we have developed a new plasma etch process to improve laser cutting edge damage removal and decrease acid use. We will be evaluating this process in the manufacturing line in the coming year to help in meeting both mechanical yield and waste remediation objectives of this program.

Subtask 4.2 - Statistical Process Control (SPC) This task of using SPC and DoE's to improve the manufacturing of solar cells at ASE Americas falls within the goal of providing and using *efficient* manufacturing management systems to achieve high yields of quality product at high production volumes. A basic concept in SPC is that "continuous improvement" is not haphazardly made, but is targeted in a prioritized manner, focusing on those areas whose output is most sensitive to the success of the final product. Improvements achieved throughout 1999 are shown in Figure 3.

Defining and redefining what the "key nodes" are for the processes used to manufacture a product are a continuous activity. ASE Americas has--through the use of DoE's— determined which areas are key nodes, then focused on SPC charting and the use of control action plans at these areas. Accompanying the Control Charts are "Control Action Plan's" (CAP's). These essentially are flowcharts, which define what the operator should do when the process has produced an out-of-control condition. Each CAP is being developed by engineering personnel with operational staff input. The CAP will then be executed by the manufacturing personnel on the floor. Before a control chart is implemented on-line, everyone using the chart is trained on how to use and read the chart, as well as how to follow the CAP. The CAP's developed include different actions for different conditions (i.e. out-of-control high vs. out-of-control low).

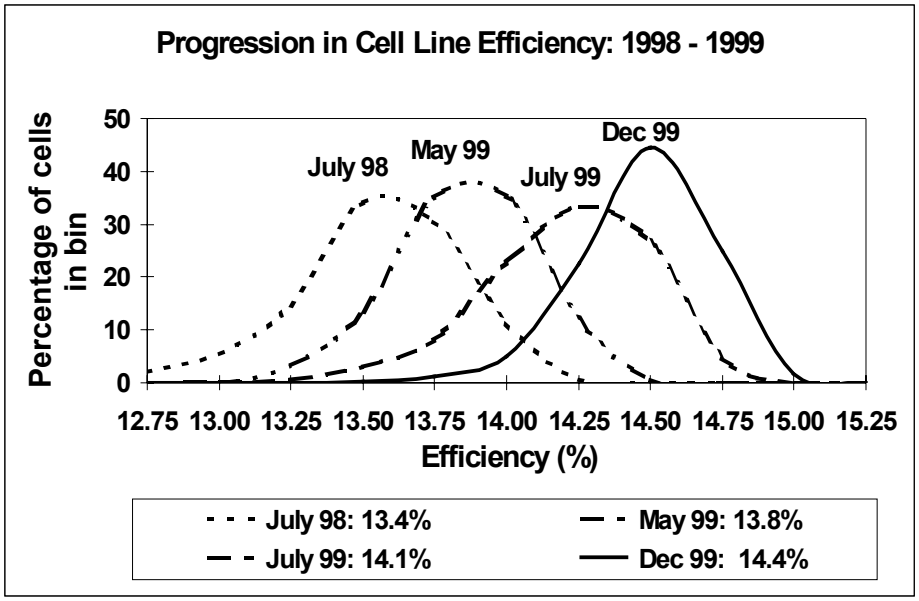

Figure 3. Improvements in cell efficiency for production lots throughout 1999

Year 2 Accomplishments We have continued to carry out Design of Experiments to identify the key nodes in the cell manufacturing. The work this year has included antireflection coating thickness, index of refraction and deposition process variables, cell sheet resistivity, and bulk wafer resistivity. More details of some of this work may be found in Ref. [3].

The implementation of control charts has been expanded to include several more process steps this year. In addition to the trial areas we initiated last year in sheet resistivity and busbar

area, we have now introduced additional charts in areas of short circuit current at cell test, interconnect bond strength, and laser flashlamp lifetime.

Subtask 4.3 - Flexible Manufacturing Manufacturing Systems implementation in the wafer and module areas include the definition, development and implementation of quality and management systems that are built on controlled documents and calibration standards that are traceable to primary and secondary standards. Metrics for equipment performance (uptime, repair time, waiting for parts, qualification time) will be developed and tracked in the new electronic database system. These systems will add stability to the manufacturing process and will be used to document acceptable ranges of variability of all key parameters, and enable systems to come on line in a controlled fashion.

Year 2 Accomplishments In the initial phase of this Subtask, a data collection system for our wafer fabrication department was installed. This encompassed the Crystal Growth, Laser Cutting, Silicon Etch, and Wafer Packing areas. The heart of the system is a Microsoft SQL Server, which collects information from computers along the 'spokes' of the network. These other computers include those on equipment itself, such as our crystal growth furnaces, and independent stations where operators enter information about group of wafers in progress, such as how many wafers entered and left a specific processing station such as the Si etch machine. Information is transferred along the regular network connections and cables, and the SQL server is instructed to either poll for certain information from computers along the network at specific times, or to receive information automatically sent from the remote computers. The user interface available within the SQL server software has been customized to allow production supervisors and engineers to access the information stored within the resulting database.

Subtask 4.4 - ISO 14000 Certification This work will formalize safety and environmental issues within a framework of acceptable practices and gain recognition for the photovoltaic industry for leadership in this area. This certification mandates that the manufacturing line be developed to be consistent with minimizing its effect on the environment through fundamental understanding of the chemical usage, waste and environmental impact of the manufacturing process. It also mandates a system to be developed that enables continuous improvement, training, and reporting on safety and environmental issues. We plan to use developments on the EFG manufacturing line as a template to structure and formalize our environmental concerns within the comprehensive and generic approach provided by ISO 14000.

Year 2 Accomplishments Initial work in this area consisted of working on the Documentation and Statistical sections of ISO 9000. At this juncture, we estimate that we have completed about 90% of the Documentation, Work Instructions and Document Control work required. A summary of the progress in given in the chart in Fig. 4. However, work in other areas has not progressed as well. The original internal company goal of achieving ISO 9000 certification in 2000 has not been met. This work mainly is not funded on the PVMaT program, but it will impact on the schedule of completion of tasks in ISO 14000 which is partly dependent on completion of ISO 9000. A Gap Audit was contracted out to a consultant and completed this year.

The objective of this audit is to assess the state of readiness of our facility to become ISO 14001 certified. A number of areas were singled out for their high compliance. This included our chemical storage, waste treatment and rooftop exhaust treatment. We are continuing to improve the database for baseline material and chemical usage information. Details of this work may be found in Ref. [4].

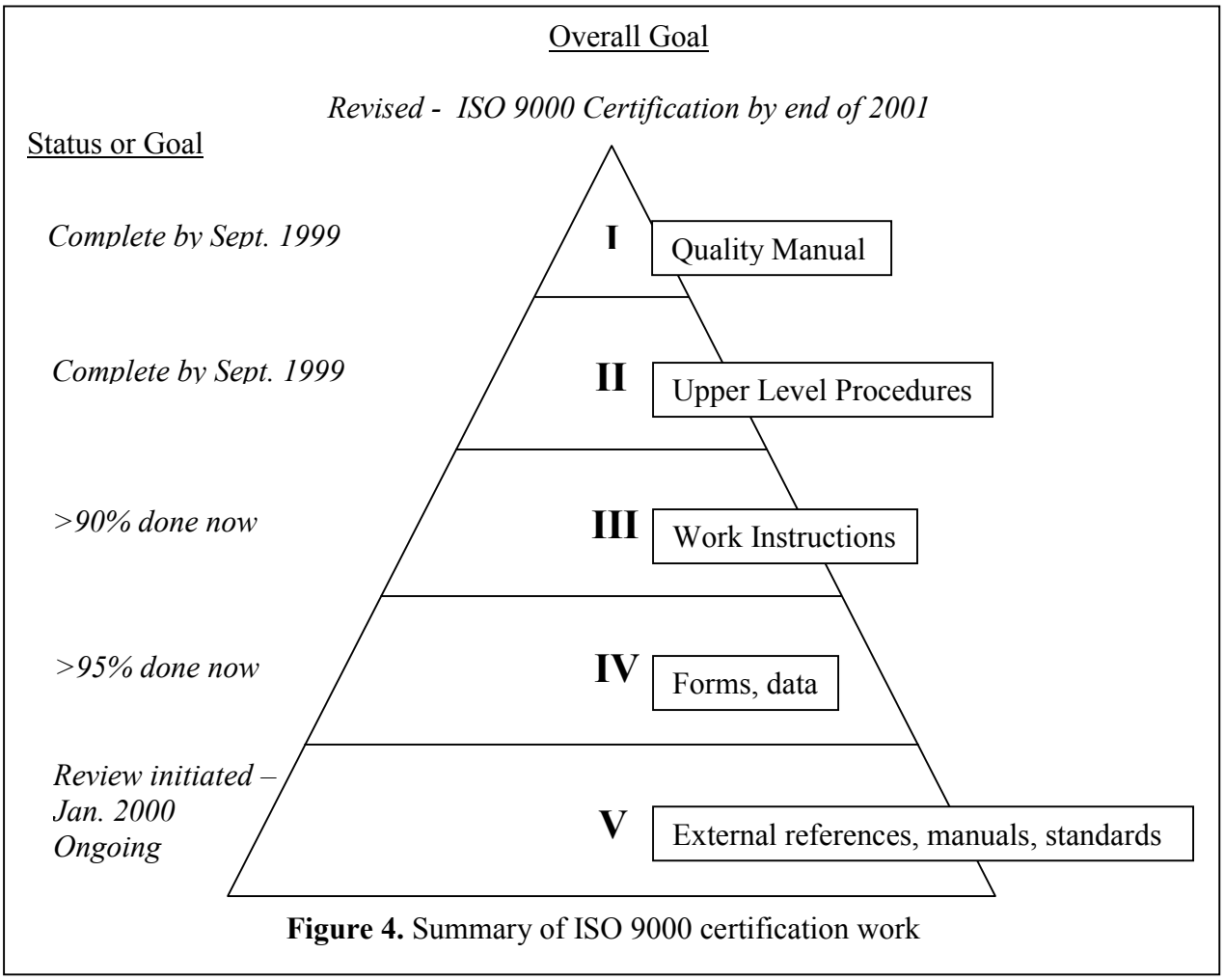

Figure 4. Summary of ISO 9000 certification work

The objective of this audit is to assess the state of readiness of our facility to become ISO14001 certified. A number of areas were singled out for their high compliance. This included our chemical storage, waste treatment and rooftop exhaust treatment. We are continuing to improve the database for baseline material and chemical usage information. Details of this work may be found in Ref. [4].

Cost reduction in Task 4 over the three year program will be achieved through decreasing the variability in products (wafers, cells, modules) and optimizing their performance. We expect to improve average rated cell efficiency by 5-10% (relative) by reducing the amplitude and duration of efficiency swings experienced in the past. We plan to stabilize machine performance

and enhance throughput at near the maximum capability of the line demonstrated on an interim basis in the past. This will reduce labor costs by 10% on average. The overall module cost reduction in manufacturing from such stabilization of operating conditions and achieving optimal values is expected to be about 10%. One of the main accomplishments in the second year toward these goals has been the ability to sustain the cell efficiency improvements in the manufacturing line and to reduce fluctuations.

2.2 Task 5 - Low Cost Processes

In this Task, we are working to develop and implement advanced EFG technology. We are in the process of testing a new generation of lasers which reduce as-cut wafer edge damage, deploying a very high speed laser in production, and deploying a plasma etch process to remove edge damage in place of acid. The latter will reduce etchant consumption, hence lower the volume of hazardous processing materials usage and waste generation.

We are also exploring higher-risk, higher-reward opportunities for radically reducing x-Si PV module costs through introduction of new processing and thinner wafers. We are investigating new cell processing approaches using Rapid Thermal Processing (RTP) techniques, and planning to develop manufacturing methods for wafers down to 100-micron thicknesses. We have met our objectives in the first two years of the program in growing large 50 cm diameter EFG cylinders, cutting wafers from them and processing these wafers into solar cells to demonstrate acceptable material quality. Additionally, in Year 2, we had planned to examine the feasibility and cost advantages of extending the diameter to 1 meter and carrying out the emitter diffusion during crystal growth. The goal in pursuing these configurations is to demonstrate over a 50% reduction in manufacturing costs of the EFG wafer.

Subtask 5.1 - Laser cutting Improvements in laser technology are central to raising EFG manufacturing line mechanical yields and introduction of thinner EFG wafers. The current EFG wafer laser cutting process introduces damage in the wafer edge. This makes the wafer susceptible to increased levels of breakage as its thickness is decreased, and, as well, necessitates use of a costly acid damage-removal etch. The two main aspects of our program on lasers are: i) to evaluate new short pulse length laser technology that will provide reduced damage cutting for thin wafers; and ii) to demonstrate large, up to 75%, reductions in labor in laser cutting of current thick wafers, through use of high power lasers that can increase the cutting speed in production by up to 8x. In the first year of this task, we designed and constructed an R&D laser station for testing of new laser concepts. This has been used now to evaluate a new generation of lasers for cutting of EFG wafers.

The issue of cutting speed is being addressed in two distinct phases. In the first phase, we are working to achieve a doubling of the cutting speed without significantly changing the laser type or system presently employed at ASE Americas in manufacturing. In the second part of this work, we have evaluated a family of high power CO_2 lasers.

Year 2 Accomplishments We have completed our evaluation of the CO_2 laser in the manufacturing line, and found that it does not meet the requirements of reproducible cutting and acceptable edge quality even though it offered the distinct advantage of cutting at speeds of 4x to 8x faster than the current production lasers. Several models of both 250 and 500 W CO_2 lasers

were evaluated. Shortfalls in operation have been traced to several factors. Laser focusing, control of power, and gas flow control are all very critical to optimal operation. Although tests on the R&D station were successful, it was not possible to find a combination of these parameters, which could be consistently achieved in the laser stations currently in production. We are now investigating if there are other possible models of this laser, which may offer other options and/or have a wider window of operation.

After evaluating both the Q-Switched Nd:YAG and the copper vapor lasers in the first year of our program, we decided that neither of them could meet our program goals. Even though they demonstrated superior edge quality, the cutting speed was too slow. The former provided the best performance and was shown to be able to cut up to about 25 mm/s on the thinnest material. In the meantime we have located a supplier of a new design of laser which offers a compromise between cutting speed and quality. We have shown that we can double cutting speeds to about 2 in/s with edge quality superior to that of the lasers currently in manufacturing. We now have obtained and installed this laser in our R&D facility and plan to test and optimize it prior to evaluating it in the manufacturing line.

A new etch process has been evaluated at the vendor's site, the equipment built and received, installed and is currently being set up for operation in manufacturing. This etch equipment uses a plasma at atmospheric pressure to remove the edge damage caused by the laser. The primary objective of using the plasma process to remove edge damage is to reduce acid consumption and waste generation. The plasma etches only the wafer edge and produces a residue border of a few mm. A subsequent cleaning step is required, both to remove this border and any as-grown wafer film or contamination arising in the crystal growth and laser cutting process. We have carried out preliminary work to demonstrate that the etching required to remove these surface residues will require 50 to 80% less acid per wafer than what is currently used. However, this will take considerable optimizing of the process and downstream wafer requirements for cosmetic appearance and uniformity.

We have encouraging data which indicates that the wafer is stronger, as measured by the fracture twist test, after the plasma etch than after the normal acid etch currently used. This should result in higher yield processing. Activities under this program in this area have included design and evaluation of a number of process equipment fixtures and optimization studies. We are developing specialized fixturing to hold the wafers during the plasma process, both for the standard wafer and the larger 10 cm x 15 cm area wafer. This design of this fixturing is very critical in obtaining a strong wafer. It must be designed such that the entire perimeter of a wafer exposed to the plasma is uniformly etched. In the early designs, we had difficulties in holding the wafer in a stack in such a way as to avoid shadowing of part of the wafer edge. New designs are being fabricated which reduce this shadowing. The fixture also needs to be designed so as to maximize the throughput of the equipment. We have chosen to coin-stack the wafers and present the edges to the flame at an oblique angle. The carriers have been redesigned to maximize throughput and etch uniformity and the new equipment will be given a full production line test in the next phase of this program in order to maximize yield and minimize acid consumption.

Subtask 5.2 - Cell Efficiency EFG PV cells have reached the 14% level in commercial production with the help of programs carried out in PVMaT 4A2, about 5 - 10% (relative) lower than conventional x-Si wafer-based PV technologies. Encapsulated cell efficiencies in the module remain at bout 14% because of the optimized AR coating designed to optically match the

encapsulant and glass. In this subtask we will look for techniques to further investigate advanced processes to close this performance differential while maintaining EFG's cost advantage, and extend these processing techniques to be applicable to thin EFG wafers (100-150 microns). The objective will be to demonstrate technology to raise solar cell efficiency by 10% (relative). We have started to study cell designs, which can be applied to produce thin high efficiency cells. The goal is to achieve 15-16% efficient cells with new processing, which both can be scaled up in throughput and can be expected to be applicable to very thin wafers (down to 100 μm). The initial work in the first year in collaboration with the Georgia Institute of Technology (GIT) concentrated on process development. In the second and third years, successful candidate processes will be tested in a production environment. The overall module cost reduction from work in these improvements under Task 1 is expected to be about 15% (relative).

Year 2 Accomplishments A number of matrix experiments have been carried out at GIT on evaluation of rapid thermal processing (RTP) methods for optimizing EFG wafer base lifetime. The details of this work are given in two publications [5]. We have demonstrated to date cell efficiencies as high as 14.8% with (RTP), the approach we have selected to help us achieve our goals. Among the most significant findings relate to the synergistic effects of firing with aluminum and the SiN film. Annealing of the SiN film leads to very little passivation when done without the Al on the back. The optimal annealing temperature is increased to above 800 C when the Al is present. We are exploring this higher temperature region in more detail because it results in a superior Al back surface field which could eventually lead to higher cell efficiencies.

Subtask 5.3 - Thin EFG Cylinder Cylindrical shapes allow rotational movement of the crystal or crucible, which in turn can improve thermal uniformity, hence wafer thickness control and uniformity. Cylindrical shapes also improve laser cutting efficiency and allow thinner wafers to be processed with high yields so as to provide higher materials use efficiency. If cylinder growth is combined with on-line emitter diffusion by incorporating phosphorus diffusion sources into the EFG growth furnaces, this eliminates the costly and yield-critical processing steps of etching and diffusion in the cell line, and removes critical steps in wafer handling. The overall module cost reduction from work in breakthrough opportunities may be upwards of 50% (relative), i.e. cutting EFG PV costs in half. Given the existing cost advantage of EFG wafers relative to wafer-based x-Si PV technologies, a halving of EFG costs would dramatically change the overall commercial prospects for PV relative to other energy sources.

In the first year of the program we demonstrated growth of 50 cm diameter EFG cylinders up to 1.2 m in length and down to average 100 μm wall thickness, and developed a model for heat transfer in large diameter systems [6,7]. In this second year we have continued to develop the growth system and cutting methods for the cylinder, and evaluated solar cell processing sequences for thin cylindrical wafers. Two problems were encountered in the growth area during development of the cylinder. Difficulties were experienced with obtaining a uniform grade of graphite and this led to inconsistent and non-reproducible growth conditions. The other area problems were encountered was in the residual stress in the crystal. The latter, in particular is of major concern at this time, and the work scope in this subtask has been significantly redirected this year to efforts to reduce stress during crystal growth.

This difficulty has also resulted in a second change in work scope in this task: we have redirected the program for large diameter cylinder growth to development of concepts for larger diameter growth of the standard EFG octagons configuration with increased face width (12.5 cm

instead of 10 cm widths), and EFG tubes with an increase in the number of faces from 8 to as high as 12 (dodecagon). We will initially explore furnace designs with larger EFG furnace diameters that can accommodate an octagon with 12.5 cm wide faces, to minimize our exposure to graphite uniformity problems. In the meantime, we plan to work with graphite vendors to improve process and material reproducibility so that we are assured of obtaining the quality of graphite required for larger diameter systems. In order to most quickly obtain a wafer product that will be suitable for commercial use, we will start with growing the 12.5 cm face octagon with thicknesses of the order of 300-350 μm until we have a better understanding of the stress problems and how they change with tube wall thickness. Laser cutting tasks for thin wafers are also redirected at this time toward evaluation of a new Nd:YAG laser and development of larger diameter cutting station for the larger EFG tubes.

Year 2 Accomplishments - Crystal Growth Experiments on development of large diameter EFG cylinders were redirected to work to decrease residual stress in growth. Extensive characterization of the cylinder system and the standard octagon system with thermocouples was done to develop a database for thermal modeling and furnace design. This database is being used now for evaluation of different modifications of the hot zone. The main challenge is to develop an understanding of system components of the hot zone, which have the most impact on the critical region of the temperature profile, which influences the residual stress. We are carrying out a series of systematic comparisons using both the heat transfer model developed at the State University of New York – Stony Brook and empirical measurements and observations (details may be found in ref. [6]). The diagnostic equipment described in Subtask 4.1 above are an integral part of this work. The main challenge is to find as beneficial a temperature profile for 100 μm material as we have in the current octagon. Stress in the crystal varies with thickness proportional to the inverse square root on account of the increase in temperature gradients for a given external radiation field, i.e., hot zone configuration. The crystal temperature profile giving low stresses for 250-300 μm thick wafers is not that required at 100-150 μm thicknesses. We are planning to develop straightforward methods to change from the low stress thick wafer profile to the low stress thin wafer profile, for example by changing a single coil current or system configuration.

On account of the delay of the cylinder development for thin material growth because of the stress issues with thin material, we have redirected the effort in this task toward designs for larger diameter EFG polygon tubes. Several large diameter systems are under review at this time for cost effectiveness and risk. The most straightforward and lowest risk option is to extend the face width of the octagon to 12.5 cm from the current 10 cm. A higher risk option is to develop a dodecagon with 12.5 cm face widths.

We have completed development work on several advanced laser systems and demonstrated prototype cutting fixtures for the cylinder. The short pulse length Nd:YAG laser and the Cu vapor laser under development both have shown that very thin tubes can be cut with acceptable speeds of 0.5-1 in/s. However, because as-grown material stress levels were high in the cylinder, even these lasers with reduced edge damage did not result in high yield cutting, and this program has been redirected toward evaluation of an intermediate speed laser (see above) and toward work to cut larger diameter EFG polygons until progress can be made to reduce stress in thin EFG tubes.

In Situ p-n Junctions Formation of p-n junctions during crystal growth was previously demonstrated for EFG [8]. We have studied the feasibility of introducing diffusion sources in the large diameter cylinder hot zone this year. It was concluded that it would not be possible to do this in the current design of hot zone because a lack of control of the ambient gases and because rotation could not be carried out. An alternate processing scheme is being examined in which the diffusion would be done on the cylinder in a separate chamber prior to cutting it. The length of the cylinder and the growth speed can be matched so that the growth and processing times do not result in throughput loss during growth.

Thin Solar Cells We have successfully made 13% efficient 5 cm x 5 cm and 6 cm x 6 cm area solar cells from sections cut from EFG cylinders down to as thin as 150 μm. Full details are presented in a publication [7]. On account of low yields because of the growth stress in the thinnest sections, we could not obtain wafers thinner than 150 μm from the cylinder. We had to adapt several of the processing steps in our manufacturing line to handle this thickness of curved wafer. Wafers were given a cleaning HNO_3:HF etch prior to processing to remove surface films. Phosphorus diffusion was carried out on the concave side of the wafer. With the Al application and sintering now on the convex side, this tended to reduce the curvature of the solar cell. Special fixturing was made to allow processing of the curved wafer during the AR coating in the PECVD nitride deposition step. The curved wafer was affixed to a support wafer during the metal application step. The solar cell results are tabulated below.

Cells were produced using ASE's standard cell fabrication scheme, with adaptations made as required to handle the curved material. Wafer sizes of 5 cm and 6 cm squares were used due to the curvature of the 50 cm diameter cylinder. (A one meter diameter cylinder, which was the ultimate intention for such a cylinder, would have allowed 10 x 10 cm squares, our present production line size, to be used.) Wafers were given a HNO_3:HF etch to remove surface films. Phosphorus diffusion was effected on the concave side: this was done so that the Al print step applied later would be on the convex side. A special concave graphite plate was built to hold the wafers during our SiN AR coating deposition step. For the metalization steps, the cylindrical wafers were affixed to 10 x 10 cm support wafers. Results of the cell fabrication are given in Table 1 below.

Table 1. Cell test parameters for cylindrical EFG multicrystalline Si solar cells.

Ave. Thick. (μm)	Jsc (mA/cm^2)	Voc (V)	FF	PP (mW/cm^2)
150	30.64	0.583	0.725	13.0
190	31.36	0.590	0.707	13.1
200	31.12	0.588	0.696	12.7
210	31.00	0.582	0.686	12.4
290	28.84	0.575	0.739	12.3

Firing profile optimization for the thinner material should result in additional gains. The J_{sc} and V_{oc} values on the best cells are consistent with our standard EFG cells of about 14% efficiency. Low fill factors are partly due to non-optimized means for probing these smaller, more fragile cells during the measurement process.

Highlights for the year for this task have been: 1) fabrication of solar cells on thin wafers from the EFG cylinder, and 2) qualification and development of equipment to be introduced into manufacturing for a process of plasma etching which has potential to reduce acid waste and increase strength and yield of EFG wafers.

2.3 Task 6 - Flexible Manufacturing

This task has worked on improving the manufacture of larger EFG wafers, and on module failure analysis. The goals in pursuing such product design and fabrication improvements are to deliver better value to the customer, to better respond to customer requirements, and to achieve longer field service life and lower field failure rates.

Subtask 6.1 – Large EFG Wafers The trend in crystalline Si wafer technology is towards larger wafers so as to decrease cell processing costs, thus amortizing the unit cell processing cost over a larger area. EFG technology is not limited, as are conventional ingot/block + sawing wafer technologies, by ingot/block size and/or by maximum sawing length. In principle, EFG wafers may be cut to any length, to produce a wafer encompassing up to the full length of an EFG tube or cylinder. The first step toward larger wafers at ASE Americas was completed in the first two years of this subcontract. We expanded our product offering to include 10 cm x 15 cm wafers in addition to the standard 10 cm x 10 cm wafers. We therefore developed a strategy for laser cutting station modifications and wafer handling that are high yield and cost effective for producing larger rectangular EFG wafers.

Wafer fracture during cutting and processing is a major contributor to productivity losses in manufacturing. We initiated under this task a study to identify the causes of mechanical yield loss for wafers throughout the crystal growth and laser cutting areas. The initial work set up a baseline on the regular size 10 cm x 10 cm wafers. The goal of this work was to improve understanding of the processing steps which are most detrimental to fracturing wafers, and pay attention particularly to which steps both in wafer cutting and cell processing are going to be of highest concern as we produce thinner wafers. We also are working on diagnostic techniques for crack detection (see Subtask 4.1). In the mature high speed manufacturing line, diagnostic equipment for detection of cracks will be needed at more than one process step. At this point we expect more than one technique will be needed, as there are different requirements in different locations of the line. Cracks in EFG wafers are propagated from the damaged laser cut edge into the interior of the wafers during handling and loading of carriers. They do not extend sufficiently far to be visible or to lead to fracture of the wafer into several pieces. The wafer is weakened, however, and if the cracks extend more than a few mm into the wafer then there is a high probability that it will fracture in subsequent cell processing, interconnect or module fabrication. Thus the first inspection location in likely will be after the laser step, or the subsequent etch step prior to diffusion. Other locations where crack detection may be required are midway through the cell line and at interconnect. We have initiated work on both ultrasonic and optical metrology of crack detection to determine the feasibility of their application in high-speed manufacturing.

We have already described (in Subtask 4.1 above) a proprietary plasma etch method with which to remove the damaged region of the wafer edge after it is laser cut. This would reduce the incidence of cracks propagating to fracture in handling, raise overall mechanical yield, and contribute toward the goals of reducing chemical usage in the ASE Americas' manufacturing

line by reducing acid etch requirements. As we are going to higher volumes with our wafer expansion, this process becomes a bottleneck and expansion of manufacturing equipment becomes very costly. Another approach (see Subtask 5.1) is to reduce the damage through utilization of new laser technologies.

A new element in this subtask in the coming year will be the evaluation of the cost effectiveness of production of 12.5 cm x 12.5 cm wafers. Competitive pressures to make available this size EFG wafers in the marketplace and standardization to this area in the future have put a high priority on this work. In the case of EFG technology changing to this wafer size is not a straightforward procedure as both a larger diameter EFG octagon and a laser cutting station have to be designed, fabricated and tested before full scale manufacturing of these wafers would begin.

We plan also as part of this task to develop statistical methods to measure and compare wafer manufacturing processes for the different size wafers, and closely coordinate our research with customer requirements for wafer edge quality and strength. We have initiated a program with a consultant to install and evaluate a data-tracking program for machine performance. This will evaluate up time, track maintenance routines and provide real time information on operating status of manufacturing equipment.

Year 2 Accomplishments A sonic method to detect cracks in EFG wafers was not successful, and we have expanded the search for other approaches. The most promising approach at this point appears to be an ultrasonic resonance method (see Subtask 4.1). Carrier designs and process configurations are being developed for plasma etching of wafers of different sizes. A software package is under evaluation to assist in tracking of machine performance. This program is being developed first to monitor laser cutting equipment performance and its scope will be expanded to other parts of the manufacturing line next year if it is successful. This will be the first step toward instituting Total Preventative Maintenance (TPM) systems and implementation of continuous improvement methodology using Computer Integrated Manufacturing (CIM).

Subtask 6.2 – Modules As EFG PV products accumulate field exposure and as EFG PV products are applied in an increasingly wide array of applications, it is inevitable that some field failures will occur. It is important to promptly analyze any failures and quickly translate the lessons learned into manufacturing improvements. In this Subtask, we will establish feedback systems from end users and field failure information that tie field experience back to the manufacturing process. We plan to develop the capability to close the loop between the manufacturing process and the observed product defects to be corrected. Fundamental to achieving improvement in high volume manufacturing will be the establishment of Failure Analysis and Root-Cause-of-Failure capabilities.

Year 2 Accomplishments - Module Field Studies We have continued to evaluate occurrences of fracture of glass in our large ASE 300-DG module in the field and categorize and analyze glass where failure mechanisms are not obvious. To date, we have seen a number of diverse failure mechanisms, and there has not been any systematic failure mode which can be related to manufacturing practices or shortcomings. We completed a study of AC module field performance in collaboration with Ascension Technology and found that these modules have performed very well in their introduction into the marketplace.

Subtask 6.2 –Encapsulants One task under PVMaT 4A2 successfully evaluated new encapsulants, and provided future options for manufacturing, both for reduced costs and expectations for a longer module field lifetime. This work had two purposes. One was to develop an improved encapsulant to overcome some shortcomings in the current encapsulant in use in the ASE Americas manufacturing line. Tests were successfully completed and recommendations to manufacturing have been made. Test modules with this encapsulant will be included as part of the above field study program to compare them to our existing product line. The second PVMaT 4A2 objective was to examine options provided by resin encapsulants which are liquid at room temperature. Several of these also have very fast cure times using UV light. These are desirable both to provide flexibility in manufacturing with respect to increasing throughput and improving yield of current products, and to increase yields with thin wafers. We have previously found that the stiffness and the relatively long process cycle time of our current encapsulant were limitations which are crucial to overcome if we are to successfully reduce module manufacturing costs with future thin EFG wafer technology. Several alternatives were identified, and some already have been under test.

Year 2 Accomplishments – Encapsulants A study of field performance of the AC module was completed and has indicted that this module design is operating up to expectations. We evaluated the fire rating of our encapsulant in a fire brand test and demonstrated that the ASE Americas' non-EVA encapsulant passes the UL790 Fire Resistance Roof Covering Materials test and in it performs significantly better than the EVA encapsulant of many of our competitors which did not pass this test.

We have completed tests on a modified formulation of our standard encapsulant, which has several advantages and possible cost savings. The transmission is improved by several percent, it has a lower level of moisture retention, it has a lower lamination temperature and higher melt flow index, thus being better for thinner wafers, and eliminates some cosmetic defects occurring from time to time with our standard formulation. The module cost reduction from this encapsulant is expected to be about 5% (relative), and help drive introduction of new customer-driven product offerings.

We have not been successful in making prototype modules with a liquid resin, which shows the most promise to use with thin EFG wafers. Delamination of the encapsulant from the glass and excessive formation of bubbles during lamination and cure attempts have been the main problems. We have stopped this work to concentrate return to another module development program next year. Prototype construction of the reflector module, which we first evaluated in our PVMaT 4A2 program is under way again. This work was interrupted because the original vendor for the reflector material could not produce material that met our specifications, and we have since been searching for an alternate material. A new vendor has been found and this program is now going ahead. We expect that we can gain up to a 20% cost reduction with the reflector module.

Highlights of this year in this task have been the qualification of a modified encapsulation with a potential to reduce module costs 5%.

3. Highlights of the Year 2 Program

The main accomplishments of the second year program at ASE Americas have been:

- Cell efficiencies in the ASE Americas manufacturing line are continuing to improve, and have reached as high as 14.4% with the help of application of Design of Experiments and Statistical Process Control methods.
- Solar cells of 13% efficiency have been made on 6 cm x 6 cm areas of wafers cut from EFG cylinders with wall thicknesses down to 150 μm.
- Equipment for a plasma etch process for removing wafer edge damage produced by laser cutting, for reducing acid processing and waste and for strengthening the wafer so as to enhance yield is being introduced into manufacturin.
- New laser technologies producing low damage cutting have been demonstrated and a new short pulse length laser is being configured for manufacturing trials.
- A new formulation of our standard encapsulant has potential to reduce manufacturing costs of modules by 5%.
- ASE Americas' non-EVA encapsulant passes the UL790 Fire Resistance of Roof Covering Test and its performance is significantly better than that of EVA.

4. Future Work

Objectives in Year 3 work in the various tasks of the ASE Americas' PVMaT program will be as follows:

Task 7 – Manufacturing Systems

- Demonstrate manufacturing chemical waste, mechanical and electrical yield loss reductions of 10% each
- Complete evaluation of software for equipment performance and demonstrate Total Preventative Maintenance (TPM) strategy on 75% of most critical process stations sand wafer yield tracking
- Complete ISO 9000 and ISO 14000 documents and compliance implementation and begin certification process
- Demonstrate feasibility of new diagnostics in support of SPC in areas of crack detection, photoluminescence and stress measurement

Task 8 – Low Cost Processes

- Complete a design review of large diameter EFG furnace growth performance and processing of solar cells and document large area (up to 12.5 cm x 12.5 cm) cell performance as a commercial product
- Complete integration of crystal growth processes, advance laser cutting technology and etching processes to produce lower stress and stronger large EFG wafers for manufacturing
- Evaluate design review on new Georgia Tech processes for increasing EFG solar cell efficiency

Task 9 – Flexible Manufacturing

- Develop database for quality control procedures in EFG wafer manufacturing for diversification of EFG wafer size to 10 cm x 10 cm and 12.5 cm x 12.5 cm areas
- Deploy alternative plasma etch equipment and processes for diverse wafer sizes
- Complete manufacturing demonstrations of new encapsulation processes and module designs
- Achieve a 9% module manufacturing cost reduction

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13. ABSTRACT *(Maximum 200 words)*
The PVMaT 5A2 program at ASE Americas is a three-year program that addresses topics in the development of manufacturing systems, low-cost processing approaches, and flexible manufacturing methods. The three-year objectives are as follows: (1) implementation of computer-aided manufacturing systems, including Statistical Process Control, to aid in electrical and mechanical yield improvements of 10%, (2) development and implementation of ISO 9000 and ISO 14000, (3) deployment of wafer production from large-diameter (up to 1 m) EFG cylinders and wafer thicknesses down to 95 microns, (4) development of low-damage, high-yield laser-cutting methods for thin wafers, (5) cell designs for >15% cell efficiencies on 100-micron-thick EFG wafers, (6) development of Rapid Thermal Anneal processing for thin high-efficiency EFG cells, and (7) deployment of flexible manufacturing methods for diversification in wafer size and module design. In the second year of this program, the significant accomplishments in each of three tasks that cover these areas are as follows: Task 4—Manufacturing systems, Task 5—Low-cost processes, and Task 6—Flexible manufacturing.

14. SUBJECT TERMS
photovoltaics; PVMaT; cost reductions; high-volume PV manufacturing; computer-aided manufacturing systems; statistical process control; wafer production; laser-cutting methods; thin wafers; rapid thermal anneal processing; high-efficiency EFG cells

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