July 2001 • NREL/SR-520-30618

Subcontractor Report

Commercialization of CIS-Based Thin-Film PV

Annual Technical Report—Phase II
September 1999 – August 2000

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Siemens Solar Industries
Camarillo, California

National Renewable Energy Laboratory

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Preface

Siemens Solar Industries (SSI) has pursued the research and development of $CuInSe_2$-based thin film PV technology since 1980 [1]. At the start of subcontract activities with NREL, SSI had demonstrated a 14.1% efficient 3.4 cm^2 active-area cell, unencapsulated integrated modules with aperture efficiencies of 11.2% on 940 cm^2 and 9.1% on 3900 cm^2, and an encapsulated module with 8.7% efficiency on 3883 cm^2 (verified by NREL).

SSI began a 3-year, 3 phase cost-shared subcontract (No. ZN-1-19019-5) on May 1, 1991 with the overall project goal of fabricating a large area, stable, 12.5% aperture efficient encapsulated CIS module by scaleable, low-cost techniques on inexpensive substrates. Subcontract accomplishments were facilitated by addressing module reproducibility using small area test devices and mini-modules, and statistical process control disciplines were adopted to rigorously quantify process reproducibility. SSI addressed uniformity and reproducibility of absorber formation, interactions of the substrate with the absorber, and performance losses near interconnects. Subcontract accomplishments included demonstration of encapsulated module efficiencies that were at that time the highest reported mini-module efficiencies for any thin film technology (encapsulated 12.8% efficient mini-module on 68.9 cm^2 and an NREL-verified 12.7% efficient unencapsulated circuit on 69 cm^2 with a prismatic cover), demonstration of a champion large area (3860 cm^2) encapsulated module efficiency of 10.3% (verified by NREL) that was the first thin film module of its size to exceed the 10% efficiency level, and delivery to NREL of a one kilowatt array of large area (~3890 cm^2) approximately 30 watt modules [2].

From September 1995 through December 1998, SSI participated in a 3-year, 3 phase cost-shared TFPPP subcontract (No. ZAF-5-14142-03). The primary objective of this subcontract was to establish reliable high-throughput, high-yield thin film deposition processes in order to make CIS a viable option for the next generation of photovoltaics. Outdoor testing, accelerated environmental testing, and packaging development progressed throughout all phases of this subcontract. During Phase 1, SSI rigorously demonstrating process reproducibility and yield for a 10x10-cm monolithically interconnected "mini-module" baseline process and demonstrated a 13.6% aperture area efficient mini-module (verified by NREL). During Phase 2, SSI demonstrated the need to replace an existing large area reactor with a reactor based on a more direct scale-up of the baseline reactor, built a new large area reactor, and demonstrated comparable performance for the mini-modules baseline and 28x30-cm circuit plates. SSI developed products and prototype large area modules using a new package designed to integrate small circuit plates into larger modules. A one kilowatt array of $Cu(In,Ga)(S,Se)_2$ modules was delivered to NREL replacing a previously installed array based on an older absorber formation technology without sulfur incorporated in the absorber ($Cu(In,Ga)Se_2$). This array demonstrated significant improvements in efficiency and the temperature coefficient for power. SSI introduced two new 5-watt (ST5) and 10-watt (ST10) CIS-based products designed for use in 12 V systems, and NREL confirmed a new world-record efficiency of 11.1% on a SSI large area (3665 cm^2) module. During subcontract Phase 3, substrate size was scaled from ~30x30 cm to ~30x120 cm and good process control was demonstrated with an average efficiency of 10.8%. Commercial product samples were delivered to NREL and a second set of ~30x120 cm modules (32 modules totaling ~1.2 kW) was delivered to the NREL Outdoor Test Facility. The NREL measured average efficiency at standard test conditions of 11.4% was at that time the highest large area efficiency for any thin-film technology and NREL confirmed a world-record 11.8% large area (3651 cm^2) efficiency for the champion module [3].

The primary objectives of this subcontract are to scale up substrate size and to scale up production capacity of the baseline SSI CIS-based module process while introducing CIS-based products. The primary goals of this subcontract are to scale the substrate size from approximately 900 cm^2 (1 ft^2) to

approximately 4000 cm^2 by the middle of the Phase II, and to achieve pilot production rates of 500 kW per year by the end of Phase III. Deliverables for the subcontract include CIS-based products and representative modules delivered to the NREL Module Testing Team for outdoor testing and evaluation. SSI will continue mid-term and longer-term thin-film R&D with the goals of:

- Assuring future product competitiveness
- Improving module performance
- Reducing cost per watt
- Assuring product reliability

This document reports on progress toward these objectives and goals through approximately the second year of this three year subcontract; September 1999 through August 2000.

Acknowledgments

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The Siemens Solar Industries CIS Team:
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Siemens AG
Washington State University

Summary

Compared to traditional wafer-based crystalline silicon technologies, monolithic integration of thin film technologies can lead to products of comparable performance but with significant manufacturing advantages [1]: lower consumption of direct and indirect materials, fewer processing steps and easier automation. Monolithic integration is required to achieve these advantages since this eliminates multiple process steps and handling operations during formation of the absorber and during module assembly. The basic module elements for all thin-film technologies (alloys of amorphous silicon, cadmium telluride and CIS) are the same; the module elements are a circuit-glass/cover-glass laminate, a frame, and a junction box. The basic circuit elements are also very similar; they each have a base electrode, an absorber, a junction, a top electrode and three patterning steps for monolithic integration. While the details of these module elements or equivalent module elements differ, the basic cost structures are the same on an area-related basis. Since the cost per unit area is the same, the cost per watt is inversely proportional to the module efficiency. CIS cells and monolithically integrated modules have demonstrated the highest efficiencies of any candidate thin-film technologies; therefore, CIS is expected to have the lowest manufacturing cost/watt.

The primary objectives of the SSI "Commercialization of CIS-Based Thin-Film PV" subcontract are to scale-up substrate size and to increase production capacity of the baseline CIS module process while introducing CIS-based products. An additional mid- to longer-term objective is to advance CIS based thin-film technology thereby assuring future product competitiveness by improving module performance, cost per watt produced, and reliability. The foundation of the SSI's approach to process scale-up, process optimization, and demonstration of product durability is the application of design of experiment and statistical process control methodologies. These combined objectives are pursued to fabricate efficient and stable thin-film modules made by scaleable, manufacturable, low-cost techniques. SSI milestones for this subcontract are to:

- Scale from a substrate size of approximately 900 cm^2 to a substrate size of approximately 4000 cm^2 (4 ft^2) by the middle of the second phase of this subcontract. The criteria for achievement of this milestone is a 4000 cm^2 circuit plate process that has been adopted for SSI commercial activities and is reproducible as determined by statistical process control criteria.
- Achieve a pilot production rate 500 kW per year by the end of subcontract

During this subcontract phase, significant circuit plate efficiency improvements are again demonstrated with the peak in the distribution up from 10.8% at the beginning of the subcontract to 11.6%. The improvement during this subcontract period is particularly notable since it was achieved along with an increase in production volume of over 300%. Since the beginning of this subcontract, circuit plate production has increased by nearly an order of magnitude. The second subcontract milestone was met for one month of production during the last month of the second phase - pilot production rate 500 kW per year. The distribution of production modules is sharply peaked at nearly 11% efficiency with a full width of only ± 0.5%; almost all production modules efficiencies are above 10%!

Twenty (20) ST-40 modules taken from SSI's normal production were shipped to NREL as deliverables for this subcontract period. All of these modules are over 11% and two of these production modules slightly exceed SSI's previous NREL confirmed 12.1% world-record conversion efficiency for large area thin-film modules.

Process R&D tasks have been addressed for all processes by applying systematic research, development and production methodologies such as SPC, ANOVA and DOE. Generally good process control

continues to be demonstrated while scaling up capacity. Performance and capacity scale-up achievements have been made even though more R&D resources than anticipated were expended on process development for new absorber formation reactors. One of two new reactors is now used for production. A second major effort during this subcontract period has been study of the interdependence of Mo properties and laser processing. Process R&D has led to the demonstration of improved laser scribe quality and consistency for previously existing and new high throughput sputtering equipment. This know-how is largely responsible for defining a Mo deposition process for new sputtering equipment and improved circuit electrical yield from about 90% to typically above 95%!

SSI capabilities are leveraged as a Technology Partner participating in NREL team oriented TFPPP activities to address near-term to longer-term R&D topics. SSI's participation in Team activities is focused primarily on understanding the fundamental mechanisms responsible for transient effects in CIGS-based devices with the objective of eliminating or minimizing their impact. SSI receives support from NREL for several other specialty device and material measurements. NREL also supports SSI through long term testing of arrays and individual modules at the NREL Outdoor Test Facility (OTF). Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules have undergone testing for over twelve years.

TABLE OF CONTENTS

List of Figures

List of Tables

Introduction

Overview

Multinary $Cu(In,Ga)(Se,S)_2$ absorbers (CIS-based absorbers) are promising candidates for reducing the cost of photovoltaics well below the cost of crystalline silicon. CIS champion solar cells have exceeded 18% efficiency for devices fabricated at NREL [4]. Small area, fully integrated modules exceeding 13% in efficiency have been demonstrated by several groups [5]. Long-term outdoor stability has been demonstrated at NREL by ~30x30 cm and ~30x120 cm SSI modules which have been in field testing for as long as twelve years. Projections based on current processing indicate production costs well below the cost of crystalline silicon [5].

Compared to traditional wafer-based crystalline silicon technologies, new thin film technologies yield products of comparable performance but with significant advantages in manufacturing [5]:

- Lower consumption of direct and indirect materials
- Fewer processing steps
- Easier automation

Lower consumption of direct and indirect materials results in part from the thin-film structure for the semiconductor used to collect solar energy. All three of these manufacturing advantages are in part due to an integrated, monolithic circuit design illustrated in Figure 1. Monolithic integration eliminates multiple process steps that are otherwise required to handle individual wafers and assemble individual solar cells into the final product.

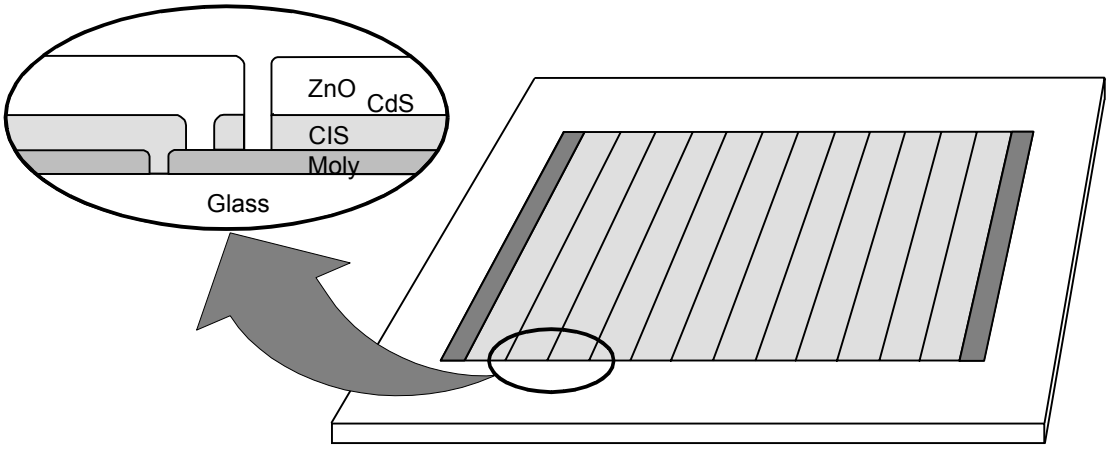

Figure 1. Structure of SSI's monolithically integrated thin-film circuits.

A number of thin film photovoltaic technologies have been developed as alternatives to the traditional solar cells based on crystalline silicon wafers [5]. Those technologies with the greatest potential to significantly reduce manufacturing costs are based on alloys of amorphous silicon (a-Si), cadmium

telluride (CdTe), CIS, and film silicon (Si-film). These photovoltaic thin film technologies have similar manufacturing costs per unit area since all share common elements of design and construction:

- Deposition of typically three layers on a suitable substrate – window/electrode, absorber, and back electrode
- Patterning to create monolithically integrated circuit plates
- Encapsulation to construct modules

Cost per watt is a more appropriate figure of merit than cost per unit area [5]. All thin film technologies have similar manufacturing costs per unit area since they all use similar or equivalent deposition, patterning, and encapsulation processes. About half of the total module cost – material, labor, and overhead – originates in the encapsulation scheme which is for the most part independent of the thin film technology. Costs for alternative encapsulation schemes are typically similar or even higher. The average efficiency of large, ~30x120 cm modules in pilot production at Siemens Solar is approximately 11%. This performance is comparable to many modules based on crystalline silicon, and is substantially better than the performance reported for competing thin-film technologies. The lowest cost per peak watt will result from the technology with the highest efficiency, CIS technology, since most thin film technologies have similar cost per unit area.

SSI CIS Process

Most terrestrial photovoltaic products today are designed to charge a 12-volt battery, however the output voltage of an individual solar cell is typically about 0.5 volts. Wafer-based technologies build up the voltage by connecting individual solar cells in series. In contrast, CIS circuits are fabricated monolithically (Figure 1); the interconnection is accomplished as part of the processing sequence to form the solar cell by alternately depositing a layer in the cell structure and patterning the layer using laser or mechanical scribing.

The structure of a SSI CIS solar cell is shown in Figure 2. The full process to form CIS circuit plates, including monolithic integration, is outlined in Figure 3. This process starts with ordinary sodalime window glass, which is cleaned and an SiO_2 barrier layer is deposited to control sodium diffusion and improve adhesion between the CIS and the molybdenum (Mo) base electrode. The Mo base electrode is sputtered onto the substrate. This is followed by the first patterning step (referred to as "P1") required to create monolithically integrated circuit plates – laser scribing to cut an isolation scribe in the Mo electrode. Copper, gallium and indium precursors to CIS formation are then deposited by sputtering. CIS formation is accomplished by heating the precursors in H_2Se and H_2S to form the CIS absorber. This deposition of copper and indium precursors followed by reaction to form CIS is often referred to as the two-stage process. A very thin coating of cadmium sulfide (CdS) is deposited by chemical bath deposition (CBD). This layer is often referred to as a "buffer layer." A second patterning step (P2) is performed by mechanical scribing through the CIS absorber to the Mo substrate thereby forming an interconnect via. A transparent contact is made by chemical vapor deposition (CVD) of zinc oxide (ZnO). This layer is often referred to as a "window layer" or a transparent conducting oxide (TCO). Simultaneously, ZnO is deposited on the exposed part of the Mo substrate in the interconnect via and thereby connects the Mo and ZnO electrodes of adjacent cells. A third and final patterning step (P3) is performed by mechanical scribing through the ZnO and CIS absorber to isolate adjacent cells.

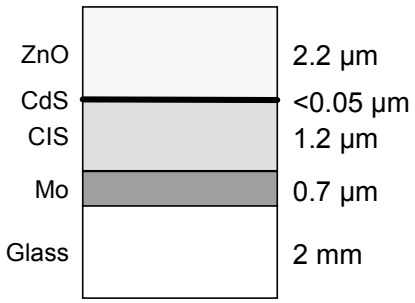

Figure 2. Structure of SSI's CIS cell structure (not to scale).

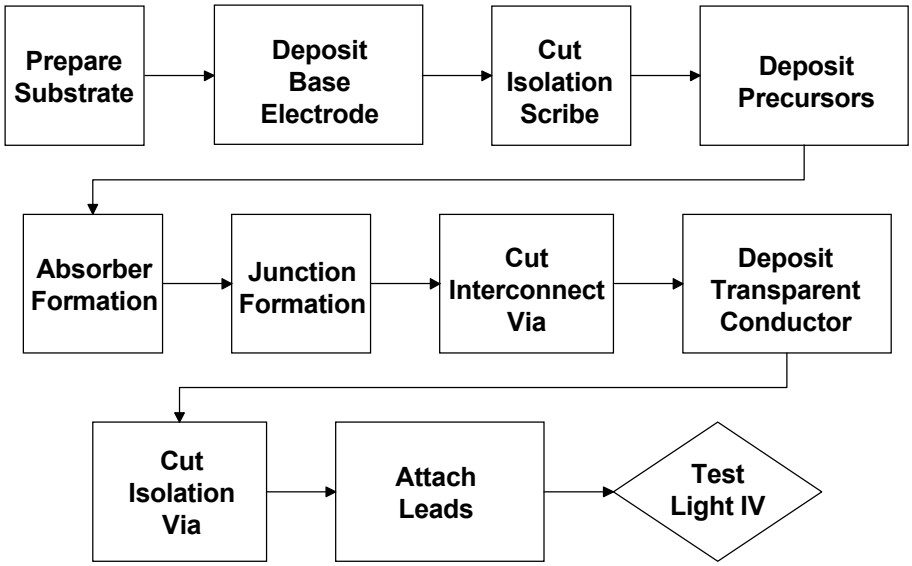

Figure 3. SSI CIS Circuit Processing Sequence.

The CIS-based absorber referred to in this report is composed of the ternary compound $CuInSe_2$ combined with sulfur and gallium to form the multinary compound $Cu(In,Ga)(S,Se)_2$. Gallium and sulfur are not uniformly distributed throughout the absorber but the concentrations are graded; hence, this structure is referred to as a "graded absorber." The graded absorber structure is a graded $Cu(In,Ga)(Se,S)_2$ multinary with higher sulfur concentration at the front and back and higher Ga concentration at the back. Elemental profiles typical of the SSI graded absorber structures are presented in Figure 4. Efficiency, voltage, and adhesion improvements have been reported for the SSI graded absorber structure [2, 6, 7].

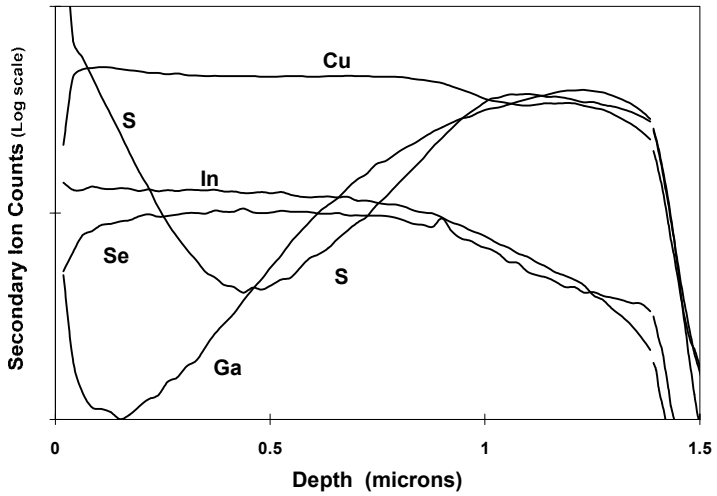

Figure 4. Typical elemental profile for the SSI graded absorber (SIMS from NREL).

Figure 5 illustrates the module configuration used for prototypes and ST products during this subcontract period [3]. EVA is used to laminate circuit plates to a tempered cover glass and a Tedlar/polyester/Al/Tedlar (TPAT) backsheet provides a hermetic seal. Aluminum extrusions are used to build frames for the modules. In addition to providing a hermetic seal, the combination of the TPAT backsheet and the offset between the circuit plate and the frame provides electrical isolation from the frame.

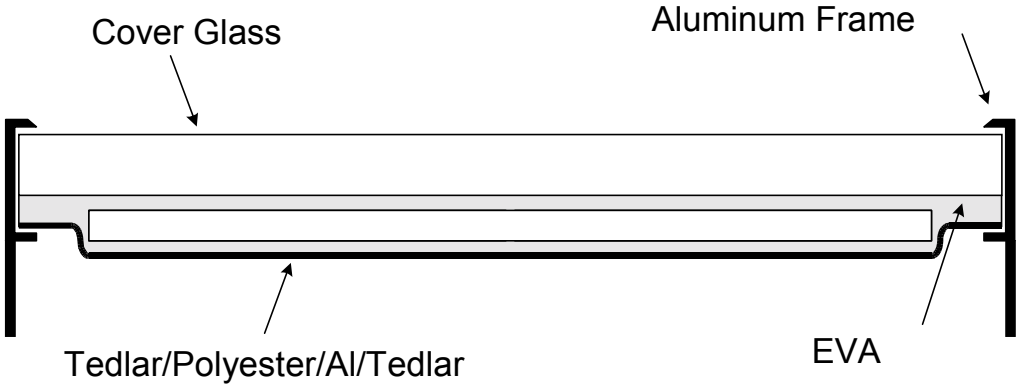

Figure 5. Single circuit plate module configuration with a TPAT backsheet.

SSI's R&D Approach

From the industrial perspective, the full process sequence anticipated for use in large-scale production must be mastered and rigorously demonstrated. The SSI research approach is composed of two main elements:

- Experimentation and development using device structures that exercise all aspects of large area module production [8]
- Application of statistical process control (SPC) as the discipline to rigorously quantify process reproducibility, and application of statistical methods such as analysis of variation (ANOVA) to rigorously quantify experimental results [9, 10].

Process predictability is a prerequisite for commercialization of thin-film PV since product performance ratings, yields and costs must be known before committing to produce products. Also, process predictability is essential for proper interpretation of process development efforts since experimental results may be ambiguous or misleading if compared to an unpredictable baseline process. SSI has adopted SPC methodologies because SPC was developed to rigorously quantify process reproducibility and process capability; the essence of SPC is predictability. Equally significantly, SPC provides the measure of systematic progress as processes are developed. Communication of this progress is typically best expressed in the language of the SPC discipline [11]. For example, process characterization results are demonstrated to be "statistically significant" based on knowledge of process repeatability measured using the SPC discipline, and confidence in the appropriate interpretation of experimental results is gained through application of statistical methods such as ANOVA to demonstrate statistically significant results.

Subcontract Activities and Milestones

The primary work of this subcontract is to advance module fabrication processes by progressively scaling substrate size and capacity for the SSI baseline CIS circuit-plate process. Simultaneously, SSI is pursuing understanding of the impact of circuit plate and module fabrication processes on device performance and module reliability. Understanding and optimization of the these processes is based on the application of DOE and SPC methodologies to identify dominant process issues and address process specific topics. Five subcontract activities have been defined to support this work:

Substrate Size Scale-up – The primary emphasis for this activity is to progressively scale substrate size from approximately 900 cm^2 (1 ft^2) approximately 4000 cm^2 (4 ft^2).

Capacity Scale-up - The technical base supporting manufacturability will be advanced as the production capacity is increased to about 500 kW/yr.

Product Durability - SSI will continue package development and qualification in parallel with substrate size and capacity scale up.

Environment, Safety and Health (ES&H) - SSI will continue internal programs and collaborative efforts such as with the TFPPP ES&H team to safely produce CIS-based devices and modules and to explore technical approaches for removing and recycling module components.

Process Improvements – This task emphasizes advancement of the technical base supporting manufacturing as SSI scales up substrate size and capacity. SSI capabilities are leveraged as a

Technology Partner participating in NREL team oriented TFPPP activities to address near-term to longer-term R&D topics.

Milestones

SSI milestones for this subcontract are to:

- Scale from a substrate size of approximately 900 cm^2 to a substrate size of approximately 4000 cm^2 (4 ft^2) by the middle of the second phase of this subcontract. The criteria for achievement of this milestone is a 4000 cm^2 circuit plate process that has been adopted for SSI commercial activities and is reproducible as determined by statistical process control criteria.
- Achieve a pilot production rate of 500 kW per year by the end of this subcontract

Deliverables

The following deliverables have been defined for each phase of this subcontract.

Phase I

D1. End of the 12th month: Deliver ten (10) 900-cm^2 (1-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10%.

D2. End of the 12th month: Deliver ten (10) 900-cm^2 (1-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10% for the NREL Module Testing Team.

Phase II

D3. End of the 24th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10%.

D4. End of the 24th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10% for the NREL Module Testing Team.

Phase III

D5. End of the 36th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 12%.

D6. End of the 36th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 12% for the NREL Module Testing Team.

Technical Review

Large Area Circuit Fabrication

Circuit Plate & Module Statistics

Progress during this subcontract phase will be discussed by comparison with circuit plate statistics from the previous periods. Circuit plate statistics representative of the beginning of this subcontract are constructed using data from the early portion of this subcontract combined with the later part of the previous TFPPP subcontract (Figure 6, Figure 7). During that time frame (January through November 1998), about 1300 ~30x120 cm circuit plates were produced including 18% that were dedicated to experiments [3, 12].

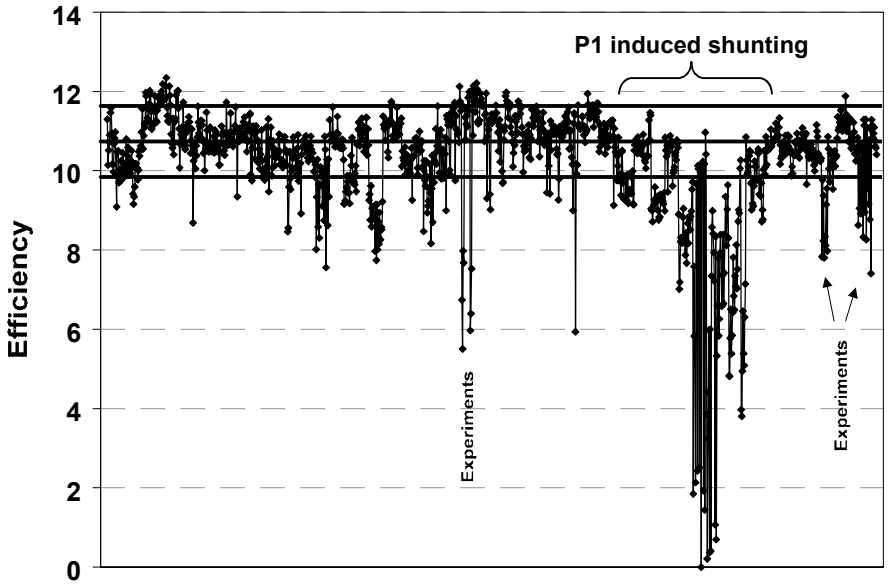

Figure 6. CIS Circuits Produced January through November 1998 (abscissa – module identifier).

The process data exhibits generally good control for extended periods with an average efficiency of 10.8% based on a Gaussian fit to the main portion of the distribution. Periodic shifts in the short-term average efficiency between about 10.25 and 11.25 were determined by shifts in V_{oc} and FF resulting from batch-to-batch variability in precursor or base electrode preparation. Similarly, periodic shunting along the laser scribed pattern lines in the Mo base electrode resulted from batch-to-batch variability in base electrode preparation.

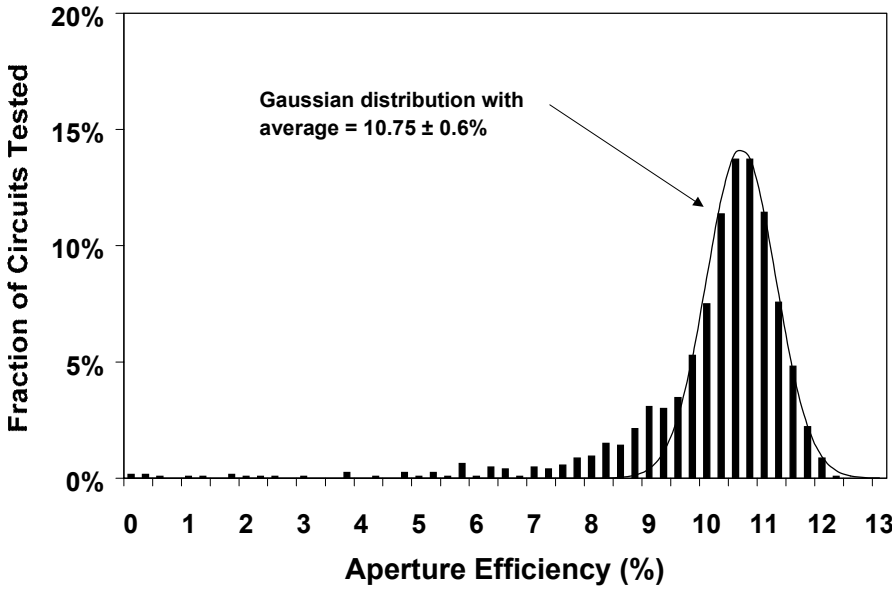

Figure 7. CIS Circuit Efficiency Distribution - January through November 1998.

Similar data representative of the previous subcontract period is presented in Figure 8 and Figure 9. This timeframe corresponds with the SSI fiscal year (October 1998 through September 1999) and there is some overlap with the previous charts. An average efficiency of 11.2% is demonstrated for 3,030 circuit plates.

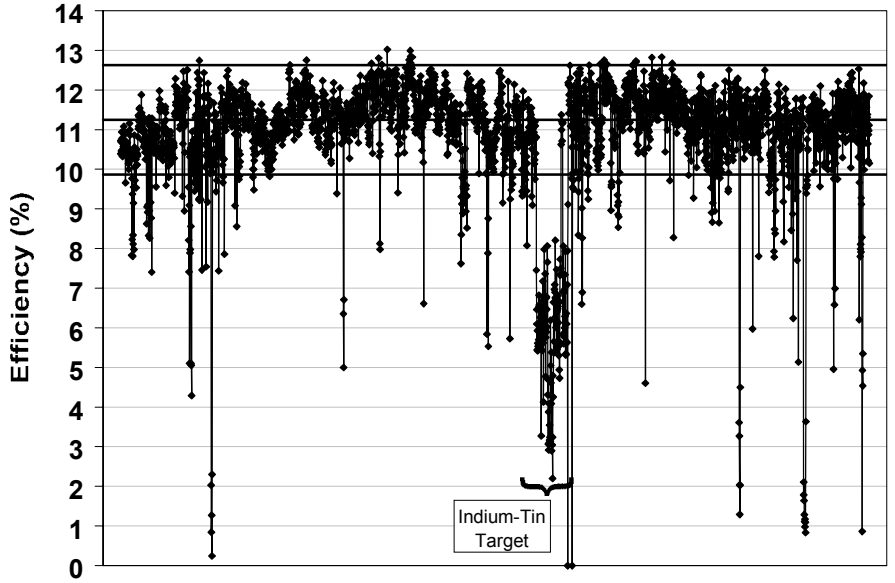

Figure 8. CIS Circuits Produced October 1998 through September 1999 (abscissa – module identifier).

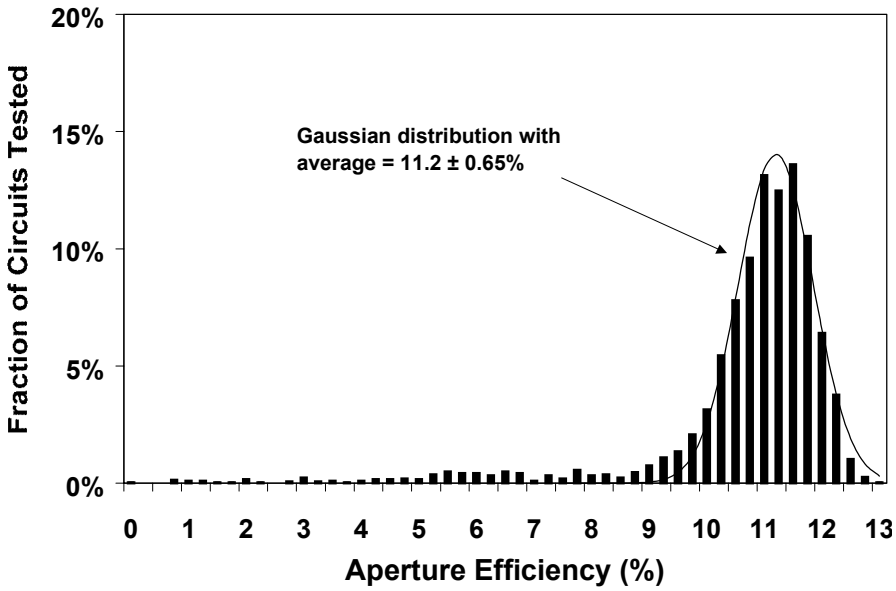

Figure 9. CIS Circuit Efficiency Distribution - October 1998 through September 1999.

During the previous subcontract period, the process data exhibited generally good control for extended periods. The average efficiency based on a Gaussian fit to the main portion of the distribution increased from 10.8% to 11.2% in part due to better overall process consistency and in part due to changes in the reaction process. Small periodic shifts in the short-term average efficiency continued that were determined by shifts in V_{oc} and FF resulting from batch-to-batch variability in precursor or base electrode preparation. Process development eliminated or greatly reduced periodic shunting along the laser scribed pattern lines. With the exception of identified special causes for irregular performance such as bad raw materials, 87% of the circuit plates were above 10% efficiency. Also during the previous subcontract period, NREL confirmed a world-record 12.1 percent conversion efficiency for a large area (3651 cm^2) CIS module.

Data representative of this subcontract period (September 1999 through August 2000) is presented in Figure 10. Efficiency improvements are again demonstrated with a peak in the Gaussian fit at 11.6%. Generally good process control continues to be demonstrated.

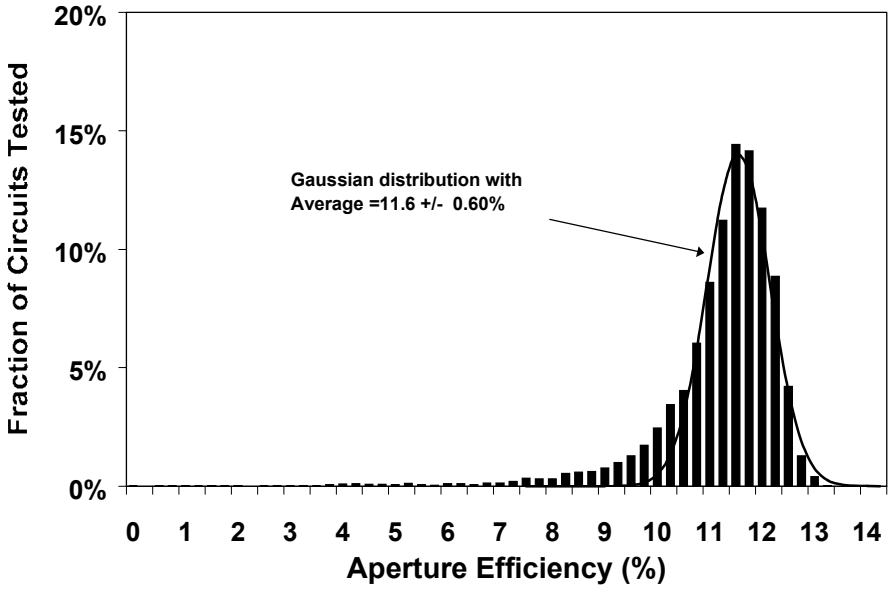

Figure 10. CIS Circuit Efficiency Distribution - September 1999 through August 2000.

The improvement during this subcontract period is particularly notable since it was achieved along with an increase in production volume of over 300%. Since the beginning of the contract, circuit plate production has increased by nearly an order of magnitude! This is summarized in the following table.

Table 1. Circuit production capacity and efficiency progress.

Year	**Circuit Production (kW)**	**Average Aperture Efficiency**	
		Unlaminated Circuit	**Laminated Module**
97-98	47	10.8%	10.3%
98-99	119	11.2%	10.7%
99-00	421	11.6%	10.9%

The result is production output with excellent performance and reproducibility, showing the strength of the SSI process foundations. Today's production distribution of modules (Figure 11) is sharply peaked at nearly 11% efficiency with a full width of only ± 0.5%; almost all production modules efficiencies are above 10%!

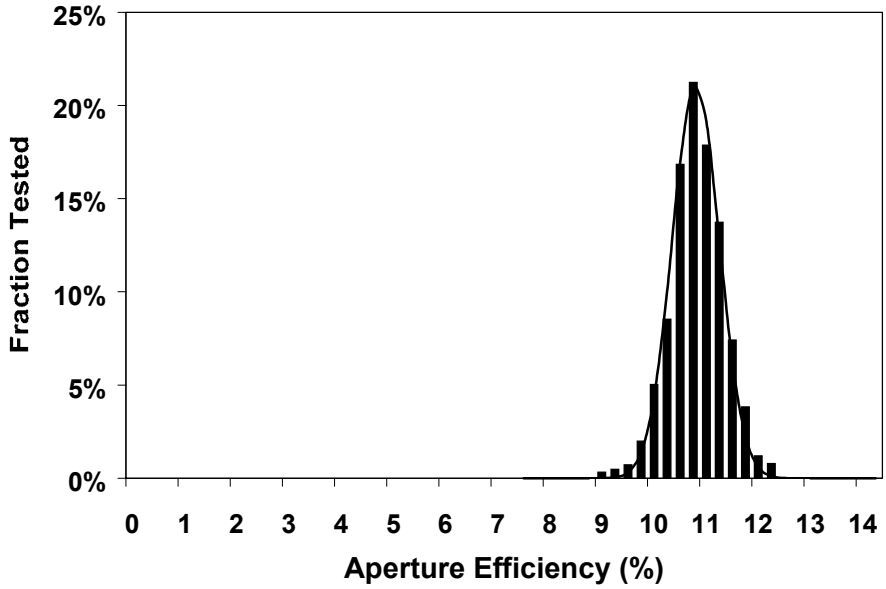

Figure 11. Module production distribution - September 1999 through August 2000.

Process Development Examples

This section will discuss examples of subcontract work in more detail.

As outlined in Table 1, circuit plate production has increased by nearly an order of magnitude while circuit and module efficiencies have steadily improved. These achievements have been made even though more R&D resources than anticipated were expended on process development for new absorber formation reactors. Implementation of two new reactors was delayed by late delivery from the equipment vendor. These reactors have exhibited poorer reliability than the prototype large area reactor. A longer than anticipated process development cycle was required to qualify the reactors for production. Efforts continue to address warping and poor CIS to Mo adhesion for some plate locations within the reactor and also to address these issues while developing processes for increased circuit plate load. This process development for new absorber formation reactors has been a major activity during this subcontract phase.

The following is an example of reactor process development efforts in collaboration with NREL during this subcontract phase. In additional to first order requirements such as reasonable temperature uniformity within the absorber formation reactors, the importance of reactor design to the CIS formation process was demonstrated when first scaling from a baseline process in small area reactors to a large area reactor. SSI demonstrated that differences between baseline and the first large area absorber formation reactor design were responsible for differences in absorber layer properties and cell performance. These differences were isolated to differences in the materials of construction and the physical design of the large reactor. As a result of these studies and advances in understanding the influence of reactor design on performance, SSI designed and built a new large area reactor (the prototype large area reactor) based on a more direct scale-up of the baseline reactor. Success with this development effort was demonstrated by comparable performance for baseline and large area circuit plates.

Small devices fabricated by NREL on complete SSI device stacks (processing through ZnO at SSI) were used to characterize the potential dependence of device performance on reactor position for one of SSI's

newer large area reactors. Performance versus temperature and position were analyzed using typical IV measurements (Eff, Voc, Jsc, FF).

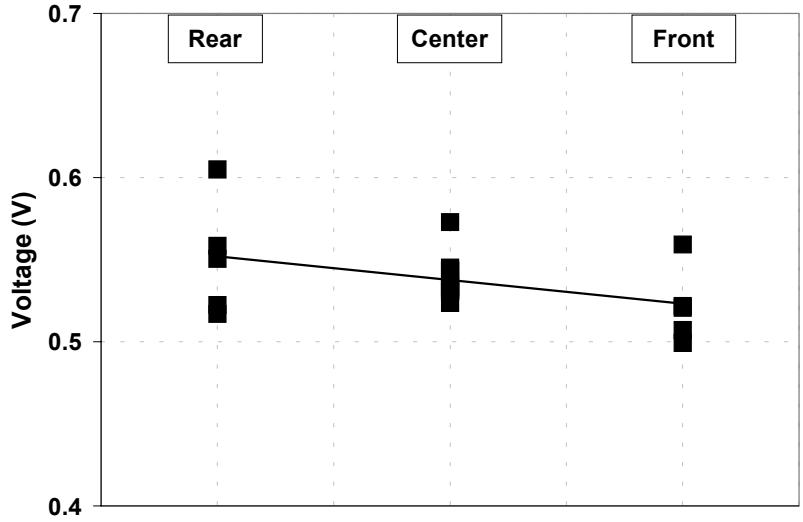

Figure 12. Dependence of Voc on reactor position.

In addition, NREL-supplied quantum efficiency data was used to generate a measure of the potential dependence of bandgap on reactor position. The intercept on the energy axis of the square of quantum efficiency versus photon energy is taken as a measure of optical bandgap. This bandgap data is actually a qualitative measure of device structure since the measured bandgap is a convolution of the affects of absorption and collection through the varying bandgap structure of these absorbers. As with Voc, these bandgap measurements indicate a difference in the absorber structure dependent on position within the reactor; in this case, a statistically significant increase in bandgap from front to rear within the reactor is observed.

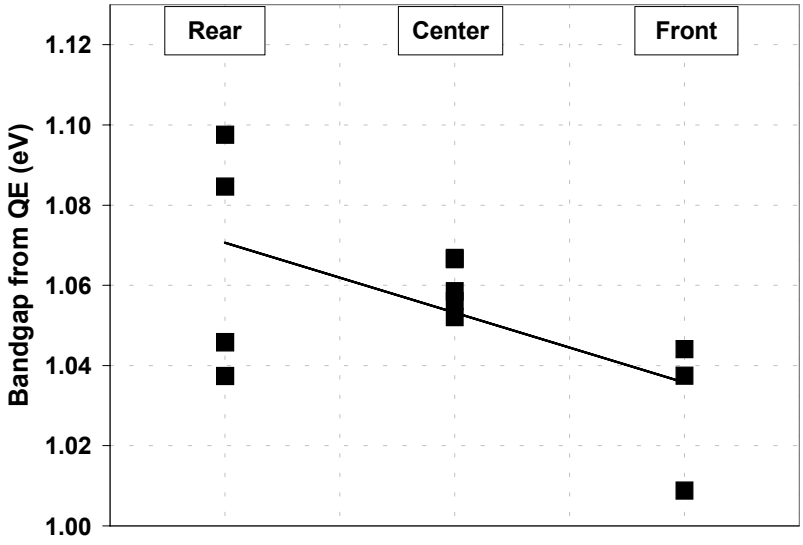

Figure 13. Dependence of bandgap on reactor position.

Temperature variations within the reactor are known from measurements using multiple thermocouples to profile temperatures throughout the reaction process. Although both Voc and bandgap are dependent on position within the reactor, there is no correlation between these parameters and the local temperature within the reactor. As when scaling from a baseline process in a small area reactor to the prototype large area reactor, this data implies that the local environment within the reactor, beyond simply the local thermal history, has an impact on the device structure and performance.

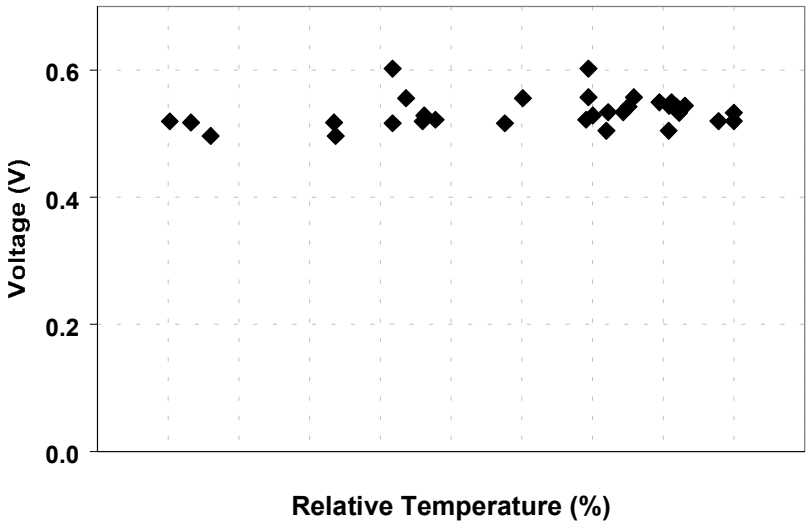

Figure 14. Lack of correlation between Voc and local temperature within the reactor.

Another major effort during this subcontract period has been study of the interdependence of Mo properties and laser processing. Process R&D has led to the demonstration of improved laser scribe quality and consistency for previously existing and new high throughput sputtering equipment. These studies have included addressing the importance of laser patterning parameters, Mo deposition hardware, Mo deposition process parameters, and the atmosphere during sputtering. These issues were pacing for both ongoing processing and capacity scale efforts during this subcontract phase since the issues impacted:

- Reproducibility of present processes
- The adequacy of specifications for new laser patterning equipment
- Potential patterning process improvements
- Potential Mo deposition process improvements
- Qualification of Mo deposition processes for new Mo deposition equipment

Ongoing process R&D includes simplification of the Mo deposition hardware and process based on gaining further understanding of the interdependence of Mo deposition conditions and laser patterning.

In previous subcontract periods, shunting along laser scribed patterns in the Mo base electrode sporadically caused poor performance. This resulted from batch-to-batch variability in base electrode preparation and a laser P1 process that may have been relatively sensitive to Mo properties. The issue

was previously addressed by laser beam delivery improvements and process development for Mo deposited in SSI's older sputtering system. However, during this subcontract period, regularly measured P1 process parameters drifted outside of the control limits on SPC charts. Studies to determine the cause for this behavior included: re-patterning Mo coatings deposited during the timeframe of drifting patterning parameters, re-patterning Mo coatings from archival samples that previously demonstrated normal patterning, measuring laser process parameters, patterning studies defined to address possible correlation with Mo deposition parameters, patterning studies defined to address possible correlation with multiple properties of the source glass, and review of long term historic SPC data. These studies indicated that the laser process parameters were unchanged, the laser process was reproducible, and that the drift in P1 results was associated with Mo deposition properties.

The following figure (Figure 15) represents the major features in Mo that has been affected by an individual laser pulse. A P1 scribe is generated by repeating this interaction forming multiple craters with an offset between adjacent craters. Mo is removed to a radius of R1. The Mo has been affected without removal in the region between R1 and R2 - referred to as the "affected Mo region."

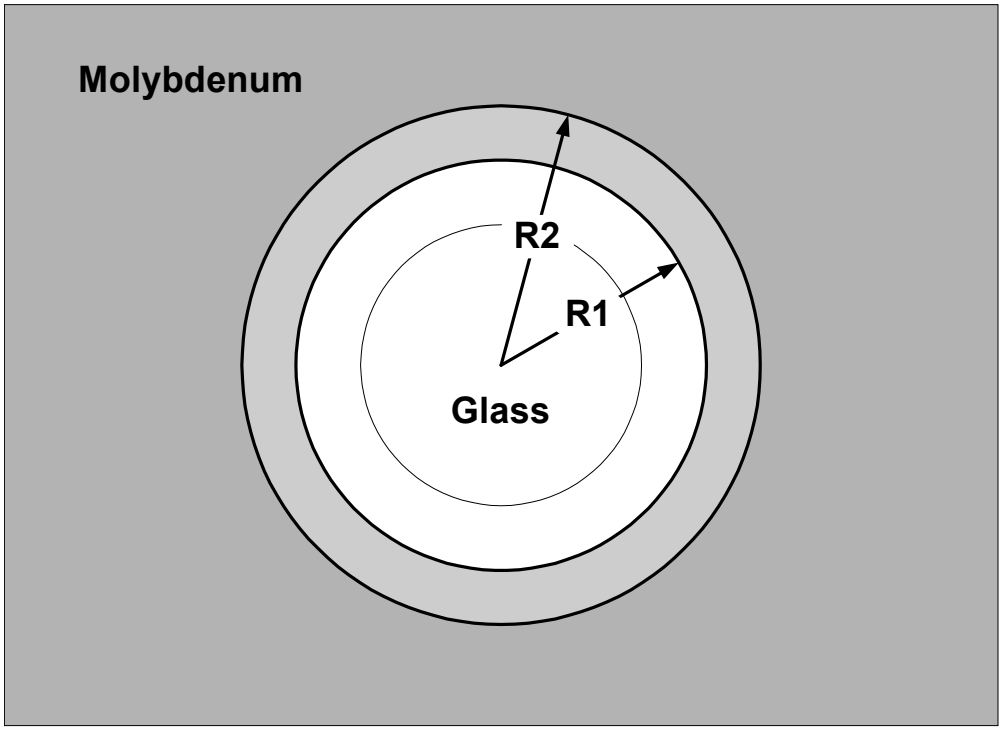

Figure 15. Diagrammatic representation of the effect of an individual laser pulse.

During this subcontract phase, laser processing studies indicated that the dimensions of the region where Mo is removed is predictably modeled by laser parameters. Correlation between Mo deposition process parameters and the extent of the affected Mo region were also demonstrated. The understanding gained from the combination of these results was applied to process definition and definition of process capabilities. The following summarizes the results of these studies and observations:

- The baseline process is not critically sensitive to laser focus – the process depth of field is large relative to normally encountered variations in substrate surface position.

- Removal of Mo by a laser pulse is hindered by the presence of the affected Mo region from previous pulses; the presence of the affected Mo region can interfere with continuously connecting well formed craters to achieve electrical isolation.
- Shunting can be caused by an extensive affected Mo region.
- The extent of the affected Mo region is dependent on Mo properties and laser parameters such as the relative dimensions of the laser beam. This is illustrated in the following chart, which demonstrates monotonically increasing relative dimensions of the affected Mo region as a function of the relative dimensions of the laser beam.
- Variations in quality of the laser produced pattern are related to variations of the properties of Mo across 1x4 ft. substrates and batch to batch variations in Mo properties.

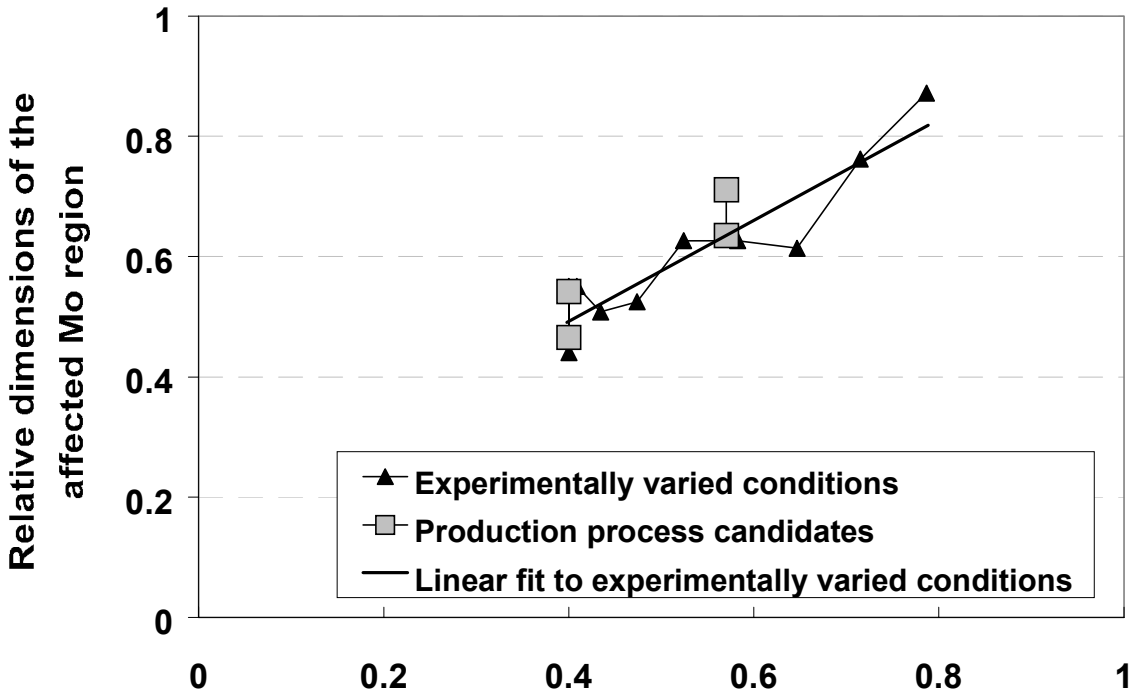

Figure 16. Relative dimensions of the affected Mo region versus normalized laser beam dimensions.

Candidates for improved laser processes that may allow 100% testing after patterning were evaluated based on P1 isolation and by fabricating modules to demonstrate equivalent or improved performance. For example, the following chart (Figure 17) demonstrates equivalent module performance for two candidate P1 processes and the baseline P1 process.

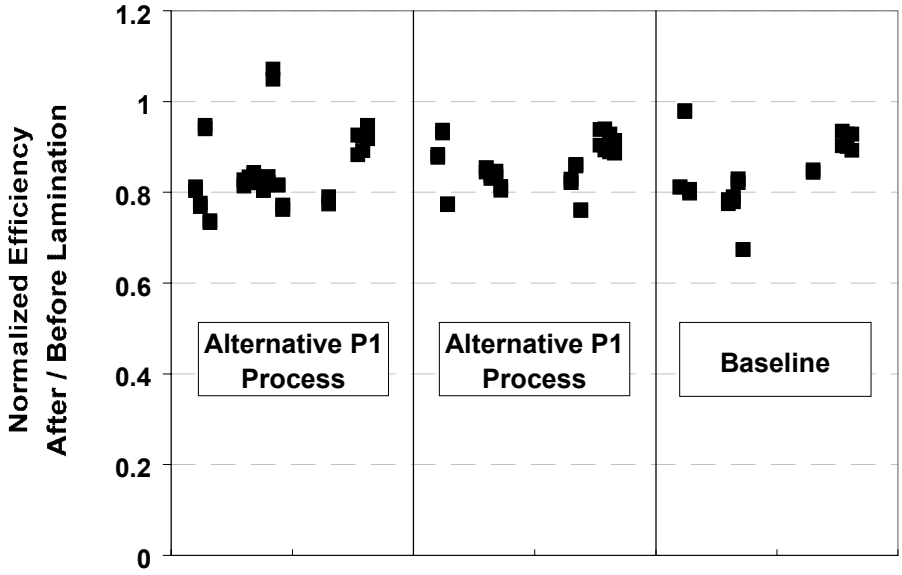

Figure 17. Demonstrated equivalence of alternative laser P1 processes (abscissa – module identifier)

The following figure (Figure 18) illustrates scribes for Mo deposition conditions leading to poor and high quality P1 scribes. The image on the left illustrates a poor quality scribe with an extensive affected Mo region. Initially, Mo deposited in a new high capacity sputtering system exhibited craters with this more extensive affected Mo region. In addition, Rick Matson (NREL) supplied SSI with SEM micrographs comparing baseline Mo with Mo from the new sputtering system. The Mo deposition process for the new sputtering system has now been modified to consistently produce quality scribes; however, at the expense of process complexity and potential process drift. Further improvements and more desirable depositions process conditions are expected with further R&D.

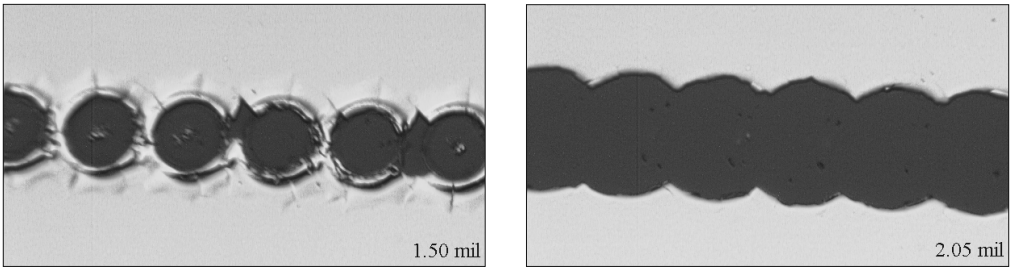

Figure 18. Laser scribes for Mo deposition conditions leading to poor and high quality P1 scribes.

R&D to quantify the dependence of scribe quality on laser parameters was necessary to evaluate sporadic shunting along laser P1 scribes. This knowledge may also lead to laser patterning processes that are less sensitivity to Mo properties and laser processes that allow 100% testing. However, the know-how derived from studies of the interdependence of Mo thin-film properties and laser processing is primarily responsible for addressing the pacing issues for both ongoing processing and capacity scale. This know-how is largely responsible for defining a Mo deposition process for new sputtering equipment and improved circuit electrical yield from about 90% to typically above 95%!

As another example of SSI/NREL collaborations, analysis at NREL by Rick Matson was particularly helpful in SSI's continuing efforts to identify the source of scratches. Scratches degrade performance and it is relatively easy to inspect just the degraded modules and at times find scratches. However, it is difficult to inspect all large area modules during each stage of processing to determine when the scratches occur. Figure 19 is an optical micrograph illustrating a scratch across the interconnect patterns (patterns 1, 2 & 3). Acetic acid was used to remove the ZnO electrode. Similar CdS depositions are expected in the scratch and in pattern 2 if the scratch occurred before CdS deposition. EDS analysis did not find evidence of CdS in the scratch. This implies that, at least for this particular scratch, the scratch occurred after CdS deposition and before ZnO deposition.

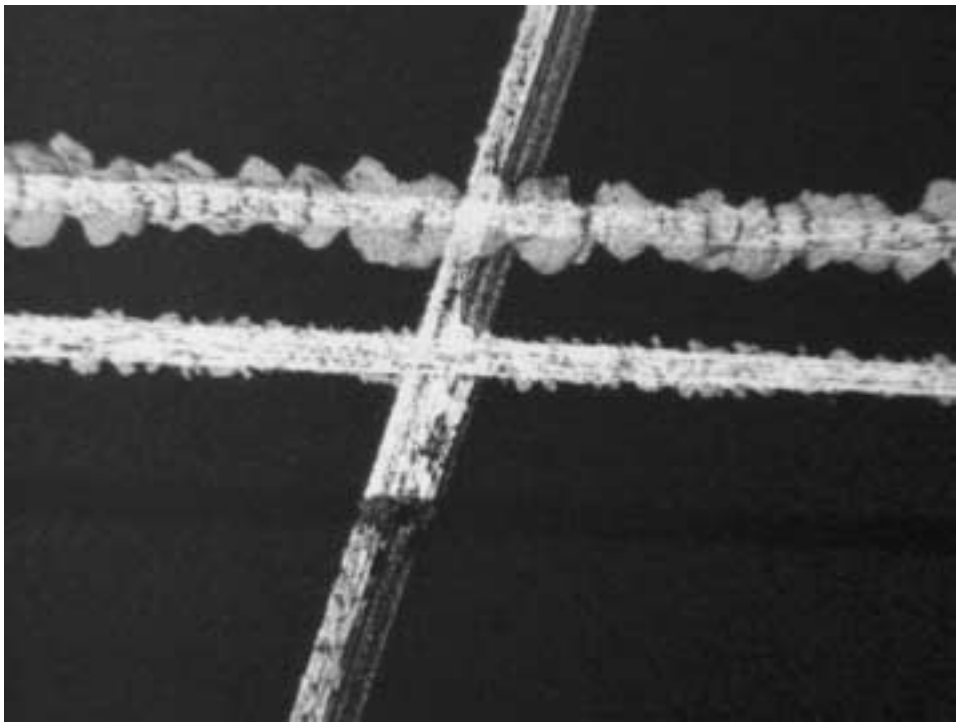

Figure 19. Optical micrograph of a patterned and scratched area analyzed by NREL.

Production losses due to the delivery of the wrong process gas were previously reported. During this subcontract period, an indium-tin target was supplied instead of an indium target. Poor circuit performance resulted from this inadvertent test of changes in the relative concentrations of precursors and the addition of tin. Another significant yield loss during this subcontract period was caused by the failure of our glass vendor to supply substrate glass as specified. These events introduced materials with extreme differences from specified materials and illustrate the vigilance required in obtaining the proper materials to achieve high yield.

Significant improvements in control of the precursor deposition process were made during this subcontract period [13]. Precursor sputtering diagnostics characterize and lead to the control of the absorber thickness and the Cu/(In+Ga) ratio (CIG ratio) which are critical parameters in production of high efficiency CIS devices. Deposition of the metallic elements of CIS on production substrates occurs sequentially from two targets in an in-line sputtering system, first from a copper-gallium alloy target

(17 at% Ga) and then from a pure indium target. The deposition rate of each target is measured using a modified quartz crystal technique; a quartz crystal is run through the sputtering system twice, the first pass for deposition of the copper-gallium film only, and the second for the indium film only. The resonance frequency of the quartz crystals is measured outside the vacuum system before and after each deposition pass and the thicknesses of copper-gallium and indium layers are calculated based on frequency differences before and after the depositions.

A set of 10 crystals is distributed across a substrate to characterize the uniformity of deposition across the substrate width. This is especially important since a shift in deposition uniformity for either deposition can lead to regions of unacceptable CIG ratio even when the average composition appears acceptable. This measurement procedure is executed at the beginning of each production run to set the sputter rates within specifications. The measurement procedure is then repeated after a run of substrates for production. These pre- and post-run deposition rate data are the basis for production process control. A model including the effects of changes in sputter rate with target age predicts how sputter rates and thus CIG ratio drifts during a run of substrates. This model is applied to define the maximum duration for a run of substrates and determine when it is appropriate to change targets [13].

In addition, process R&D for performance improvements and capacity scale up has included:

- Addressing major yield issues such as scratches, mechanical yield, operator errors, and equipment malfunctions and improper setup
- Demonstrating and addressing loss of FF with lamination related to capacity scale up of the CdS deposition process.
- Background exploration of XRF analysis as a replacement for measurements using quartz crystals to monitor the Cu/(In+Ga) ratio for precursors
- Qualification of new vendors for precursors.
- Demonstration and addressing performance losses related to the use of plastic boxes for transporting plates.
- Exploring the possibility of replacing CVD ZnO with sputtered ZnO.
- Qualification of a new continuous light-source tester for 1x4 ft. circuit plates and the elimination of an outdoor light exposure prior to circuit plate measurement.

National CIS R&D Team Participation

The dependence of transient effects on circuit fabrication process have been examined in collaboration with NREL TFPPP Teams and as studies at SSI extending results from Team activities. The NREL TFPPP "Transient Effects Group" is composed of representatives from industry, NREL and universities:

Joe delCueto	NREL
Joe Cuiffi	Pennsylvania State University
Neelkanth Dhere	Florida Solar Energy Center
Keith Emery	NREL
Pamela Johnson	Colorado State University
Rommel Noufi	NREL
Larry Olsen	WSU
Kannan Ramanathan	NREL
Angus Rockett	University of Illinois

William Shafarman	Institute of Energy Conversion
James Sites	Colorado State University
Dale Tarrant	Siemens Solar Industries
Hong Zhu	Penn State University

SSI's participation in Team activities is focused primarily on understanding the fundamental mechanisms responsible for transient effects in CIGS-based devices with the objective of eliminating or minimizing their impact. Buffer layer technology is directly related to transient effects and alternative buffer layer approaches are also of particular interest for process scale-up. Therefore, team objectives also include defining improved buffer layer processes. Summarizing results for all of the extensive team activities is not attempted in this report since the expertise for most team activities resides with the team members.

As an example of team activities, data from SSI/NREL collaborations related to buffer layers and transient effects were analyzed and discussed with the "Reliability & Transient Effects in CIS-Based Cells and Modules" subteam of the National CIS R&D Team. Kannan Ramanathan (NREL) defined and executed an experiment exploring the influences on SSI absorbers of a KCN etch prior to CdS deposition and annealing in air at 200°C after completion of device structures. The following chart (Figure 20) indicates that FF improves with etching and air annealing. Samples of these devices were distributed to other team members for further study of transients.

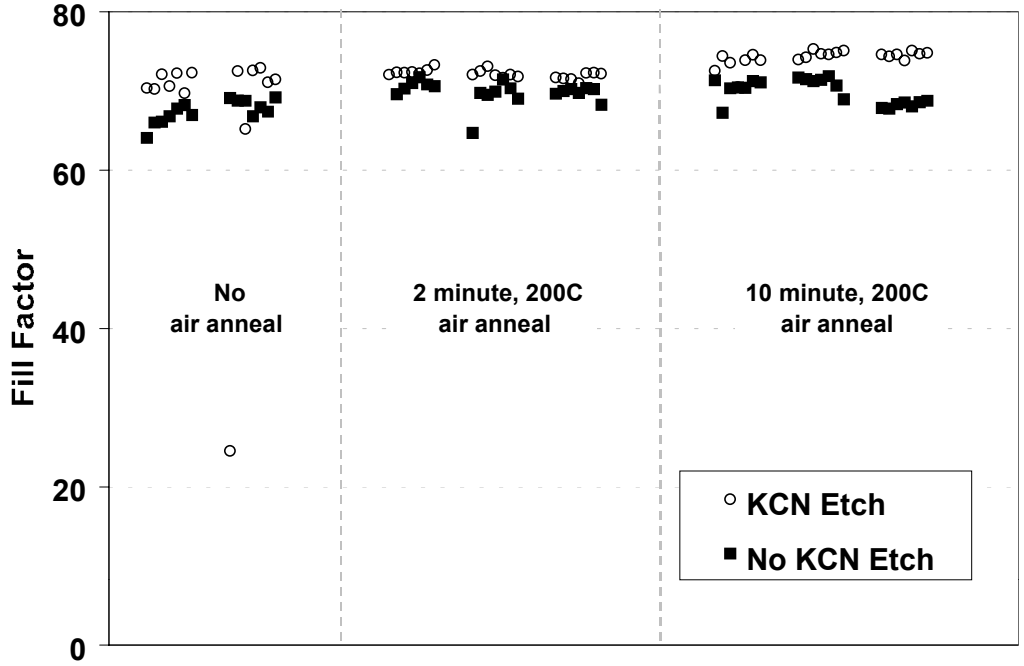

Figure 20. Data from SSI/NREL collaborations related to buffer layers (Abscissa – module Identifier)

Deliverables

The following are the deliverables for this subcontract period:

D3. End of the 24th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10%.

D4. End of the 24th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10% for the NREL Module Testing Team.

Twenty (20) ST-40 modules were shipped to Steve Rummel at the NREL OTF. These modules were taken from the warehouse and are representative of the mid to upper portion of SSI's normal production distribution. Ben Kropowski (NREL) discussed the use of these modules with others at NREL and tentatively identified applications for a large portion of the modules (PERT, long-term test bed, outdoor lighting applications). Steve Rummel (NREL) measured the modules (Test Report #2K0102) outdoors and using continuous and pulsed solar simulators (SOMS, LACSS, SPIRE). The following chart (Figure 21) of NREL (SOMS) versus SSI measurements indicates excellent agreement between SSI and NREL measurements. All of these modules are over 11% based on an aperture area of 3629 cm^2 and two of these production modules slightly exceed the NREL confirmed 12.1% conversion efficiency for large area modules.

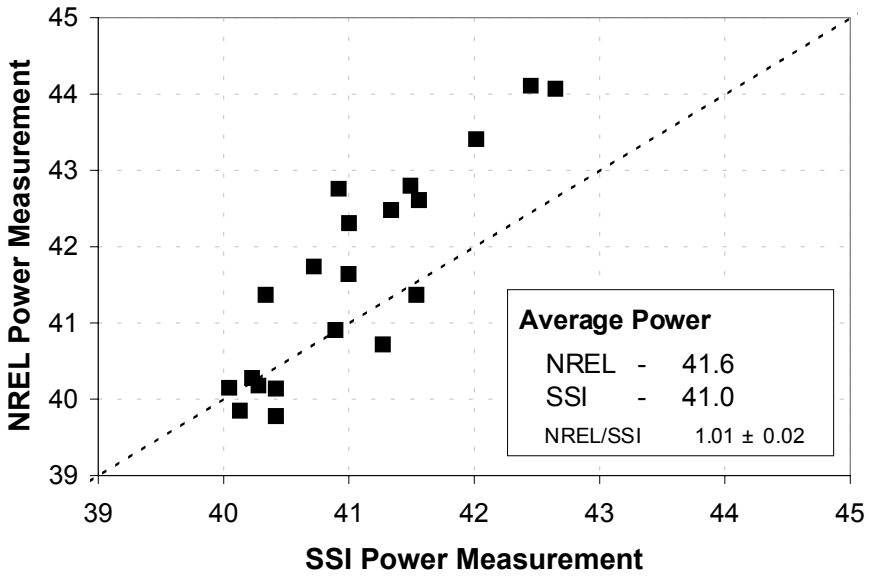

Figure 21. Correspondence between NREL and SSI measurements for deliverables.

Product Durability

NREL supports SSI through long term testing of arrays and individual modules at the NREL Outdoor Test Facility (Joe delCueto, NREL). SSI has supplied modules of increasing size and efficiency for testing since 1988. The measurements in Figure 22 were made by bringing the modules indoors, performing the measurements under standard test conditions using a pulsed solar simulator, and then returning the modules to their outdoor test location. Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules have undergone testing for over twelve years.

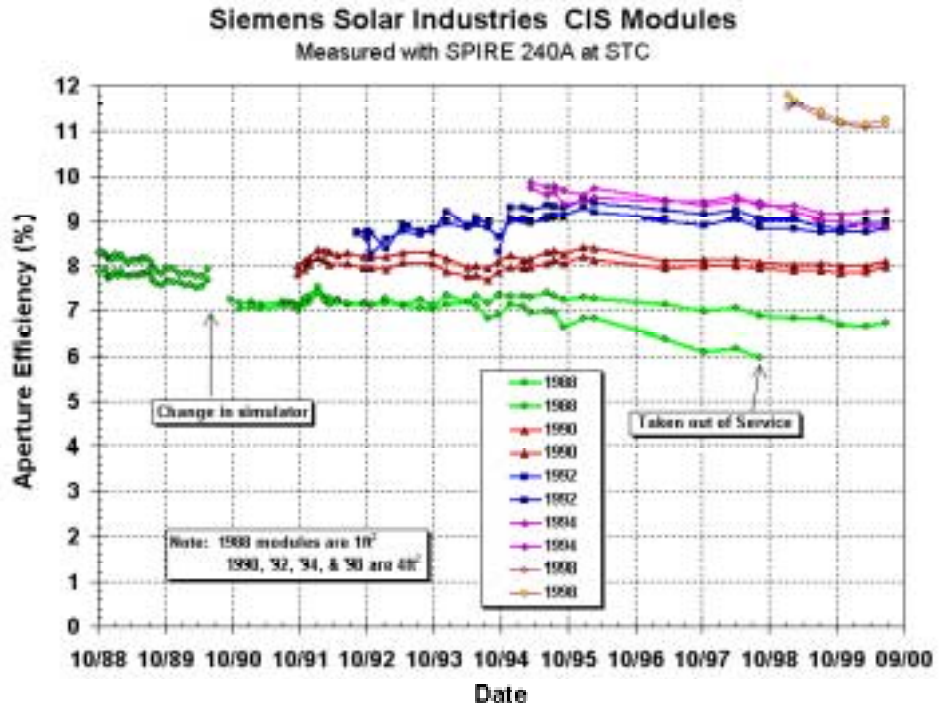

Figure 22. NREL OTF long term outdoor stability measurements - pulsed solar simulator.

NREL measurements for long term stability testing include both measurements made using a pulsed solar simulator and measurements made outdoors near standard test conditions. The data in Figure 22 was obtained using a pulsed solar simulator and might be interpreted as showing performance variation with time. However, the effects of voltage bias history and light bias history for these modules that exhibit transient effects confound the interpretation of data particularly for pulsed solar simulators [3]. Parallel data from NREL outdoors measurements near standard test conditions is presented in Figure 23 and indicates much less variation in performance with time for all modules tested.

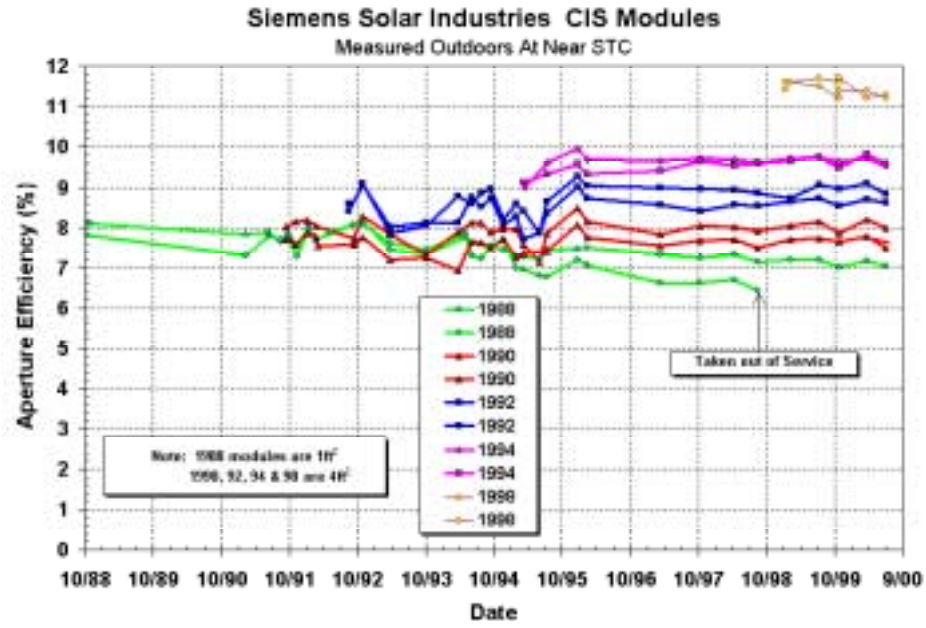

Figure 23. NREL OTF long term outdoor stability measurements - outdoors measurements.

SSI has supplied modules to the NREL OTF for three 1kW arrays. In each case, a newer generations of modules has been used to replace older designs using the same test site. The third 1kW array of modules was installed on November 17, 1998, and data acquisition started on November 18, 1998. The system is comprised of 28 modules with an average efficiency of 11.4% at STC. The aperture area of each module is 0.3651m^2 and of the total array is 10.2 m^2. The array is fixed at a 40° tilt aligned true south and is connected to a resistive load through 3 maximum power trackers. Data from late February of 2000 indicates stability within 2% of the measurements made shortly after array deployment (Ben Kroposki, STR00SSI.001).

Conclusions

CIS process R&D has achieved outstanding progress toward NREL/DOE goals:

- SSI introduced two new CIS products to the SSI ST family of products including an approximately 1x4 ft, 40Wp module.
- R&D Magazine awarded the prestigious R&D 100 Award to SSI, NREL, and the CEC for the SSI family of CIS modules.
- The first subcontract deliverables were larger and higher in efficiency than specified in the SOW.
- The first subcontract milestone was met by the first deliverables - scale from a substrate size of approximately 900 cm^2 to a substrate size of approximately 4000 cm^2 (4 ft^2).
- NREL confirmed a world-record 12.1% conversion efficiency large area (3651 cm^2) thin-film module.
- Capacity has been increased by nearly an order of magnitude while also increasing the average efficiency of 1x4 ft circuit plates from 10.8% to 11.6%.
- The distribution of production modules is sharply peaked at nearly 11% efficiency with a full width of only ± 0.5%; almost all production modules efficiencies are above 10%.
- The second subcontract milestone was met for one month of production during the last month of the second phase - pilot production rate 500 kW per year.
- The second set of contract deliverables, 20 ST-40 modules, demonstrate high efficiency for SSI's normal production. All of these modules are over 11% and two of these production modules slightly exceed SSI's previously confirmed 12.1% world-record conversion efficiency.
- Process R&D tasks have been addressed for *all* processes by applying systematic research, development and, production methodologies such as SPC, ANOVA and DOE.
- Performance and capacity scale-up achievements have been made even though more R&D resources than anticipated were expended on process development for new absorber formation reactors.
- Generally good process control has been demonstrated while scaling up capacity. Successes addressing issues at each increment in capacity has demonstrated the importance of cycles of learning for process R&D.
- Yield improvements have been made by implementing improvements in processes and manufacturing protocols.

- Process R&D has led to the demonstration of improved laser scribe quality and consistency for previously existing and new high throughput sputtering equipment. This know-how is largely responsible for defining a Mo deposition process for new sputtering equipment and improved circuit electrical yield from about 90% to typically above 95%.

- FM and UL approval was obtained for the ST series of products.

- Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules have undergone testing for over twelve years.

- SSI capabilities are leveraged as a Technology Partner participating in NREL team oriented TFPPP activities to address near-term to longer-term R&D topics. Additional NREL support has included specialty device and material measurements, and long term testing of arrays and individual modules at the NREL OTF.

CIS has demonstrated the prerequisites for a commitment to large scale commercialization – high efficiency, long-term outdoor stability, and attractive cost projections. Remaining R&D challenges are to scale the processes to even larger areas, to reach higher production capacity, to demonstrate in-service durability over even longer times, and to advance the fundamental understanding of CIS-based materials and devices with the goal of further efficiency improvements for future products.

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13. ABSTRACT *(Maximum 200 words)* This report describes the objective to establish reliable high-throughput, high-yield thin-film deposition processes to make CIS a viable option for the next generation of photovoltaics. Outdoor testing, accelerated environmental testing, and packaging development progressed throughout all phases of this subcontract. Siemens scaled up substrate size and scaled up production capacity of the baseline SSI CIS-based module process while introducing CIS-based products. The primary goals of this subcontract are to scale the substrate size from about 900 cm^2 (1 ft^2) to about 4000 cm^2 by the middle of the Phase II, and to achieve pilot production rates of 500 kW per year by the end of Phase III. Deliverables for the subcontract include CIS-based products and representative modules delivered to the NREL Module Testing Team for outdoor testing and evaluation. SSI will continue mid-term and longer-term thin-film R&D with the goals of:

- Assuring future product competitiveness
- Improving module performance
- Reducing cost per watt assuring product reliability.

14. SUBJECT TERMS: PV; $CuInSe_2$-based; encapsulated module efficiencies; scale up; substrate; baseline reactor; thin film; CIS

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