Subcontractor Report

March 2002 • NREL/SR-520-31722

PVMaT Cost Reductions in the EFG High Volume PV Manufacturing Line

Final Subcontract Report
5 August 1998—4 February 2001

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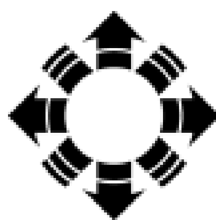
M. Ouellette, B. Piwczyk, M. Rosenblum,
and B. Southimath
ASE Americas
Billerica, Massachusetts



National Renewable Energy Laboratory

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ASE Americas
Billerica, Massachusetts

NREL Technical Monitor: C.E. Witt

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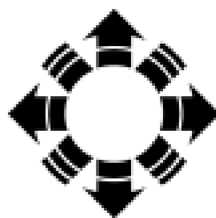

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Summary

The 3-year PVMaT 5A2 program at ASE Americas addressed topics in three major task areas:

- Manufacturing systems development
- Low cost processing technology
- Flexible manufacturing methods.

The objectives were as follows:

- Decrease electrical and mechanical yield losses by 10% each
- Reduce chemical consumption and waste products in manufacturing by 10%
- Develop procedures for certification in ISO 9001 and ISO 14001
- Develop low damage, high speed laser cutting methods
- Evaluate wafer production from large diameter EFG cylinders and polygons with wafer thicknesses down to 95 microns
- Develop low damage, high speed laser cutting methods
- Investigate cell designs for >15% cell efficiencies on 100 micron thick EFG wafers
- Develop Rapid Thermal Processing (RTP) for thin high efficiency EFG cells
- Develop and introduce flexible manufacturing methods for manufacturing floor diversifications in wafer size and module design
- Demonstrate new module encapsulants, designs, and manufacturing technologies
- Develop Root-Mean-Cause-Of-Failure methodology for modules using field studies

Significant accomplishments in this program have been:

Manufacturing Systems:

- Increase in average cell line efficiencies by 0.5% absolute to 14%, reduction of cell line electrical yield losses and wafer and cell manufacturing yield losses by over 50%
- Completion of testing of new dry etching atmospheric plasma process and reduction in acid consumption and waste product generation by more than 50%
- Identification of diagnostic tools for manufacturing process improvements in areas of crack detection, stress measurement and yield tracking (collaboration with University of South Florida)
- Introduction of Statistical Process Control (SPC) charting for measurement of diffused-layer sheet resistivity, front metalization grid line widths, and interconnect bond strength.
- Completion of development of software for Total Preventative Maintenance (TPM) applications
- Completion of over 90% of documentation for ISO 9001 and ISO 14000

Low Cost Processes:

- Identification of new laser technology capable of cutting with 2x the standard speed and with reduced wafer edge damage
- Demonstration of growth of EFG cylinders with diameters up to 50 cm and thickness down to 100 microns, and fabrication of solar cells from 150 micron thick material
- Completion of R&D on furnace and laser cutting technology for producing 12.5 cm x 12.5 cm EFG wafers
- Demonstration of potential for Rapid Thermal Processing (RTP) to produce >15% EFG solar cells on thin wafers (collaboration with Georgia Tech).

Flexible Manufacturing:

- Completion of implementation of new computer-aided manufacturing data base
- Completion of diversification to 10 cm x 15 cm EFG wafers in wafer manufacturing
- Completion of the evaluation and environmental testing of improved encapsulant and introduction into full scale manufacturing to achieve 6% savings in manufacturing cost.
- Demonstration of new module designs with 10% savings in manufacturing cost
- Use of results of field studies on fracture and electrical performance of ASE modules to improve quality control in manufacturing processes
- Demonstration of superior fire resistance and class A fire rating in UL790 Fire tests with ASE encapsulant and module design

The program goals targeted an overall module cost reduction of 25% from these improvements. We anticipate that we will achieve well over a 30% reduction when all advances are incorporated into manufacturing.

1. Introduction - PVMaT 5A2 Program Overview

We give here an overview of the accomplishments in EFG manufacturing technology advancement from a three year PVMaT 5A2 program at ASE Americas, which covered the period from 1998 to 2001. ASE Americas has been engaged in a rapid scale-up of its EFG PV manufacturing capacity since 1995. Wafer, cell and module capacity grew fourfold to 4 MW between 1995 and 1997, and has continued expanding at a similar rate from 1998 to 2001. Currently wafer manufacturing is producing the equivalent of about 14.5 million 10 cm x 10 cm wafers annually. Cell and module manufacturing has grown more slowly to a 6 MW level in 2001. Planning is under way for balancing the wafer, cell and module capacities at 20 MW within the next two years. This continued expansion will start with construction of a new 10 MW cell line and addition of module capacity to reach 10+ MW in 2002.

The EFG wafer manufacturing line has diversified its production from the standard 10 cm x 10 cm wafer to a larger 10 cm x 15 cm area wafer. Under our PVMaT program, R&D has been completed for demonstration of a production technology for a 12.5 cm x 12.5 cm EFG wafer. We have attacked in our PVMaT 5A2 program a number of essential technical and organizational challenges posed by this rapid scale up, and successfully completed the planned expansions while maintaining throughput and cost goals to stay competitive in the marketplace.

Technology improvements developed under PVMaT 2A (1992-1994) and PVMaT 4A2 (1995-98) were of critical importance in supporting the early scale-up to commercial production. In the PVMaT 5A2 program at ASE Americas, we continued on a multi-faceted technology development effort aimed at implementing manufacturing line improvements to keep EFG PV products as low-cost PV leaders. We introduced and integrated design, materials and processing improvements related to all major cost elements of the EFG PV module. These elements included new generations of EFG material growth processes and laser cutting technology, more efficient cell processing, and reduced cost module construction strategies, which match key growing PV market applications.

We have continued to make improvements in our regular manufacturing facilities on many of the technology developments initiated under PVMaT 4A2. There we demonstrated and developed better silicon feedstock utilization, improved purification for graphite to help raise solar cell efficiencies, longer EFG wafer furnace run-time approaches, and optimized laser cutting technology. In cell manufacturing, we have improved on data gathering and information tracking capabilities to support and allow demonstration and testing of Statistical Process Control (SPC) methodology, and demonstrated a low cost and environmentally advantageous glass etch process which dramatically reduces fluorine ion effluents. We have continued to evaluate and develop novel module designs and to work on advanced encapsulation technologies for improving manufacturing yield and enhancing product field performance and lifetime.

In PVMaT 5A2, new technology developments have been undertaken while at the same time we worked to maintain our gains in technology during expansion of our manufacturing line. The higher capacity leverages the incremental advances and enhances the competitiveness of EFG PV products. In the following sections, we will report on PVMaT 5A2 programs in three Tasks. In the task on Manufacturing Systems we have worked on implementation and utilization of SPC on a larger scale through development of supporting systems for computer aided data bases and equipment and process tracking methodology, development and implementation of new diagnostic techniques, reduction of acid use and waste products by introduction of a new dry

etch process, and formalizing documentation and training procedures for manufacturing processes (ISO 9000) and for waste product and safety management (ISO 14000) to assist in handle the larger manufacturing organization. In the Task on Low Cost Processes, we will report on progress in demonstrating low damage, high throughput laser technology, studies on Rapid Thermal Processing approaches to improving cell efficiency, evaluation of new thin wafer technology using EFG cylinders, and development of a large EFG octagon and laser cutting technology for production of 12.5 cm x 12.5 cm wafers. In the Task on Flexible Manufacturing, we completed introduction of manufacturing data bases for wafer and cell manufacturing, process modifications to accommodate manufacture of 10 cm x 15 cm wafers, and module field performance studies and defect tracking to be used to improve manufacturing processes, new encapsulant qualification and introduction into manufacturing, and progress in development of designs for low cost modules.

2. Manufacturing Systems

This task addressed efficient manufacturing management systems essential to achieving high-yields at high production volumes. Yield goals proposed for our program were achieved with 10% reductions in each of the electrical and mechanical yield losses in our manufacturing line. Yield improvements were supported through key subtask areas, which focused on process feedback, statistical process control, diagnostic technique development, and documentation procedures and initiating efforts toward ISO 9001 and 14001 certification. These manufacturing management systems improvements help provide efficient, cost-effective manufacturing. This task was a core activity of our PVMaT 5A2 work plan. An additional goal in pursuing these manufacturing management improvements was to maintain gains while at the same time to increase production output, and to lay a solid foundation for more substantial improvements from other new technology advances in high-volume production. A further objective for this task was also to reduce chemical wastes by 10%. This goal was met through introduction of a new dry etch process. These activities are described in more detail in what follows.

2.1 Subtask - Electrical and Mechanical Yield Improvements

During the first half of our 3-year program we focused on improving electrical yield in our cell processing line, and demonstrated production line cell efficiency increases of about 0.5% absolute[1]. These improvements predominantly came as a result of optimizing process setpoints as determined from Design of Experiments (DoE), establishing Statistical Process Control (SPC) in key areas, and upgrading manufacturing equipment. Mechanical yield improvements were the focus of year 2 and 3 work. This involved in improving procedures in wafer and laser cutting areas, introducing diagnostic techniques for monitoring growth stress and laser damage, working on process standardization and documentation, and testing of computer software for equipment uptime monitoring. We first look at the accomplishments in the cell area, then in mechanical yield below.

2.1.1. Accomplishments - Cell Area

Fig. 2-1 shows the improvements made over the first year. Efforts in this area for the remainder of the program were aimed at monitoring and improving the changes implemented

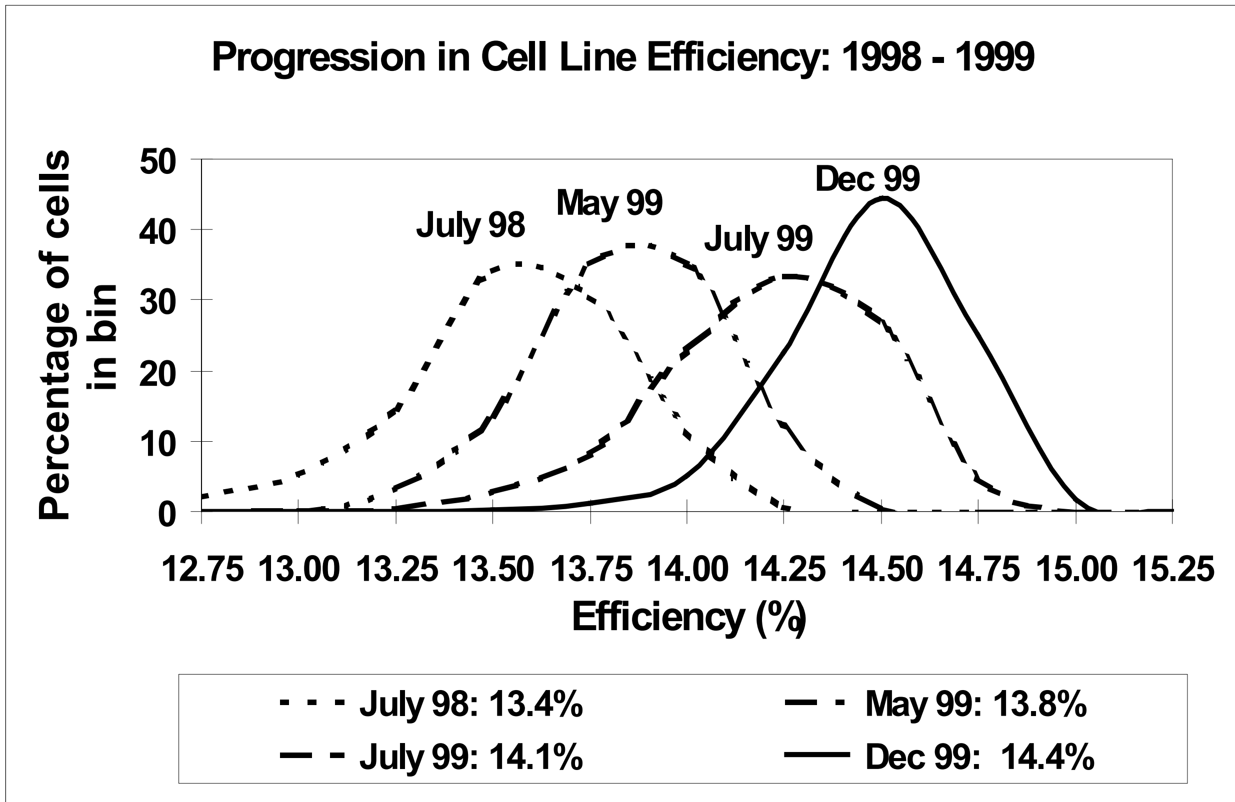


Figure 2-1. Progression in manufacturing line efficiency increase in 1998 and 1999.

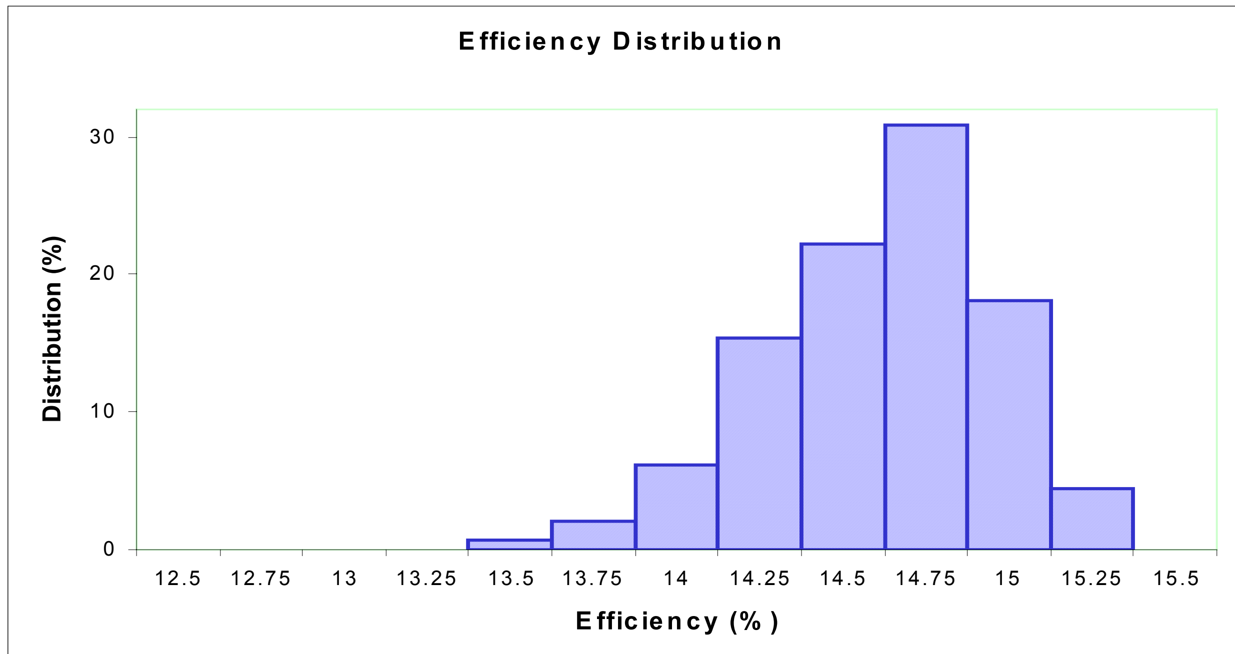


Figure 2-2. Histogram of a single lot of >250 cells averaging 14.7+%.

during a rapid expansion of other parts of our production line, e.g., wafering. Factors which contributed to these improvements in efficiency are described in section 2.1.2.

As a result of increases in average cell efficiency, individual lots of >250 cells exceeding 14.7% efficiency were achieved in production. In such lots, as many as one third of the individual cells exceeded 15% efficiency. Figure 2-2 shows the efficiency distribution for one such lot.

Concomitant with a movement toward a higher efficiency average is a reduction in the production of cells at lower efficiencies. The program efforts mentioned above tighten the efficiency distribution. Separate efforts identified resistive components in the cell tester which needed to be replaced to provide reproducible, accurate measurements of fill factor. This particularly helped to reduce the extent of the lower efficiency tail of the distribution. As the electrical yield is largely determined by how many low-powered cells are produced, the efficiency improvements simultaneously improved our electrical yield. A plot of the electrical yield throughout this program is shown in Fig. 2-3.

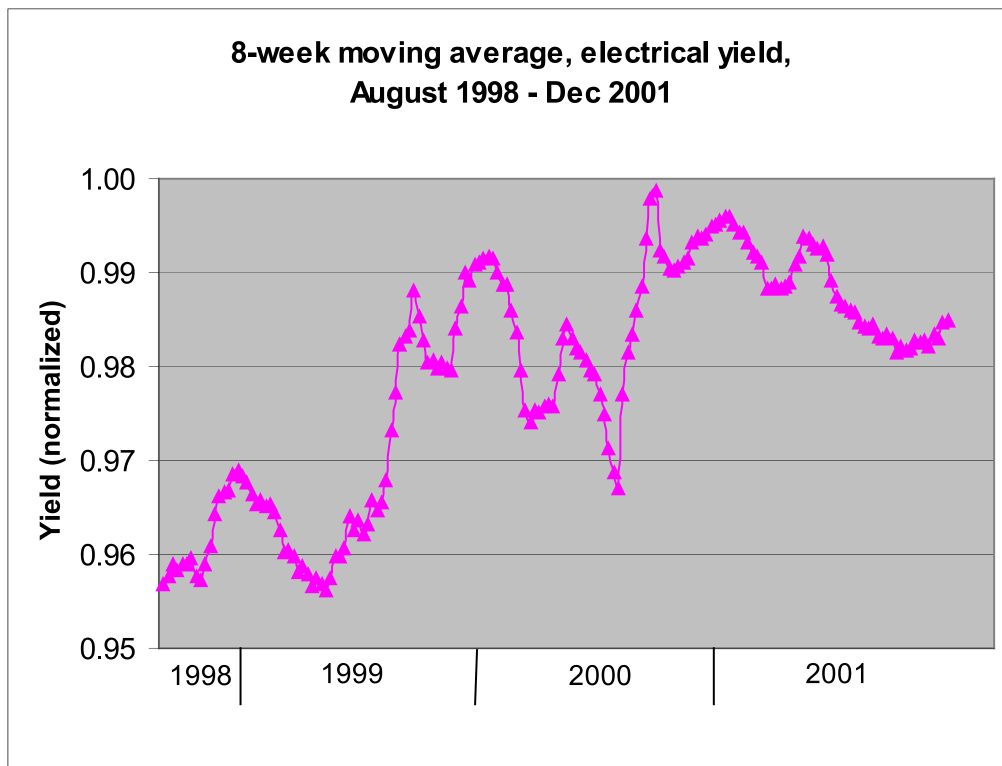


Figure 2-3. Plot of the increases in electrical yield over the 3 years of the program.

These efforts produced a 50% electrical yield loss reduction by the end of 1999 and allowed us to significantly exceed our program goal of a 10% loss reduction. At that point, our focus in this task switched to work on improvement of mechanical yields.

2.1.2 Accomplishments - Statistical Process Control (SPC) and Design of Experiments (DoE).

This task of using SPC and DoE's to improve the manufacturing of solar cells at ASE Americas falls within the goal of providing and using *efficient* manufacturing management systems to achieve high yields of quality product at high production volumes. A basic concept in SPC is that "continuous improvement" is not haphazardly made, but is targeted in a prioritized manner, focusing on those areas whose output most impacts the success of the final product.

Defining and redefining what the "key nodes" are for the processes used to manufacture a product are a continuous activity. ASE Americas --through the use of DoE's— determined which areas are key nodes, then focused on SPC charting and the use of control action plans at these areas. Accompanying the Control Charts were "Control Action Plan's" (CAP's). These are flowcharts which define what the operator should do when the process has produced an out-of-control condition. Each CAP was developed by engineering personnel with operational staff input. The CAP was then executed by the manufacturing personnel on the floor. Staff were trained on how to use and read the chart, as well as how to follow the CAP. The CAP's developed include different actions for different conditions (i.e. out-of-control high vs. out-of-control low).

DoE methodology was used to help identify the key nodes in the cell manufacturing, then to improve the areas identified. Areas of improvement included antireflection coating thickness,

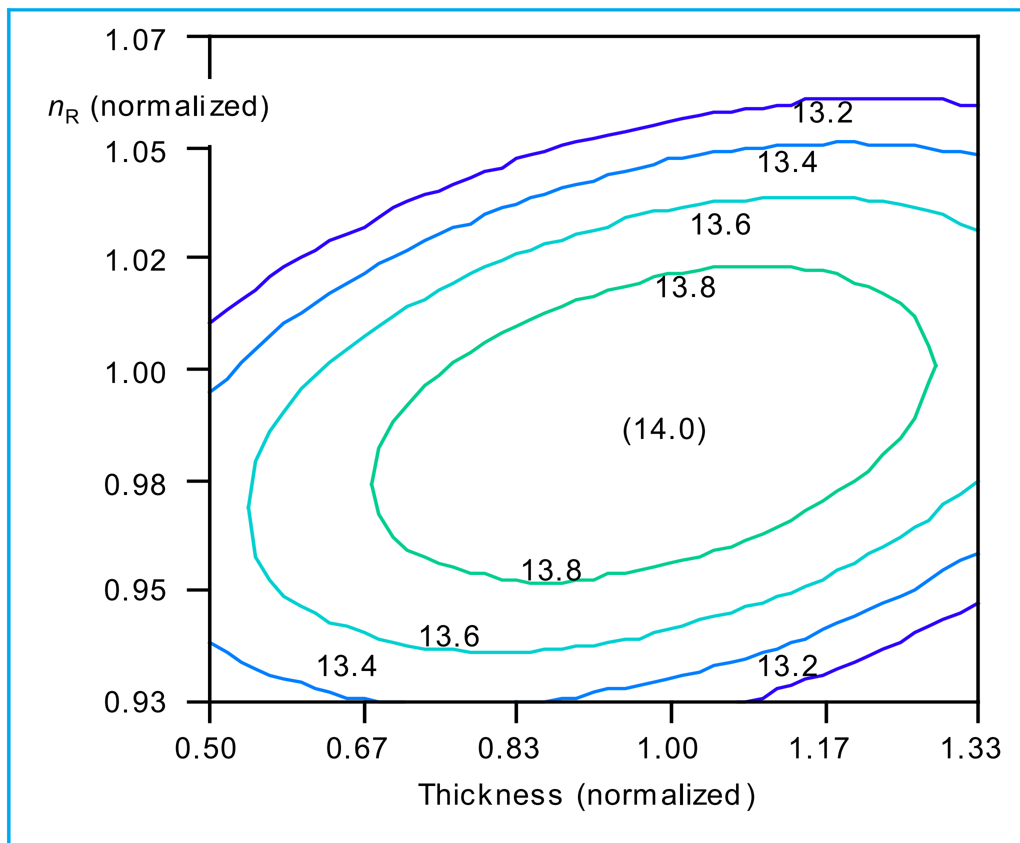


Figure 2-4. Contour plots of cell efficiency (%) as a function of the index of refraction, n_R, and thickness for a silicon nitride antireflection coating.

index of refraction and deposition process variables, cell sheet resistivity, and bulk wafer resistivity. More details of some of this work are found in Ref. [1].

The implementation of control charts was expanded to include other process steps during the course of the program. In addition to the trial areas we initiated last year in diffused-layer sheet resistivity, front metal grid thickness and busbar area, we have added short-circuit current at cell test, and laser flashlamp lifetime charting this year. Examples of DoE study results are provided in Figs. 2-4 and 2-5.

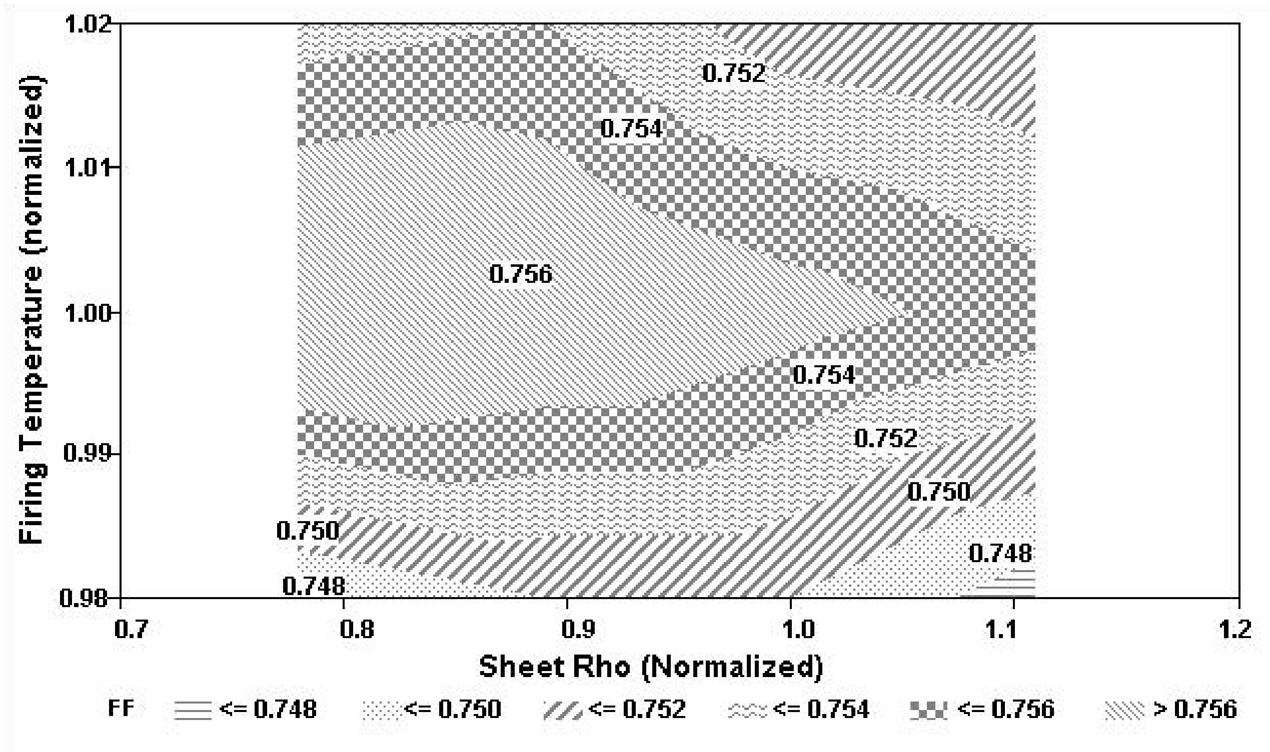


Figure 2-5. Contour plot of Fill Factor vs diffused-layer sheet resistivity and metalization firing temperature.

2.1.3 Accomplishments - Mechanical Yield Improvements

In the second year of the program, we initiated programs to improve the mechanical yield, which succeeded in exceeding our program target of a 10% reduction in mechanical yield losses throughout the wafer, cell and module fabrication areas. The improved yields were maintained in the third year of the program, as demonstrated in Fig. 2-6.

Yield improvements in wafer manufacturing were achieved with the help of new developments of a number of diagnostic techniques. Feasibility studies were carried out on crack detection methods, residual stress measurement and yield loss monitoring on-line using a flatness measurement technique. A plot of yield gains made in wafer manufacturing over the latter part of the program are shown in Fig. 2-7. Overall yield losses, determined by a number of growth related factors, were decreased by over 50%, far exceeding the program target of 10%.

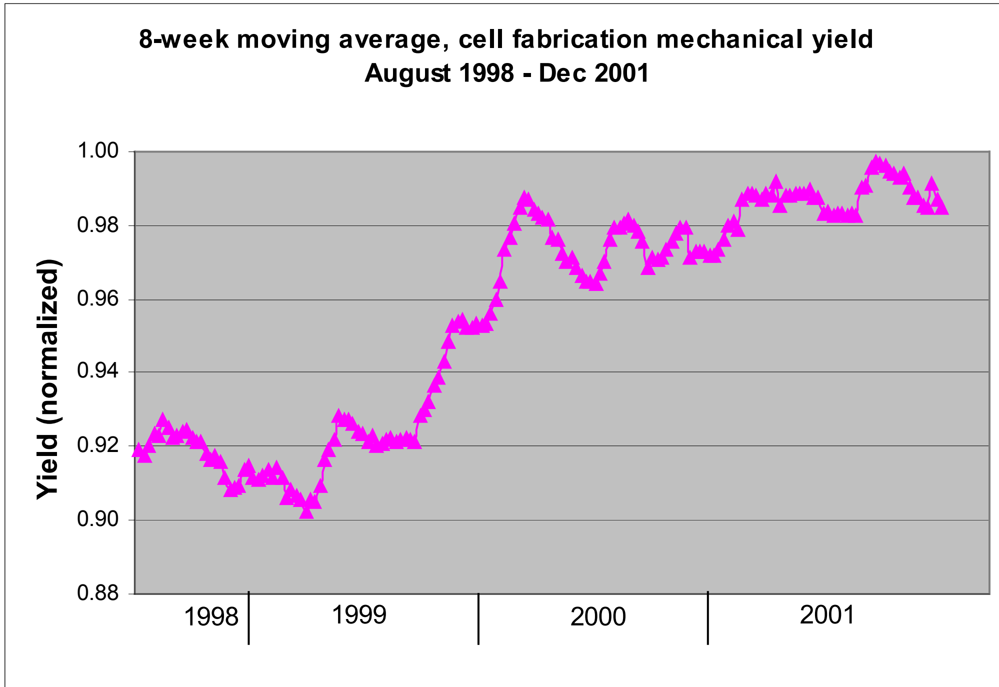


Figure 2-6. Improvements in cell fabrication mechanical yield over the three years of PVMaT 5A2.

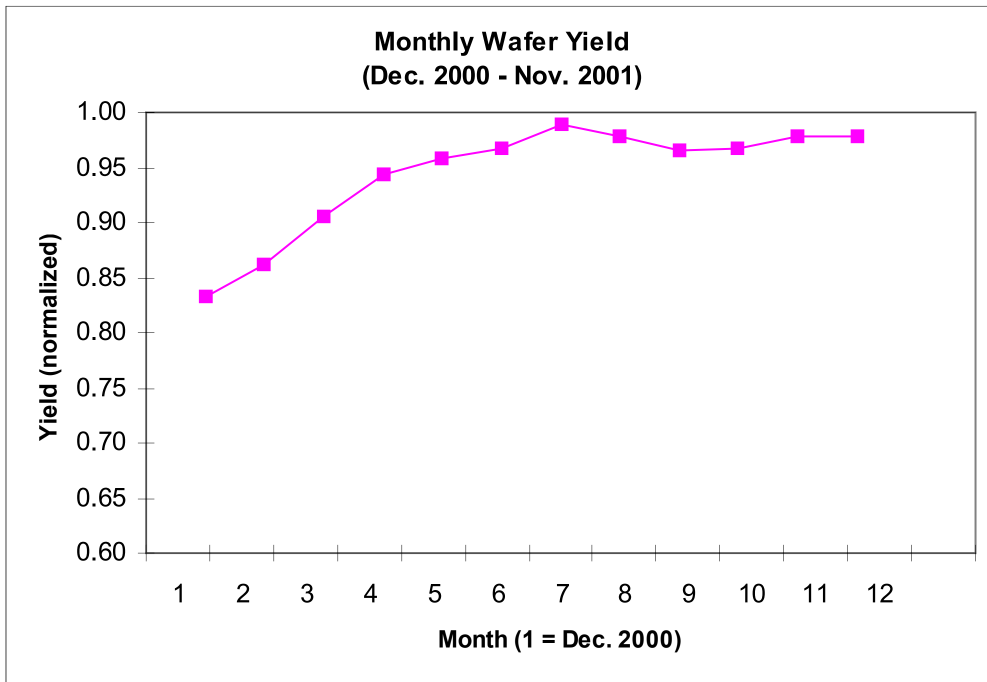


Figure 2-7. Normalized wafer yield from 12/00 to 12/01.

2.1.4 Accomplishments – Diagnostic Techniques

Exploratory programs were started to develop new diagnostic techniques and equipment for monitoring various steps in the manufacturing line. As volumes increase in production, it becomes increasingly important to have available in-line measurement methods, or statistical methods which can be applied on a daily basis. Timely application of these techniques must be implemented in order to prevent production of out-of-specification product. Two areas of diagnostics implemented in earlier programs were fracture testing of wafer edge quality and strength and a pull test for solder bonds. We developed additional diagnostic techniques and qualified methods to help in diagnosing wafer area problems in this task. The current status of these methods is described next.

2.1.4.1. Wafer fracture. Fracture during cutting and processing is a significant contributor to productivity losses in manufacturing. We initiated under this task a study to identify the causes of mechanical yield loss for wafers throughout the crystal growth and laser cutting areas. The initial work set up a baseline on the regular size 10 cm x 10 cm wafers. The goal of this work was to improve understanding of the processing steps which are most detrimental to fracturing wafers, and pay attention particularly to which steps both in wafer cutting and cell processing are going to be of highest concern as we produce thinner wafers.

As part of this diagnostic approach, we used a fracture twist test (FTT) to evaluate the strength of wafers after various stages of processing [2]. Our test very specifically probes for defects at the wafer edge. This test has been useful to obtain information on the population of defects in the wafers after a given processing step.

2.1.4.2. Crack detection. In the mature high speed manufacturing line, diagnostic equipment for detection of cracks will be needed at more than one process step. At this point we expect more than one technique will be needed as there are different requirements in different locations of the line. Cracks in EFG wafers are propagated from the damaged laser cut edge into the interior of the wafers during handling and loading of carriers. They do not extend sufficiently far to be visible or to lead to fracture of the wafer into several pieces. The wafer is weakened, however, and if the cracks extend more than a few mm into the wafer then there is a high probability that it will fracture in subsequent cell processing, interconnect or module fabrication. Thus the first inspection location likely will be after the laser step, or after the subsequent etch step prior to diffusion. Other locations where crack detection may be required are midway through the cell line, and at interconnect. We have developed both ultrasonic and optical metrology of crack detection to determine the feasibility of their application in high speed manufacturing. A description of both these techniques follows.

Ultrasonic detection. Development of an ultrasonic method to inspect for cracks under a lower tier subcontract at the University of South Florida (USF) was carried out in this program [3]. We are now planning to build test equipment for a large scale evaluation of the method under production line conditions. The method has shown promise for observing different acoustic features in wafers with various stress values. Standard acoustic equipment used for Cz silicon was modified in order to accommodate the EFG wafer, and a technique developed to use measurements of the harmonic vibrations of the wafer rather than the sub-harmonic.

As an example of the method, in Fig. 2-8 we show two radial scans of the harmonic amplitude measured by scanning acoustic probe above the wafer starting from the corner towards

the center. Two curves represent identical line-scans measured with and without the wafer. The acoustic field of the transducer has relatively higher amplitude at the wafer center, while at wafer periphery close to the corner the wafer vibrations give a major contribution to the f-signal (harmonic). These locations at the wafer corners were used in the subsequent scans. The harmonic acoustic amplitude differs from corner to corner in EFG wafers. This can be a result of residual stress. One can anticipate that in a stress-free wafer these amplitudes will be close to

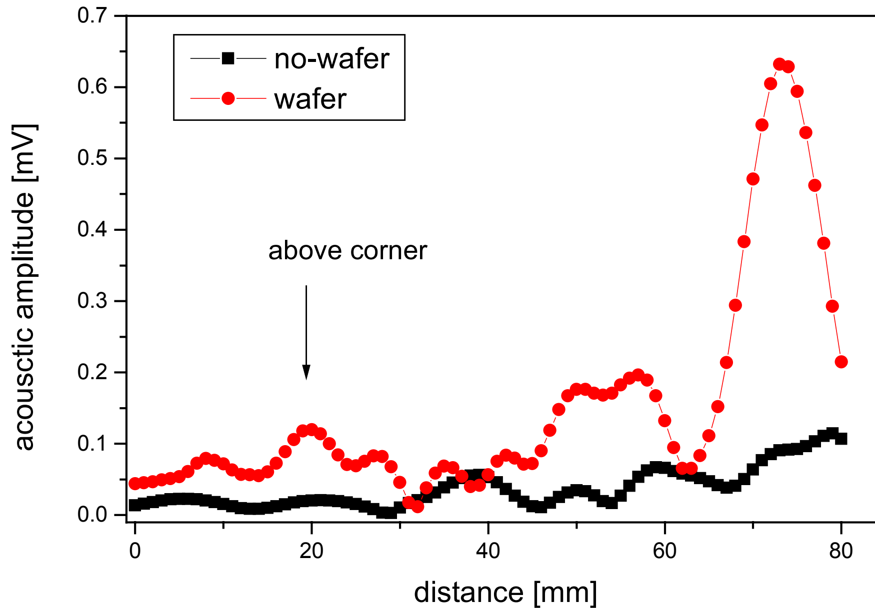


Figure 2-8. Line scans of the f-harmonic along wafer diagonal (courtesy of S. Ostapenko, USF).

each other. We have also compared the acoustic signal in low and high stress wafers, as measured by another diagnostic technique (see section on residual stress below). In the higher stress wafer, the width of f-scans (full-width at half maximum, FWHM) is larger compared to those in the lower stress wafer. To confirm these results will require a statistical approach on a significant set of samples with larger variation of the stress from wafer to wafer.

In Fig. 2-9 we plot the acoustic amplitude for the four corners versus average stress for the high-stress (6.3 MPa) and low-stress (2.5 MPa) EFG wafers. This diagnostic technique now has to be developed further through measurement of a larger number of wafers to establish a statistical basis for this diagnostic.

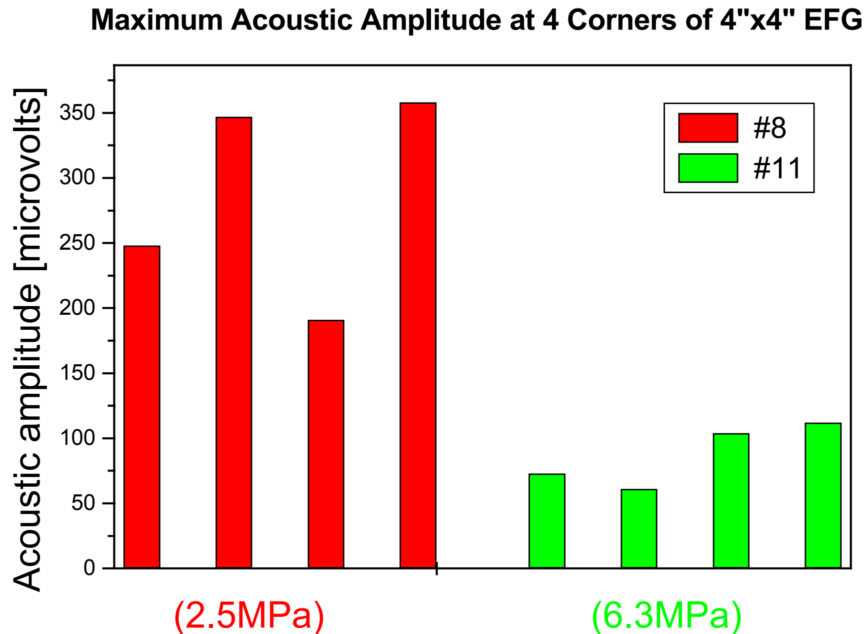


Figure 2-9. Acoustic amplitude at corners for high and low stress EFG wafers (courtesy of S. Ostapenko, USF).

Light Metrology. A second technique for detecting cracks, which was investigated in this program, was a laser-based method. In this approach, cracks are detected via transmitted light using a diode detector. This method works well as long as the crack plane is perpendicular to the surface of the wafer. At the conclusion of this program, initial studies had been completed with a subcontractor at the State University of New York – Stony Brook, and specifications for equipment for a more comprehensive R&D detection unit prepared.

2.1.4.3. Residual stress. *Measurement techniques for residual stress*. This is primarily needed to assist in stress reduction in crystal growth. Under a lower-tier subcontract at the University of South Florida, equipment was constructed and methods developed to provide maps of IR response of the wafers indicating areas of high strain [2]. Representative stress maps measured by IR polariscopy in the two EFG wafers used to correlate to acoustic microscopy signals above are shown in Fig. 2-10. The average stress level in this set is typical for EFG wafers and ranges from 2.5 MPa to 6.3 MPa.

In this previous study, we examined the correlation of stress with tube wall (wafer) thickness. In the crystal growth process, it is expected that the dislocation densities and residual stress will increase as the thickness of the tube wall decreases for a given external growth environment, because the temperature gradients drive the stress increase with decreasing crystal thickness. In addition we have examined the relationship between dislocation density and residual stress in a wafer [4]. There we found that regions of low dislocation density generally have higher residual stress, and visa versa.

The IR polariscopy method also has been compared with other methods of stress measurement and with dislocation mapping studies in our program. Although the feasibility of using this technique for measuring stress in EFG wafers is proven, additional work needs to be done to make IR polariscopy a practical diagnostic method for wafer analysis.

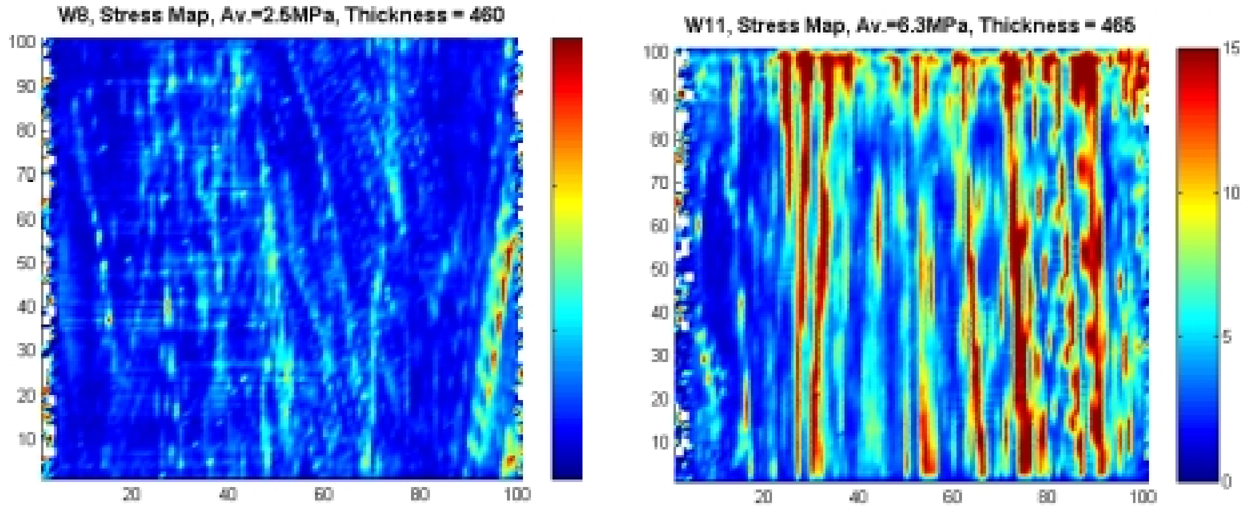


Figure 2-10. Stress distribution in two EFG wafers (courtesy of S. Ostapenko, USF).

In Situ tube flatness monitoring. We have installed and are operating a set of capacitance sensors in the crystal growth furnace to provide traces of the surface profile of the growing tube. The flatness measurement reflects the extent of the stress acting on the tube during growth, and these sensors can measure deviations from flatness with a sensitivity of about 25 microns. By getting real time data on the deviations from flatness, we can develop a feedback loop to temperature settings in the furnace and correlate changes in operating conditions or furnace hot zone configuration to temperature fields and stress. We have developing an on-line Fast Fourier Transform (FFT) capability in real time to assist in this analysis.

A typical trace for the surface profile of a growing tube in an experimental growth furnace given by one such capacitance sensor is shown in Fig. 2-11. The wall position in this figure denotes the distance between the sensor and the face of the octagon, while the abscissa is the length of octagon grown. In this figure, it can be seen that the buckles are very regular, and their amplitude decreases as the octagon tube length increases. Initially, the peak-to-peak amplitude of the buckles is about 1.5 mm. A mechanical perturbation of the tube has occurred at about 62 in of growth which is not associated with stress but is from the puller system. Such displacements do not lead to yield losses. After this perturbation, the regular buckle pattern appears to be interrupted and deteriorates.

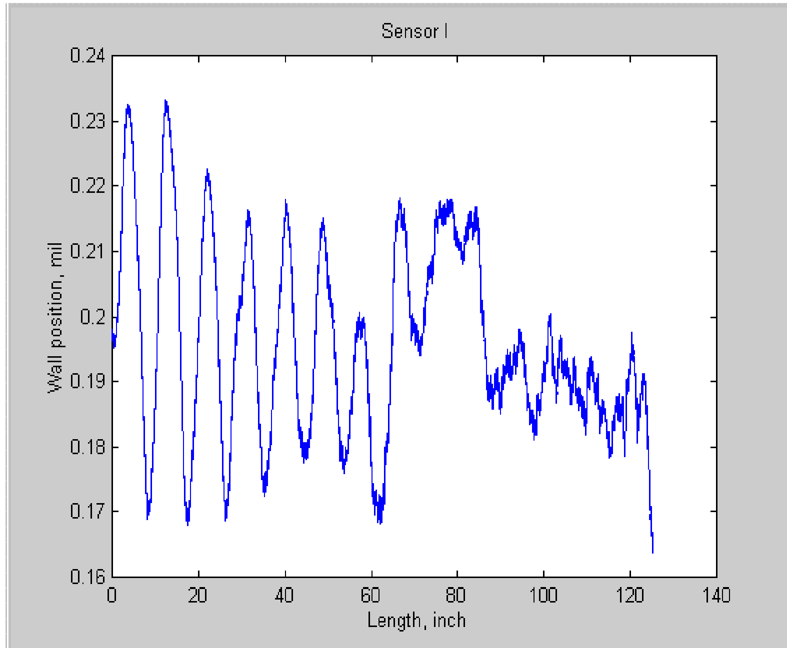


Figure 2-11. Capacitance sensor measurement of position of the surface of a growing experimental octagon tube.

The Fast Fourier Transform (FFT) analysis of the buckle pattern in Fig. 2-11 is given in Fig. 2-12. This shows the major buckle period is in the range of 8-10 in., or 20-25 cm, about twice the width of the 10 cm octagon face. We observe more distinctly in other data a Fourier component at about half this period, or 4.5 in (9 cm) which becomes dominant at higher stress levels. There currently is no theory available that can account for this periodicity.

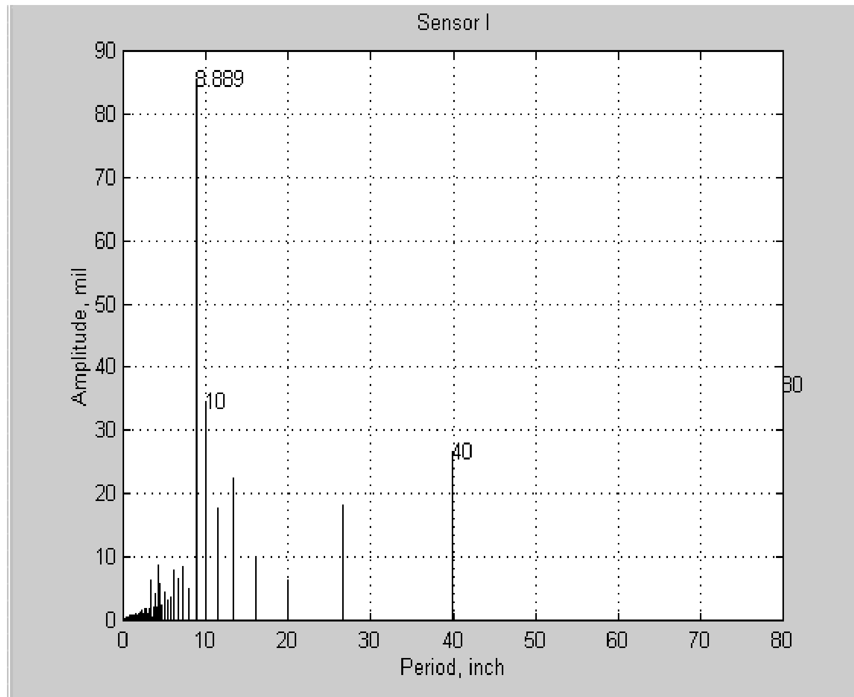


Figure 2-12. Fast Fourier Transform (FFT) spectrum of buckle pattern in Fig.2.11.

Process automation can now proceed when confidence is obtained in the reliability and ability to calibrate these sensors. We plan to develop this measurement system into an in-line process control capability for the EFG growth system. The signal processing and analysis software for the FFT measurement was developed at the University of South Florida.

2.2 Subtask - Chemical Waste Reduction

After development of the process and testing of equipment at the vendor, we introduced a new dry etching process into our wafer manufacturing line in the third year of our program. This addressed both the mechanical yield and waste remediation objectives. The dry etch process, the atmospheric downstream plasma™ [5] (ADP) method, removes laser damage from the wafer edge, and also displaces part of the silicon acid etch.

2.2.1 Accomplishments – Dry Etching. We have acquired a plasma etch unit and installed it in our manufacturing line and demonstrated that the etching required to remove these surface residues requires about 50% less acid per wafer than what is currently used.

Figure 2-13. View of Tru-Si Atmospheric Downstream Plasma™ equipment.

A photograph of the ADP unit is shown in Fig. 2-13. The equipment to the right in this view shows the loading dock for the carousel and carriers which hold the wafers. Optimization of the process in manufacturing was completed under this subtask. We found that the plasma-etched wafer is stronger, as measured by the fracture twist test, after the plasma etch plus postplasma acid etch, than after the normal acid etch currently used. Large scale experiments in

manufacturing are in progress to examine the relationship between the stronger wafer and yield improvements in downstream processing of the wafers.

Activities under this program in this area have included design and evaluation of a number of process equipment fixtures and optimization studies. We have now fully integrated

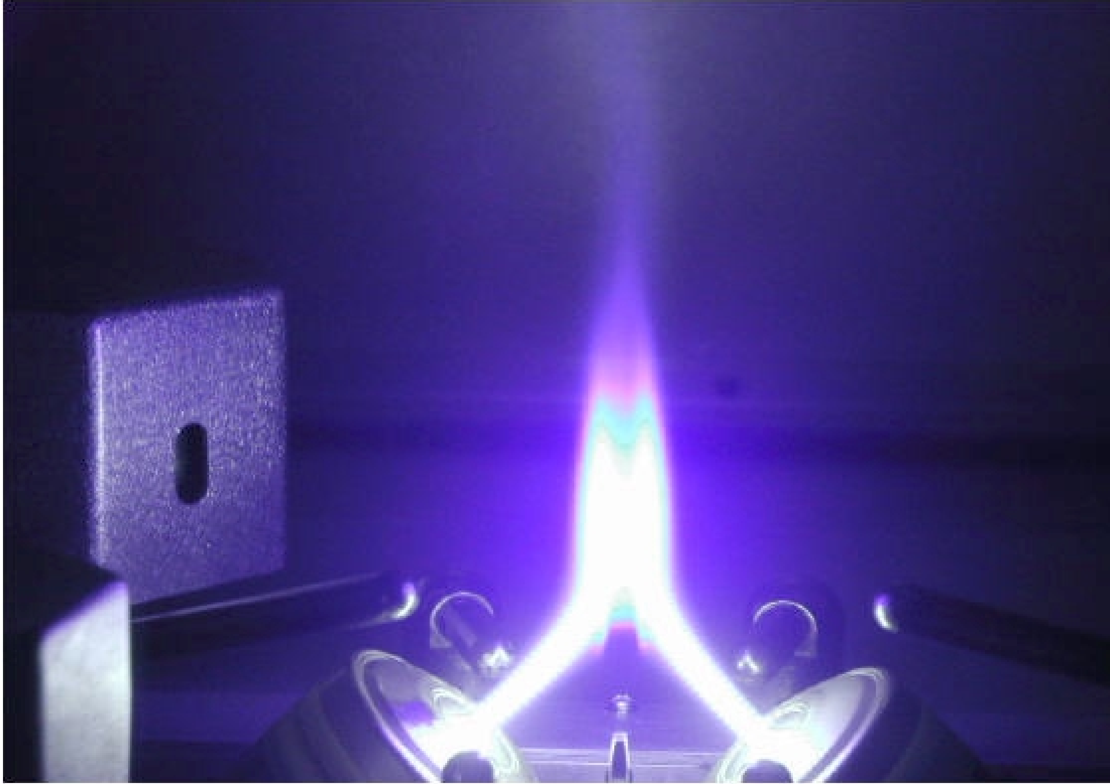


Figure 2-14. Plasma flame configuration for the ADP™ process.

plasma etching of Si into our manufacturing line to reduce acid consumption. The plasma flame configuration is illustrated in Fig. 2-14. The figure shows plasma flame, which impinges on wafers held in carriers (not shown) rotated through the upper region of the flame. Reactant gas is introduced from below in an argon carrier gas, where it then dissociates into highly reactive ion species. Coin-stacked wafers are placed in specially designed carriers and rotated through a plasma flame into which CF_4 is injected. Wafer carriers are rotated about their long axis for multiple runs, in order to expose all edges to the plasma. Etching rates of the wafer edges are significantly enhanced over conventional plasma processing.

We designed and evaluated specialized fixturing for the plasma process for both the standard 10 cm x 10 cm size wafer and the larger 10 cm x 15 cm area wafer. This design of this fixturing is very critical in obtaining a strong wafer. It was designed such that the entire perimeter of a wafer exposed to the plasma is uniformly etched. The fixture also was designed to maximize the throughput of the equipment in order to reduce overall operation costs. We have chosen to coin-stack the wafers and present the edges to the flame at an oblique angle. The carriers have been redesigned to maximize throughput and etch uniformity and the new equipment is now in full manufacturing use where studies are in progress to maximize yield and minimize acid consumption.

2.3 Subtask - Flexible Manufacturing.

Manufacturing Systems implementation in the wafer and module areas include the definition, development and implementation of quality and management systems that are built on controlled documents and calibration standards that are traceable to primary and secondary standards. Metrics for equipment performance (uptime, repair time, waiting for parts, qualification time) will be developed and tracked in the new electronic database system. These systems will add stability to the manufacturing process and will be used to document acceptable ranges of variability of all key parameters, and enable systems to come on line in a controlled fashion.

2.3.1 Accomplishments - Flexible Manufacturing

A data collection system for our wafer fabrication department was installed and improved upon during this program. Specific steps covered include Crystal Growth, Laser Cutting, Silicon Etch, and Wafer Packing. Plasma Etch was added when it came on-line. The heart of the system is a server, which collects information from computers along the 'spokes' of the network. These other computers include those on equipment itself, such as our crystal growth furnaces, and independent stations where operators enter information about group of wafers in progress, such as how many wafers entered and left a specific processing station such as the Si etch machine. Information is transferred along the regular network connections and cables, and the server is

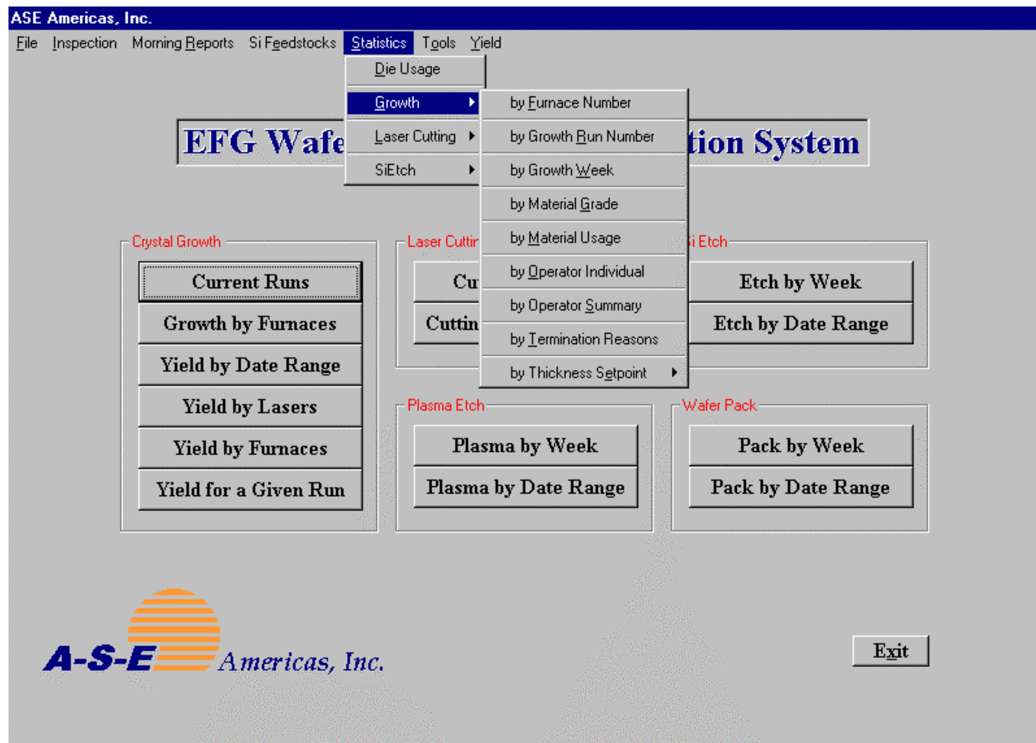


Figure 2-15. Example of submenu options available for statistical data analysis.

instructed to either poll for certain information from computers along the network at specific times, or to receive information automatically sent from the remote computers. The user interface available within the server software has been customized to allow production

supervisors and engineers to access the information stored within the resulting database. A depiction of one of the screens for interacting with the database is presented in Fig. 2-15.

2.3.2 Accomplishments – Total Productive Maintenance (TPM)

TPM comprises a number of activities whose overall aim is to minimize unplanned maintenance and to maximize productivity from the machines. It stresses a number of systematic approaches for achieving these goals, including:

- routine daily maintenance checks
- downtime tracking
- predictive and preventive maintenance
- continuous machine and process improvement
- autonomous maintenance
- greater emphasis on operator involvement in all these activities.

The largest effort for implementing TPM occurred in our Laser Cutting area. An example of downtime tracking, making use of data stored in our manufacturing database (Section 2.3.1) is shown in Fig. 2-16. Follow-up work from this and similar efforts have led to improvements in productivity in laser cutting; similar efforts are extending into other areas.

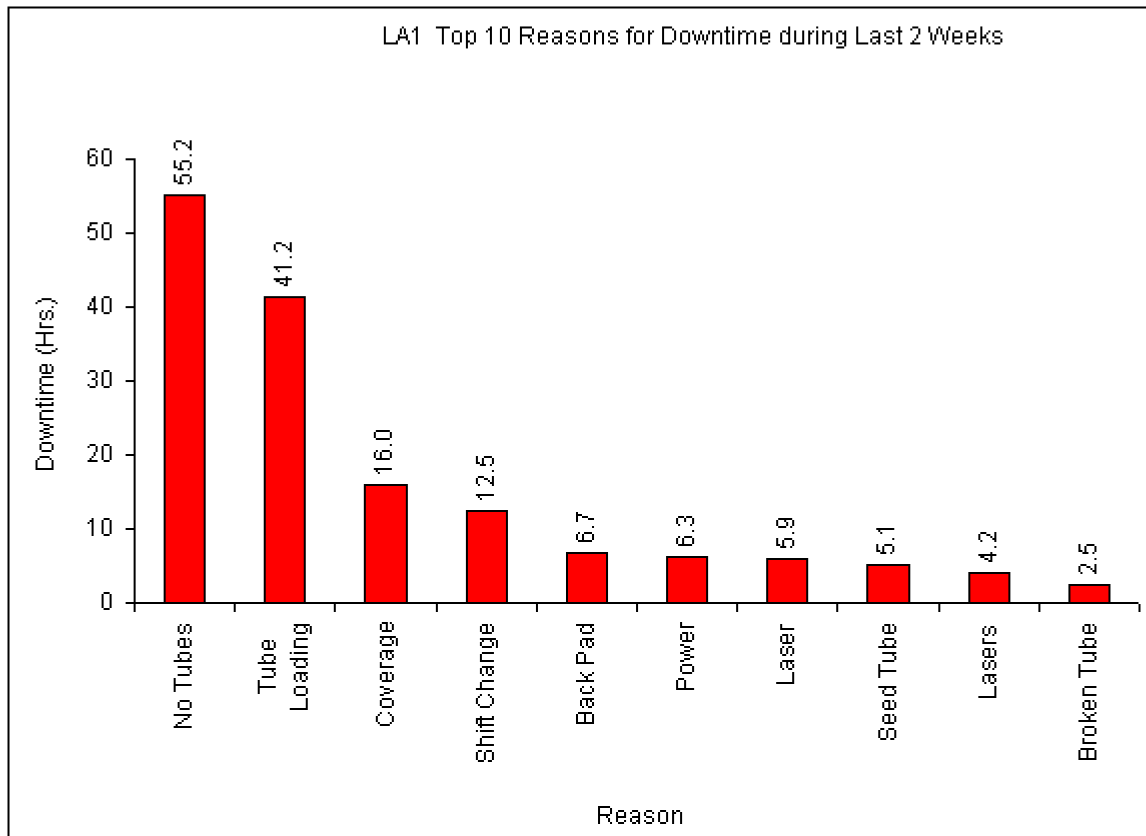


Figure 2-16. Pareto chart showing major contributing factors to Laser Cutting downtime.

2.4 Subtask– ISO 9001 and ISO 14001

This work formalized policy, documentation, training, and quality (ISO 9001) and safety and environmental issues (ISO 14001) within a framework of acceptable practices. One aim is to gain recognition for the photovoltaic industry for leadership in this area. The latter certification mandates that the manufacturing line be developed to be consistent with minimizing its effect on the environment through fundamental understanding of the chemical usage, waste and environmental impact of the manufacturing process. It also mandates a system to be developed that enables continuous improvement, training, and reporting on safety and environmental issues.

2.4.1 Accomplishments - ISO 9001 and ISO 14001

Over 90% of the work toward ISO 9001 certification, and more than 50% toward ISO 14001 certification was achieved during this program. General information about the relevance of ISO 14001 toward the photovoltaics industry and of our initial efforts has previously been described.[6]

A framework for ISO 9001, for which the basic structure applies to ISO 14001, is shown in Fig. 2-17.

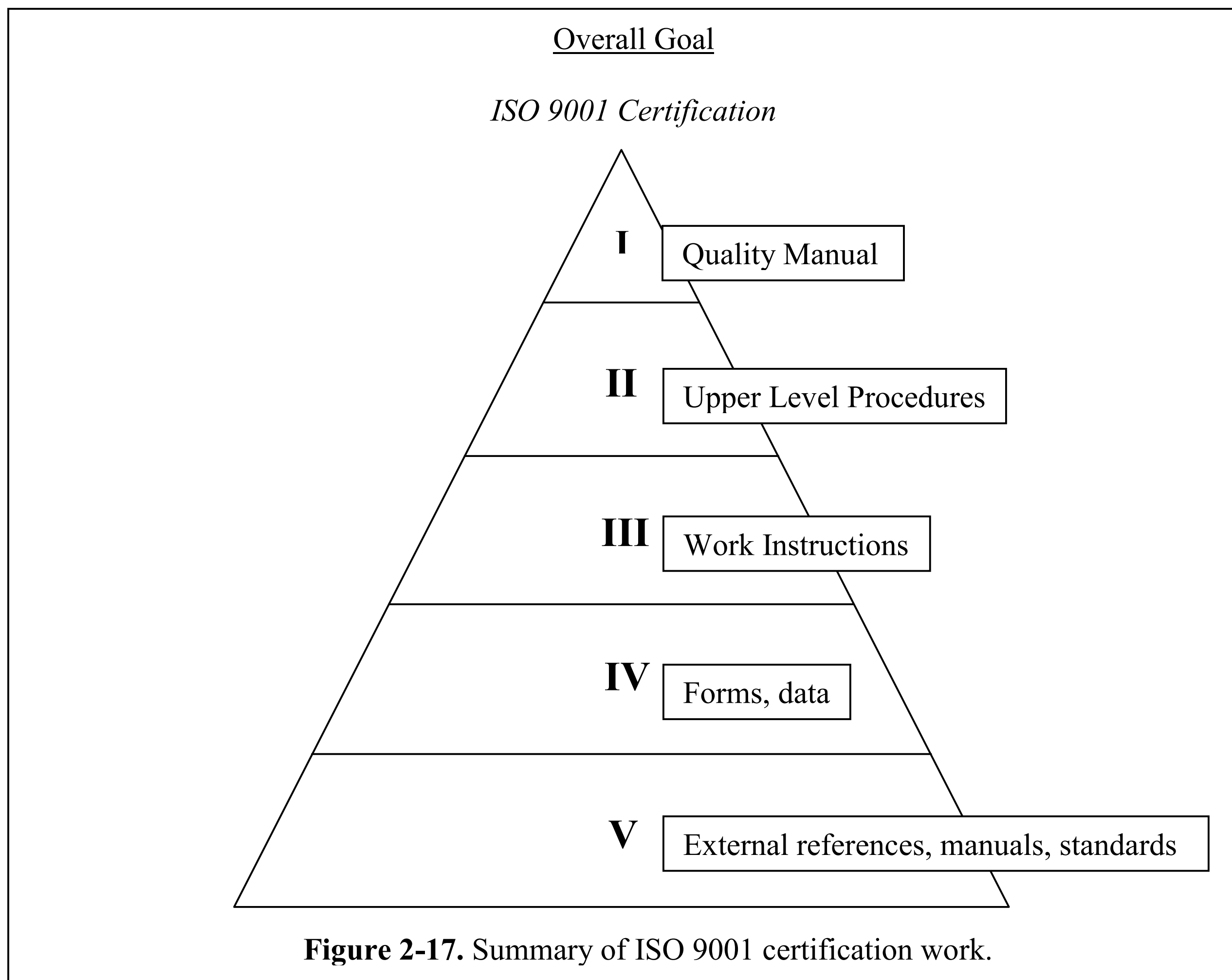


Figure 2-17. Summary of ISO 9001 certification work.

Of the different levels in the 'pyramid' of supporting layers that comprise ISO 9001 and 14001, the largest layer than needs to be created specifically to meet certification are the Work Instructions. Significant efforts were made during this program to generate work instructions throughout the company, and while formal certification has not yet been attained, the benefits have been accrued in terms of better operator knowledge, performance, and subsequently, our process performance in terms of throughput, efficiency, and yield have improved.

In the area of ISO 14001, we have more recently generated documents describing how we handle wastes and operate the equipment for its treatment, improved our database for chemical usage information, and written a formal policy statement which provides the philosophical framework for safety and environmental issues.

3. Low Cost Processes

In this Task, we developed new concepts and implemented advanced EFG technology. In the laser cutting area, we have tested a new generation of short pulse length lasers which reduce as-cut wafer edge damage, and evaluated very high speed lasers under production conditions, and evaluated options for cutting with more than one laser per station.

We explored higher-risk, higher-reward opportunities for radically reducing crystalline silicon PV module costs through introduction of new processing and thinner wafers. We investigated new cell processing approaches using Rapid Thermal Processing (RTP) techniques, to be used for manufacturing of wafers down to 100 micron thicknesses. This work was done in collaboration with Georgia Institute of Technology, and it has demonstrated the feasibility of a number of RTP processing options and achieved over 15% small area (2 cm x 2 cm) cells with RTP techniques.

We met our objectives in the first two years of the program in designing equipment for and successfully growing 50 cm diameter EFG cylinders. We cut small numbers of wafers from the cylindrical tubes using a short pulse laser specially developed to achieve low damage, and processed these wafers into solar cells to demonstrate acceptable material quality. However, we encountered several technical barriers which have led to redirection of the objectives of cylinder growth in the third year. We had planned to examine the feasibility and cost advantages of extending the diameter to 1 meter and carrying out the emitter diffusion during crystal growth in Year 3 of the program, but these technical barriers have led to redirection of the program to emphasis on growth of larger diameter EFG octagons. In Year 3 we successfully produced octagons with 12.5 cm faces, with a 25% increase in perimeter and productivity per furnace over our standard 10 cm face octagon, and developed manufacturing technology for production of 12.5 cm x 12.5 cm wafers.

A more detailed examination of the work and accomplishments follows.

3.1 Subtask - Laser Development

Improvements in laser technology are central to raising EFG manufacturing line mechanical yields and producing solar cells with thinner EFG wafers. The current EFG wafer laser cutting process introduces damage in the wafer edge. This makes the wafer susceptible to breakage, which increases as wafer thickness is decreased. The effects of edge damage are

mitigated by using a damage-removal acid etch, but this generates waste products which it would be desirable to reduce. The main aspects of our program on lasers were:

i) to evaluate new short pulse length laser technology that will provide reduced damage cutting for thin wafers;

ii) to demonstrate reductions in labor in laser cutting of current wafers, through use of high power lasers that can increase the cutting speed in production; and

iii) to reduce laser costs and costs of the laser cutting station by increasing capacity through use of more than one laser per cutting station.

In the first year of the program, we designed and constructed an R&D laser station for testing of new laser concepts. This was used in subsequent years of the program to evaluate a number of new lasers.

3.1.1 Accomplishments – Laser Development

i) Several short pulse length lasers capable of cutting with a reduced level of damage were evaluated in this program. After evaluating both the Q-Switched Nd:YAG and the copper vapor lasers in the first year of our program, we decided that neither of them could meet our program goals. Even though they demonstrated superior edge quality, the cutting speed was too slow. The former provided the best performance and was shown to be able to cut up to about 25 mm/s on the thinnest material of 150 μm thickness.

After we completed development work on several advanced laser systems we constructed a prototype fixture for demonstrating cutting of the cylinder. The short pulse length Nd:YAG laser and the Cu vapor laser both were used to cut very thin tubes. Because as-grown material stress levels were high in the cylinder, even these lasers with reduced edge damage did not result in high yield cutting. However, a number of medium size wafers 5-6 cm square were produced so that solar cells could be made from the cylinder and the material and processing techniques evaluated (see below).

ii) The first attempt to increase throughput in laser cutting was to evaluate a high power CO_2 laser in the manufacturing line. Requirements of reproducible cutting and acceptable edge quality were not met, even though this laser offered the advantage of cutting at speeds of 4x to 8x faster than the current production lasers.

A new generation of short pulse length lasers were subsequently evaluated. These have shown potential for cutting with moderate speed increases of 2x over standard cutting, but with reduced edge damage. Optimization studies were carried out in the R&D station to define operational parameters for optimal cutting for each new laser. The first laser evaluated worked well in R&D but failed under production line operation. In the meantime we have located a supplier of a new design of laser, which offers a compromise between cutting speed and quality. We have shown that we can double cutting speeds to about 2 in/s with edge quality superior to that of the lasers currently in manufacturing. This laser is now on order and will be evaluated under production conditions next quarter.

iii) An alternative to higher speed cutting is the use of more than one laser per cutting station. This will reduce both the laser cost and the capital cost of investment, and improve the cost-effectiveness of future factory expansions. We completed a design study to examine multi-

laser cutting configurations for a single cutting station. A number of options were evaluated: two and three lasers cutting at one time on one side, and two lasers cutting on opposite sides of the tube. Wafer handling and tube positioning times were found to be bottlenecks in throughput for several of the configurations. The most favorable case was found to be the use of two lasers cutting on opposite sides of the tube. This design is in the evaluation stage.

3.2 Subtask - Cell Efficiency

EFG PV cells have reached the 14% level in commercial production with the help of programs carried out in PVMaT 4A2, about 5 - 10% (relative) lower than conventional x-Si wafer-based PV technologies. Encapsulated cell efficiencies in the module remain at about 14% because of the optimized AR coating designed to optically match the encapsulant and glass. In the work described in Section 2 above, we have worked to maintain the EFG product cost advantages during our expansion of our wafer manufacturing facility from 4 to 20 MW. In this subtask, we attempted to extend these processing techniques to thin EFG wafers (100-150 microns). We have studied cell designs and new processing approaches in collaboration with the Georgia Institute of Technology (GIT), which can be applied to produce thin high efficiency cells. The goal was to achieve 15-16% efficient cells with new processing which both can be scaled up in throughput and can be expected to be applicable to very thin (100-150 μm) wafers.

3.2.1 Accomplishments – Cell Efficiency

The goals of this program were: 1) to define new cell process sequences for EFG silicon material with the potential to increase the cell efficiency, and 2) to identify equipment alternatives allowing higher throughput processing, which can produce cell efficiencies in excess of 15%. For this research, Rapid Thermal Processing (RTP) was substituted at Georgia Tech (GIT) for a number of conventional belt furnace steps used in the ASE cell manufacturing line in order to define new technology capable of high throughput. Table 3-1 shows the different areas which were explored in this research.

Table 3-1. Comparison of standard ASE Americas cell process and proposed modifications using RTP methods.

Standard process	Variant involving RTP
- Phosphorus diffusion via belt furnace, ~40 min	- RTP 1-2 min - RTP co-fired with Al on the back side
- *no surface oxide*	- Rapid Thermal Oxide
- AR coating – silicon nitride	- *no alternative sought*

Table 3-1 (Continued)

Standard process	Variant involving RTP
- Pad printed thick Al paste co-fired along with front contacts	- Screen-printed Al alloyed at 850 C or RTP co-fired with front contact
- Hydrogen passivation during metal firing via belt furnace, 90 s	- RTP firing

Matrix experiments were carried out at GIT during the first year to evaluate rapid thermal processing (RTP) methods for optimizing EFG wafer base lifetime. The details of this work are given in two publications [7,8]. The most significant findings related to the synergistic effects of firing with aluminum and the SiN film. Fig. 3-1 shows the differences in lifetime observed for various processing sequences. Annealing of the SiN film leads to very little passivation when done without the Al on the back. The optimal annealing temperature is increased to above 800 C when the Al is present.

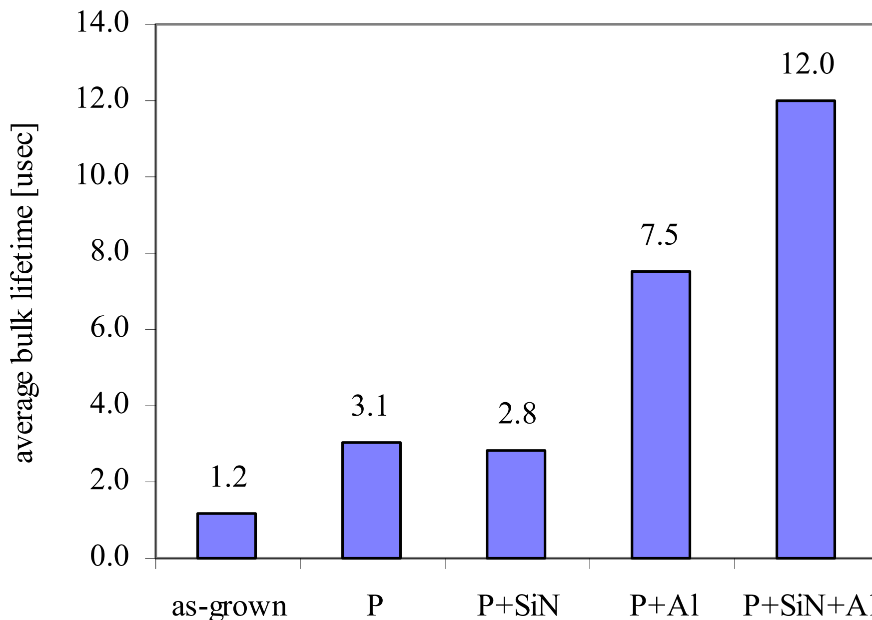


Figure 3-1. Bulk lifetime improvement due to P, Al gettering and SiN hydrogenation.

Theoretical analysis of thin (75 – 200 micron) Si wafers was performed. Obtaining low surface recombination velocity surfaces becomes more critical, the thinner the wafer. One methodology explored was to try to incorporate an oxide passivating layer on the front side of the cell, formed either with RTP or with a conventional furnace oxide, to reduce recombination and improve cell efficiency. These efforts were unsuccessful. Significant irregularities were observed in the SiN layer after firing. This may have been due to a 'microscopic blistering' phenomenon we have observed in the past, which is highly dependent on surface conditions.

Cell efficiencies were not promising and further analysis to determine whether the source of this condition came directly from the thermal oxide or not was not performed.

Exploration of RTP diffusion offered some promise. Efficiencies exceeding 13% were eventually obtained, but were not optimized fully. For the moment, the use of conventional continuous belt-conveyor furnace processing still offers good efficiency with high throughput and remains the favored technology, but sufficient promise was demonstrated here to warrant further exploration.

The most successful results came from the use of RTP for co-firing of the metalized contacts on the wafer. Careful optimization was made to ramp-up rate, peak temperature, firing time at the peak temperature, and cool-down rate. A comparison between RTP and belt furnace processing and showed superior results for the RTP firing of 14.3% vs. 13.9% [9]. With the use of evaporated metal contacts, which then afforded the ability to have a more optimal firing and annealing step for the aluminum contact, efficiencies as high as 15.8% were obtained. The RTP firing results demonstrate two opportunities: either the development of specialized RTP equipment for firing solar cell contacts or to use the information from the experiments in designing newer conveyor belt furnaces which would enable the optimized warm-up and cool-down profiles to be achieved.

3.3 Subtask – Large Diameter Thin EFG Cylinders and Polygons

Cylindrical shapes have reduced thermoelastic stress acting on them during growth and allow rotational movement of the crystal or crucible. These factors can improve quality and thermal uniformity, hence wafer thickness control and uniformity. Cylindrical shapes also improve laser cutting efficiency and allow thinner wafers to be processed with high yields so as to provide higher materials use efficiency. If cylinder growth is combined with on-line emitter diffusion by incorporating phosphorus diffusion sources into the EFG growth furnaces, this eliminates the costly and yield-critical processing steps of etching and diffusion in the cell line, and removes critical steps in wafer handling. The overall module cost reduction from work in breakthrough opportunities may be upwards of 50% (relative), i.e. cutting EFG PV costs in half. Given the existing cost advantage of EFG wafers relative to wafer-based x-Si PV technologies, a halving of EFG costs would dramatically change the overall commercial prospects for PV relative to other energy sources.

3.3.1 Accomplishments - Cylinder Growth

In the first year of the program we demonstrated growth of 50 cm diameter EFG cylinders up to 1.2 m in length and down to average 100 μm wall thickness, and developed a model for heat transfer in large diameter systems [10,11]. One such cylinder is shown in Fig. 3-2. In Year 2 we continued the development of the growth system and cutting methods for the cylinder, and evaluated solar cell processing sequences for thin cylindrical wafers.

Two problems were encountered in the growth area during development of the cylinder. Difficulties were experienced with obtaining a uniform grade of graphite. This led to inconsistent

Figure 3-2. 50 cm diameter EFG cylinder.

and non-reproducible growth conditions. The other area problems were encountered was in the residual stress in the crystal. These difficulties redirected the program for large diameter cylinder growth to development of concepts for growth in the EFG octagons configuration with increased face width, 12.5 cm instead of 10 cm. See discussion in Section 3.3.2.

3.3.1.1 *In situ* p-n junctions. Formation of p-n junctions during crystal growth was previously demonstrated for EFG [12]. We have studied the feasibility of introducing diffusion sources in the large diameter cylinder hot zone this year. It was concluded that it would not be possible to do this in the current design of hot zone because a lack of control of the ambient gases and because rotation could not be carried out.

3.3.1.2 Thin solar cells using curved EFG wafers. We successfully made 13% efficient 5 cm x 5 cm and 6 cm x 6 cm area solar cells from sections cut from EFG cylinders down to as thin as 150 µm (see Table 3-2). Full details are presented in a publication [11]. On account of low yields because of the growth stress in the thinnest sections, we could not obtain wafers thinner than 150 µm from the cylinder.

Processing steps in the manufacturing line were adapted to handle the thin, curved wafers. Standard processes of phosphorus diffusion, AR coating application, and front and back metal application and Al sintering were carried out to make the solar cells. Fixturing was made to allow processing of the curved wafer during the AR coating in the PECVD nitride deposition and the metal application steps. The solar cell results are tabulated below. The J_{sc} and V_{oc} values

on the best cells are consistent with our standard EFG cells of about 14% efficiency. Low fill factors are partly due to problems in probing the smaller, more fragile cells during the measurement process, and non-optimal firing.

Table 3-2. Cell test parameters for cylindrical EFG multicrystalline Si solar cells.

Ave. thickness (μm)	J_{sc} (mA/cm^2)	V_{oc} (V)	FF	PP (mW/cm^2)
150	30.64	0.583	0.725	13.0
190	31.36	0.590	0.707	13.1
200	31.12	0.588	0.696	12.7
210	31.00	0.582	0.686	12.4
290	28.84	0.575	0.739	12.3

3.3.2 Accomplishments - Crystal Growth for 12.5 cm square EFG Wafers.

A cost benefit and risk study indicated that the highest risk occurs because of the uncertainty in securing a reliable graphite supply for dies for the very large diameter EFG tube production, e.g., at a 50 cm diameter with a polygon with up to 12 sides. We explored furnace designs with larger EFG furnace diameters that can accommodate an octagon with 12.5 cm wide faces, to minimize our exposure to graphite uniformity problems. In order to most quickly obtain a wafer product that is suitable for commercial use, we decided to develop growth of a 12.5 cm face octagon with standard thicknesses of the order of 300-350 μm until we have a better understanding of the stress problems and how they change with tube wall thickness.

The design and fabrication of the 12.5 cm face octagon furnace and laser cutting station have been completed. First growth attempts were successful in producing EFG octagons up to 2.5 m in length. 12.5 x 12.5 cm EFG wafers have been cut from the octagons. Continued work on this large diameter octagon will optimize growth conditions and attempt to produce wafers equivalent in both mechanical and electrical quality to the standard octagon now in production.

Other experiments on development of large diameter EFG cylinders were redirected to work to decrease residual stress in growth. Extensive characterization of the cylinder system and the standard octagon system with thermocouples was done to develop a database for thermal modeling and furnace design. This database is being used now for evaluation of different modifications of the hot zone. A heat transfer model was developed at the State University of New York – Stony Brook to help in this task (details may be found in ref. [10]).

4. Flexible Manufacturing

EFG wafer manufacturing at ASE Americas has undergone rapid expansion during the course of the three years of this PVMaT program. At the start of the program in 1998, the initial wafer expansion from 4 to 12 MW was in progress, and a second expansion from 12 to 20 MW has just been completed in this past year. This increased annual EFG wafer production from

about 3 million to the present 14.5 million (measured as 10 cm x 10 cm equivalents). At the same time, a new 10 cm x 15 cm area wafer was introduced to complement the standard 10 cm x 10 cm wafer, and we have described in Section 3 the progress on the R&D for development of crystal growth and laser cutting technology for production of 12.5 cm x 12.5 cm EFG wafers. This rapid pace of growth in capacity and diversification in wafer area has required development of new data collection and monitoring methods for our manufacturing line. We discuss here key components of this effort: a central server for handling information gathered from an expanded and automated data base, and equipment performance tracking and analysis software.

This task also has worked on improving manufacturing equipment for handling different sizes of EFG wafers, on module field failure identification and analysis, and on developing low cost designs and encapsulants for the basic ASE Americas product line. The goals in pursuing such product design and fabrication improvements are to deliver better value to the customer, to better respond to customer requirements, and to achieve longer field service life and lower field failure rates.

We describe all these activities in more detail below. A number of these in the wafer diversification area will be seen to overlap with work already described in previous sections. It will be evident that the integrated effect of the manufacturing line improvements from this task has been critical to maintaining yields and throughputs and supporting process improvements during this rapid pace of expansion of EFG wafer capacities.

4.1 Subtask - Large EFG Wafers

The trend in crystalline Si wafer technology is towards larger wafers so as to decrease cell processing costs, thus amortizing the unit cell processing cost over a larger area. EFG technology is not limited, as are conventional ingot/block + sawing wafer technologies, by ingot/block size and/or by maximum sawing length. In principle, EFG wafers may be cut to any length, to produce a wafer encompassing up to the full length of an EFG tube or cylinder. The first step toward larger wafers at ASE Americas was completed in the first two years of this subcontract. We expanded our product offering to include 10 cm x 15 cm wafers in addition to the standard 10 cm x 10 cm wafers. We consequently developed a strategy for wafer handling during laser cutting and etching that are high yield and cost effective in the production of the larger rectangular EFG wafers.

We have already described in Section 3 a proprietary plasma etch method with which to remove the damaged region of the wafer edge after it is laser cut. This reduces the incidence of cracks propagating to fracture in handling, raises overall mechanical yield, and contributes toward the goals of reducing chemical usage in the ASE Americas' manufacturing line by reducing acid etch requirements. As we increased wafer volumes to above 11 million annually in our most recent expansion, the conventional acid etching process became a bottleneck. Thus it was critical to implement the plasma etch, which shortened the conventional acid etch time and acid use by over 50%. Another approach pursued (Subtask in Section 3) is to reduce the damage through utilization of new laser technologies.

A new element in this subtask in year 3 of our program has been the evaluation of the cost effectiveness of production of 12.5 cm x 12.5 cm wafers. Competitive pressures to make available this size EFG wafers in the marketplace and standardization to this area in the future have put a high priority on this work. In the case of EFG technology, changing to this wafer size is not a straightforward procedure: both a larger diameter EFG octagon and a laser cutting station

have to be designed, fabricated and tested before full scale manufacturing of these wafers would begin. The work in this area has been already described in Section 3.

4.1.1 Accomplishments - Large EFG Wafers

4.1.1.1 Manufacturing database. Manufacturing Systems implementation in the wafer and module areas include the definition, development and implementation of quality and management systems that are built on controlled documents and calibration standards that are traceable to primary and secondary standards. Metrics were developed for equipment performance (uptime, repair time, waiting for parts, qualification time) and tracking them in an electronic database system. These systems add stability to the manufacturing process and are being used to document acceptable ranges of variability of all key parameters, and to enable systems to come on line in a controlled fashion.

In the initial phase of this work, a data collection system for our wafer fabrication department was installed. This encompassed the Crystal Growth, Laser Cutting, Silicon Etch, and Wafer Packing areas. The heart of the system is a central server, which collects information from computers along the ‘spokes’ of the network. These other computers include those on equipment itself, such as our crystal growth furnaces, as well as independent stations where operators enter information about group of wafers in progress. Information is transferred along the regular network connections and cables, and the server is instructed to either poll for certain information from computers along the network at specific times, or to receive information automatically sent from the remote computers.

The user interface available within the server software has been customized to allow production supervisors and engineers to access the information stored within the resulting database. The main menu for this user interface appears in Fig. 4-1.

Information such as growth data from each furnace, yield from a given growth run, laser cutting performance for each laser, etc., can be extracted from this interface. An example of such a query is given in Fig. 4-2. Here, the “flatness loss”, as measured by an arbitrary standard established for experimental purposes in order to define the loss, is plotted for an entire growth run of 57 tubes.

Prior to the establishment of the server database, this type of information was available, but it was stored in several different smaller databases, and some of the information was kept only in written records. Unifying all of this data in one area has greatly simplified the tasks of production personnel in keeping track of and analyzing the data in the Wafer Fabrication area. Linkages of this data to a cell test database has also been extremely useful in tracking growth information to process performance, which has proven to be a great aid in both monitoring and troubleshooting our production cell efficiencies.

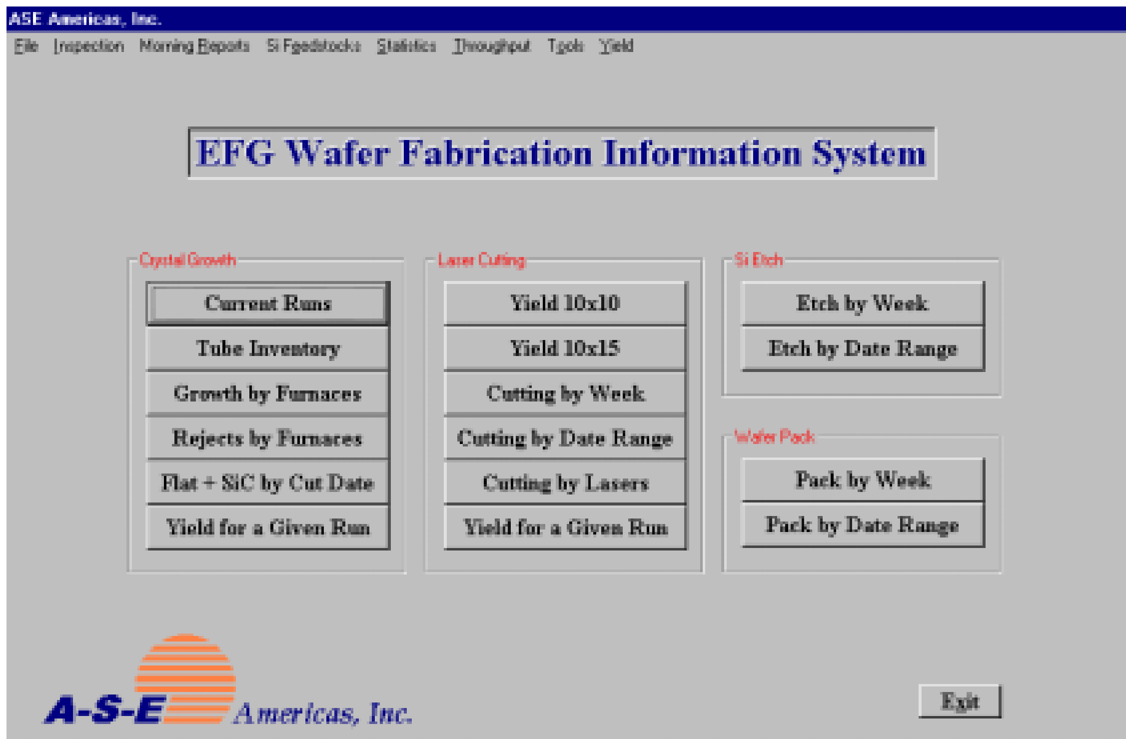


Figure 4-1. Main menu from server database querying user interface.

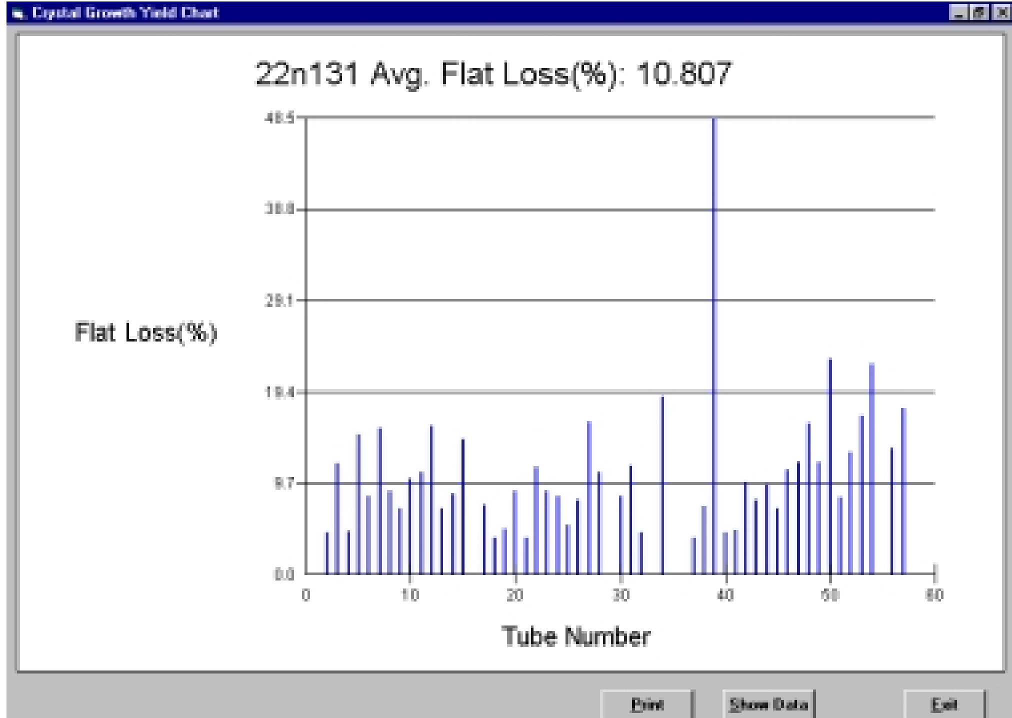


Figure 4-2. Results of a query in the server database for Flatness Losses vs. Tube Number for an experimental growth run of 57 octagon tubes.

4.1.1.2 Equipment performance tracking. A software package was evaluated and tested in the manufacturing line to assist in tracking of machine performance. This program was developed first to monitor laser cutting equipment performance, and it now has become an integral part of our Total Preventative Maintenance (TPM) system, as discussed in Section 2.3 above.

4.1.1.3 Wafer size diversification.

Wafer cutting. In the first two years of the program, redesign of the laser cutting station focused on improvements for cutting of 10 cm x 15 cm wafers which would allow a quick change over from this cutting configuration to that for cutting10 cm x 10 cm wafers. Software modifications were made to reduce handling time and increase the percentage of time the laser is on in a cutting cycle vs the tube rotation. This also required redesign of the backpad holding the wafers in place during cutting. In addition, program changes to the control software were written and the modified cut pattern installed in order to complete the work for this task.

Wet Etching. Modifications to the existing silicon acid etching equipment to etch, rinse and then dry 10 cm x 15 cm were carried out in three phases: a) development of carriers for 10 x 15 cm wafers; b) development of racks for 10 x 15 cm wafers, and c) modification of the rotor basket for the spin/rinse-dryer to accommodate the carriers. Initial concepts and prototypes were first developed, and then transferred to a manufacturing phase Other fixturing work involved modifications in racks that had previously been built to house 10 x 10 cm wafer carriers for transport in and out of acid etching and water rinsing tanks. Creating additional racks which could only handle the larger size wafers was not desirable. Designs were developed to handle both 10 cm x 10 cm and 10 cm x 15 cm wafers, and which allowed the racks to be easily used in our manufacturing line.

Dry Etching. Carrier designs and process configurations were also evaluated for the two different wafer sizes for plasma etching. The machine overall is capable of handling a variety of wafer sizes. The specific areas in which wafer size becomes critical is in the design of carriers to hold the wafers, and in the disk-shaped process carrier carousel (PCC) which holds the carriers. Several iterations of carrier and PCC designs were developed initially for the 10 cm square size wafer, and introduced into manufacturing. When this design was finally robust and acceptable, carrier design for 10 cm x 15 cm wafers was next carried out. The PCC for these wafers will hold 5 of these larger carriers, whereas the PCC for the smaller wafers holds 6 carriers. In total, approximately 1800 coin-stacked 10 cm x 10 cm wafers can be held in the former PCC; almost 1500 coin-stacked 10 cm x 15 cm wafers are expected to be held in the latter PCC. Thus, while the wafer throughput will be less for the larger sized wafers, the areal throughput will be greater. In all of these designs, total weight of the PCC (including carriers and wafers) became one of the most important design criteria so as not to overload the motors. The greater areal load of the larger wafers adds about 5 lbs to the total PCC weight. The weight of the PCC was minimized by removing metal in non-essential locations. The lighter the PCC, the faster it can be accelerated during processing, which can shorten the processing time.

4.2 Subtask - Module Field Studies

As EFG PV products accumulate field exposure and are used in an increasingly wide array of applications, it is inevitable that some field failures will occur. It is important to promptly analyze any failures and quickly translate the lessons learned into manufacturing improvements. In this Subtask, we established feedback networks from end users and field

failure information and field experience was tied back to the manufacturing process. We have developed the capability to close the loop between the manufacturing process and the observed product defects to be corrected in several areas under this program: module glass breakage, AC module field performance, glass delamination and cable interconnect. Fundamental to achieving improvement in high volume manufacturing will be the establishment of Failure Analysis and Root-Cause-of-Failure capabilities which will be based on these initial studies. In addition, a comparison study was done between our module and those of several competitors on the susceptibility to fire and ability to withstand flame-outs under standard ASTM test conditions

Overall responses from these studies have been very favorable, as a number of new quality control procedures for incoming materials and manufacturing procedures have been instituted at ASE Americas to reduce in advance the possibility of manufacture of modules with these defects.

4.2.1 Accomplishments – Module Field Studies

4.2.1.1 Glass Fracture. We have studied a number of occurrences of fracture of glass in our large ASE 300-DG module in the field under this Subtask and have categorized and analyzed glass fracture where failure mechanisms are not obvious. Glass fracture was chosen initially because it is the area which has the largest warranty claim total. Our initial customer survey evaluated all claims and found glass fracture represents about one tenth of one per cent of all claims. To date, we have seen a number of diverse failure mechanisms, but there have not been any fracture failure modes which can be related to systematic manufacturing practices or shortcomings.

We used an expert on glass fracture to perform analysis of modules returned from the filed to back up field observations. By far the most failures were found to be related to environmental factors, in particular, caused by sharp rocks that were blown onto the surface of the glass by the wind from nearby locations. However, several other smaller occurrences of fracture arose from other factors related to glass manufacture.

In Fig. 4-3 below there is shown a close up view of an area of the broken glass in a module retrieved from one of the field sites investigated. We additionally prepared smaller samples for microscope examination from a number of modules in order to confirm the causes of fracture such as this. In a minority of cases, it was suspected that fracture could have been caused by inclusions in the glass.

4.2.1.2 AC module. We completed a study of AC module field performance in collaboration with Ascension Technology. This module was manufactured using the platform of the standard ASE 3000/DG module and the SunSine inverter of Ascension Technologies. Module parameters investigated were the silicon adhesive bond reliability between the module and the inverter, anti-islanding characteristics, and diode failures. It was found that these modules have performed very well in this introductory phase. However, the manufacture of this AC module was discontinued by Ascension Technology in the last year of the program, and field study efforts were redirected elsewhere for the remainder of the program.

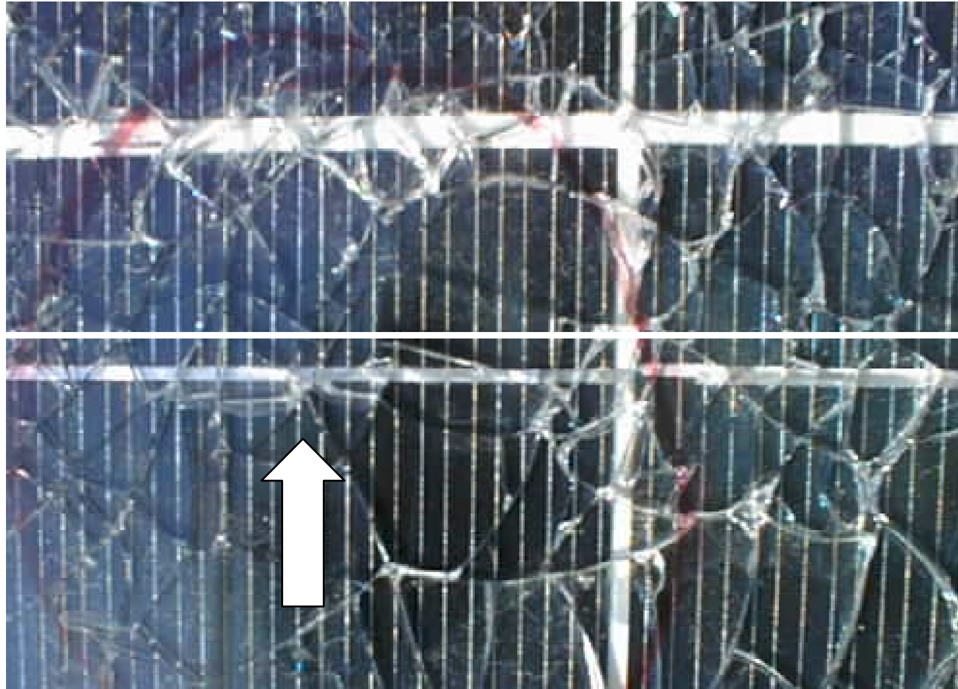


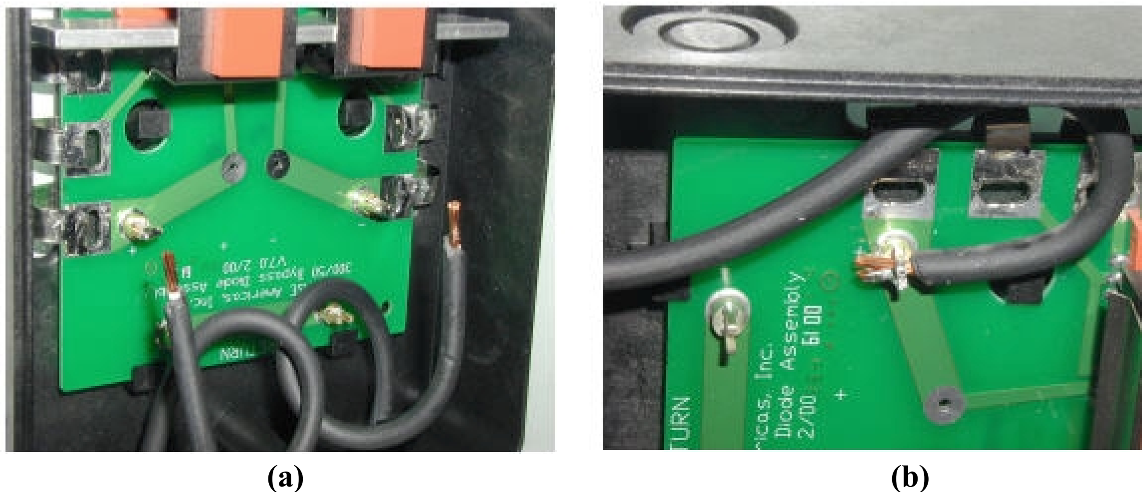
Figure 4-3. View of module broken due to impact from wind-borne crushed roofing pieces. Arrow shows one of the several impact points.

4.2.1.3 Cable joints. Investigations were carried out to check on reports of deficiencies in the soldering quality in modules which were in the field for less than one year; and in another case, some delamination in modules which had been in the field for 5 years in an associated installation.. The affected population of modules was thoroughly inspected in 746 modules. The junction box cover from every module was removed and all internal components inspected. and faults documented and corrected. Defects such as delamination, white spot discoloration, flux residue, and glass conditions were also documented.

Severe delamination problems were not found. Representative faults observed in the case of cable connections are shown in Fig. 4-4 below. In all, 768 modules were inspected. Cable joint faults were found in 55% of the cases and repairs were carried out. The information gathered has been used to tighten up and improve cable soldering procedures in the ASE Americas module manufacturing line.

4.3 Subtask - Encapsulants. One task under PVMaT 5A2 successfully evaluated new encapsulants, and provided future options for manufacturing, both for reduced costs and expectations for a longer module field lifetime. This work had two purposes. One was to develop an improved encapsulant to overcome some shortcomings in the current encapsulant in use in the ASE Americas manufacturing line. Tests were successfully completed and recommendations to manufacturing have been made. The second objective was to examine options provided by resin encapsulants which are liquid at room temperature. Several of these also have very fast cure times using UV light. These are desirable both to provide flexibility in manufacturing with respect to increasing throughput and improving yield of current products, and to increase yields

with thin wafers. We have not been successful in making prototype modules with a liquid resin which shows the most promise to use with thin EFG wafers. Delamination of the encapsulant



(a) **(b)**

Figure 4-4. (a) Disconnected cable in junction box due to poor soldering. (b) Partially wetted solder joint in cable box.

from the glass and excessive formation of bubbles during lamination and cure attempts have been the main problems. Consequently, we have discontinued all work on liquid encapsulants.

4.3.1 Accomplishments - Encapsulant Development

We have completed tests on a modified formulation of our standard encapsulant which has several advantages and possible cost savings. The transmission is improved by several percent, it has a lower level of moisture retention, it has a lower lamination temperature and higher melt flow index, thus being better for thinner wafers, and eliminates some cosmetic defects occurring from time to time with our standard formulation. The module cost reduction from this encapsulant is expected to be about 5% (relative), and it has helped to drive introduction of new customer-driven product offerings (see below).

We have completed all environmental testing of a new encapsulant formulation and it has been introduced in manufacturing. The higher melt flow index allows lower lamination temperatures to be used. This has increased throughput and decreased labor costs in manufacturing. Increased yields also have been achieved because less pressure is exerted on cells during lamination. This encapsulant also has superior adherence to glass. Its good UV cutoff and increased transmission in other parts of the spectrum contributes to the gain of 2-3% in module performance.

Our standard encapsulant is very sensitive to moisture. If flux solute is not completely evaporated during the interconnect process, or trapped in the solder joint, then the water content eventually leads to a discoloration in the solder joint area. This area appears a white spot. This is primarily a cosmetic defect but not tolerated by some customers. The affinity of our standard encapsulant for water also has required the use of a moisture barrier in the back of the module to prevent water from entering, *viz*, our standard double glass (DG) module construction, or a vapor barrier in the backskin. This both complicates module construction and makes it more costly. As

discussed further below, the introduction of the new encapsulant, without the requirement that it be sealed against moisture ingress, now has allowed us to proceed to even greater reductions in module cost by going to an entirely new module platform. This platform preserves the most desirable features of our double glass module, while reducing module weight and cost.
Fire Resistance Testing. We evaluated the fire rating of our encapsulant in a fire brand test and demonstrated that the ASE Americas' non-EVA encapsulant passes the UL790 Fire Resistance Roof Covering Materials test and in it performs significantly better than the EVA encapsulant of many of our competitors which did not pass this test. The fire testing was carried out by Wyle Laboratories. All appropriate instrumentation, measurements and test equipment used were calibrated in accordance with their Quality Assurance Program, which complies with the requirements of ANSI/NCSL Z5400-1, ISO 10012-1, and Military Specification MIL-STD-45662A. All standards are traceable to the National Institute of Standards and Technology (NIST) by report number and date. When no national standards exist, the standards are traceable to international or documented internal calibrations.

The fire test is called the Burning Brand Test (Brand Type A) specified in UL790, Section 8, and consists of placing a wooden structure made from wood of a designated heat content so that specified temperatures will be achieved in burning. Each wood test structure is made from Douglas Fir lumber clear of knots and pitch pockets. The module and the wooden structure are placed on a inclined fixture with a 5/12 slope. The test structure of firebrand and module to be tested is placed in an air delivery hood enclosing a fan, which simulates an airflow of ~12 mph (1056 fpm). The test is run until the firebrand is consumed and all evidence of flame, glow and smoke disappears. During the test, the module is monitored for evidence of sustained flaming on the module underside, production of flaming or glowing brands of (support structure) roof covering material, displacement of the test sample, and falling away of portions of the (support structure) roof deck. A calibrated Anemometer was used in monitoring of the tests.

The ASE-100ATF/34 module did not exhibit any sustained flaming of the module underside, nor did it exhibit the production of flaming or glowing brands. The panel surface glass located on the underside of the module opposite the location of the firebrand broke. No burn-through of the panel was observed. A typical EVA construct module from a module from a competitor had a complete burn-through of the glass and backing material where the brand had been placed. Additionally, during burn-through, flaming drippings were observed dropping from the underside of the panel.

The burning brand test simulates the test that needs to be passed to obtain certification UL790 of Section 8, and required to obtain a Class A Fire Rating from UL. The ASE module made with our non-EVA encapsulant was certified as achieving a Class A rating. The typical EVA-based module typically can achieve only a Class C fire Rating.

4.4 Subtask - Soft Backskin Module

A cost reduction of about 10% in module manufacturing cost can be gained by replacing the back glass of the standard ASE 300 W double glass module. The development of the new encapsulant above, with its reduced water retention properties, has made possible the new module construct shown in Fig. 4-5 below. This module design has now been taken through its prototype phase and is under environmental testing. It is scheduled to be introduced in manufacturing by the middle of 2002.

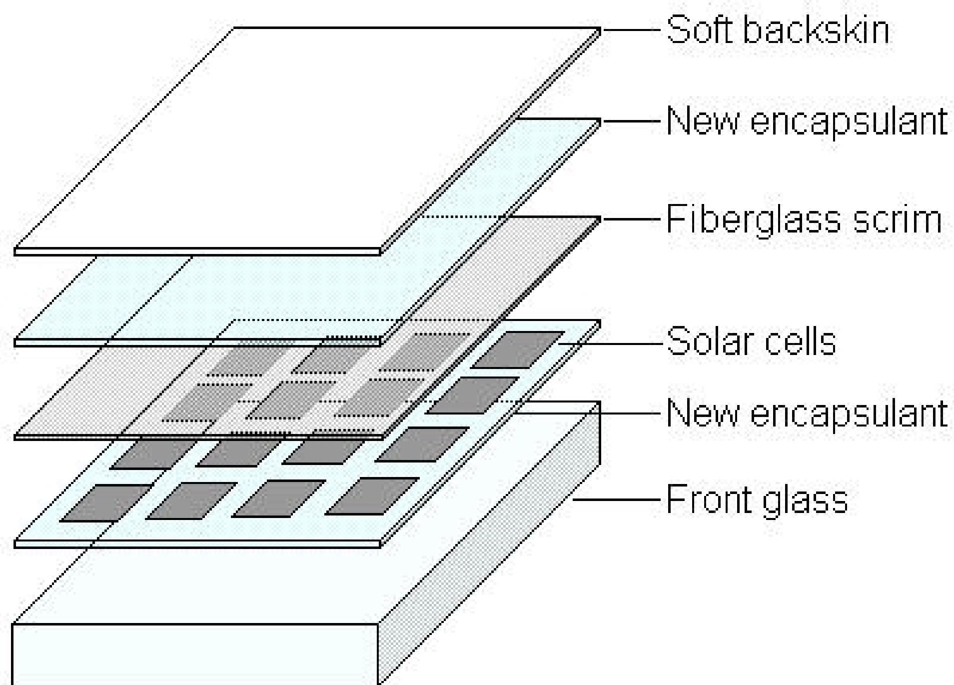


Figure 4-5. Layering schematic for lamination structure for new ASE Americas' module design.

4.5 Subtask - Reflector Module

Prototype development of the reflector module, which we first developed and evaluated in our PVMaT 4A2 program was continued in this subtask. This work was interrupted because the original vendor for the reflector material could not produce material that met our specifications, and we have since been searching for an alternate material. Several additional vendors have been contacted, and we are proceeding with an evaluation of their tooling and design capabilities. Our current estimates of performance enhancement due to the reflector indicate that up to 50% of the cells in the module may be replaced and still obtain the same output performance. We expect that we can gain up to an additional 20% cost reduction with the reflector module design.

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J. Kalejs, B. Bathey, B. Brown, J. Cao, J. Doedderlein, S. Ebers, R. Gonsiorawski, B. Heath, M. Kardauskas, B. Mackintosh, M. Ouellette, B. Piwczyk, M. Rosenblum, and B. Southimath

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ASE Americas
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13. ABSTRACT *(Maximum 200 words)* This report describes the three major task areas: manufacturing systems development, low-cost processing technology, and flexible manufacturing methods. In Manufacturing Systems, we have worked on implementing and utilizing SPC on a larger scale by developing support systems for computer-aided data bases and equipment and process-tracking methodology; developing and implementing new diagnostic techniques; reducing acid use and waste products by introducing a new dry-etch process; and formalizing documentation and training procedures for manufacturing processes (ISO 9000) and for waste product and safety management (ISO 14000) to assist in handling the larger manufacturing organization. Low-Cost Processes, we report on progress in demonstrating low-damage, high-throughput laser technology; studies on Rapid Thermal Processing approaches to improving cell efficiency; evaluating new thin-wafer technology using EFG cylinders; and developing a large EFG octagon and laser-cutting technology for producing 12.5 cm x 12.5 cm wafers. For Flexible Manufacturing, we completed introduction of manufacturing data bases for wafer and cell manufacturing; process modifications to accommodate manufacture of 10 cm x 15 cm wafers; and module field-performance studies and defect tracking to be used to improve manufacturing processes, new encapsulant qualification and introduction into manufacturing, and progress in developing designs for low-cost modules.

14. SUBJECT TERMS: PV; manufacturing line; EFG PV module; solar cell efficiencies; dry-etch process; octagon and laser-cutting technology; low-cost modules; lamination structure; multicrystalline Si solar cells; silicon nitride antireflection coating; plasma flame configuration; EFG wafer

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