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Subcontractor Report

Technology Support for High-Throughput Processing of Thin-Film CdTe PV Modules

Final Technical Report
April 1998—October 2001

D.H. Rose and R.C. Powell
First Solar Technology Center
Perrysburg, Ohio

National Renewable Energy Laboratory

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Abstract

Results of a 3-½ year subcontract are presented. The subcontract, entitled "Technology Support for High-Throughput Processing of Thin-Film CdTe PV Modules," is First Solar's portion of the Thin Film Photovoltaic Partnership Program. The four areas of effort in the subcontract are 1) process and equipment development, 2) efficiency improvement, 3) characterization and analysis, and 4) environmental, health, and safety. Significant progress was made in all four areas.

As part of the process and equipment development effort, vapor-transport deposition (VTD) was implemented first on a 60cm-web pilot-production system, then on a 120cm-web high-throughput coater. Deposition of CdS and CdTe films at a throughput of 3 m^2/min was demonstrated, and over 56,000 plates (each 0.72 m^2) were coated -- 16 times the total number coated prior to the start of the contract. Progress was also made in the conversion efficiency and yield of both standard and next-generation modules, with data from over 3000 sequentially-deposited modules having an average total-area conversion efficiency of 7% and next-generation modules with efficiency as high as 9.3% (10.15% aperture-area efficiency as measured by NREL) produced.

Successful implementation of in-situ CdS thickness measurement was important to progress in thickness uniformity and control. Within-plate and plate-to-plate standard deviations for CdS thickness were found to be only ~4% (relative) for an 1190-plate run. Excellent CdTe thickness was also demonstrated -- the same 1190-plate run showed standard deviations within-plate and plate-to-plate using 13-points-per-plate measurements to be only ~5%. Other film properties, such as surface photovoltage and specular reflectance, showed excellent down-web uniformity, but variation at the cross-web edges. This presents an opportunity for improvement of the baseline module efficiency as uniformity is improved via deposition-system engineering changes.

Net CdTe material utilization of 82% was demonstrated. The ability to raise the utilization further was shown with the demonstration of inherent CdS and CdTe material utilizations of over 90%. Progress was also made in glass handling as well as modeling and distributor development.

Post-CdTe-deposition process development, which included process space exploration and problem diagnosis, was an important part of advances in efficiency and yield. Vapor $CdCl_2$ and reduced-time (i.e., 1 minute) recrystallization were successful on the small scale, but progress was not sufficient to replace current processes. Interfacial layer and back contact development work included the delivery of three modules to NREL with alternative contact process and aperture efficiencies greater than 8%.

As part of the efficiency-improvement task, research was done on cells and modules with reduced CdS thickness in order to increase photocurrent. In order to prevent loss of other cell parameters from the reduced CdS thickness, a high resistivity buffer layer was used between the transparent front contact and the CdS. Buffer layers deposited by sputtering and atmospheric-pressure chemical vapor deposition (APCVD) were investigated. The high-throughput potential of APCVD led to focus in this area, with success achieved with both in-house deposited and on-float-line deposited layers. The development of research equipment, including a large-area sputter system, a small-area VTD system, three small-area APCVD systems, and a large-area APCVD system, was vital to progress in efficiency.

A number of activities were part of the characterization and analysis task, including:

- A system was developed for the rapid measurement of cell IVs. Over 360,000 cell light IVs were taken.
- Two systems were built for the characterization of films on 60 x 120 cm^2 plates. The systems were used to map sheet resistivity, CdS thickness, CdTe thickness, surface reflectance, surface photovoltage, and pinhole density.
- A system was developed and used for the mapping of submodule V_{oc}s.
- A monochromator-based spectral response system was developed and used for the measurement of cell quantum efficiencies.
- A new admittance spectroscopy system, with a range of 0.001-100 kHz, was developed and used to characterize cells.
- A spectrophotometer was purchased and used to measure band-edge sharpness and other optical characteristics of films and devices.
- Scribe contact resistance was measured for various material pairs using a laser-scribed structure. It was found that the normal TCO/back-contact resistance is negligible, but the contact resistance of other material pairs can be high.
- Planar electron-beam induced current (EBIC) was used to characterize intra-grain vs. grain-boundary regions of cells and cell non-uniformity.
- Low-temperature photoluminescence (PL) was used to investigate the electronic states of impurities in CdTe films and cells.
- The performance of modules under non-standard conditions was investigated. The somewhat higher output at high temperature and late afternoon conditions of CdTe relative to similarly-rated modules of other technologies was explained, but further quantification will come with Module Energy Ratings standards.
- The effect of back contacts on cell open-circuit voltage was investigated, and micro-non-uniformity was proposed as the cause of large suppression of open-circuit voltage in some cells. Given the potential importance of micro- and macro-non-uniformity, the effect of non-uniformity was modeled, and an analytical solution based on the mean-field approximation was developed.
- An analytical solution to shunt screening in cells was developed and verified.
- Advances were made in accelerated-testing, including additional light-soak capabilities, rough correlation between light soak and field performance, and exploration of potential high-acceleration factor tests. Accelerated tests were used to investigate the stability of alternative processes at First Solar and for National CdTe Team members' contacts on First Solar substrates.
- Two potential failure mechanisms (defect mutation and micro-nonuniformity) were identified and investigated. Temperature and contact effects on cells were also investigated.
- Field stability to a period of greater than 5 years was verified with further analysis of the array at NREL.

As part of the environmental, health, and safety task, an emissions survey was conducted which showed hazardous emissions are essentially zero (< 1% of the level required for permitting even for a 100MW/yr production). The retention of a "de minimus" level of emissions for the manufacturing plant was achieved with the replacement of the methanol-based $CdCl_2$ process with an aqueous-$CdCl_2$ process. Other improvements and success with worker protection are also reported.

Acknowledgements

Principal Investigators: Rick Powell and Doug Rose
Program Manager: Doug Rose for Phase III, Gary Dorer for Phase I and II

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1. Introduction

This is the final technical report for the Thin-Film Photovoltaic Partnership subcontract awarded to Solar Cells, Inc. (SCI) in 1998. In February 1999, SCI and True North Partners, LLC of Phoenix, AZ jointly formed First Solar, LLC with the intent of reducing the time for the company to realize the vision of low-cost, high-volume photovoltaics. First Solar assumed all activities of SCI. For brevity in this report, "First Solar" (or FS) is used to refer to all activities and accomplishments of SCI or First Solar, LLC.

The production of multi-GW of photovoltaics (PV) per year has long been the vision of many researchers and industrialists. CdTe is a candidate material to fulfill that vision because i) Cd and Te are readily available in the quantities required [1], ii) CdTe has a direct bandgap of about 1.5 eV, which is ideal for PV conversion of sunlight [2], iii) high efficiency and stability have been demonstrated with high-speed processes [3, 4], iv) projected costs are sufficiently low [5], and v) CdTe modules can be manufactured, used, and recycled in a safe and environmentally-responsible manner [6-10].

It is because of these attributes that First Solar began research on thin-film CdTe solar cells in 1991. Limited pilot production began in 1994 to improve the process for full-sized modules, and in 1997 a new high-speed technique called vapor-transport deposition (VTD) was developed that created the possibility of significantly lowering manufacturing costs [11]. In 1999, ground was broken for a new 75,000 ft^2 manufacturing facility (Figure 1.1), which opened in 2000 with a semiconductor deposition system designed for 4 plates per minute throughput (each plate is 60 x 120 cm^2) and equipment for all the processes after CdTe deposition designed for a throughput of 1 plate per minute. Full production of 8%-efficient modules at these rates would provide approximately 80 MW/yr of CdS/CdTe-coated plates and 20 MW/yr of finished modules. Presently, 7% module efficiency has been demonstrated over an extended period of production and a champion module with an efficiency of 9.3% (10.1% aperture-area efficiency) has been produced.

Figure 1.1. New production facility

1.1 Device

Figure 1.2 shows the PV device structure employed for the majority of the research described in this report.

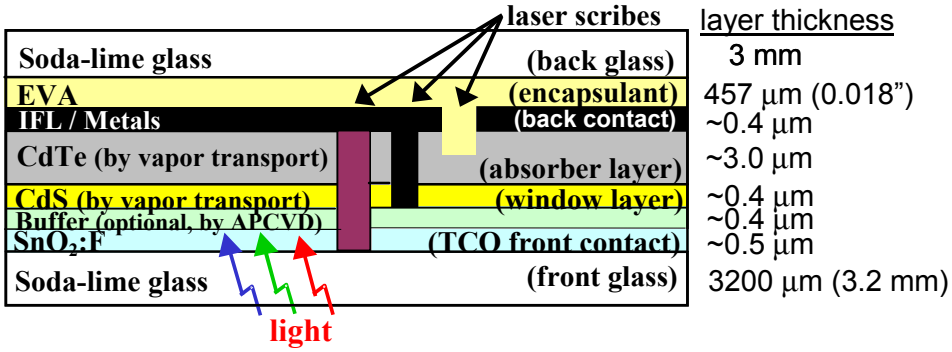

Figure 1.2. Basic device (with monolithic integration by laser scribing).

1.2 Process and equipment

The basic manufacturing process is as follows. First, 60 x 120 cm^2 SnO_2:F-coated soda-lime glass plates are edge seamed to eliminate sharp edges and prevent breakage during processing. The use of two 6-axis robots (Figure 1.3) allows a throughput of more than 4 plates per minute. The robots then load the plates onto a conveyor that takes the plates through an in-line washer and dryer and then on to a high-speed-index load lock system for entry into the semiconductor deposition system.

Figure 1.3. Loading/edge-seaming robots at start of process line.

The semiconductor deposition system (Figure 1.4), also called the production coater in this report, has a 1.2 m (4 ft) web width and a line speed of approximately 2.5 m/min. The high line speed is made possible by the high growth rate achieved with vapor transport deposition (VTD) -- the ~3.5 µm-thick CdTe film is grown at ~1 µm/sec. High-speed-index load locks enable continuous glass flow into the deposition region, thus achieving the target throughput of four 0.72 m^2 plates/min. If run at this throughput for

Figure 1.4. High-speed CdS/CdTe deposition system with 3 m^2/min throughput.

three 40-hr shifts/week, the system would produce 1.5 million CdS/CdTe-coated plates per year. If these plates were finished into 8%-efficient modules with a 93% combined uptime and yield, the PV production would be 80 MW_p/year.

After deposition, the plates are unloaded from the deposition conveyor directly onto the $CdCl_2$ conveyer, or are stacked for later processing (as shown in Figure 1.5). It is at this step that the throughput steps down from the designed level of 4 plates/min for the production coater to 1 plate/min for the rest of the line. The $CdCl_2$ process consists of a $CdCl_2$-in-water application followed by an atmospheric-pressure thermal anneal. Pre-metalization contact processes are then done, including application of an interfacial layer and a dopant. Following deposition of the contact metals by sputtering, the plates go through an atmospheric-pressure contact anneal. Laser scribing is done to provide a monolithically-integrated submodule with 116 series-connected cells. The current-voltage characteristics (I-V) of the plate (called a submodule at this stage) are then taken with a solar simulator.

The submodule is then encapsulated with Ethylene Vinyl Acetate (EVA) and a back sheet of glass. A cord plate is used to protect the two electrical leads that pass through a hole in the back glass plate. The I-V is taken with another in-line simulator (Figure 1.6) and then the safety of each module is tested with a wet high-pot system (Figure 1.7).

Figure 1.5. $CdCl_2$-line loading.

Figure 1.6. Module solar simulator

Figure 1.7. Hi-Pot system.

1.3 Subcontract and report overview

The goal of the Thin-Film Photovoltaic Partnership program is to advance the state-of-the-art of large-scale, thin-film module fabrication. The subcontract awarded to First Solar under the program leveraged First Solar's extensive knowledge and equipment base to achieve that goal. The subcontract is divided into four areas of effort: i) process and equipment development, ii) efficiency improvement, iii) characterization and analysis, and iv) environmental, health, and safety. This final technical report is organized in the same manner as the task description of the subcontract, with the exceptions that Task 3.5 of the statement of work (Research VTD chamber design) is reported in section 3.6.2 of this report, and Task 3.6 (buffer-layer research) is reported in section 3.2.

2. Equipment, Process, and Fabrication Development

2.1 Vapor-transport deposition development

2.1.1 Large-scale deposition systems

High-rate CdS/CdTe vapor-transport deposition (VTD) was implemented on the module scale (60 cm x 120 cm) using a pilot-production system in Phase I [12]. This system, which had a 60cm-wide web, showed that VTD was capable of depositing CdS/CdTe films at line speeds of 1.2 m/min and higher with only one vapor distributor for each material. Normally, however, the system was not run in a continuous mode because of limitations on load-lock and glass-heating speeds. Despite these throughput limitations, ramp-up of pilot-production volumes continued as a way to learn about the process and make product for evaluation purposes. An example of knowledge gained from problem diagnosis and machine upgrades of this system was the identification of feed-line vacuum leaks as a source of a coating problem.

In Phase II, the design and construction of a high-throughput system (also called the 120cm-wide system, production coater, or GDS) was completed (see Figure 1.4). While the production coater uses the same basic deposition technology as the pilot system, significant changes were made to increase throughput and lower per-unit production costs. First, the width of the deposition zone was doubled (from 60 cm to 120 cm). Second, the system has continuous glass and raw material flow, with the capability to have glass under the distributors up to ~96% of the time while in operation. Third, the system uses a radiation cavity instead of a large amount of fibrous insulation.

The high-throughput system consists of an entrance load-lock, a glass heating section, a deposition section, an exit load-lock, and a cooling section. The cylindrical geometry of the glass heating and deposition sections supports the atmospheric pressure load and provides a radiation cavity to achieve uniform glass temperature. Multiple heating zones allow adjustment of cross-web glass temperature. Glass sheets are supported and moved throughout the system using ceramic rolls that are tangentially driven by a flat chain.

Multiple, redundant coating subsystems are located within the deposition section of the furnace. Injected source material is vaporized, the vapors distributed, and the inert carrier gas exhausted in each coating subsystem. In the present configuration, only one distributor is used to form the CdS layer and one to form the CdTe layer providing a deposition zone of only a few inches. The high throughput is made possible despite this small deposition zone by the extremely high deposition rate that is possible with VTD. Growth rates of ~1 μm/s are typical and CdTe film thickness is less than 4 μm.

The first CdS/CdTe coatings were made with the system in February 2000. The first CdS/CdTe-coated plate from the system yielded cells of up to 11% efficiency after light soaking. Progress in production volume, throughput, module efficiency, system durability, film properties, material utilization, and distributor research are discussed in subsequent sections.

2.1.2 Volume

The number of plates coated gives some measure of the number of experiments performed and the progress made with the deposition systems and manufacturing line. At the start of the contract, full-size module research and limited pilot-production were conducted using the pilot line, which included the 60cm-wide deposition system. In phase II, module-scale research was transferred over to the 120cm-wide deposition system and high-throughput finishing line described in section 1.2. As can be seen in Figure 2.1, the number of plates coated during the contract period was over 16 times the total number coated prior to the start of the contract.

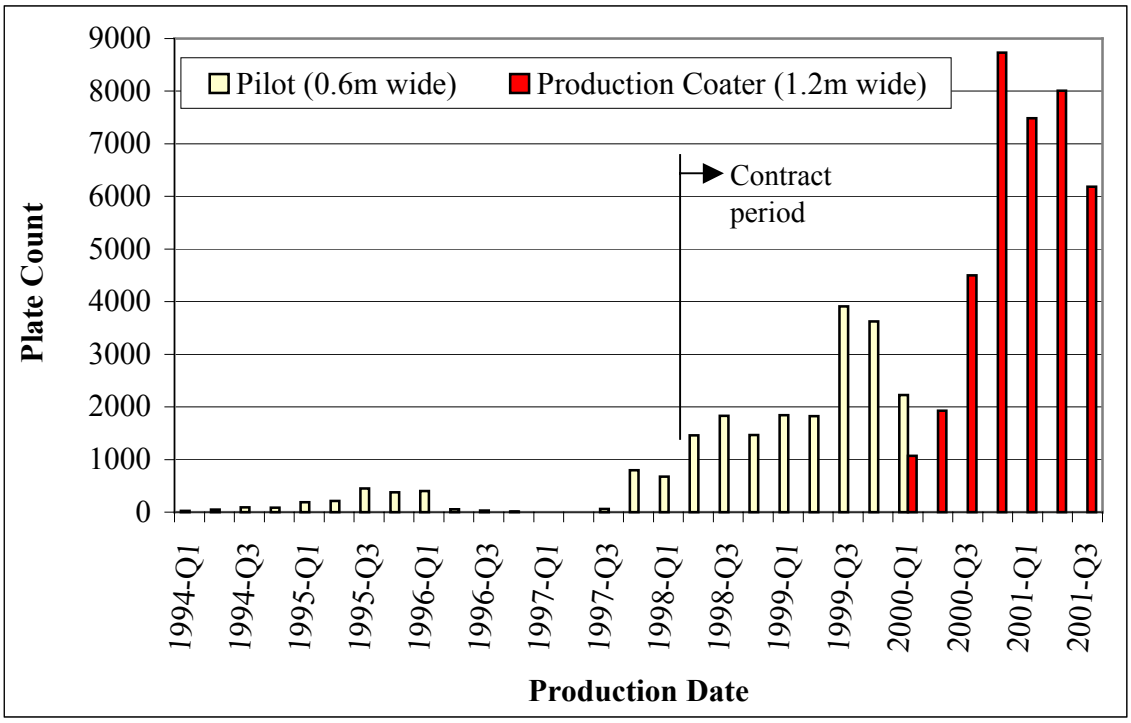

Figure 2.1. CdS/CdTe plates produced per quarter.

2.1.3 Throughput

The production coater has been run successfully with throughput of 3 m^2/min; this is over four 60 x 120 cm^2 plates per minute. Extended runs have been done at a slower speed, for example, 1220 plates (each 0.72 m^2) were deposited in 10 h.

2.1.4 Module efficiency

Progress was made in the conversion efficiency of both next-generation and standard modules. Next generation modules, with total-area efficiencies over 9%, are discussed in section 3.5. Progress with standard modules is demonstrated by Figure 2.2. The figure shows the total-area efficiency results from 3128 sequentially-coated plates (from 8 sequential deposition runs) processed with in-line module finishing equipment. The average total-area efficiency from the data is 7.0% (7.6% aperture-area) despite the fact that the data has not been filtered to remove experiments or non-standard processing.

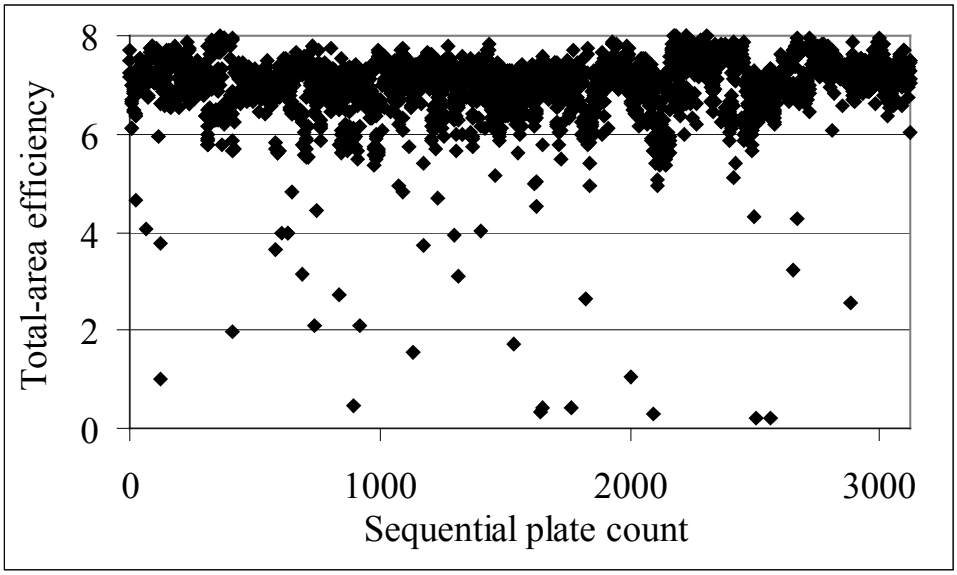

Figure 2.2. Total-area efficiencies for 3128 sequentially-deposited modules (unencapsulated, 0.72 m^2 each) -- average is 7.0%.

2.1.5 Coater durability

Coater durability is measured by the number of plates coated between shut downs for cleaning, source material replacement, or repairs. The goal for durability was > 5000 plates produced without internal coater maintenance. Because of the need to clean some internal components, the maximum achieved was 1944 plates. Many of the challenges that have limited coater durability have been overcome in the course of the contract, but some remain.

In the 60cm-wide system the primary VTD components performed well with small incidence of breakage or chemical corrosion. In the 120cm-wide system the incidence of breakage of some ceramic distributor components increased dramatically due to thermal stresses at some operating conditions. A change to multi-piece design for vapor distributors in Phase III completely eliminated this problem. If distributors are not broken in handling during maintenance they have shown life up to 6 months and over 10,000 coated plates. Some distributor aging has been observed as an increase in thickness deviation with extended use, but this is expected to be eliminated with next generation distributor design.

Over the course of the contract significant progress was also made in durability and run-time of non-distributor components. For example, new hoppers were added to allow feeder refill without system shutdown, clogging of material supply lines was solved, and roll-installation and drive-bearing problems were fixed.

At this time, the limiting factor for durability is coating of some key internal components, which necessitates frequent internal system cleaning. Fortunately, the components that directly control the coating itself, the vaporizer and distributor, generally remain clean, as they are the hottest components. However, presently some material that is not deposited

on the plates is condensing on components other than the exhaust filters. Condensation on the glass-transport rollers has been the primary problem. Installation of under-roll heaters did not fully solve the problem and additional engineering remedies are required.

2.1.6 On-line diagnostics

The high-throughput coater has over 80 channels of temperature, pressure, position and speed control, continuous residual gas analysis, a scanning infrared imaging system, and an internal laser absorption system to measure CdS thickness.

Infrared radiation emitted from the SnO_2-coated glass surface is detected by an imaging system located between the heating chamber and the deposition chamber. The emitted radiation passes through a ZnSe vacuum window. A spinning mirror sequentially reflects radiation from across the web towards a single detector to create a 2-dimensional map of the glass surface temperature. Emissivity and angle of incidence effects can lead to misleading results, however, so proximity thermocouples are used to verify experiments.

Since the CdS layer is soon buried by the lower bandgap CdTe, CdS thickness detection is best done *in-situ* at deposition temperature. Therefore, an array of fixed-position lasers and paired detectors was installed in the deposition system to infer CdS thickness based on optical absorption. Fortuitously, the decrease in CdS bandgap with temperature is sufficient to allow the use of inexpensive solid-state 532 nm green lasers. The use of a custom laser package provided acceptable stability, signal strength, and lifetime. The system uses between-plate signals to compensate for drift caused by window coating, the severity of which is less than anticipated. These on-line sensors have become an integral part of operation and have largely eliminated the need for separate CdS verification runs.

2.1.7 Film thickness uniformity and consistency

Uniformity of performance over the area of the 60 cm x 120 cm module is crucial for high performance modules. Uniformity of semiconductor film thickness is an important metric because 1) film thickness can directly affect performance (e.g., thinner CdS can result in increased J_{sc} but lower V_{oc}, and changes in CdTe thickness could result in differences in performance after the $CdCl_2$ anneal), and 2) film thickness is indicative of other variables which could affect performance (e.g., deposition temperature and species-flux during growth).

The Phase III goal for uniformity was to demonstrate thickness control of ±5% within a plate and ±10% plate-to-plate over a production run of 1000 plates. To evaluate progress against this goal, data from the May 7, 2001 run (1190 plates) was analyzed. Data from the 4 *in-situ* CdS thickness gages is shown in Table 2.1.

Table 3.1. CdS thickness (μm) from the 4 *in-situ* monitors for the 1190 plate run. Data was taken every 2 seconds during the 10h run.

	Gage 1	Gage 2	Gage 3	Gage 4
Average	0.37	0.36	0.34	0.35
Std Dev	0.01	0.02	0.01	0.02

As can be seen in the table, the down-web standard deviation is ~4% over the course of the full run, indicating excellent uniformity and consistency in the down-web direction. The standard deviation of the 4 gages (which indicates the cross-web uniformity) is 0.013 μm which is also ~4%. Measurements of plates run without CdTe enable full mapping of the CdS. Fine-resolution plotting of the CdS thickness shows the same mean and average standard deviation as the *in-situ* measurements, but indicates even better uniformity in the down-web direction and somewhat lower uniformity cross-web. Data showing down-web standard deviation of 1% and cross-web of 7% was presented previously [13].

CdTe thickness data from the same May 7, 2001 production run was also analyzed. Table 3.2 shows that the within-plate standard deviation averaged 5%. The plate-to-plate deviation of the mean thickness within the set was also 5%.

Table 3.2. CdTe thickness data sampled from May 7, 2001 production run. Each plate is measured at 13 proscribed points with a calibrated beta-backscatter system.

SUB_ID	Average Thickness	StdDev Thickness	Std Deviation	Min Thick	Max Thick
B05070004	3.193	0.133	4%	2.983	3.449
B05070008	3.518	0.222	6%	3.226	3.902
B05070039	3.468	0.243	7%	3.074	3.894
B05070199	3.640	0.198	5%	3.289	3.943
B05070359	3.432	0.146	4%	3.271	3.622
B05070521	3.454	0.163	5%	3.263	3.699
B05070677	3.671	0.187	5%	3.376	3.928
B05070837	3.256	0.101	3%	3.041	3.399
B05070997	3.210	0.170	5%	2.965	3.474
B05071157	3.278	0.140	4%	3.089	3.488
Average:	3.412	0.170	5%	3.158	3.680

Higher resolution measurements of samples plates from this and other runs show excellent uniformity in the down-web direction (standard deviation of less than 1%) with higher non-uniformity in the cross-web direction. 20-point cross-web measurements on the same plates used for Table 3.2 showed and average cross-web standard deviation of 11%. Data from high-spatial-resolution measurements was presented previously [13] with profiles from two deposition conditions shown (with cross-web standard deviations of 6% and 11%).

Histograms and summaries of on-line CdS and off-line CdTe thickness measurements from several runs during Phase III also demonstrated the consistency of the excellent down-web and mean thickness control. Histogram data was also included in the Phase II report.

2.1.8 Other film properties

Like film thickness, other film properties tend to have excellent down-web uniformity but some cross-web variation. Improvement in this variation presents an opportunity for improvement in efficiency over the 7% efficiency baseline shown in Figure 2.2.

Surface photovoltage (SPV, as measured using a high-impedance meter with a graphite pad in contact with the CdTe side while illuminating from the glass side) has been used to characterize coated plates. Figure 2.3a shows the excellent down-web, but non-uniform cross-web, SPV that can be present with some deposition conditions. Similarly, Figure 2.3b shows cross-web non-uniformity in the specular reflectance of a plate under certain deposition conditions. The specular reflectance is indicative of grain size and structure. Figure 2.3b also shows the excellent cross-web uniformity of a plate deposited with a 60cm leading edge in the 120cm-wide coater. This shows that greater uniformity, with a concomitant increase in efficiency, is possible with engineering changes that will replicate the conditions of the center 60cm over the full 120cm web width.

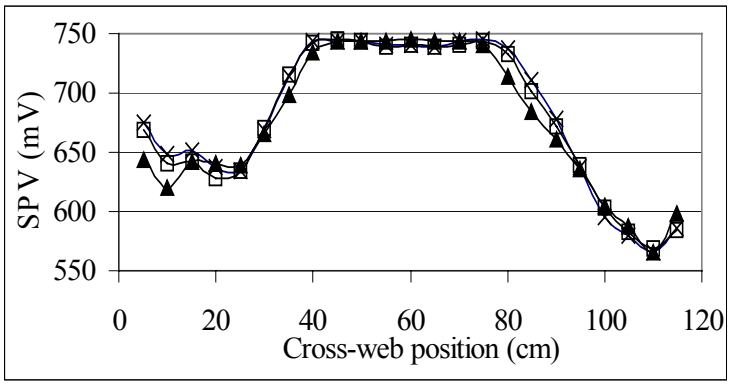

Figure 2.3a. SPV from glass/SnO_2/CdS/ CdTe plate (3 different down-web positions on one plate)

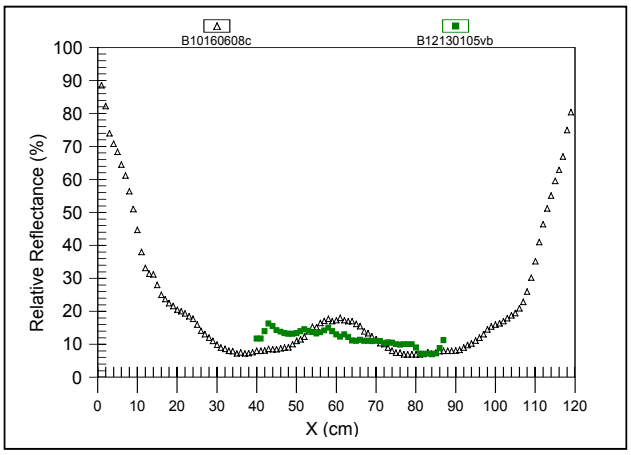

Figure 2.3b. Cross-web specular reflectance for normal and lengthwise deposition orientation

One film property that is no longer a concern is CdTe pinhole density. As reported in Phase II, the cause of pinholes in the pilot system was identified as homogeneous CdS nucleation. The flow dynamics of the production coater are such that CdS particulate, and thus CdTe pinhole, formation is no longer a problem.

2.1.9 Material utilization

High utilization of costly semiconductor source material is important for low-cost and low-maintenance production. In our case, the utilization of CdTe is much more important than that of CdS due to the relative layer thicknesses in the device. The net material utilization can be separated into 3 components:

$U_{Net} \equiv U_0 \times f_P \times f_W$, where

U_{Net} = Net utilization

U_0 = Inherent utilization

f_P = Packing fraction (i.e., the fraction of time glass is present under distributors)

f_W = Web fraction (i.e., the ratio of glass width to vapor curtain width)

Net utilization is calculated by comparing the total material used vs. material on the film side plates (i.e., the total number of plates times the average film thickness per plate). While net utilization is the true long-term metric of success, inherent utilization is the metric that predicts what net utilization is possible with engineering improvements.

In Phase III the goal was CdTe utilization ≥95% over an 8-hour production run of 200 plates. Table 2.1 shows CdTe utilization calculations from Phase III which demonstrate an inherent utilization > 90% in production with the high-throughput coater. At higher line speeds, net utilization suffers due to a poor packing fraction. The poor packing fraction at higher line speeds can be caused by limitations in robot load rates, load lock pumping speeds, smooth high-speed transport, and needed quench time.

Table 2.1 CdTe material utilization in production VTD system.

Line Speed (m/s)	Net Utilization	Packing Fraction	Web Fraction	Inherent Utilization
1.44	82%	95%	91%	94%
1.92	59%	71%	91%	91%

The web fraction loss is due to vapor overspray on the web edges. We currently err on the safe side for uniformity and accept ~9% overspray loss. Experiments indicate that this loss can be cut by more than half with some straightforward engineering changes.

Included in inherent utilization is CdTe re-sublimation loss. Re-sublimation of CdTe occurs after deposition while the film/glass remains hot and in vacuum. A non-negligible loss of 10% or greater can occur at high deposition temperatures, with the leading edge affected more. Re-sublimation loss can be reduced with the use of slightly lower glass temperature and higher ambient pressure. Presently the greater concern with re-sublimation is net movement of hazardous material into the quench section.

Because of the small CdS thickness (10% as thick as the CdTe now and dropping to less than 5% with efforts to reduce CdS to increase module efficiency) relatively little effort has been spent on monitoring or improving the CdS utilization. Recent calculations indicated an inherent CdS utilization of ~91% and net utilization of ~59% over a 6 month period, but this differs from an earlier calculation which indicated a net utilization of 50%. The earlier, lower utilization was attributed to the fact that polyatomic S_x species (x = 2 to 8) might require adsorption and dissociation prior to incorporation, but it could have merely been the result of utilization accounting problems, including feeder calibrations.

2.1.10 Glass properties

Glass is an inexpensive material that serves as an excellent transparent substrate for high efficiency CdS/CdTe devices, but processing temperatures above 500°C make glass-handling issues non-trivial. Failure to properly quench or otherwise manage the cooling profile of plates can result in glass breakage, which disrupts production. Ideally, residual compressive surface stress (generally > 2000 psi) should be introduced during initial cooling and glass flatness maintained to prevent breakage in lamination or the field. Maintenance of these glass properties over the course of a long run is complicated by start-up transients that are the result of the large relative thermal mass of the glass stream. Heater design changes and modifications of quench conditions have improved the consistency of the glass properties. Figure 2.4 shows the result of flatness measurements for two different heat/quench conditions.

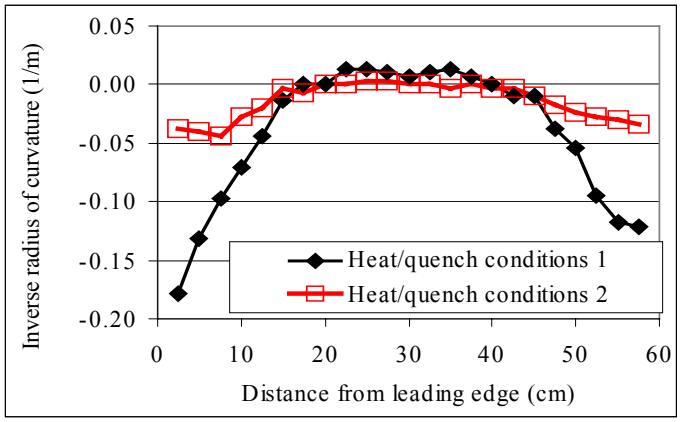

Figure 2.4. Cross-web flatness measurements for two different heat/quench conditions.

2.1.11 Modeling and distributor development

VTD has significant advantages as a deposition method, among them are very high film growth rates, the ability to continuously deliver material into a vacuum, the ability to closely control material delivery and thus film thickness, and the ability to have a different ambient at the growth surface than at the location of material vaporization. Additional indications that VTD was a low-cost, robust manufacturing approach came from the early successes with both the 60cm and the 120cm-wide deposition systems. Variations on distributor designs, however, did not result in striking improvement over early results, indicating that the VTD concept is simple, but the physics are not. The complexity comes from the combination of heat transfer to the semiconductor powder and the glass and the need for uniform distribution of a three-component vapor. Furthermore, distributor components must have relatively simple geometries since materials that can tolerate the high temperature and corrosive environment of the distributors come in only a few shapes. Nonetheless, modeling of VTD and experiments with distributor designs have greatly increased understanding of the method and point to promising pathways for continued improvement. Examples of experiments that were conducted include the following:

- An experiment verified the extremely short depletion lengths that were predicted by modeling. Modeling had predicted that down-web depletion lengths of < 1 cm should result from diffusion transport with a large diffusion coefficient and low pressure.

- An experiment with distributor configurations and process parameters showed that the cross-web film-thickness profile was a function of both the inlet-tube geometry and the feed and flow parameters.
- An experiment with a new distributor-design concept showed that the V_{oc} pattern on plates can be a function of distributor design. Another experiment showed that film contamination from high-temperature distributor components was possible for certain distributor designs and process conditions.
- Test of a distributor with a material change showed that deposition with substantially higher incoming radiation was not problematic. The distributor had a higher radiative emissivity and ~2x the normal heating power. Film visual appearance and cell V_{oc} were spatially more uniform than the controls, but total performance was slightly lower.

In addition to the process architecture and variable experiments, a system was constructed using an IR imaging camera to measure variation in the distributor heaters. The system was capable of detecting significant non-uniformity in several heaters that caused previous film non-uniformity.

2.2 Post-deposition processing development

2.2.1 Production line development support

Significant effort was spent in support of the set-up, debug, and start-up of the submodule production line. Early success with efficiency and yield was presented at the IEEE conference [13]. Success over a greater number of runs can be seen in the efficiency/yield data of Figure 2.2. Examples of activities done as part of production line development support include the following:

- Conducted an experiment to determine the effect of buffing-compound residue and post-buffing rinsing.
- Conducted experiments to determine the interaction of CdTe morphology with 1) post-CdTe-deposition processing conditions and device performance, and 2) metal sputtering conditions and metal adhesion.
- Modeled the effect of low shunt resistance in modules and offered guidance to production.
- Provided support for the design and execution of experiments on the production line to determine the effect of certain process parameters on initial efficiency and stability.
- Helped make new xenon-lamp module solar simulators operational and repeatable; new methods were devised for illumination-uniformity measurement and adjustment and for reference-cell mounting and use.
- Diagnosed good and poor modules and provided guidance for focus on improvement; anomalous results as part of the diagnosis effort led to increased understanding of cell characteristics and measurement procedures, which are discussed in section 4.1.15 of this report.
- Developed formal diagnostic procedures, including a program for a laser system to allow separation of cell and scribing problems. A procedure was also developed

for the rapid determination of scribe shunt resistances in a submodule via measurement of low light resistances of each cell. Fourier transform analysis of the results showed some scribing problems with a periodicity consistent with a certain laser beam and scribe direction on the old laser-scribing system.

2.2.2 Recrystallization

2.2.2.1 Vapor $CdCl_2$

A small-area vapor-$CdCl_2$ system was constructed and described in the Phase I report. The system was used to explore the vapor-$CdCl_2$ process space and demonstrate that the process is capable of providing a more uniform treatment and a more pristine surface compared to wet-$CdCl_2$ treatment, with data provided in the Phase I report. In Phase II, the system was used to explore the effect of treatment ambient. Data included in the Phase II report showed that for the set studied, treatment ambient had little impact on initial cell efficiency, but treatment in wetted air resulted in poor cell stability compared to treatment in dry air or nitrogen.

Vapor $CdCl_2$ was also explored on the module scale. A pilot-production vapor-$CdCl_2$ system with a 60cm-web and a throughput of one module every 3 minutes was constructed in Phase I. During Phase II, the mechanical and heating aspects of the system were verified by successfully using the system to heat treat plates that had received a spray with wet-$CdCl_2$. However, attempts to run the system as intended with $CdCl_2$ vapor generators or open boats resulted in inadequate treatment of plates. Subsequent modifications to provide a more confined space for the vapor gave indications of better treatment, but possible machine life/uptime problems. By this time, the urgency for a vapor-$CdCl_2$ system was removed by the success of the aqueous $CdCl_2$-treatement approach (see section 5.3.1) since the vapor-$CdCl_2$ system was no longer needed to achieve the goal of a no-emissions plant. Interest in the process remains, though, since efficiency and process robustness benefits are still expected from the process due to the higher uniformity of treatment and reduced surface oxidation. Work with this system, however, revealed the difficulty of performing an adequate treatment on the module scale with an atmospheric-pressure vapor $CdCl_2$ treatment.

2.2.2.2 Reduced-duration

The subcontract goal was to demonstrate a full-scale re-crystallization with a process time $\leq$ 2 min. This goal was achieved for small substrates, but not for full modules. Cells of > 9% efficiency were made with treatment times of only 1 minute, but at a cost to process latitude. Because there was potential for reduction of the robustness of the manufacturing process, it was decided to delay experimentation and implementation on the module scale until the process is better understood.

2.2.3 Interfacial layer / back contact development

Investigation of alternative back contact product and/or process architecture was done to determine if opportunity existed for increased module efficiency, stability, or process robustness. Investigation of a vacuum-deposited interfacial layer (IFL) received

particular interest because of the demonstration of remarkable product stability in long-term, high-temperature, open-circuit light soak tests.

Three different alternative-contact procedures were developed on the small scale that showed promise of exceeding the performance of the standard contact. Translation of these processes to the module scale was non-trivial, however, because of scribe-resistance problems in one of the cases and problems associated with a discontinuous, R&D mode of processing with equipment in two locations in all of the cases. Nevertheless, modules with acceptable performance were made with alternative contacts and were delivered to NREL per the Statement of Work. The IV parameters are shown in Table 2.2.

Table 2.2. NREL-measured IV parameters of 3 alternative-contact modules. Each module had a total area of 7200 cm^2 and an aperture area of 6600 cm^2 (Efficiency, I_{sc}, and P_{max} values are from spectrally- and intensity-corrected SOMS and V_{oc}, V_{mp}, and FF are from LACSS-storage-state measurements)

Module ID#	Contact type	Aperture η (%)	Total-area η (%)	P_{mp} (W)	V_{oc} (V)	I_{sc} (A)	FF (%)	V_{mp} (V)
CV114143	Mixed chemistry	8.0	7.3	52.5	91.8	1.09	53.0	58.0
CV114144	Deposited IFL	8.3	7.6	54.8	91.6	1.11	54.8	64.9
CV114147	Deposited IFL and modified S2	8.4	7.7	55.2	89.3	1.13	55.6	63.9

2.2.4 Interconnect process

To make a monolithically-connected module, laser scribing is used to turn the filmed plate into 116 series-connected cells. As can be seen in Figure 1.2, scribe-1 isolates the front contact of the cells, scribe-2 enables the series connection to the next cell, and scribe-3 isolates the back contact of the cells. In pilot-production, laser scribing of modules was done with two multi-beam laser systems at ~5 min/module. New concepts were thus needed to reach the goal of 1 plate/min throughput with low capital costs.

In Phase I, one concept explored was the use of a large number of fixed lasers. In Phase II, a new concept was explored and developed that enables a full scribe set (e.g., all of scribe 3) to be done with one system with one laser in less than a minute. The use of just one laser has the advantages of lower initial cost and higher system up-time compared to the previous concepts. Technology support of this new concept was done under this contract, with machine development by PVMaT and internal funds. The approach provides an increase in scribing accuracy, linear scribing speeds up to 3 m/s (an order of magnitude increase), and a 50% reduction of capital costs.

In Phase III, technical support (e.g., the development of a problem diagnosis protocol) continued for the old laser approach until the new laser system was brought on line. Technical support (e.g., analysis of scribes by SEM and electrical means) was also given in the effort to explore the processing window of the new system and increase process robustness.

2.2.5 Module materials and finishing

Currently, encapsulation is done with a standard EVA/back glass lamination. Investigation of polyester resin systems as a potential replacement of EVA was described in the Phase I report. Results of damp heat and temperature cycling tests with alternative encapsulants were also reported and two modules with polyester encapsulation were included in the deliverables to NREL. Results were encouraging, but not compelling enough to push for a rapid change from the standard process.

3. Efficiency Improvement

Improvement of module conversion efficiency has considerable leverage in decreasing total installed PV system costs. Work described below, as well as work described in sections 2 and 4, was part of the effort to improve efficiency. Progress in the efficiency of modules delivered to NREL is reported in section 3.5.

3.1 Loss Analysis

The maximum efficiency for a single-junction PV device with 1 sun illumination has been predicted to be approximately 31% [2]. The difference between the baseline total-area module efficiency of ~7% and this value is the result of 1) area losses from edge delete and scribing, 2) module-related defects, such as non-uniformity, 3) reduced cell photocurrent from CdS absorption and other losses, 4) reduced cell voltage from non-ideal electrical properties, and 5) reduced cell FF from voltage-dependent collection and parasitic losses.

Of these sources of reduced efficiency compared to the theoretical limit, the largest is reduced photocurrent from CdS absorption and other losses. At 1 sun intensity, the AM1.5 spectrum would produce ~30.6 mA/cm^2 in an ideal device with the bandgap of CdTe. Standard FS modules typically have an active-area J_{sc} of ~18.5 mA/cm^2, thus providing the opportunity for up to 65% improvement in efficiency by reducing J_{sc} losses. Optical analysis of three different vintages of FS devices [14] determined losses of between 5.2 and 5.7 mA/cm^2 from absorption in the CdS. Other losses (all in mA/cm^2) were 1.6-1.8 from reflection, 1.3-2.0 from absorption in the glass, 1.1-1.8 from absorption in the TCO, 0.6-1.7 from deep penetration, and 0.2-1.2 from an unknown loss.

3.2 Buffer layer and thin CdS

The high J_{sc} loss from absorption in the CdS described in the previous paragraph is the result of the over 3000Å-thick CdS layer in standard cells (photo-generated carriers in the CdS are generally lost to recombination). Simply reducing the thickness of the VTD CdS layer results in increased J_{sc}, but reduced V_{oc}. The incorporation of a thin high-resistivity layer, commonly called a buffer layer, between the conductive front contact (SnO_2:F) and the CdS has been shown to allow thinning of CdS without loss of V_{oc} [15, 16]. Efforts to develop a high-throughput process for a buffer layer are discussed in the next section and module results are given in section 3.5.

In Phase I, the focus of buffer-layer research was sputtered zinc stannate and sprayed-SnO_2 layers. In Phase II and III, the focus of buffer-layer research was atmospheric-pressure chemical vapor deposition (APCVD).

3.2.1 Zinc stannate buffer layer

Research at NREL [15] showed that zinc stannate (Zn_2SnO_4, or ZTO) can perform very well as a buffer layer, with benefits to cell efficiency and CdS adhesion. Section 2.1.1.1 of the Phase I report described FS results with ZTO. Cells produced using CSS-

deposited CdS/CdTe, a wet $CdCl_2$ treatment, and X3 back contact (at FS) on borosilicate glass/TCO/ZTO substrates (from Dr. Xuanzhi Wu, NREL) had an average efficiency of 12.6% with a champion cell of 13.9% after 9 days lightsoak. Cells produced at FS using soda-lime glass/TCO substrates (Tec-8) with sputtered ZTO had a champion of 11.4% with unannealed ZTO/400Å-thick-CdS. Analysis of the results, however, showed no performance advantage of ZTO compared to other buffer-layer options that may be more suited to high-throughput manufacture. While additional work with ZTO might have revealed an advantage, focus was shifted to other material systems.

3.2.2 Sprayed-SnO_2 buffer layer

The Phase I report detailed the results of cell fabrication and stress done with spray-pyrolosis buffer layers supplied from ITN as part of CdTe National R&D Team work. The buffer (or HRT, for high-resistance tin oxide) layers were on LOF substrates and were either undoped or 1%-doped with Cd or Zn, with the Zn-doped layers being the most resistive of the three. Cells were made on the nine substrates provided, with CdS thickness of 0Å, 500Å or 1000Å on each of the types of substrates. The CdS (when it was used) and the CdTe layers were deposited by CSS. A portion of the results presented in the Phase I report is shown in Table 3.1.

Table 3.1 Average cell efficiency initially, and after 65°C light soak at open circuit bias, for substrates with ITN-supplied spray-deposited buffer layers.

	Initial efficiency			Efficiency at 1day LS			Effic. after 42day LS		
Buffer layer	0Å CdS	500Å CdS	1000Å CdS	0Å CdS	500Å CdS	1000Å CdS	0Å CdS	500Å CdS	1000Å CdS
Undoped	4.9	11.1	11.4	9.4	11.6	11.1	5.4	9.0	9.6
Zn-doped	7.6	11.8	12.0	10.9	11.3	11.6	6.2	8.9	9.3
Cd-doped	6.8	11.1	12.3	7.6	11.2	11.8	4.6	8.6	7.5

The following conclusions were drawn from the spray-pyrolosis-buffer cell results:

- Zn- and Cd-doped HRT layers marginally improved initial efficiency. Although the cells made on undoped HRT had a lower initial efficiency, after continued light soaking the cells with the updoped HRT and a CdS layer had somewhat better efficiency than cells made on doped HRT layers.
- Most of the cells made without a CdS layer were initially poor due to low V_{oc} and FF, but one no-CdS cell had an efficiency of 12.4% after 1-day lightsoak (which might be a record for a CdTe cell without CdS). All of the no-CdS cells improved under light soak at the outset, and then rapidly degraded under continued light soak.
- J_{sc} improved with decreased CdS thickness for this set, but not as much as would be expected. Researchers at some other organizations on the National Team reported an even stronger effect; they observed no increase in J_{sc} with thinner CdS.

3.2.3 Buffer layers by APCVD

Atmospheric-pressure chemical vapor deposition (APCVD) is capable of being a very high-throughput, low-cost process -- it is the dominant technology used by the glass industry to make low-e coated glass on float lines. In Phase II and III, progress was made

with a new approach for APCVD buffer layers and application (with thin CdS) to high efficiency cells and modules.

A description of the equipment built for this APCVD work is given in sections 3.6.3 and 3.6.4. The approach selected for the early development work, including the criterion for screening for new APCVD chemical systems, was presented during Phase II [17]. New chemistries were identified and successfully tested on 100 cm^2 and then 7200 cm^2 substrates.

The majority of the APCVD buffer/thin-CdS work in Phase III centered around improvement of in-house deposited films on 60cm x 120cm plates. Improvements and experiments included the following:

- Demonstrated buffer-layer deposition at 1 m^2/min throughput
- Investigated effects of flow and geometry on buffer film thickness uniformity and observed possible effects of flow and geometry on resistivity; modification of system design resulted in improved film thickness uniformity
- Demonstrated control of resistivity in buffer layer using substrate temperature
- Investigated alternate non-toxic dopants and alternate methods of introducing chemicals to the reaction zone
- Made significant improvements in run-to-run and plate-to-plate reproducibility with system modifications that solved an exhaust-system clogging problem
- Improved control of the precursor delivery by replacing the bubbler with a liquid mass flow controller.
- Designed a new tandem nozzle for the module-scale system with intent of providing the capability of depositing two different films in one pass.
- Characterized buffer layers for thickness, resistance, optical transmission, elemental makeup, and surface roughness.
- Deposited buffer layers used in cells with efficiency as high as 13.4% and modules as high as 9.0%.

The capability of outside vendors to make buffer layers was also explored. The first batch from one vendor was found to be outside the range of electrical properties needed, and the first batch from another vendor was found to be unstable at cell processing temperatures. In Phase III, runs were conducted at a glass company to test the feasibility of producing a SnO_2:F/buffer film stack on a float line. A seven-hour, float-line test was used to produce three different variations of the TCO/buffer stack. The tests provided very encouraging results, including the FS record efficiency module in section 3.5.

3.2.4 Cells and modules with APCVD-deposited buffer layers

The function of the buffer layer is to allow thinning of the CdS in order to increase J_{sc} without loss in other I-V parameters (primarily V_{oc}, but also FF). In Phase II the function of APCVD buffer layers was verified on cells and modules (e.g., a cell with APCVD buffer on commercial soda-lime glass TCO was produced with an NREL-confirmed efficiency of 13.2% efficiency). In Phase III, progress continued in improving the buffer layers and their use with thin CdS for high efficiency modules. Figure 3.2 provides the relative spectral response of a buffer layer/thin-CdS module with the response of a

standard module also shown for comparison. As can be seen in the figure, module CV114153 (see section 3.1 for IV parameters) has significant response in the wavelengths that would normally be lost in absorption in the CdS (350-500 nm).

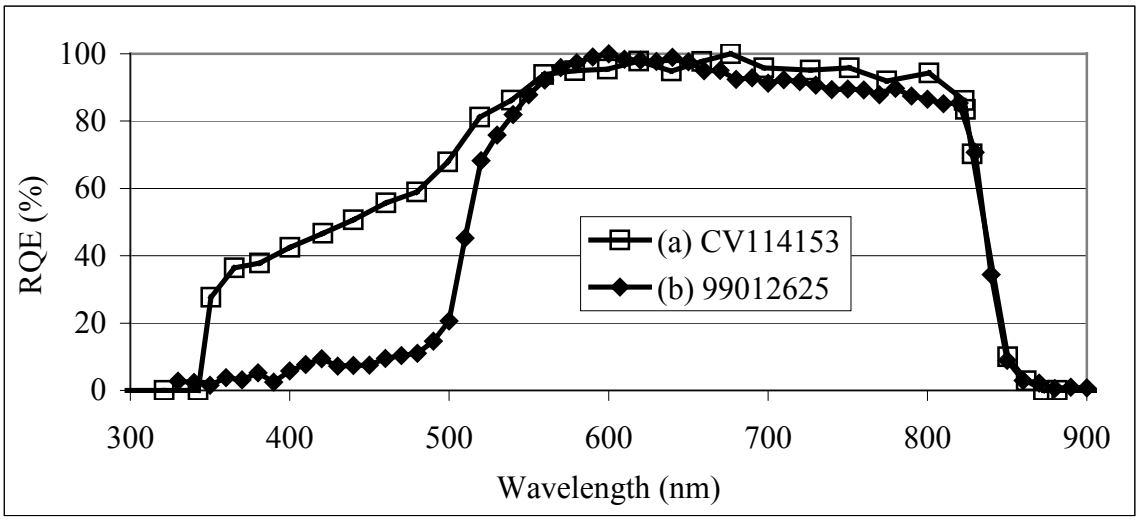

Figure 3.1. Relative spectral response of (a) module with APCVD buffer layer and thin CdS, and (b) standard production cell.

3.3 Improved TCOs

As listed in section 3.1, absorption losses in the commercial TCO used now are on the order of 1.5 mA/cm^2. Decreasing absorption in the TCO from this level to that achieved in lab-deposited TCOs (< 0.5 mA/cm^2) would result in more than a 5% relative increase in module efficiency. Decreasing the sheet resistance of the TCO from 15 ohms/sq to ~6 would provide a similar increase in efficiency. As a result, new TCO layers developed at NREL and other glass/TCO vendors were evaluated for suitability in our process. It was further recognized that the chemistry and deposition-technique developments for buffer layers might be able to advance the state-of-the art for TCOs, either by providing technology to glass/TCO vendors or for in-house for TCO deposition.

3.4 Other loss reduction and diagnosis

The Phase II report included data and analysis on the impact of module non-uniformity. Much of the activity of Phase III has been directed to improving module efficiency by increasing module uniformity.

Module diagnosis has also been increasingly used to improve average production efficiency. Identifying causes of low efficiency enable corrective action to be taken. Proactive experiments to investigate potential problems were also conducted. For example**,** experiments showed that placing a bias on a cell during post-metal heat treat (PMHT) strongly affects the resulting cell -- bias in either direction is highly detrimental to cells. Since cells and modules are sometimes exposed to varying degrees of room light and/or heat prior to the PMHT, another experiment was done to make sure that this was

not a source of variability in product performance. The experiment exposed cells to light (and thus bias and heat) immediately prior to PMHT to find if it was detrimental to cell efficiency or stability. Fortunately, the results of the experiment showed that even 2 days of open-circuit light soak immediately prior to PMHT did not affect the cell efficiency or stability after the heat treat is performed.

3.5 High efficiency modules

Progress in module efficiency was made in each of the contract phases as shown in Table 3.2.

Table 3.2. NREL-measured aperture efficiencies for the 12 modules delivered under each phase of the contract (each module ~0.66 m^2 aperture area and 0.72 m^2 total area).

Contract phase	Champion module aperture-area efficiency	Average aperture-area efficiency for the 12 modules
Phase I	8.1%	7.8%
Phase II	8.9%	8.3%
Phase III	10.1%	9.7%

Detailed results for modules delivered under Phase III of the contract are provided in Table 3.3. The Phase III aperture-efficiency goals for the champion and a 12-module average were 11% and 10% (or best effort), respectively. The modules were produced with high-speed deposited SnO_2 buffer layers by APCVD on a float line and thin CdS by vapor-transport on the production coater.

Table 3.3. NREL-measured IV parameters of 12 modules delivered in Phase III. Each module had a total area of 7200 cm^2 and an aperture area of 6612 cm^2 (Efficiency, I_{sc}, and P_{max} values are from spectrally- and intensity-corrected SOMS and V_{oc} and FF are from LACSS-storage-state measurements)

Module ID	Aperture Efficiency	Total-area Efficiency	P_{max} (W)	I_{sc} (A)	V_{oc} (V)	FF (%)
CV114096	9.57	8.79	63.30	1.14	91.3	60.3
CV114106	9.51	8.73	62.89	1.14	91.6	59.4
CV114107	9.49	8.71	62.75	1.12	92.3	59.6
CV114110	9.59	8.81	63.41	1.13	93.2	60.0
CV114124	9.55	8.77	63.18	1.12	93.6	59.8
CV114125	9.61	8.83	63.52	1.12	94.0	59.9
CV114131	9.58	8.80	63.33	1.13	92.3	60.2
CV114132	9.65	8.86	63.83	1.13	93.2	60.3
CV114136	9.66	8.87	63.90	1.12	93.1	60.7
CV114138	9.70	8.91	64.12	1.12	93.5	60.7
CV114153	**10.15**	**9.32**	**67.12**	**1.16**	**94.8**	**60.4**
CV114175	9.77	8.97	64.57	1.16	93.9	59.1
Average	9.65	8.86	63.83	1.13	91.3	60.0

In order to more easily compare module results to cell results, IV parameters can be converted to an average per-cell basis. Taking the parameters for the champion module above, the average cell V_{oc} (116 cells per module) was 827 mV and the average J_{sc} (53 cm^2 per cell) was 21.9 mA/cm^2.

3.6 Research equipment development

The construction and improvement of research equipment was vital to the progress made in efficiency (as well as the other progress) described in this report. Equipment not described elsewhere in this report that was constructed at the FS Technology Center for use in research is described below.

3.6.1 Large-area sputter deposition system

A multi-cathode sputtering system was constructed that is capable of depositing films on 60 x 120 cm^2 plates. Problems that were overcome, such as system leaks and power dissipation difficulties, were discussed in quarterly reports. The system has excellent uniformity (< 10% variation in thickness and resistivity) and base pressure (3 x 10^{-6} torr). The system was used for deposition of buffer layers by sputtering (for comparison to the APCVD buffer layer), for deposition of standard contacts for R&D, and for alternative contacts research on the cell and module level.

3.6.2 Small-area VTD system

A small-area VTD system was constructed to enable additional deposition research, including experiments where contamination risk would be unacceptable for the large-scale systems. Substrates up to 4" x 8" in size are introduced through an entrance load lock and are pushed onto a moving mesh belt. The substrates creep through a pre-heat zone, then are accelerated for transport past the vapor distributors at speeds similar to those used in module-scale equipment. After deposition, the substrates slide off the belt into a tray that shuttles into the exit load lock. In Phase II a more robust stainless steel exhaust manifold was installed, but concerns about flaking from the oxidized stainless led to replacement with a ceramic manifold. A period of non-standard deposition behavior, characterized by low cell short-circuit currents and unplanned sublimation of CdTe from an internal surface within the system, provided some information about non-optimum CdS/CdTe junction formation. In Phase III, additional modifications were made after more periods of non-standard deposition behavior were traced to thermometry and contamination problems.

3.6.3 Small-area APCVD systems

Three small-area APCVD systems were built. One was a small reactor that used SiC-fiber substrates in order to explore new chemical systems; the reactor uses laboratory-glass components and was inexpensive to construct and easy to clean. Two other systems were built to investigate deposition on glass. These systems accommodate 10 x 10 cm^2 glass substrates and were used to investigate deposition, film, and device characteristics. The systems use stainless steel chambers with the glass substrate heated by a graphite

block. Chemical precursors are carried into a mixing manifold, which is a double-wall tube with heated air passed through the outer tube for temperature control.

3.6.4 Large-area APCVD system

A module-scale system for APCVD of buffer layers (Figure 3.2) was developed by using the glass heating and transport portions from a previous-generation semiconductor deposition system. The system is capable of depositing on a 60cm-wide web. While this system is limited to a speed of ~1.8 m/min, the process is suitable for a glass line speed of 12 m/min. Additional details about the development of the system were provided in section 3.2.3.

Figure 3.2. APCVD system for module-scale buffer-layer deposition.

4. Characterization and Analysis

4.1 Characterization of films and devices

4.1.1 Cell I-V measurements

In order to increase the speed and ease of taking cell I-V measurements, an 18-probe contacting head for automated I-V measurements was designed, built, and placed in operation (Fig 4.1). With this probe, which uses spherical-radius gold-plated POGO pins, light and dark I-V measurements for 18 cells (in a proscribed pattern on a 10cm x 10cm sample) can be done in 130 seconds. Due to the air-cooling provided during the measurements, the temperature rise before and after a light and dark eighteen-cell measurement is less than 2ºC. During the contract period, over 360,000 cell light I-Vs (and the same number of dark I-Vs) were taken.

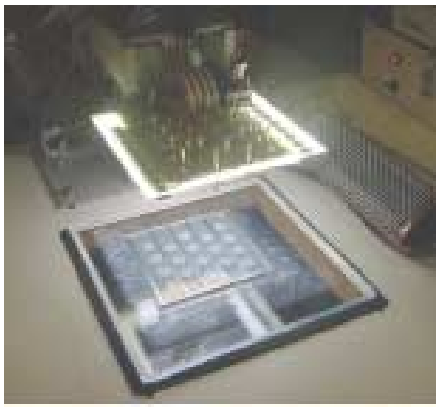

Figure 4.1. Cell IV system with 18-pogo-probe contacting head and pneumatic actuation

4.1.2 Large-area film characterization

New automated measurement systems and techniques were developed to provide spatial mapping of film characteristics on full-size (60 x 120 cm^2) plates. The systems use fixed-position excitation/detector pairs with X-Y movement of the plate enabling high-density mapping of film qualities. One system, shown in Figure 4.2a, has the ability to map CdS thickness, CdTe thickness, surface reflectance (as in indication of surface roughness), cell efficiency, contactless-V_{oc}, and pinhole density. The output of the system in the CdTe thickness mode is shown in Figure 4.2b -- this plate was deposited with a 30" wide slot to determine the sharpness of the deposition edge. The contour plot for this module was done with an 1800-point map of the plate (system output can also be done in color contour maps).

Figure 4.2a. X-Y characterization system #1

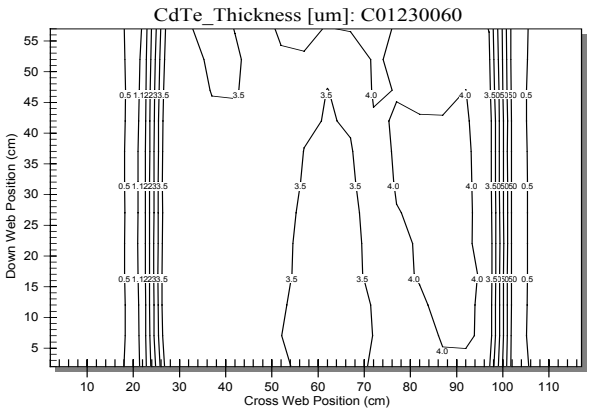

Figure 4.2b. Example of system output (contour plot of CdTe thickness for experimental plate with 30" wide slot)

The CdS thickness mapping is done using optical absorption of a gallium nitride quantum-well LED with improved detection electronics so that calibration before each scan is not required. CdTe thickness mapping is done with an 808 nm 5 mW laser with thermo-electric cooling of the diode to prevent mode hopping and a DSP lock-in to improve signal acquisition. CdTe thicknesses up to 5 μm can be measured with only 0.5 s per data point. The upper end of the thickness range was achieved by the use of a filter that eliminates signal from photoluminescence from the film. Cell efficiency is mapped using a simple W-filament backlight and contactless-V_{oc} (also called the SPV, or quasi surface photovoltage) is mapped using a graphite pad and high-impedance electrometer. The system had the capability of mapping pinholes using a CCD camera and frame grabber, but the lack of pinholes in recent CdTe deposition eliminated the need for this measurement.

The second system (see Figure 4.3a) uses the same basic X-Y motion, but focuses on sheet resistance mapping. A 4-point probe on a pneumatic extender provides a range of 0.01-10MΩ/square. Repeatability of the system was verified by taking 128 measurements on the same spot, spread out over a 1-hour period -- the error in the measurements was only +/- 0.02%. Speed of the system was verified by mapping a 60 cm x 120 cm plate with 128 points in less than 4 minutes. The system was used to find (and verify the fix for) an asymmetry in the R&D module-size sputtering system. An example of output from the system is shown in Figure 4.3b.

Figure 4.3a X-Y characterization system #2

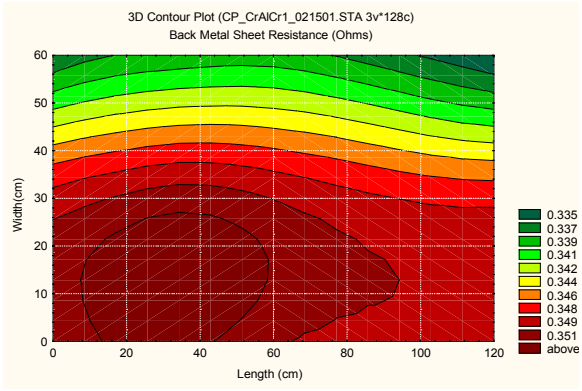

Figure 4.3b Example of system output (sheet resistivity function)

4.1.3 Submodule V_{oc} mapping

A system was developed to map the open-circuit voltage of submodules using ~0.1 sun illumination (see Figure 4.4). Use of fluorescent lamps with intensity feedback allows low-cost, uniform illumination, and the low light level allows for extensive characterization of plates without significant substrate heating. Use of the system allowed correlation of V_{oc} to film characteristics.

Figure 4.4a Low-light V_{oc} mapping system

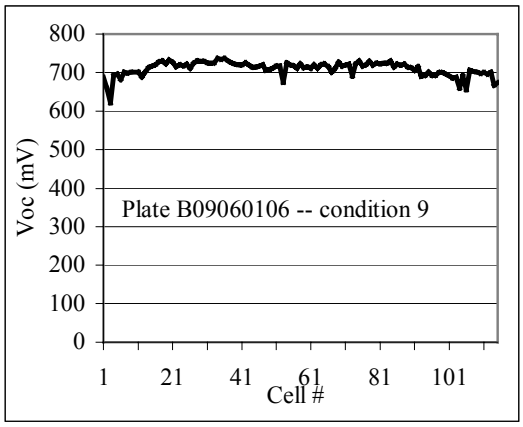

Figure 4.4b. Example of output of system (experimental-condition plate)

4.1.4 Spectral response

A grating-monochromator-based quantum efficiency (QE) system was designed, assembled, and used to characterize cells. The system provides high-resolution measurement of the spectral response of solar cells, with scans normally done over the range of 320 to 1000 nm. In addition to characterization of next generation cells (e.g. to determine the blue-light response of thin-CdS cells), the system was used for failure analysis (e.g., to determine whether low J_{sc} cells were the result of low carrier lifetime or a deeply-buried electrical junction).

4.1.5 C-V and C-F characterization

A new admittance (capacitance, C, and conductance, G) measurement system was developed. The system measures admittance as a function of voltage (V) and frequency (F) to provide information on doping profile and trap density in cells. As described in the phase II report, the system uses Digital Signal Processing to extend the low frequency measurement limit to 0.001 kHz and the phase angle acceptance to near zero, in contrast to commercial systems which typically are limited to above 10 kHz and phase angles of ~5°. The new capability enabled the characterization of deep trap levels, even in devices with low shunt resistance. Use of the system over a broad frequency range indicated the presence of a continuous distribution of defects around the Fermi level in devices [18].

4.1.6 Spectrophotometry – band edge sharpness

A spectrophotometer with infrared to UV range and an integrating sphere was purchased and installed. The system provides the ability to do optical characterization (spectral and total R and T) of films and devices. The system was used to investigate the sharpness of the CdTe band-edge in cells as a metric of material quality. It was found that the sharpness, as judged by the slope of the total reflectance curve, significantly increased after $CdCl_2$ treatment (as expected) and that subtle differences could be found between samples after $CdCl_2$ treatment. In particular, it was found that the $CdCl_2$ temperature previously determined to give the best performing devices had a slightly sharper

transition than cells with $CdCl_2$ treatment done at temperatures 10ºC higher or lower. However, the differences between samples of different morphologies, but similar performance, were found to be greater than the differences caused by the $CdCl_2$ temperature. It would thus not be possible to infer strictly from the test whether or not the material is above a performance threshold.

4.1.8 Scribe contact resistance

As described in the Phase II report, contact resistance (ρ_c) measurements were made using a 25 μm scribe-width laser pattern. The ρ_c of the standard IFL/metal to the TCO was found to be only 0.00025 Ωcm^2, which would result in minimal module losses (only ~1.6% of the loss from lateral transport resistance of the TCO). In contrast, the ρ_c of an alternative IFL to the TCO was found to be high enough to significantly affect module performance and would thus require scribing after the IFL is deposited. The ρ_c of metal to CdS, which would occur in the case of incomplete ablation in scribe 2, was also found to be non-negligible -- the 0.0022 Ωcm^2 value would add ~14% to the loss from TCO lateral resistance.

4.1.9 Electron-Beam Induced Current (EBIC)

EBIC was used extensively to characterize CdS/CdTe films and devices. Increased collection at the grain boundaries was noted and was explained by the presence of built-in electric fields that effectively separate non-equilibrium electron and holes and thus suppress their recombination. Non-uniformities in planar EBIC response were noted and used to explain cell behavior. Degradation of EBIC collection under extended electron-beam exposure was studied as a high-acceleration-factor life test, and is discussed in section 4.2.1.3. Detailed results of the EBIC studies were presented in the Phase II report and in publications [19, 20].

4.1.10 SEM/EDS

The SEM/EDS system in R&D was improved with a new data acquisition system and an EDS (energy dispersive spectroscopy) system upgrade to allow light-element detection, including oxygen.

4.1.11 Photoluminescence studies

In cooperation with the University of Toledo, photoluminescence (PL) was used to investigate the electronic states of impurities in CdTe films and cells. Details beyond those given below were included in the Phase II report and publications [21-23]. An important result of the study was the proposal that the shallow acceptor seen with Cu-doped/Te-annealed samples (the 1.555eV transition) is due to Cu_i-V_{Cd} states rather than Cu_i-Cu_{Cd} or Cu_{Cd}-Cd_i. This complex was also found to be more stable than acceptor complexes in Cd-rich samples. In Cd-annealed samples the amplitude of the bound-exciton region of the spectrum dropped by a factor of 2-3 and shifted towards higher energies. This shift is due to the drop in intensity of the 1.59 eV exciton-bound to Cu_{Cd} relative to bound-exciton transitions at higher energies. In addition, the 1.45 eV DAP band exhibited a drop of 6000 times. In contrast, the Te-annealed sample exhibited a

relatively constant overall luminescence signal although it is much weaker than for the fresh Cd-annealed sample. The decrease of the Cu_{Cd} related PL transitions in samples annealed in a Cd overpressure compared to their stability in samples annealed in a Te overpressure indicated the important role played by the Cd vacancies in "stabilizing" Cu atoms in the CdTe lattice. It was suggested that Cu_{Cd} states are likely to dissociate at a similar rate regardless of the density of Cd vacancies, but a diffusing Cu_i^+ ion has a higher probability to recombine with a new V_{Cd}^- in a sample with an increased number of Cd vacancies. In the absence of the Cd vacancies, Cu ions are more likely to precipitate or otherwise participate in the formation of non-radiative recombination centers.

A separate study was done with instrumentation at the University of Toledo in which the effects of an applied field on junction photoluminescence were studied. Results are consistent with the idea that applying a bias strongly influences the ability of the carriers to recombine radiatively; moreover, this process is dependent on intrinsic characteristics of the device.

4.1.12 Performance of modules under non-standard conditions

The Phase II report described the results of investigation of the performance of our modules at non-standard conditions. Briefly, a paper study and some experiments were done in response to reports from the field that First Solar modules were doing well relative to other technologies in non-standard conditions such as high temperature, low light, and end-of-day conditions. Good performance in late afternoon is consistent with the cosine response of the modules and the fact that they are single junction. Good performance at elevated temperature is consistent with the lower temperature coefficient of the modules relative to crystalline silicon (an average of -0.15%/C vs. -0.45%/C). The temperature coefficient did, however, show a broad range for different vintages of modules and different measurement techniques. In total, the energy output of the modules may have been 3-10% greater than equally-rated silicon modules. Greater reproducibility from larger-scale production and implementation of the expected Module Energy Rating standards will better quantify the total energy advantage for the CdS/CdTe modules vs. other technologies.

4.1.13 Back contact effect on V_{oc} -- micro-nonuniformity

Experimentation and modeling about back contact effects was done and presented at Team meetings. At the January 2000 National R&D Team Meeting [24] we showed the I-V of two cells where the presence of the metal layers without an interfacial layer (IFL) suppressed cell V_{oc} by 500mV; i.e., the cell with no IFL had low V_{oc} (~300mV) with metal contact on, but had ~normal quasi-surface photovoltage (~780mV) with metals stripped off. These cells IVs are shown below in Figure 4.5a. We had proposed that standard one-dimensional models had not been able to explain a 500 mV suppression of V_{oc} from the back contact. At the January 2001 National R&D Team Meeting [25] we presented finite difference modeling of a discreet network of diodes with one network node assumed to have a significantly higher j_o -- this simple modeling showed that micro-nonuniformity is capable of producing the large suppression of V_{oc} (when the back contact metals are on the device and thus able to provide high lateral conductivity). The

IVs from the finite difference (FD) modeling are shown in Figure 4.5b. The results of LBIC maps done by Jason Hiltner (Colorado State University) on a set of devices we had provided for this purpose (including cells with the IFL layer omitted and cells subjected to accelerated testing) showed that high micro-nonuniformity was consistent with low efficiency for the set -- two of the images are included below in Figure 4.6 and additional scans were presented at the CdTe National R&D Team meeting [25]. It was also presented, however, that cells that start out with high non-uniformity did not necessarily increase in non-uniformity with accelerated stress testing and changes in micro-uniformity are likely not the only effects from accelerated stress testing.

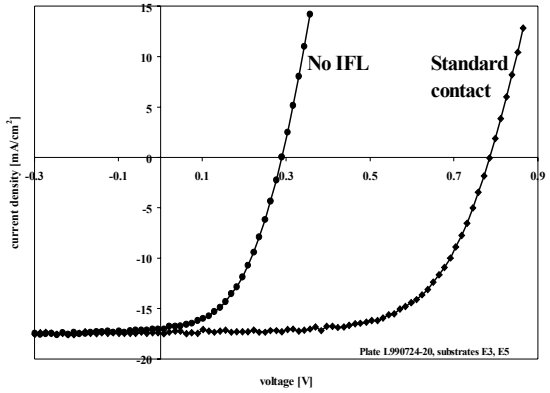

Figure 4.5a. IVs of two cells (high V_{oc} cell with standard contact and low V_{oc} cell with IFL omitted)

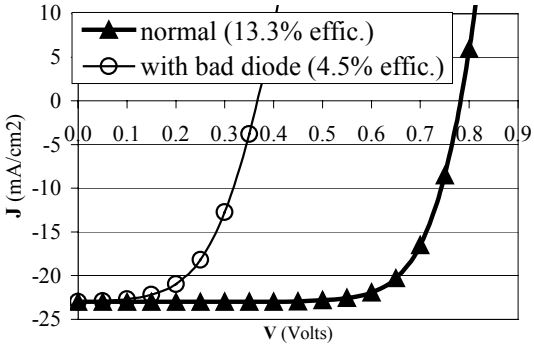

Figure 4.5b. FD-modeled IVs of two cells (one uniform and one with a small area of high j_o)

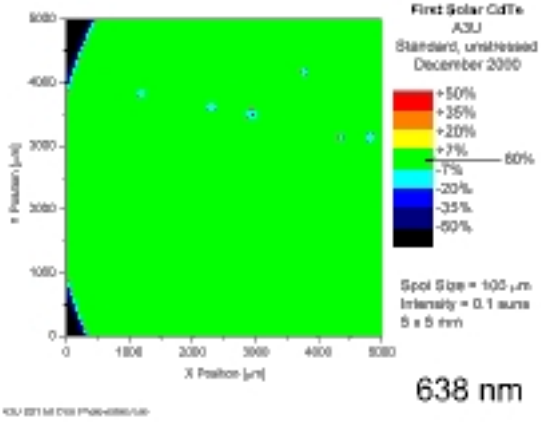

Figure 4.6a. OBIC map of 10.3% η standard cell (courtesy of J. Hiltner, CSU)

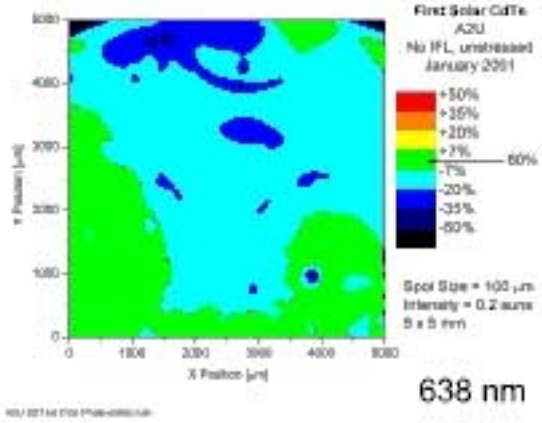

Figure 4.6b. OBIC map of 2.2% η "no IFL" cell (courtesy of J. Hiltner, CSU)

Micro-nonuniformity was also studied from a more fundamental standpoint. Other evidence of micro-nonuniformity in cells (from EBIC, PL, thermal paper, and experiments with very thin metal layers) was detailed in the Phase II report. In response to the potential importance of micro-nonuniformity in the performance of thin-film photovoltaics, a new approach to closed-form analysis of the problem was developed and published [26].

4.1.14 Shunts, screening effects, and I/V interpretation

An area of investigation closely related to the issue of non-uniformity (which was discussed in the previous section) is the effect of shunts on the performance of cells. A closed form-solution, verified by numerical modeling, was developed that enables calculation of the area affected by a point-perturbation such as a shunt. In addition to providing a useful tool for analysis of cells with shunts, the solution has the important implication that the voltage (V) applied to a cell by attaching two electrodes is not the voltage seen by all parts of the cell and that the effect of the deviation from the uniform-voltage assumption is governed by the same screening relationship as shunts. Thus the measured I-V characteristics of the cell will depend on the relationship between the cell size (l) and the screening length (L), being markedly different for the cases of small ($l<<L$) and large ($l>>L$) cells. Because L is voltage dependent, the standard interpretation of the PV cell I-V characteristics needs to be revised. Details of the analysis and the implications to cell analysis were given in the Phase II report and subsequent publications [27, 28].

4.1.15 Diagnostic procedures

Staff doing diagnostics of a submodule got two unexpected results: 1) some cells had appreciable V_{oc} in the dark, and 2) some cells had higher V_{oc} on a low light table than on a 1-sun simulator. Analysis was done to try to determine the cause of these results, which if left unexplained, would have resulted in decreased confidence in, and use of, our diagnostic procedures. It was determined that the V_{oc} in the "dark" was actually V_{oc} in very low light -- the cells had such high shunt resistance that leakage of room light from the top through the scribes and from the bottom by reflection was enough to give V_{oc}s above 400mV. It was also determined that the low-light/high-light anomaly was the result of a current loop caused by the front contact probe not being placed close to the cell of interest. Diagnostic procedures were modified accordingly.

4.1.16 External characterization results

Several groups, including NREL, the Institute of Energy Conversion, Colorado School of Mines, and Colorado State University, have provided characterization to aid in our effort to understand the operation of CdS/CdTe cells. The Phase II report included results of AFM and XRD characterization of TCO and CdS layers and concluded that SnO_2 grain size could influence CdS grain size.

In Phase III, external characterization included room-temperature, high-injection photoluminescence measurements on a cell set we prepared. Brian Keyes of NREL performed continuous-wave PL spectroscopy (CW-PL) and time-resolved PL (TRPL), but the results showed no differentiation among cells that had degraded or were susceptible to degradation with light soak from unstressed or stable cells (i.e., PL and TRPL did not correlate with the efficiency of the cells or any degradation metrics). Dr. Keyes specifically looked for evidence of non-uniformity in the cells, and found none except for a small amount in one cell (the one cell was a degraded cell that had been mostly revived with an anneal - it had a small area with a 700 nm broad peak, possibly a defect level in the CdS). The search for non-uniformity was done using a spot size of ~1 mm, and was of course only able to measure differences detectable by PL and TRPL (primarily material quality of the CdTe). These results do not rule out a change in carrier-concentration in the CdTe, but they do indicate that there was not a significant decrease in CdTe material quality with light soak in the set studied.

4.2 Reliability Verification and Improvement

4.2.1 Accelerated-test development

To the extent that they can be correlated with field performance, accelerated-life tests (ALTs) are useful in setting module warranties and to be able to make process changes with confidence. However, even without proven correlation, ALTs can be valuable because i) a failure mechanism in an ALT that is not currently seen in the field could be a problem later if some unknown protector is lost, ii) improved performance of cells in ALTs could lead to cost savings by reducing encapsulation or other requirements otherwise needed to protect performance, and iii) the fact that something changes in cells with ALTs (including improvement in performance in some cases) is an important source of understanding for cell operation and could thus lead to better conceptual and numerical models and higher performance.

4.2.1.1 Light-soak equipment and technique development

A new environmentally-controlled light soak system was constructed and described in the Phase II report. In Phase III, light-soak testing space for modules was expanded to accommodate 40 modules at a time.

A preliminary attempt was made to correlate field data with light soak data and the results were presented at the National CdTe R&D Team meeting in January 2001 [29]. A numerical correlation requires fielded modules with before- and after measurements that have cells made and stressed on plates from the same batch. The data set meeting these conditions turned out to be small (70 data points) and was not monolithic (e.g., included different durations and field conditions); nevertheless, a correlation of 67% was found for the set. Comparison of typical light soak and field performance for different eras and recipes also suggested some correlation.

4.2.1.2 Laser-soak equipment and technique development

The Phase II report introduced laser-light soaking with an 808 nm IR diode laser system as a potential for a very-high-acceleration factor stress test. In Phase III, work continued

with verification that even at high intensity, heating of the microcell (0.87 mm^2) from the laser was small. The cell temperature under illumination was measured by contacting a type T micro thermocouple to the cell with a minute amount of heat sink compound. The temperature rise as a function of intensity was found to be 0.15°C/sun (thus 100 sun intensity resulted in a cell temperature only 15°C above ambient). To better test whether laser-soak might provide a useful indicator of cell stability, a system with 8 lasers was built to expand throughput of the testing.

Initial results of laser soak (from the first 120 cells) showed some correlation with light soak (a correlation coefficient of 0.56 between 24 hours of laser soak and 14 days of open-circuit (OC) light soak), but continued collection of statistics showed a worsening correlation. Further analysis revealed that the initial correlation was the result of inclusion of low-efficiency cells that significantly increased in efficiency in both laser and light soak. The fact that in laser soak the primary failure mode was loss of J_{sc} while in light soak the primary modes were V_{oc} and FF gave additional cause for concern. While the laser soak technique likely offers some information on changes in material properties under stress, it was decided that it did not provide a simple, high-acceleration factor stress test.

4.2.1.3 EBIC accelerated-test technique development

In Phase II, we introduced planar EBIC (electron-beam induced current) as a potential for a very-high-acceleration factor stress test [19, 20, 30]. Analysis of statistics from the first 16 plates (6 cells per plate) showed a correlation coefficient of 0.58 between 20 sec of EBIC exposure and 14 days of OC light soak. The fact that there was some correlation seemed to support the possibility of a degradation mechanism related to non-equilibrium electrons and holes. Like laser-soak, however, 1) some of this correlation was from the inclusion of lower-efficiency cells that increased in efficiency from light soak, and 2) the correlation weakened with measurement of additional cells. The technique continues to provide useful information about material properties, but does not appear to offer a simple, high-acceleration factor stress test at this time.

4.2.2 Documentation of reliability of devices, modules, and arrays

4.2.2.1 Field performance

A summary of the performance of some First Solar arrays (at NREL, TECO, PVUSA, and China Lake) was presented to the CdTe National R&D Team in January 2001 [29] and in the Phase II report. The data presented to the Team included two populations of modules from the TECO (Toledo Edison) array in Toledo, OH. Population 1 had a pre-fielding total-area efficiency average of 6.9% and a post-field (after 5 years in the field) of 6.7%, but there was some variation in performance within the population. Population 2 (which had a different processing condition) had a pre-fielding average of 6.8% and a post-fielding average (after 5 years in the field) of 7.6% -- 25 of the 27 modules in this population had efficiency higher after 5 years than when fielded.

The 1 kW First Solar array at NREL continued to be the best-documented demonstration of field stability for a CdTe PV array. The performance of the array was analyzed even beyond that presented in the Phase II report and to the National Team. Overall, the array

was stable over the 5-year period in the field, but with variability in individual modules (particularly in FF). A paper on the array was presented [31].

In Phase III, a new test field with high-quality monitoring was set up in Scottsdale, AZ. Work within the subcontract included development of the measurement approach. The field was designed to hold 30 arrays with inverters that can have up to 18 modules each. To enable all modules to be measured individually without disconnecting any wiring, all modules within an array are wired in parallel to each array's inverter box. Additionally, there are facilities to mount 72 modules with individual biasing (short-circuit, open-circuit, or resistive load). The measurement approach selected uses two independent calibration standards to reduce the chance of a systematic measurement error (and thus increase confidence in the results). A curve tracer is used to take module I-Vs with a filtered GaAs cell as one standard and spectrally-corrected pyranometer data as the other standard. DC/AC input/output from the inverters is also datalogged to provide additional data beyond the periodic curve-tracer measurements.

4.2.2.2 Accelerated life tests

The IV measurements for the second round of stability tests for the CdTe National Team were completed and presented to the Team [32] with details included in the Phase II report. Existence proofs of modules with increasing performance from 90 days of light soak at 65°C were also included in the report.

4.2.3 Failure-mechanism research and mitigation

In both outdoor data and light-soak tests there are examples of cells and modules that have received very long term exposure with no degradation or even with improvement of performance; thus, it is clear that degradation processes in our devices can be avoided -- one of our key objectives is to determine the degradation modes and mechanisms so that we can ensure that the stability will be excellent every time.

Several items in the characterization section of this report (4.1) are targeting to understanding device performance, which includes how cells operate and what might change with stress. For instance, the work described in section 4.1.11 and 4.1.13 identified two potential failure mechanisms. Additional work includes the following:

- Collaborative efforts were undertaken, including support of an effort at Colorado School of Mines. Samples, including CdS deposited on bare glass in the high-throughput coater, were prepared and sent to Scott Townsend. The goal is to use in-plane admittance spectroscopy to learn more about grain boundaries and the effects of various cell-processing steps.
- In-house, screening and optimization experiments have indicated that process-variables in the $CdCl_2$ and back-contact steps can affect device stability. For the $CdCl_2$ process there was lower light-soak stability for treatments significantly below or above the optimum temperature range. For the back contact process, several variables have been identified that influence short-term light-soak performance.
- An additional experiment described in the Phase II report was conducted to separate the effects of heat and light on cell degradation (separating failure modes

is important for the testing of simple analytical models and the development of failure-acceleration factors). Cells that were known to be susceptible to degradation were light soaked at 65°C and 0°C and were placed in the dark at 65°C and 0°C. The results indicated that for the product architecture used in the experiment, heat alone can result in an increase in the cell series resistance (presumably from an increase in the back contact resistance) while the combination of heat and light is necessary for appreciable degradation of the open circuit voltage.

- Because contact formulation has been identified as the most important variable in First Solar cell stability, and because alteration of contact formulation could potentially raise module efficiency and lower production costs, alternative contacts were investigated as described in section 2.2.3.

5. Environmental, Health, and Safety

5.1 General program

Despite increased research and production activities, a safe working environment was maintained. Detailed results of the medical monitoring program were published [9]. Later, a hazard recognition and internal audit program was instituted to ensure continued success, and invited independent audits (from the EPA and Ohio Bureau of Workmen's compensation department of industrial hygiene) confirmed a safe working environment. Furthermore, recycling of off-spec and end-of-life modules is done on site, and all facilities have received a *de minimus* emission rating level, so no permitting is required. The majority of the work on the EH&S program was supported by internal and PVMaT funds, but specific efforts to conduct research safely and to identify and reduce environmental and safety hazards as detailed in the Statement of Work were part of this subcontract.

5.2 Material handling and emissions review

A comprehensive emission survey was conducted in February 1999 with the results detailed in the Phase I report. The survey indicated that Cd emissions are essentially zero (< 1% of amount requiring permitting even for 100MW/yr production). Success of the EH&S program continued in Phase II and III with no additional air or water Cd emissions identified. A potential issue with organic emissions was identified (and solved) and is discussed in the next section. Near the end of Phase III, it was determined that the capacity of the closed-loop wastewater system and the volume limits for small-generator solid-waste disposal might constrain production-volume ramp-up; process and equipment improvements to address these problems will continue outside of the contract.

5.3 Process and equipment improvements

5.3.1 Aqueous $CdCl_2$

In Phase I, organic emissions from the existing wet-$CdCl_2$ process were identified as the only emissions from the new plant that would require permitting if the process were scaled to high-volume manufacturing. $CdCl_2$-in-water was thus investigated in Phase II as an alternative to the $CdCl_2$-in-methanol process as a way to reduce emissions and achieve the goal of a "zero emissions" plant. Due to lower wetting action of the aqueous solution, some modifications of the application approach were required to improve uniformity and consistency. As described in the Phase II report, the new aqueous process was made the standard for the production line after small-area and full-production experiments showed that the new process produced as good as, or better, initial efficiency and stability performance compared to the old methanol process.

5.3.2 Edge delete

Part of module finishing involves the removal of the outer ~1cm of films to prevent edge shunting and moisture ingress in encapsulated modules. Improvements to the

sandblasting technique were reported in the Phase I report that resulted in improved operator safety and a reduction of hazardous waste. Additional work with grinding wheels as a replacement of sandblasting technique (see Phase II report) showed promise, but adequate manufacturing robustness was not achieved with the process.

5.3.3 CdS material preparation

In order to maximize the quality and consistency of deposited CdS films, the physical characteristics of the CdS powder must be in a certain range. In Phase I, new equipment was added for the CdS preparation steps (grinding/sintering) that improved operator safety, improved CdS quality, and reduced CdS waste. In Phase III, the need for in-house pre-deposition processing was eliminated after work with a CdS vendor resulted in that vendor being able to provide the necessary CdS characteristics as-delivered.

5.3.4 Other improvements

Other process and equipment improvements, such as the introduction of a waste compactor, a $CdCl_2$ vapor collection system, and a wastewater treatment system were reported in Phase I. In Phase III, testing and equipment upgrades were done for research equipment as part of the hazard identification and audit program. For example, environmental exposure testing was conducted on the C24 APCVD system -- despite non-detect levels on all the tests, the fume-scrubber capacity was increased on the system to provide an extra margin of safety.

Glossary of Abbreviations

ALT	Accelerated life test
APVCD	Atmospheric-pressure chemical-vapor deposition
C	Capacitance
Cd_i	Interstitial cadmium
Cu_{Cd}	Copper on a cadmium site
Cu_i	Interstitial copper
DAP	Donor-acceptor pair
DSP	Digital signal processor
EBIC	Electron beam induced current
EDS	Energy dispersive spectroscopy
EVA	Ethylene vinyl acetate
F	Frequency
FD	Finite difference (numerical solution)
FF	Fill factor
FSEC	Florida Solar Energy Center
G	Conductance
IFL	Interfacial layer
I-V	Current-Voltage measurement
J_{sc}	Short circuit current
LED	Light emitting diode
LOF	Libbey-Owens Ford
MW_p	Peak megawatts (at standard conditions) of PV produced
NREL	National Renewable Energy Laboratory
OBIC	Optical beam induced current
OC	Open circuit (bias during stress)
PL	Photoluminescence
PV	Photovoltaics
PVMaT	Photovoltaic Manufacturing Technology Program
PVUSA	Photovoltaics for Utility Scale Applications program
RL	Resistive load (bias during stress - near maximum power point)
R_{oc}	Resistance at open circuit (~series resistance)
R_{sc}	Resistance at short circuit (~shunt resistance)
SC	Short circuit (bias during stress)
SIMS	Secondary-ion mass spectroscopy
SnO_2:F	Fluorine-doped tin oxide
TCO	Transparent conducting oxide
V	Voltage
V_{Cd}	Cadmium vacancy
V_{oc}	Open circuit voltage
VTD	Vapor transport deposition

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13. ABSTRACT *(Maximum 200 words)* This report describes the significant progress made in four areas of this subcontract: process and equipment development; efficiency improvement; characterization and analysis; and environmental, health, and safety. As part of the process and equipment development effort, vapor-transport deposition (VTD) was implemented first on a 60-cm-web pilot-production system, then on a 120-cm-web high-throughput coater. Deposition of CdS and CdTe films at a throughput of 3 m^2/min was demonstrated, and more than 56,000 plates (each 0.72 m^2) were coated -- 16 times the total number coated prior to the start of the contract. Progress was also made in the conversion efficiency and yield of both standard and next-generation modules, with data from more than 3000 sequentially deposited modules having an average total-area conversion efficiency of 7% and next-generation modules produced with efficiency as high as 9.3% (10.15% aperture-area efficiency as measured by NREL). Successful implementation of in-situ CdS thickness measurements was important to progress in thickness uniformity and control. Net CdTe material utilization of 82% was demonstrated. The ability to raise the utilization further was shown with the demonstration of inherent CdS and CdTe material utilizations of over 90%. Post-CdTe-deposition process development, which included process space exploration and problem diagnosis, was an important part of advances in efficiency and yield. As part of the efficiency-improvement task, research was done on cells and modules with reduced CdS thickness to increase photocurrent.

SUBJECT TERMS: PV; vapor-transport deposition; coater durability; semiconductor film thickness; interfacial layer; back-contact; recrystallization; electron-beam-induced current; photoluminescence; open-circuit voltage; finite difference; light-emitting diode

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