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Subcontractor Report

Atmospheric Pressure Chemical Vapor Deposition and Jet Vapor Deposition of CdTe for High Efficiency Thin Film PV Devices

Final Technical Report
26 January 2000 — 15 August 2002

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ITN Energy Systems
Littleton, Colorado

National Renewable Energy Laboratory

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Title: **Atmospheric Pressure Chemical Vapor Deposition and Jet Vapor Deposition of CdTe for High Efficiency Thin Film PV Devices**

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Abstract: ITN's three year project Atmospheric Pressure Chemical Vapor Deposition (APCVD) of CdTe for High Efficiency Thin Film PV Devices has the overall objectives of improving thin film CdTe PV manufacturing technology and increasing CdTe PV device power conversion efficiency. CdTe deposition by APCVD employs the same reaction chemistry as has been used to deposit 16% efficient CdTe PV films, i.e., close spaced sublimation, but employs forced convection rather than diffusion as a mechanism of mass transport. Tasks of the APCVD program center on demonstration of APCVD of CdTe films, discovery of fundamental mass transport parameters, application of established engineering principles to the deposition of CdTe films, and verification of reactor design principles which could be used to design high throughput, high yield manufacturing equipment. Additional tasks relate to improved device measurement and characterization procedures that can lead to a more fundamental understanding of CdTe PV device operation and ultimately to higher device conversion efficiency and greater stability. Under the APCVD program, device analysis goes beyond conventional one-dimensional device characterization and analysis toward two dimension measurements and modeling. Accomplishments of the concluding year and extension of the APCVD subcontract included: incorporation of HRT buffer layers and achievement of 12.3% efficient (NREL measured, but not certified) devices by APCVD; analysis of scale-up issues related to APCVD, analysis of dust formation dynamics; demonstration of the inherent deficiencies of APCVD for CdTe manufacturing; modeling effects of CdSTe and SnO_x layers; and electrical modeling of grain boundaries. design and construction of a low-pressure jet vapor deposition (JVD) reactor; JVD CdTe film characterization as a function of substrate and source temperature; demonstration of high growth rates using JVD; and superstrate type and substrate type device fabrication using low substrate temperature JVD CdTe films.

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1 Project objective

ITN's three year project Atmospheric Pressure Chemical Vapor Deposition (APCVD) of CdTe for High Efficiency Thin Film PV Devices has the overall objectives of improving thin film CdTe photovoltaic (PV) manufacturing technology and increasing CdTe PV device power conversion efficiency. Tasks required to accomplish the overall goals are grouped into 1) development of APCVD apparatus and procedures which enable controlled deposition of device-quality film over large areas and 2) development of advanced measurement and analytical procedures which provide useful and effective device characterization. It was found through the course of this work that that APCVD has inherent limitations that limit its ability to meet the overall objectives described above. An alternative technique, Jet Vapor Deposition (JVD), was proposed and developed.

2 Approach

CdTe deposition by APCVD employs the same reaction chemistry as has been used to deposit 16% efficient CdTe PV films[1,2], i.e., close spaced sublimation (CSS), but employs forced convection rather than diffusion as a mechanism of mass transport. Tasks of the APCVD program center on 1) demonstration of APCVD of CdTe films, 2) discovery of fundamental mass transport parameters, 3) application of established engineering principles to the deposition of CdTe films and, 4) verification of the reactor design principles which could be used to design high-throughput, high-yield manufacturing equipment. During the last phase there was a major change in the direction of the project, based on extensive experimental studies and theoretical support of the APCVD deposition process. It was determined that APCVD was not a process conducive to the large area, economic processing of CdTe solar cells. As such we turned to a process described as jet vapor deposition (JVD). This low-pressure process maintains the stagnation flow aspects of the original APCVD, but offers the requisite mass transport and residence times necessary for obtaining manufacturing scale deposition rates without particle formation.

Additional tasks relate to improved device measurement and characterization procedures, which can lead to a more fundamental understanding of CdTe PV device operation. Specifically, under the APCVD program, device analysis goes beyond conventional one-dimensional device characterization and analysis toward two-dimension measurements and modeling.

2.1 APCVD deposition technology

Although there are many demonstrated methods for producing high-efficiency CdTe solar cells, large-scale commercial production of thin-film CdTe PV modules has not yet been realized.[3] An important contributor to the commercial production of thin-film CdTe will be development of advanced deposition reactors. APCVD represents a generation beyond CSS. APCVD combines proven CSS reaction chemistry with state-of-the-art engineering principles to enable design of thin film deposition reactors for the manufacturing environment. The following list includes APCVD's proposed advantages:

- Low equipment cost compared to vacuum processing because equipment will need neither the structural strength nor the pumping systems of a vacuum chamber.
- Large area uniformity achieved through control of temperature and gas flow - both of which are subject to rigorous engineering design.
- Simplified process control and source replenishment because the source gas generation is physically separated from the deposition chamber.

CdTe PV device fabrication process compatibility in that APCVD is presently used commercially to deposit transparent conducting oxide (TCO) films commonly used in CdTe solar cells. In fact, the processing sequence: deposit TCO, deposit CdS, deposit CdTe, dry $CdCl_2$ heat treatment and

- metalorganic CVD of electrodes could be performed in a single continuous process.
- Low raw material costs as CdTe is used in its least expensive form - chunks.
- Simplified continuous processing because gas curtains replace load locks.

2.2 APCVD Limitations

Based on our experience we have found that APCVD has the following liabilities:

- APCVD is ***extremely*** susceptible to oxidation due to the greater gas density and residence times, both a factor of 100 - 1000X higher than CSS. As such vacuum-caliber reactor construction is required, eliminating many of the purported advantages of APCVD
- In addition, tremendous quantities of liquid nitrogen would be required to operate APCVD, representing a utility cost that is substantially greater than operating a vacuum pump.
- APCVD has inherently poor utilization; approximately 90% of the CdTe passes by the substrate. Although in principal this material could be recovered and reused, from a practical standpoint this is a major drawback.
- The mass transport conditions in APCVD are about 100X worse than CSS at 20 torr.
- Growth rate primarily controlled by the bubbler temperature
- Due to the presence of a boundary layer, dust formation is thermodynamically favored to occur Experimentally it was shown repeatedly that at bubbler temperatures ≥ 725 ºC caused dust formation in APCVD.
- As such maximum obtainable growth rates with APCVD are only ~0.1 μm/min
- The above limitations would make it very difficult to implement APCVD as a viable manufacturing approach for CdTe.

2.3 Jet Vapor Deposition Technology

The alternative approach advocated here for high rate deposition is a process called jet vapor deposition (JVD). JVD has been used for a number of other material systems including ceramics and metals. JVD employs the same geometry as APCVD, however there are two major differences. First, the operating pressure is quite low, on the order of ~1 torr. Second the jet velocity is established by choke flow conditions, with values approaching the speed of sound.

The major advantages of JVD over APCVD include:

- High materials utilization (>90%)
- 1000X greater mass transport, which will allow the CdTe vapor pressure (and thus growth rates) to be increased 1000X without dust formation
- Potential for reduced substrate temperature deposition
- Source and substrate temperature remain decoupled
- The design remains scalable to large area

- Potential to be employed for other layers such as CdS

2.4 Device analysis

Operation of thin film PV devices is normally analyzed in one dimension – distance perpendicular to the device surface. One dimensional (1D) modeling is justified in that thin film PV devices are basically comprised of a stack of thin films of various compositions and properties and through which light and electricity flow in a direction essentially perpendicular to the plane of the films. There is no question that 1D modeling successfully describes the fundamentals of thin film PV device operation. Nonetheless, quantitative analyses of PV device operation, its dependence on device fabrication procedures, and factors affecting stability in the field have not been achieved. Furthermore, we know that individual films are not homogeneous, but rather are comprised of grains. Each grain is surrounded by grain boundaries that are oriented in all directions and which have different physical, electrical and optical properties than the interior of the grain. Tasks of this program are directed toward techniques that quantify the properties of grain boundaries and the effects grain boundaries have on thin film PV device operation.

An important distinction between the commonly used one dimensional (1D) models and a two dimensional (2D) model is that the 2D model allows for electric fields and carrier transport both parallel and perpendicular to the direction from which light is incident. These perpendicular components are brought about by differences in carrier type, carrier concentration, and carrier lifetime associated with grain boundaries. In this project efforts are being directed toward identification and application of experimental techniques for characterization of grain boundaries and the investigation of the relationships between grain boundary characteristics and operating properties of working devices. An important aspect of this approach is maintenance of a close connection between measurement, modeling and analysis.

3 APCVD of CdTe

3.1 APCVD Version 1.0: Original Reactor

During the first years of the program the first generation APCVD reactor was designed, built and evaluated. A schematic of this reactor is shown below in Figure 1. As discussed below, there have been several modifications made to the design of the bubbler/gas delivery system, but the reactor and the substrate configuration have remained generally unchanged throughout. Here the results obtained with this are summarized. For further details please refer to previous reports. In all cases the substrates were LOF coated SnO_2:F glass that has been coated with a CdS window layer by chemical bath deposition.

- Film deposition was achieved, but oxidation was a major problem as evidenced by significant white deposits on the film surface.
- Auger analysis performed by Amy Swartzlander, NREL, and XPS analysis by Tim Ohno identified the white deposits in these first APCVD CdTe films as TeO_2
- Due to extensive oxidation no successful devices were fabricated
- The suspected causes for oxidation were leaks in the reactor and potentially impurities in the industrial nitrogen source

3.2 APCVD Version 2.0: Elimination of Bypass Valve

For reasons of safety and environmental control, the bubbler is operated slightly below ambient room pressure. Thus leaks in the reactor allow room air to mix with the source and curtain gasses and to affect

source gas generation and film growth. It is believed that the presence of white TeO_2 powder prior to intentional film deposition was the result of leaks upstream of the bubbler that allowed room air to be drawn through the bubbler by the lower pressure downstream in the reaction chamber. Leaks in the reactor were addressed through design of a simplified bubbler and through improved high temperature stainless steel to quartz joints.

One concession made in order to reduce leaks in the new design is that the provision for source gas bypass of the bubbler was eliminated. Provision for the source gas to bypass the bubbler had been included so that the substrate temperature and other reactor operating conditions could be established at steady state conditions prior to introducing the Cd and Te_2 source gasses. Unfortunately the bypass tubing included a two-position valve that had to operate at ~700°C and which is suspected to have been a major source of leaks. The concept of trying to find a valve/seal that operates properly at ~700°C was a major problem with APCVD that was never satisfactorily resolved.

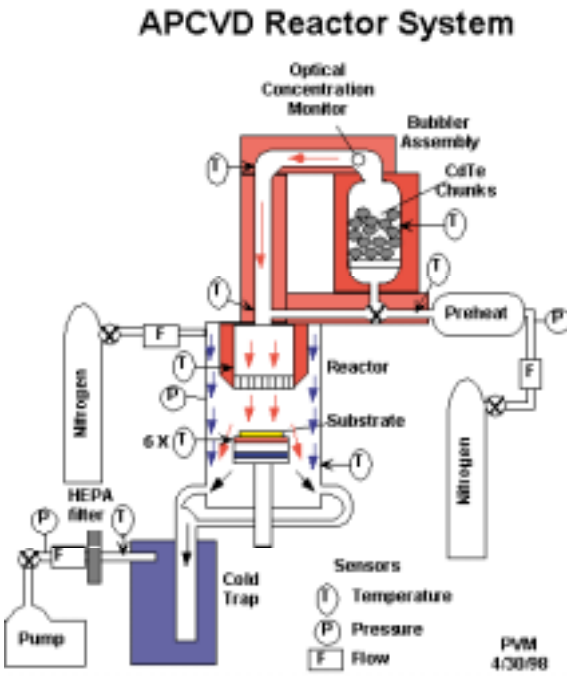


Figure 1. Schematic of original APCVD reactor.

3.2.1 First Devices

Once satisfactory dry run performance had been achieved, additional reactor evaluation runs began using CdTe. First films deposited in the simplified reactor were deposited onto LOF SnO_2:F substrates using procedures intended more to investigate reactor performance than to deposit good films. Nevertheless and in spite of several deficiencies in the reactor – including a broken showerhead, the first run produced an adherent black film. XPS depth profiling of this film indicates an oxygen content ~18 at% - possibly in the form of CdO, suggesting that there still are air leaks in the reactor.

Still operating in the "shake down" mode, additional films were deposited onto thin (~500 Å) CBD CdS-coated LOF glass. Substrate temperature was estimated at 580˚C. Deposition time was about 10 minutes and film thickness varied over the range 1-4 µm. In spite of the preliminary nature of CdTe film deposition, Ahklesh Gupta, CSM, agreed to produce devices on the APCVD CdTe film using CSM standard processing – including a 20 min $CdCl_2$ heat treatment at 410˚C and application of evaporated Au back contacts. Best device efficiency achieved was 3.8% (373 mV Voc, 20.9 mA/cm^2 J_{sc} and 0.49 FF). Low V_{oc} is attributed to the thin CdS layer that appeared to be completely consumed during CdTe deposition and processing.

3.2.2 Next Devices: Positive Pressure

Issues with oxidation were not fully resolved. To validate that oxidation was due to leaks to the ambient a few runs were performed at slightly positive pressure. Although the reactor was at a slight positive pressure, there was the secondary containment system that was ventilated through a HEPA filter. In addition, swab samples were taken and no detectable Cd was detected outside of the reactor. These experiments produced much higher quality films. Low oxygen content was confirmed by XPS. In

addition, a thicker CdS later (~ Å) was deposited on these films. Device efficiency improved dramatically with these changes. Typical cell efficiencies were in the range of 8 – 10%, with the best cell achieving an NREL-confirmed value of 10.6%.

3.2.3 Best Devices: Positive Pressure + HRT Buffer layer

The final devices made using the 2nd Generation reactor (no source gas bypass) included a high resistivity transparent (HRT) buffer layers. The HRT layer consisted of tin oxide that was deposited by plasma-enhanced chemical vapor deposition by the Wolden laboratory at CSM.[4] The HRT layer was deposited on commercial TCO-coated films prior to CdS chemical bath deposition. The following set of experiments were run. A normal 3 x 5" substrate was divided into 6 pieces. Three of these were coated with HRT layers of various conductivity. After this all six pieces were treated identically: including CdS deposition, CdTe APCVD, and subsequent $CdCl_2$ treatment and device processing. Figure 2 shows the arrangement of these substrates during CdTe deposition. Devices were made out of the 4 shaded area shown in Figure 2. Nominal cell properties were CdS thickness: 1600 Å, CdTe thickness: 5 µm, Cu/Au back contact, and indium solder front contact.

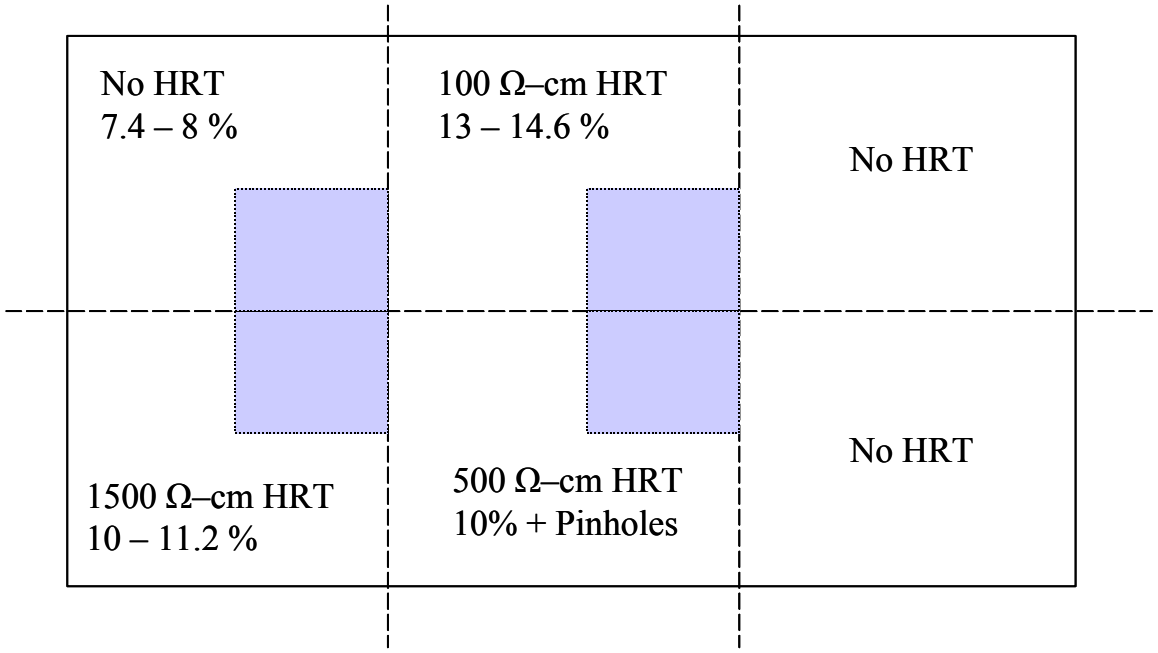


Figure 2. Arrangement of HRT-coated and uncoated samples during CdTe deposition.

The resulting device efficiency's are summarized in Figure 2. The uncoated sample delivered values around 8%, which was quite typical for this generation of the reactor. In each case the device efficiency with the tin oxide buffer layer was much better. The highest efficiency being 14.6%. All of the device measurements were performed at CSM. NREL measured this same device at 12.3 %, but due to the small size of the devices, 0.03 cm^2, they declined to confirm these measurements. Figure 3 compares the IV curves of the best device with one that had no HRT layer.

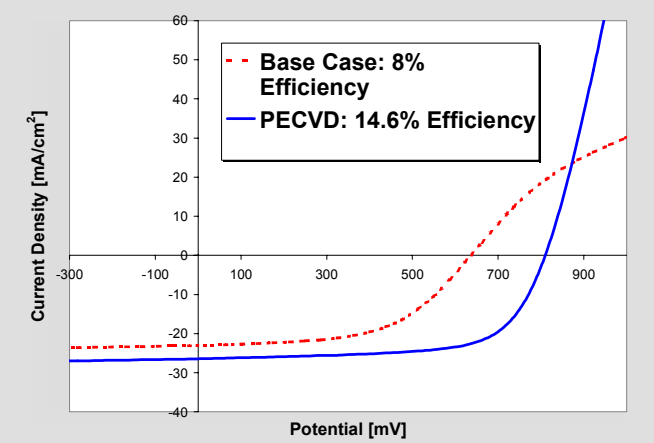


Figure 3: I-V curves of APCVD with and without an HRT buffer layer.

3.3 APCVD Version 3.0: Split Source Reactor

As noted in Figure 2, the formation of pinholes was major issue with APCVD Version 2.0. Small fines generated in the bubbler were carried over onto the film. The issues limited operation to relatively low flowrates, with maximum nozzle velocities ~ 25 cm/s. To remove these constraints a third generation, or so-called split source reactor was designed. Figure 4 shows a schematic diagram of this reactor. The idea was this: a small flowrate of high density Cd/Te_2 vapor would exit the bubbler and mix with a large flowrate of heated nitrogen. As such we could maintain high vapor pressure and also maximize transport. An exhaustive amount of effort went into the design, fabrication and installation of this reactor. Indeed, the majority of the 3rd year of this project was dedicated to this endeavor. Numerous films were also deposited and solar cells were made. However, they all films deposited using this configuration was substantially inferior to those produced in APCVD Version 2.0. At this point the concept of APCVD was abandoned in favor of JVD for the reasons described below.

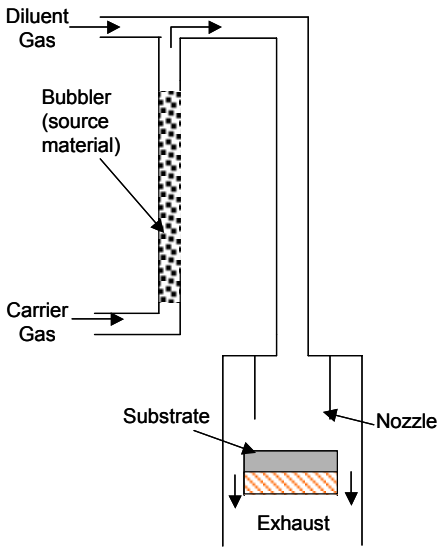


Figure 4: Schematic of split source reactor.

4 The Inherent Limitations of APCVD

4.1 Thermodynamic Limitations

In laminar flow deposition systems a stagnant boundary layer is formed between the bulk fluid and the substrate. Across this boundary layer diffusion and conduction are the means of transport for mass and heat, respectively. The solution to Fick's and Fourier's equation result in linear concentration/temperature profiles across the boundary layer. Although the concentration decreases linearly, the saturation point decreases exponentially. This situation is illustrated in Figure 5. The solid line indicates the temperature profile across a unit boundary layer. The dashed line corresponds to the saturation temperature that would be in equilibrium with the vapor pressure present. The difference between these two lines, ΔT, represents the degree of supersaturation. The gas-phase is supersaturated across the boundary layer. The propensity for gas-phase nucleation increases exponentially with ΔT. In the CdTe system the substrate temperature is essentially fixed at 600 ºC, while the bubbler temperature may be altered to affect the growth rate. Although increasing the bubbler temperature would increase growth rate, it also dramatically increases the rate at which particles form.

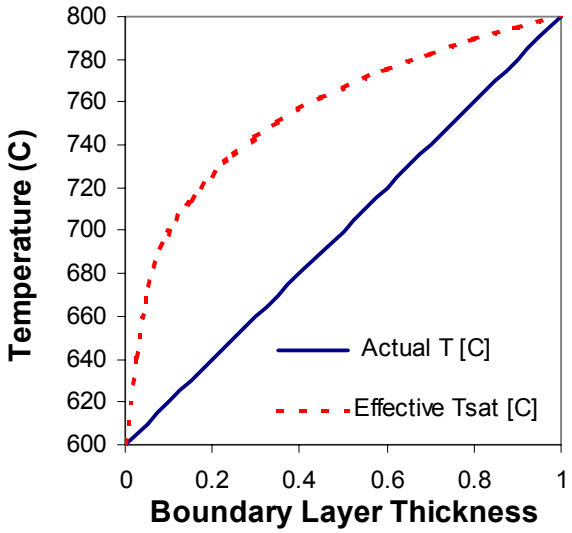


Figure 5: The actual and effective saturation temperature across a unit thick boundary layer. For $T_{bubbler}$ = 800 ºC, T_{sub} = 600 ºC.

Figure 6 plots both the average (dashed line) and maximum (solid line) extent of supersaturation as a function of bubbler temperature. The average value was obtained by integrating the difference between curves such as those shown in Figure 5. Even at a moderate bubbler such as 700 ºC, the average degree of supersaturation is ΔT = 16 º, and the maximum is ΔT = 28 ºC. A good analogy would be trying to cool steam to 84 ºC and NOT have water droplets form. As the ΔT increases the task becomes exponentially more difficult.

From a practical point of view it was demonstrated experimentally that the bubbler temperature could not exceed 725 ºC without extensive dust formation. Thus CdTe deposition, and for that matter any physical vapor deposition technique, is inherently thermodynamically unstable. To be performed successfully, mass transport rates must be faster than the kinetics of particle nucleation.

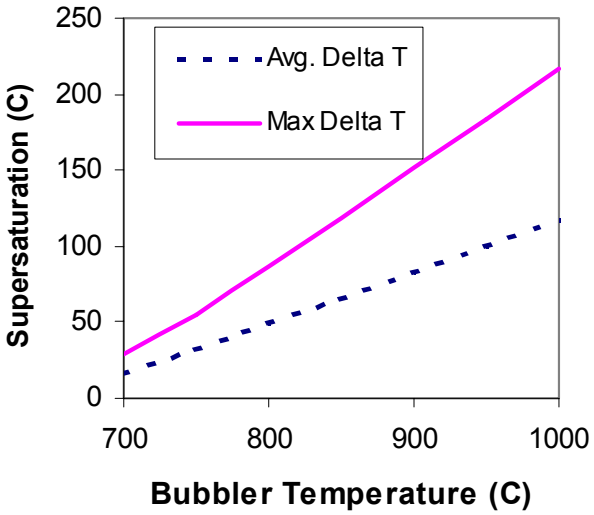


Figure 6: The average and maximum degree of supersaturation as a function of bubbler temperature.

4.2 Mass Transport Limitations

The premise of APCVD is based on mass transport by forced convection. For the stagnation flow geometry mass transport is very well understood.[5] In dimensionless terms the mass transfer coefficient may be estimated using correlations for the Sherwood number:

$$(1) \qquad Sh_L = h_m L/D_{AB} = 0.78 Re_L^{1/2} Sc^{1/3}$$

The resulting mass transfer coefficient, h_m, is on the order of 5 cm/s. In contrast CSS process rely on diffusion for mass transport. In these cases the mass transfer coefficient is equal to the diffusivity divided by the plate spacing. For typical CSS conditions (P = 20 torr, gap = 2 mm) the corresponding transport coefficient is ~150 cm/s, 30 times greater than APCVD.

Figure 7 at right shows contour plots of CdTe concentration that were generated by a computational fluid dynamic (CFD) simulation. As shown in Figure 7, most of the Cd and Te_2 vapors flow past the substrate and are lost. Figure 8 compares % utilization and mass transfer coefficient as a function of flowrate for ideal stagnation flow at nominal APCVD process conditions. At no conditions does the mass transfer coefficient exceed 10 cm/s.

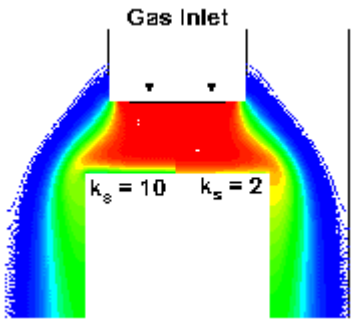


Figure 7: Concentration contour plot for stagnation flow. (2 different surface reaction rates).

Figure 8 shows that the utilization rate drops precipitously as the inlet velocity is increased. Based on these considerations of transport, and the thermodynamic arguments presented above, it was concluded that APCVD could never be a viable CdTe manufacturing technology.

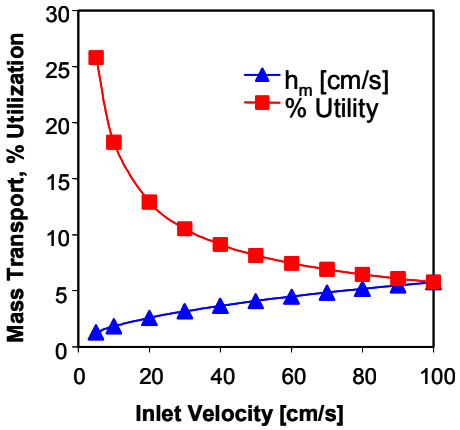


Figure 8: % Utilization and mass as planar transfer coefficient as a function of inlet velocity.

5 Microscopic Characterization of Polycrystalline APCVD CdTe [6]

5.1 Overview

APCVD material is examined with several techniques and compared with close-space sublimation (CSS). Transmission and scanning electron microscopy studies show a similar morphology to CSS CdTe. However high resolution TEM scans show the formation of a disordered layer between the CdTe and CdS, and the removal of defects within some grain structures upon annealing. Cathodoluminescence shows electronic defect states localized to grain boundaries. A large concentration of trap states was also observed with deep-level transient spectroscopy that may correspond to hole traps found in lower amounts in other materials. The presence of traps was also indicated in impedance spectroscopy measurements. The latter studies indicate a high grain boundary resistance contributes to transport.

5.2 Experimental Details

All APCVD samples prepared for comparisons in this study had common processing steps through the CdTe deposition. Substrates used to make these cells were commercially available (LOF) 3×5-inch sodalime glass slides coated with SnO_2:F. 2000 Å of CdS was sputter-deposited on these substrates, then pre-treated with $CdCl_2$ at 450ºC for 50 min. in nitrogen. CdTe was deposited by APCVD at ~0.2 µm/min at a substrate temperature of 580ºC. The 3-5 µm thick CdTe was then treated with $CdCl_2$ for 35 min at 410ºC, followed by a 10 second etch in a 0.1% Br_2/methanol solution. Back contacts were formed by diffusing a thin layer (30 Å) of Cu into the CdTe, etching the surface to remove excess Cu and then evaporating Au. APCVD samples used in these studies were either as deposited, with $CdCl_2$ treatment, or with the Au/Cu contacts.

The structure of the films was investigated using cross-sectional transmission electron microscopy (XTEM) on a Philips CM200 Scanning-Transmission Electron Microscope operating at 200 kV. TEM samples of actual cells on glass substrates were prepared by tripod polishing followed by brief (~ 10 min) ion milling to remove polish damage. Cathodoluminescence (CL) experiments were made in a JEOL 5800 SEM equipped with an Oxford MonoCL2 system. A LN_2 cold stage was used to cool down the films to 77K. A Ge NorthCoast IR detector was used for the low energy radiation and a GaAs photomultiplier for the near band-edge luminescence. A 10 keV beam energy was used to improve the spatial resolution of the CL measurements. Cells for CL and SEM were cleaved and initially etched with

Br_2/methanol, to polish chemically the surface. The cross sections were then etched with nitric+phosphoric acids to preferentially etch the grain boundaries.

Deep Level Transient Spectroscopy (DLTS) measurements were performed at NREL using the DLTS apparatus is made by SULA Technologies. Reverse bias for the DLTS experimental data was 0.5V. The pulse width and height were 3 μs and 0.5V.

Impedance spectroscopy (IS) measurements were performed with two Hewlett-Packard LCR meters spanning the frequency range 20 Hz to 30 MHz. Hall measurements were performed on a BioRad HL 5500PC equipped with a fiber optic sheet source for illumination during measurements. Since the CdTe films cannot be shunted by either back or front contact during electrical measurements only uncontacted cells that were 'lifted-off' from the underlying TCO and CdS window layer were analyzed. Lift-off samples with smooth areas ~1 cm^2 were prepared by shearing epoxy pads attached to the glass plates, leaving the more robust TCO and much of the CdS behind. Residual CdS was removed by HCl etching before evaporating gold on the CdTe to form ohmic contacts for Hall and IS measurements.

5.3 Results and Discussion

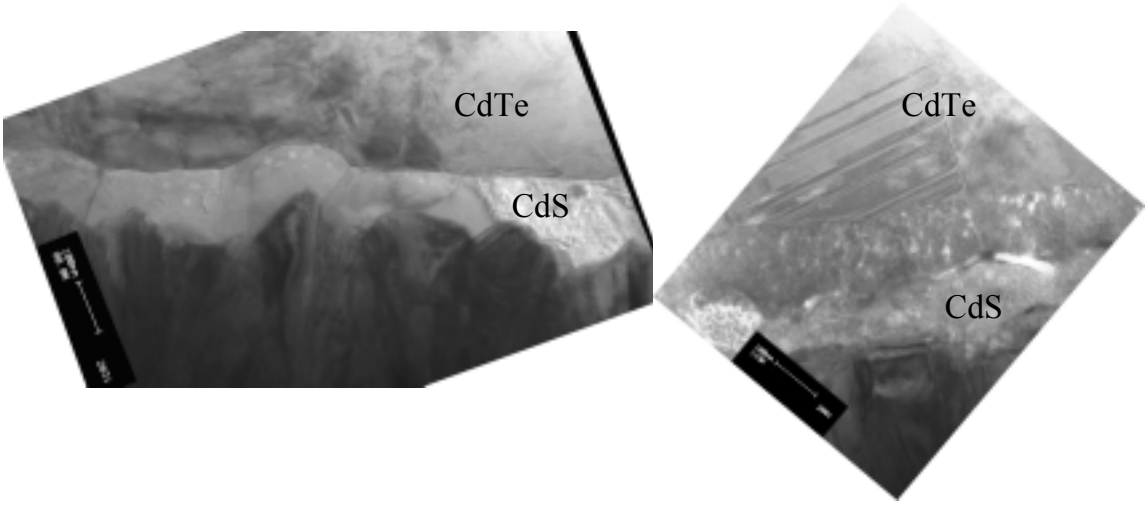


Figure 9: XTEM image of as grown APCVD CdTe (left) and completed cell with APCVD CdTe (right). Growth of an interlayer during processing is evident.

5.3.1 TEM Studies

Figure 9 shows a detailed image of the SnO_2/CdS/CdTe interface for the as-prepared APCVD CdTe. XTEM images show grains with linear structures extending the width of the individual grain as well as smaller linear and planar defects within grains. Lattice planes could be observed in most grains observed with high magnification. Such structures have been reported previously[7] for CSS CdTe samples prepared on CdS single crystals and CdS thin films on Si(100). The interface between the CdS and CdTe appears abrupt, in spite of the 580ºC growth temperature. No significant increase in defect density within the CdTe grains close to this interface was observed.

Comparison with material after cell completion shows pronounced changes in microstructure after $CdCl_2$ treatment and contacting. As with CSS CdTe the overall grain size is not dramatically altered by completion.[7] Figure 9 shows the formation of a distinct layer between the CdTe grains and the CdS layer. Higher resolution images of this ~70 nm thick layer (not shown) show a nearly unresolvable, fine grain structure. The formation of an interdiffused ternary layer is a reasonable speculation on this layer. No

notable change was observed along CdTe grain boundaries. However, in several grains small internal defects due to stacking faults were decreased relative to the as-prepared samples.

5.3.2 Cathodoluminescence

CL examinations of APCVD material from a completed cell show distinctive spectral features corresponding to near band edge emission and deeper levels. Figure 10 shows spectra obtained from cross sectional examination of APCVD CdTe and CSS CdTe at room temperature and 77 K. The CSS films were $CdCl_2$-treated but not contacted. CSS films show a single sharp feature at 1.43 eV at 300K that shifts to 1.48 eV at 77K. This is substantially lower than the bandgap of CdTe at 77K, which is ~1.59 eV. The Durham group has reported CL measurements on CSS CdTe with excitonic emission at 1.576 eV.[8] High energy emission from APCVD CdTe from a completed cell shows a broad feature peaked at 1.4 eV at 300 K and two peaks at 1.52 and 1.45 eV at 77K. The broad spectrum from APCVD CdTe is similar to MOCVD CdTe after $CdCl_2$ treatment.[9] In addition a feature at 0.91 eV is observed with APCVD material.

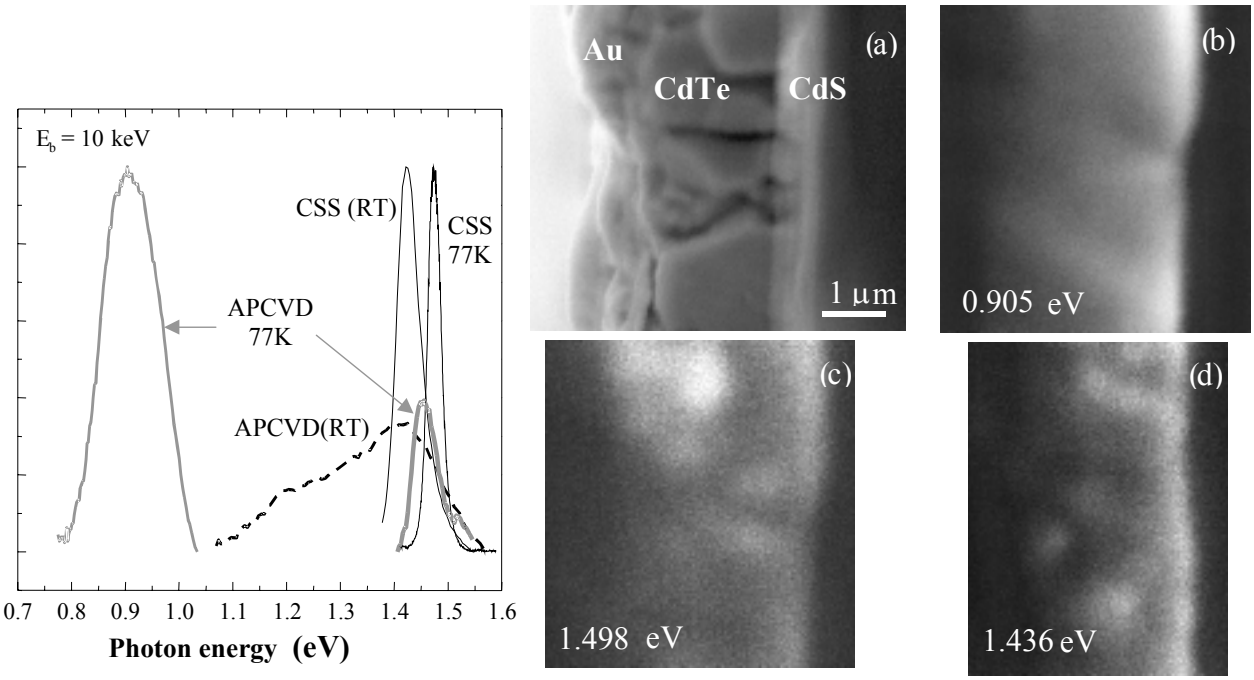


Figure 10 Cathodoluminescence from APCVD and CSS CdTe. Cross Sectional CL map of APCVD CdTe/CdS cell. (a) SEM image, (b) 0.905 eV, (c) 1.498 eV, and (d) 1.436 eV. CL images are shifted slightly relative to the SEM image, but two grain boundaries are clear in (d).

Preliminary identification of these features can be found by examination of photoluminescence (PL) results. It should be noted that CL corresponds to a very high excitation level, and relative intensities of features are highly dependent on this.[10] In PL of CdTe single crystals a broad feature peaked at ~1.47 eV measured at 10K is found that has been associated with a several donor- deep acceptor transitions.[11] Galloway et al. attribute a similar feature they observe to a D-A transition.[8] A possible source for the shift of the feature in the APCVD material may be the presence of Cu due to contacting, since a similar shift is observed in PL.[11] However other changes in deep levels may also cause this change.

The deep level band peaked at 0.91 eV in APCVD material is currently unidentified. Examination of known deep levels for CdTe suggested it may be related to an electron trap at $\varepsilon_c - 0.64$ eV that has been found in CdTe:Cl or to a hole trap at $\varepsilon_v + 0.76$ eV .[12]

CL maps provide information on the distribution of the defects causing emission. Figure 10 shows that the trap associated with the 0.9 eV emission is almost uniformly distributed throughout the film. However the higher energy transition (measured at 1.498 eV) is more confined to grains, with the grain boundaries as nonradiative recombination regions, similar to results in Ref. 8. The D-A luminescence at ~1.4 eV is more diffuse and is associated with near grain boundary areas. The D-A emission is also greater near the CdS interface and reduced near the back contact. CL maps of the 1.48 eV emission from CSS material (not shown) show suppressed emission from the grain boundaries, the opposite of the D-A emission in APCVD, suggesting different origins.

5.3.3 Deep Level Transient Spectroscopy

Insight into the defects available can be found in DLTS on APCVD completed cells. In Figure 11 DLTS measurements show two features corresponding to hole traps in APCVD CdTe. Using standard analysis methods the trap energy of the lower temperature trap was determined to be 0.39 eV ($N_T = 3.9\times10^{12}$ cm^{-3}, $\sigma=1.6\times10^{-14}$ cm^{-2}). The larger trap had an energy of 0.87 eV ($N_T = 4.0\times10^{13}$ cm^{-3}, $\sigma=2.6\times10^{-12}$ cm^{-2}). The former likely corresponds to the trap H1 identified in CSS CdTe, which was attributed to substitutional Cu impurities [9].[13] Of note is the absence of the electron trap E1 in APCVD material, which was believed to be a lifetime-limiting defect. Another comment is that the additional hole trap has an energy close to the additional feature observed in CL, but not identified in the literature [8].[12] Features resembling this peak have been detected in both CSS and electrodeposited material.[6] It is tempting to assign the hole trap to a state located ~0.9 eV above the valence band, which could explain both signatures. However correlation of DLTS data and luminescence spectra must be done carefully. In the p-CdTe the hole trap would be occupied with holes. In order for luminescence to occur the trap must first be emptied, either by excitation or by electron capture, then it must emit light upon hole capture. Competition with other processes will determine the intensity of this process. Further experiments are needed to determine the origin of this state, and if it is correlated with CL.

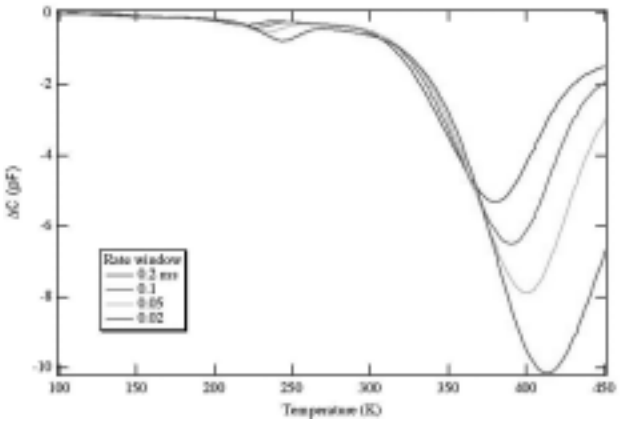


Figure 11. DLTS spectra from APCVD CdTe.

5.3.4 Impedance spectroscopy

Dark Hall measurements for the lifted-off APCVD CdTe showed resistivity = 4.8 $\times 10^6$ Ω-cm, mobility = 13 cm^2/V-s, and carrier concentration N = 1.0×10^{11} cm^{-3}. The mobility and carrier concentration values suggest that grain boundary impedance contribute significantly. This is further supported by IS measurements on the $CdCl_2$ treated lifted-off APCVD films. Figure 12 shows the real part of the measured impedance or 'resistance' using the standard RC parallel and RC series models, as measured with weak white light illumination. The resistance is high at low frequencies compared to higher frequencies. Similar decreases in capacitance (not shown) were observed as well. Upon illumination the low frequency resistance decreased to ~40× the value measured with 1/5 Sun, while the high frequency resistance was unchanged. The results are similar to vapor transport and thermally-evaporated CdTe.[14]

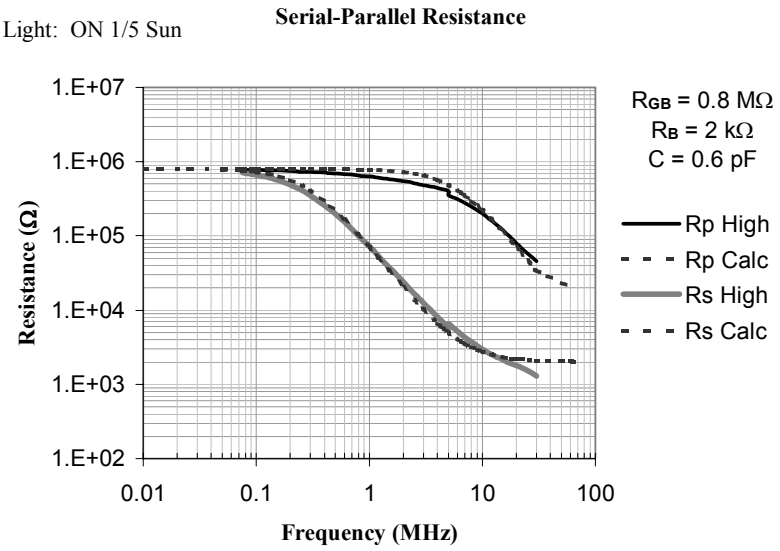


Figure 12 Modeling of Resistance of APCVD lifted-off films. Qualitative agreement with a two resistor-capacitor model is good, and suggests large contributions of grain boundary resistance.

The IS results are modeled using a simple grain resistance R_B and a parallel R_{GB} and C_{GB}.[14] Comparison of the calculated results with the measured quantities shows qualitative agreement. Our standard R_B in series with $R_{GB} \parallel C_{GB}$ model yields R_{GB} = 39 MΩ, C_{GB} = 0.4 pF, R_B ~ 1 kΩ. When illuminated R_{GB} = 800 kΩ, C_{GB} = 0.6 pF, R_B ~ 2 kΩ. There are several possible explanations of the deviation from model results, but the most likely is the presence of trap states within the grains. This introduces an apparent capacitive effect within the bulk material due to the emission rate from these trap states. The CL and DLTS results that show trap states distributed throughout the CdTe support this interpretation.

5.4 Characterization Conclusions

APCVD CdTe differs from CSS materials in ways that are measurable by microsopic techniques or electrical characterization. $CdCl_2$ annealing results in the formation of an interlayer at the CdTe/CdS interface not reported in CSS material and removal of some structural defects. The principal finding in CL and DLTS was the presence of defect electronic states not observed in CSS. The origin of these states may be related to S interdiffusion or possibly impurities such as Cu due to contact formation. The first lifted-off samples also prove fundamental measurements of electrical properties similar to observed in other CdTe.

6 Modeling of CdS/CdTe thin film solar cells

This section is repeated from the year II annual review, but is included herein for completeness of the Final Report.

6.1 Device characterization and analysis

Device characterization includes measurements of film and device properties and establishment of correlations among them. Basic film properties include thickness, composition, grain size, crystallographic orientation, film stress and dark and light AC conductivity. On films deposited on CdS the composition and location of various Cd(Te,S) alloys can be determined using combinations of XRD and TEM. Device characterization includes analysis of dark and light I-V curves as well as spectral response. Measurements and analysis will be made primarily at ITN, CSM, and NREL.

A significant objective of this task is to develop a more sophisticated 2D model of device operation. Specifically, as suggested in Figure 13, the improved model is expected to include the effects of changes in composition, conductivity and carrier type associated with grain boundaries. Preliminary descriptions of this 2D model including suggested analytical validation techniques were presented at the CdTe Team meetings in May and October 1999. Validation of this model will require measurements to probe the two dimensional nature of the device. Appropriate analytical techniques to be applied include:

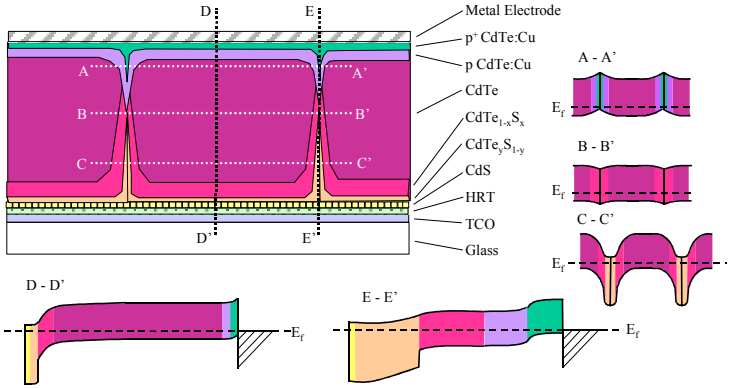


Figure 13. Schematic representation of 2-D compositional and energy level variations of an idealized polycrystalline CdTe/CdS solar cell.

1) Electrical analysis including light and dark in-plane AC impedance measurements and GB characterization of bi-crystals. These are measurements of films on relatively large scale, ~ mm, from which energy band structure around grain and grain boundaries may be inferred.

2) Microanalysis including NSOM PC, ebic, and TEM. NSOM PC measures local energy bandgap within polycrystalline films; ebic measures local electron-hole current generation; and TEM combined with EDS measures local composition, e.g., S content in CdTe.

3) Computer modeling including cross sectional 1D and 2D models enables application of measured physical parameters to models and comparison with performance of real devices.

Each approach probes device operation from a different, complementary perspective, which, when combined, are expected to define a unified representation of device operation.

6.2 AMPS Modeling of CdTe/CdS thin film PV devices[15]

6.2.1 Purposes of modeling

There are several general purposes of modeling including:

a) As a source of ideas for interpretation of measurements of materials properties and cell parameters.

b) Visualizing factors affecting carrier transport properties such as fields, carrier densities, currents, and recombination profiles, and the effects of illumination on transport in CdS/CdTe solar cells.
c) Evaluating effects of materials parameters (e.g., acceptor density) and design parameters (e.g., layer thickness) on cell operation.

An article on modeling for the CdS/CdTe cell by Burgelman et al.[16] is recommended.

The following sections include discussions of:
a) Inclusion of a CdS_xTe_{1-x} alloy layer at the CdS/CdTe interface and its effects on cell properties,
b) Preliminary model for addition of a bilayer SnO_x window to the CdS/CdTe cell,
c) Preliminary grain boundary model, and
d) Discussion of next modeling steps including two-dimensional modeling.

Associated topics in the CSU Annual Report include 1) upgrades of the AM1.5G spectrum and the absorption coefficients of CdS and CdTe used in AMPS and a comparison of AMPS and experimental spectral response curves, 2) a discussion of input parameters for AMPS modeling (especially recombination parameters), 3) effects of variation of acceptor density and minority carrier lifetime in the CdTe layer on photovoltaic performance, and 4) effects of variation of CdTe layer thickness and back contact barrier height on the on the photovoltaic variables.

A newer version AMPS-1D[17] was obtained which has the capacity to use more spectral response (SR) data points.

6.2.1.1 Choice of Parameter Values

Previous modeling used three sub-layers of CdTe with different acceptor densities (N_a) to replicate N_a profiles obtained from C-V measurements in experimental cells. Since the variations of each of the sub-layers yielded differences of only secondary magnitude, it was decided to simplify the entire CdTe layer to one N_a for this report. The measured range of N_a in real cells is 10^{13} to 10^{15} cm^{-3}, from C-V measurements.[18]

The thickness of the CdTe was chosen as 2 μm for these cases (cf., 2 to 8 μm for most experimental cells), enough to absorb virtually all sub-bandgap solar photons.

A back-contact barrier height $Ø_{bc}$ = 0.30 eV was chosen on the basis of previous modeling[19] and measurements of contact resistance vs. temperature. Above this value, the back contact barrier begins to substantially affect the ff and the J-V curves above V_{oc}.

A CdS layer thickness of 0.1 μm, a donor density $N_d = 10^{17}$ cm^{-3}, and a slightly accumulated ohmic front contact ($Ø_{fc}$ = 0.1 eV; for $N_d = 10^{17}$ cm^{-3}, $E_{CB} - E_F = 0.135$ eV), and was chosen to de-emphasize the effects of the CdS for these cases.

A summary of AMPS input parameters is given in Table 1.

Table 1: Parameter values.

	Front Contact	**SnO_x**	**n-CdS**	**p-CdS_xTe_{1-x}**	**p-CdTe**	**Back Contact**
Reflection	0.07	—	—	—	—	0.30
Barrier height (eV)	0.1	—	—	—	—	0.3, var.
Recombination. velocity, electrons (cm/sec)	10^7	—	0	0	0	10^7
Recombination. velocity, holes (cm/sec)	10^7	—	0	0	0	10^7
Thickness (μm)	—	1	0.1	0.1	2	—
Dielectric Coefficient.	—	9.0	9.0	9.4	9.4	—
Electron affinity	—	4.5	4.50	4.28	4.28	—
Band gap (eV)	—	3.1	2.42	1.41	1.50	—
Density of states, CB (cm^{-3})	—	$1.8x10^{19}$	$1.8x10^{19}$	$7.5x10^{17}$	$7.5x10^{17}$	—
Density of states, VB (cm^{-3})	—	$2.4x10^{18}$	$2.4x10^{18}$	$1.8x10^{18}$	$1.8x10^{18}$	—
Carrier density (cm^{-3})	—	10^{17}	10^{17}	10^{14}, var.	10^{14}, var.	—
Electron mobility (cm^2/V-sec)	—	350	350	500	500	—
Hole mobility (cm^2/V-sec)	—	50	50	60	60	—
Lifetime (sec)	—	$2x10^{-10}$	$2x10^{-10}$	10^{-9}	10^{-9}	—
Recombination center density N_r (cm^{-3})	—	10^{14}	10^{14}	var.	var.	—
Recombination center energy E_r (eV), wrt. VB	—	1.57	1.21	0.75	0.75	—
Recombination cross section σ_n (cm^2)	—	10^{-15}	10^{-15}	10^{-12}	10^{-12}	—
Recombination cross section σ_p (cm^2)	—	10^{-12}	10^{-12}	10^{-15}	10^{-15}	—

6.2.1.2 Target Values

Beyond being consistent with measurable materials properties (α, front and back surface optical reflection, N_d, N_a, etc.) and physical configuration (layer thicknesses, etc.), the most important requirement for a good model is to be able to duplicate the basic photovoltaic variables. For simulations of a general nature, the photovoltaic variables of the record CdS/CdTe cell of Ferekides et al.[20] were adopted. For later simulations of specific cells, their particular properties will be targets.

The simulated value of J_{sc} must be in a range consistent with the target photovoltaic variables, but it can be "fine tuned" by varying the CdS thickness (x_{CdS}, within limits of course), recombination in the CdS, and the reflection coefficients at the front and back of the cell - which are known approximately. As the specific value of Jsc is not strongly interconnected with the values of V_{oc} and ff, it was decided to focus on V_{oc} and ff and target J_{sc} separately.

On the other hand, V_{oc} and ff are strongly coupled, and for the model presented here (both in Lifetime or DOS mode), bringing V_{oc} down to target values (e.g., by decreasing τ) always resulted in a ff that was too small. Although not exhaustive, other simulations using various N_a profiles and interfacial recombination layers did not promise simultaneous targeting of V_{oc} and ff; ff was always too small if V_{oc} was targeted.

6.2.2 Addition of a CdS_xTe_{1-x} alloy layer

In this section a model was set up which includes a CdS_xTe_{1-x} alloy layer (CdSTe) at the CdS/CdTe interface, resulting from interdiffusion of S and Te and with x near the solubility limit. Such a layer is thought to be ~ 0.1 μm thick[21] with x ~ 0.04[22], giving E_g = 1.41 eV. A band offset must occur at the CdSTe/CdTe interface, either in the conduction band (ΔE_{cb}), the valence band (ΔE_{vb}), or both. Because the band offsets between CdS and CdTe occur primarily in the valence band[23], the electron affinities of CdSTe and CdTe were set to be equal, putting the discontinuity entirely in the valence band, as shown in the band diagram of Fig. 14. The lifetime $\tau = 10^{-9}$ s and $N_a = 10^{14}$ cm^{-3} were kept the same as those for the CdTe layers and the other parameters are as listed in Table 1.

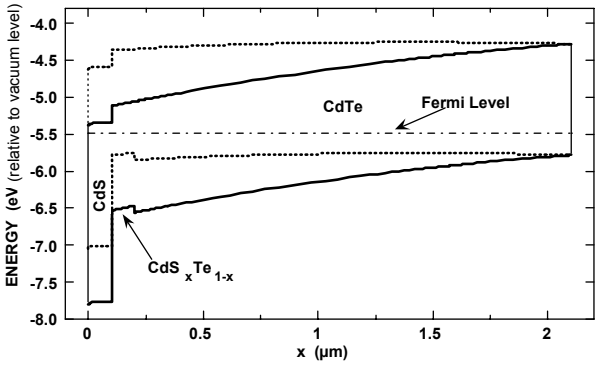


Fig. 14. Band diagram of CdSTe layer device at thermal equilibrium and at V = V_{max}.

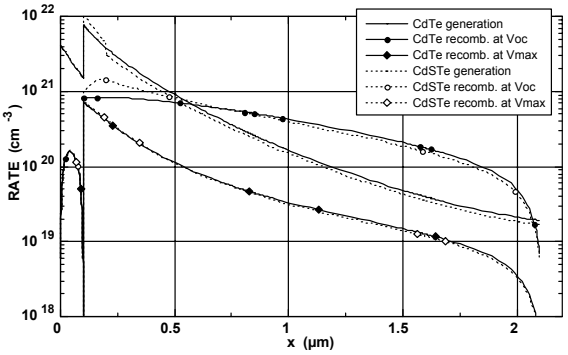


Fig. 15. Generation and recombination rates for devices with and without a CdSTe layer at V_{max} and

The generation and total recombination for the devices with and without the CdSTe layer are shown in Fig. 15. Comparison of the generation rates for the two devices shows that the distribution of generation vs. x is moved closer to the junction for the CdSTe layer but the total generation remains similar (integration of the CdSTe/CdTe and CdTe portions of the generation curves gives 22.93 mA/cm^2 with the CdSTe and 22.37 mA/cm^2 without).

Rather remarkably, this simple modification allows a consistent set of PV variables to be targeted. *Table 2* shows these for three cases: (a) no CdSTe layer, (b) CdSTe layer as described above ("ΔE_V"), and (c)

CdSTe layer with the discontinuity entirely in the conduction band ("ΔE_c"). The presence of the CdSTe layer ("ΔE_v") lowers V_{oc}, but raises the ff, leaving the efficiency almost unchanged. By adjusting the lifetime, the V_{oc} can now be adjusted to the target value (0.850 V), leaving the ff slightly above the target value (0.750), with room for slight decreases by external series resistance. The increase in ff with the CdSTe layer appears to be partially due to the movement of the generation distribution toward the junction interface, but mostly due to the decrease in V_{oc} because of the increased supply of holes for recombination near the junction interface for $V = V_{oc}$. As shown in Fig. 15, the recombination near the CdSTe layer increases dramatically between V_{max} and V_{oc}.

Table 2: Photovoltaic variables for CdS_xTe_{1-x} alloy layer device.

CASE	J_{sc} (mA/cm^2)	V_{oc} (V)	ff	Eff (%)
no CdSTe	24.0	0.905	0.757	16.4
ΔE_V	24.4	0.861	0.777	16.3
ΔE_C	22.8	0.804	0.664	12.2

6.2.3 SnO_x Window layer

In this section we set up a preliminary model which includes a SnO_x window layer and describe results for situation in which the SnO_x is subdivided into layers with high and low resistivity as shown in Fig. 16. Beside the bulk photoelectronic properties of the SnO_x layers, this adds the complexity of several interfaces, each with their own interface recombination velocity as shown in Fig. 17: S_{fc}, $S_{i,hi/lo}$, $S_{i,SnOx/CdS}$. For lack of better data, the SnO_x parameters are taken as extensions of the CdS parameters (also see Table 1): the absorption coefficient of CdS is just shifted to $E_g = 3.1$ eV and the lifetimes are the same. Case parameters are summarized in *Table 3*.

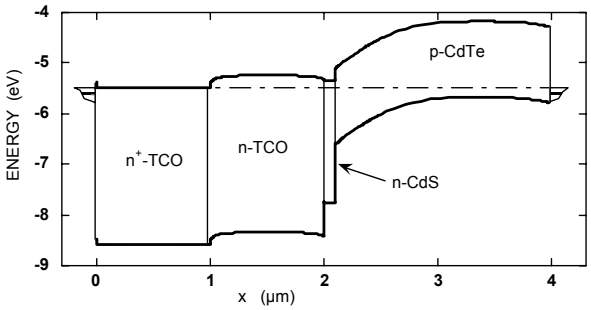


Fig. 16. Band diagram of bilayer SnO_x device. Dark, V = 0.

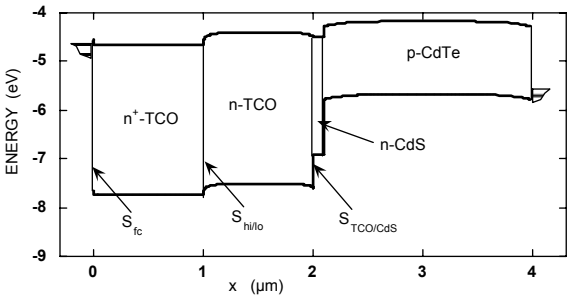


Fig. 17. Band diagram of bilayer SnO_x device. At maximum power point $V = V_{max}$.

Table 3: Variable parameters for SnO_x -layer cases.

	CASE	35.0	35.1	35.2	35.3
Contact	$Ø_{fc}$	0.1	0.1	0.1	0.1
Contact/SnO_x 1	$S_{fcn} = S_{fcp}$ (cm/s)	10^7	10^7	10^7	10^7
SnO_x 1	χ (eV)	4.50	**4.50**	**4.70**	**4.30**
"	x (μm)	1	1	1	1
"	N_d (cm^{-3})	10^{19}	10^{19}	10^{19}	10^{19}
SnO_x 1/SnO_x 2	$S_{hi/lo}$ (cm/s)	0	0	0	0
SnO_x 2	x (μm)	1	1	1	1
"	N_d(cm^{-3})	10^{15}	10^{15}	10^{15}	10^{15}
SnO_x 2/CdS	$S_{SnOx/CdS}$ (cm/s)	0	0	0	0
CdS	χ (eV)	4.50	4.50	4.50	4.50
"	x (μm)	0.1	0.1	0.1	0.1
"	N_d(cm^{-3})	**10^{17}**	**10^{15}**	10^{15}	10^{15}

The SnO_x with $N_d = 10^{20}$ cm^{-3} acts essentially as an extension of the metal contact to either the more insulating SnO_x layer or the CdS and varying its thickness has little effect on the PV variables unless its S_{fc} is considered; no useful photocurrent is generated in it.

The photovoltaic variables are compared in *Table 4* with an otherwise identical cell without the SnO_x layers (#32.5). The high carrier density in the CdS for this case (#35.0, $N_d = 10^{17}$ cm^{-3}) effectively shields the CdTe from influence of the SnO_x. The major difference between the two cells is the recombination velocity at the CdS front surface which was zero for the SnO_x case and $S_n = S_p = 10^7$ cm/sec for the no-SnO_x case. This results in about 1.5 mA/cm^2 increase in J_{sc}, generated in the CdS and the resultant small increases in V_{oc} and ff.

Table 4: SnO_x case results.

Situation	**Case #**	**$N_{d,CdS}$ (cm^{-3})**	**J_{sc} (mA/cm^2)**	**V_{oc} (V)**	**ff**	**Eff (%)**
bilayer SnO_x	35.0	10^{17}	24.58	0.956	0.784	18.4
no SnO_x	32.5	10^{17}	23.13	0.955	0.782	17.3
bilayer SnO_x	35.1	10^{15}	24.40	0.962	0.728	17.1
χ_{CdS} = 4.5, χ_{SnOx} = 4.7	35.2	10^{15}	24.19	0.961	0.622	14.4
χ_{CdS} = 4.5, χ_{SnOx} = 4.3	35.3	10^{15}	24.50	0.962	0.734	17.2

Reducing N_d in the CdS to 10^{15} moves the junction voltage drop from being almost entirely in the CdTe to being split between the CdTe and the SnO_x/CdS pair. This increases V_{oc} somewhat but decreases the ff substantially.

Increasing the electron affinity of the SnO_X reduces the diffusion voltage on both sides of the junction, so that the bands are bent in reverse as bias is increased near V_{max}. This reduces the light-generated current [i.e., $|J_L(V_{max})|$ is smaller for the $\chi_{SnOx} = 4.7$ eV case than for $\chi_{SnOx} = 4.7$ eV case] and results in a large reduction in ff. The dark JV curves are virtually the same for both of these cases.

Decreasing the electron affinity of the SnO_X increases the diffusion voltage on both sides of the junction, but this has little effect relative to the case for which $\chi_{SnOx} = \chi_{CdS} = 4.5$ eV. The photovoltaic variables are virtually the same for both cases.

6.2.4 AMPS grain boundary simulation

A preliminary grain boundary potential barrier model was set up in AMPS to gain insight on conditions in the CdTe parallel to the junction plane in a polycrystalline (PX) CdS/CdTe cell and how these are affected by illumination. Assumed parameters are shown in *Table 5* (remaining CdTe parameters are given in Table 1). The illumination wavelength is set at 0.81–0.82 μm, which is weakly absorbed so that the photogeneration is nearly uniform throughout the CdTe, with an intensity level such that the generation is equal to that at a depth of 0.9μm into the CdTe of a CdS/CdTe cell.

Table 5: Grain boundary barrier parameters.

	Front Contact	**p-CdTe**	**n-CdTe**	**p-CdTe**	**Back Contact**
Reflection	0.07	—	—	—	0.30
Barrier height (eV)	0.1	—	—	—	0.1
Recombination. velocity, electrons (cm/sec)	10^7	—	—	—	10^7
Recombination. velocity, holes (cm/sec)	10^7	—	—	—	10^7
Thickness (μm)	—	1	0.1	1	—
Carrier density (cm^{-3})	—	10^{16}	10^{17}	10^{16}	—
Electron mobility (cm^2/V-sec)	—	350	350	350	—
Hole mobility (cm^2/V-sec)	—	60	60	60	—
Lifetime (sec)	—	10^{-9}	10^{-10}	10^{-9}	—

AMPS is not optimized for this situation and it was unable to finish the first trial case. By reducing the voltage step size (on the advice of Hong Zhu at Penn State), the case worked, but some of the results (e.g., the dark JV data) were noisy.

Figs. 18A and 18B show the resulting band diagrams for light and dark, showing a reduction in barrier height from 1.2 to 0.50 eV (relative to valence band) with this level of illumination. The plot of recombination rate shows that the depletion layers are very efficient at collecting photogenerated carriers for recombination under the given set of assumptions.

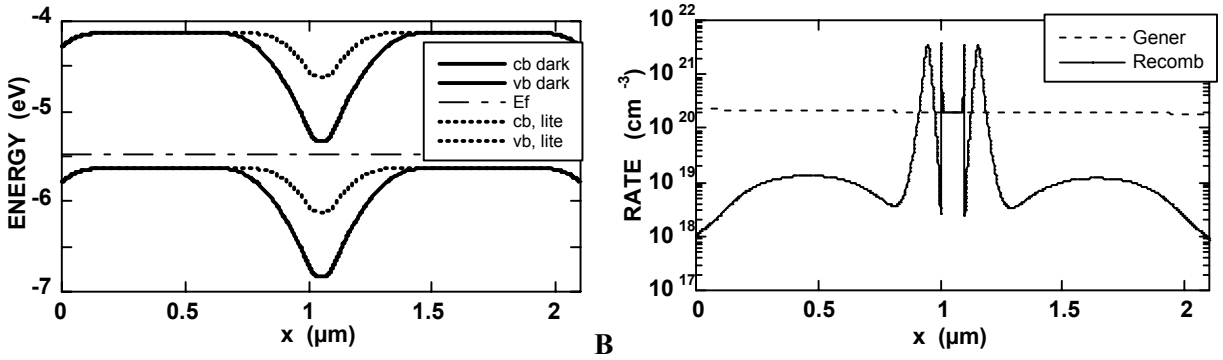


Fig. 18. (A) Grain boundary band diagram light and dark, with (B) corresponding generation and recombination profiles

6.2.5 AMPS modeling conclusions

- The AM1.5G spectrum and the absorption coefficients of CdS and CdTe used in AMPS were upgraded and cases are available for download by email attachment.[24]
- Insertion of a CdS_XTe_{1-X} alloy layer allows a consistent set of PV variables to be targeted exactly by small variations of reflection and CdS layer thickness for J_{sc} and variation of lifetime and the CdSTe layer thickness for V_{oc} and ff.
- Preliminary modeling of cells with TCO layers has been done, indicating the need for more experimental data on interface recombination velocities and band discontinuities.

Next steps:

- Redo the CdSTe alloy layer analysis using the DOS mode and determine sensitivity to recombination center parameters (especially Nr) in the CdSTe layer.
- Up to this point simulation has been targeted at generic cell variables. Simulation of particular cells (those with the most experimental data), hopefully following them through stressing, should be used to test and strengthen the models, and
- Refine the grain boundary model using the DOS mode, to obtain more realistic values of barrier height and then do activation energy analyses.

7 Description of Jet Vapor Deposition

The idea of jet vapor deposition (JVD) was conceived in the early 1990s. JVD is basically a marriage of the principles of APCVD together with the process conditions of CSS. A great advantage of APCVD over CSS is the ability to decouple the substrate and source temperatures. This remains the case in JVD. The JVD process is shown schematically in Figure 19. The similarities between APCVD and JVD are apparent. The only major difference is the operating pressures. In JVD the CdTe material is supported by a porous quartz frit. A carrier gas is introduced at low pressure ~ 5-10 torr. The carrier gas becomes saturated with CdTe in the heated zone. This mixture is then expanded through the frit into the reaction

zone, which is evacuated by a large mechanical pump to a pressure of order 0.1 – 1 torr. The quartz frit plays two critical roles in this setup. First, it behaves as a filter so particles do not get transmitted onto the substrate. Second, the frit creates a large pressure drop – essentially decoupling the two zones of the reactor. As such the gas exiting the frit does so at near choke flow conditions with velocities approaching the speed of sound. The combination of rapid transport and the low operating pressure minimize the chance of molecules having time to nucleate and condense before reaching the substrate. The exiting beam is collimated, so the material is deposited in a confined geometry, and not allowed to pass around the substrate as is the case with APCVD as shown above in Figure 7. Another advantage is that the sonic jet can impart significant amounts of kinetic energy to the impinging molecules, which can enhance their ability to diffuse and incorporate into the lattice. This may result in the ability to reduce substrate temperature without compromising materials quality.

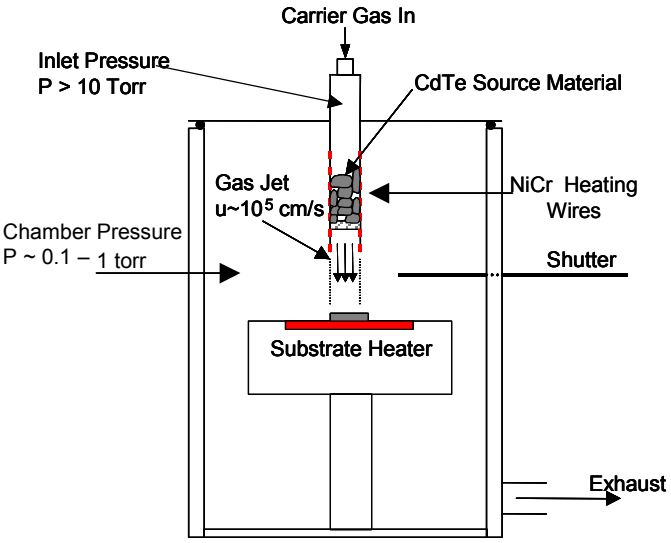
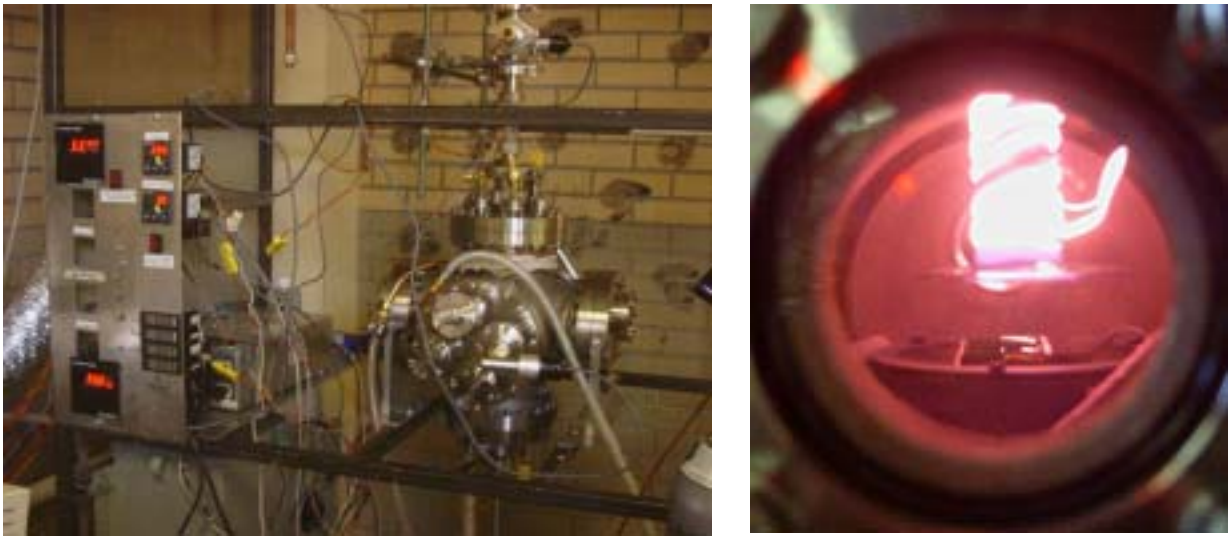


Figure 19: Schematic Diagram of JVD

7.1 Construction and Implementation of JVD

The new reactor has been completed and is operational. Figure 20 shows pictures of the JVD reactor in operation. The quartz tube was loaded with CdTe chunks and wrapped with nichrome heating wire. A type K thermocouple embedded with the CdTe chunks was used to determine and control the source heater. The quartz assembly shown in Figure 19 is mounted in a 6-way stainless steel cross using a standard compression fitting. The chamber was evacuated by and Edwards E2M80 pump equipped with

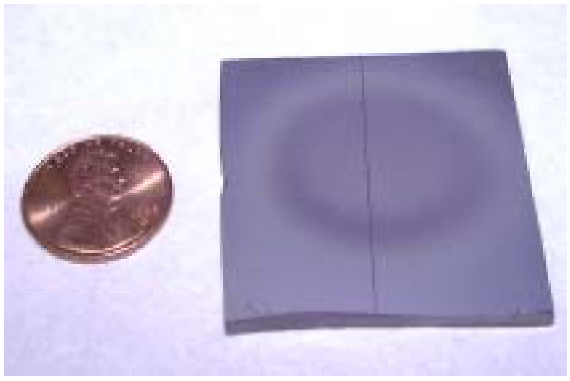


Figures 20: Picture of JVD reactor in operation (left). View through window during deposition (right). The source is glowing due to the nichrome heating wires. The substrate is reflective below it. For scale the source diameter is 1 inch.

Fomblin oil. As shown in Figure 20 the chamber is designed for high vacuum operation. The substrates were placed on a resistively heated copper block whose temperature was maintained by PID feedback control. The substrate temperature could not be directly measured due to the complications of attaching a thermocouple to the glass substrates. However, a calibration was made between substrate temperature and the temperature of thermocouple clamped on the edge of the substrate holder. The latter thermocouple was always present, and it was the one employed to control the substrate temperature. Despite the calibration, one must view absolute temperatures reported in this work with some caution. One issue was that the substrate temperature jumps at the start of deposition by ~50ºC when the shutter was opened due to radiation from the source tube.

The typical deposition process was as follows. The substrates were commercial TCO-coated glass coated with ~ 2000 Å of CdS deposited by chemical bath deposition. Large area substrates were cut into square pieces measuring ~4 cm on each side. The sample was placed on the center of the substrate holder and the reactor was sealed. The shutter was positioned to block the substrate from the source. Next the chamber was evacuated to its base pressure to eliminate any ambient moisture. At this point the carrier gas helium was turned on and sent through the system at a flowrate of 140 sccm. Under these conditions the pressure in the deposition chamber was maintained at P = 0.4 torr. This combination of flowrate and pressure resulted in a nozzle exit velocity of ~ 1500 cm/s. The nozzle position was fixed at a distance of 2 cm above the substrate. The shutter was mounted on a translation stage that could be moved between the nozzle and substrate without disturbing the vacuum. Once the gas was flowing the substrate heater was turned on. Once the substrate reached the desired temperature the nozzle heater was started. Once it ramped to the desired source temperature the deposition was initiated by opening the shutter. After the desired deposition time (1- 5 minutes) the shutter was replaced. The source and substrate heaters were both turned off, and the assembly cooled under helium flow. Once the temperature was < 50 ºC, the helium flow was turned off. The pump was turned off, the chamber was vented, and the sample was removed for *ex-situ* characterization.

Figure 21 shows a picture of typical film. The radial symmetry is visually apparent. A scribe was made as shown in Figure 21 and thickness measurements were performed with a Tencor profilometer. Figure 22 shows the results of typical film uniformity measurements for two different films.



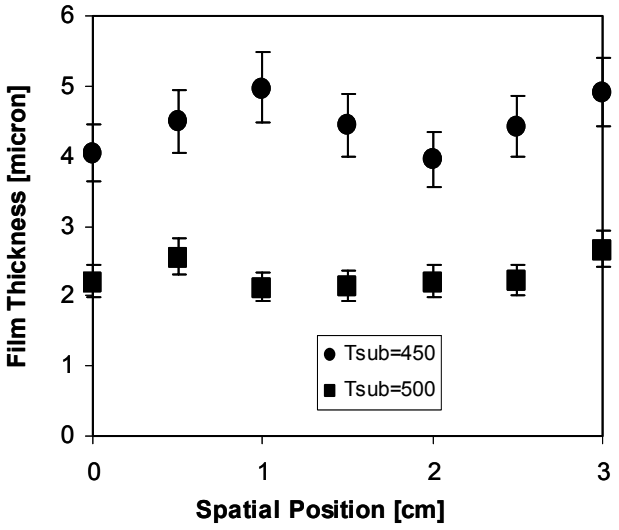


Figure 21: Picture of a deposited film ***Figure 22: Cross-Sectional Uniformity of the two films***

In all the experiments conducted to date no dust formation has been observed. In addition, the materials utilization is much greater than in the case of APCVD. While the utilization is difficult to quantify, it is visually apparent that the majority of the CdTe is deposited on the substrate as shown in Figure 21. In

addition there is minimal CdTe deposition on the substrate holder or the walls of the chamber as compared with APCVD. The films are indeed CdTe. Figure 23 shows a TAUC plot obtained from the transmission spectra of a typical film. The optical bandgap can be estimated by extrapolating the line shown in the figure, and it intercepts at ~1.5 eV as expected.

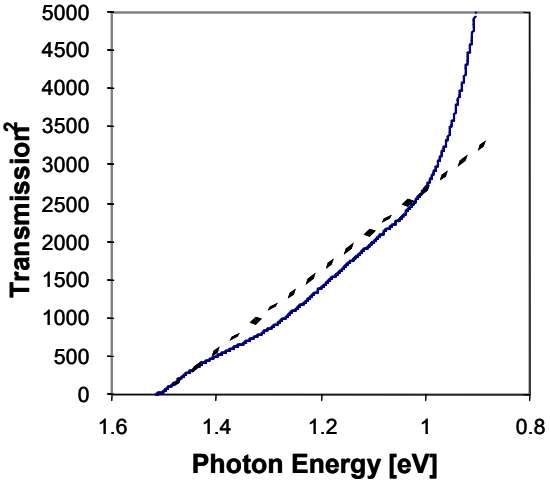


Figure 23: TAUC plot demonstrating the optical bandgap of a typical film

The influences of source temperature and substrate temperature have been examined. Characterization has included film thickness, X-ray diffraction (XRD), atomic force microscopy (AFM) and scanning electron microscopy (SEM). In addition to the JVD CdTe film characterization, a small study was conducted on the optimization of the $CdCl_2$ vapor treatment with JVD material in the typical superstrate-configuration (as described above) cells. Lastly JVD CdTe films were used to make atypical *substrate*-configuration cells. All of these experimental results are reported and discussed in the following section.

7.2 1.2 JVD: Results and Discussion

7.2.1 The Influence of Source Temperature

The first variable that was explored was source temperature. Films were grown to a desired thickness of 6 ± 1 μm by adjusting the deposition time. Having films of the same nominal thickness is critical, particularly for obtaining fair comparison of structural features. For this study all films were deposited at a nominal substrate temperature of 400 ºC. Figure 24 shows a plot of deposition rate as a function of source temperature in an Arrhenius format. For comparison the vapor pressure of CdTe is plotted as the solid line. This figure contains 2 sets of data. The nichrome heating wires embrittle and occasionally break after extended use at high temperature. Each time the quartz tube is re-wrapped, the position of the thermocouple in the CdTe packed bed is moved, which can significantly influence the temperature measurement from wrap to wrap. In the case of the data shown in Figure 24 the data from Series 1 were offset by 90 ºC in order to bring them into agreement with Series 2. Though the absolute temperature is in question, the important thing is that both sets of data have the same slope, which is very similar to the CdTe vapor pressure curve. This demonstrates that rates are determined by the degree of CdTe saturation in the source, and there are no limitations due to transport effects. The nominal source temperatures ranged from 600 – 800 ºC, and maximum growth rate obtained was 20 μm/min. For reference this value is two orders of magnitude greater than best rates obtained via APCVD. It should be noted that this is not a fundamental limit, as higher source temperatures could be obtained. However from a practical point of view the NiCr heating wire lifetime becomes quite limited at temperatures greater than shown here.

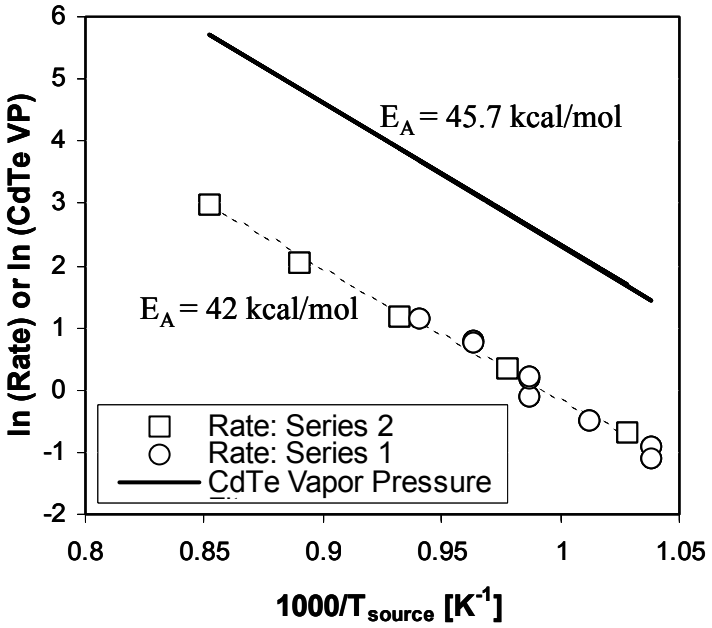


Figure 14: Arrhenius plot of deposition rate as a function of source temperature.

For structural characterization, the films were examined by XRD, AFM, and SEM. Figure 25 shows XRD patterns as a function of source temperature. Again all films had the same nominal thickness. All of the films had nominally identical patterns of cubic CdTe, and displaying a preferred (111) orientation relative to the powder data.

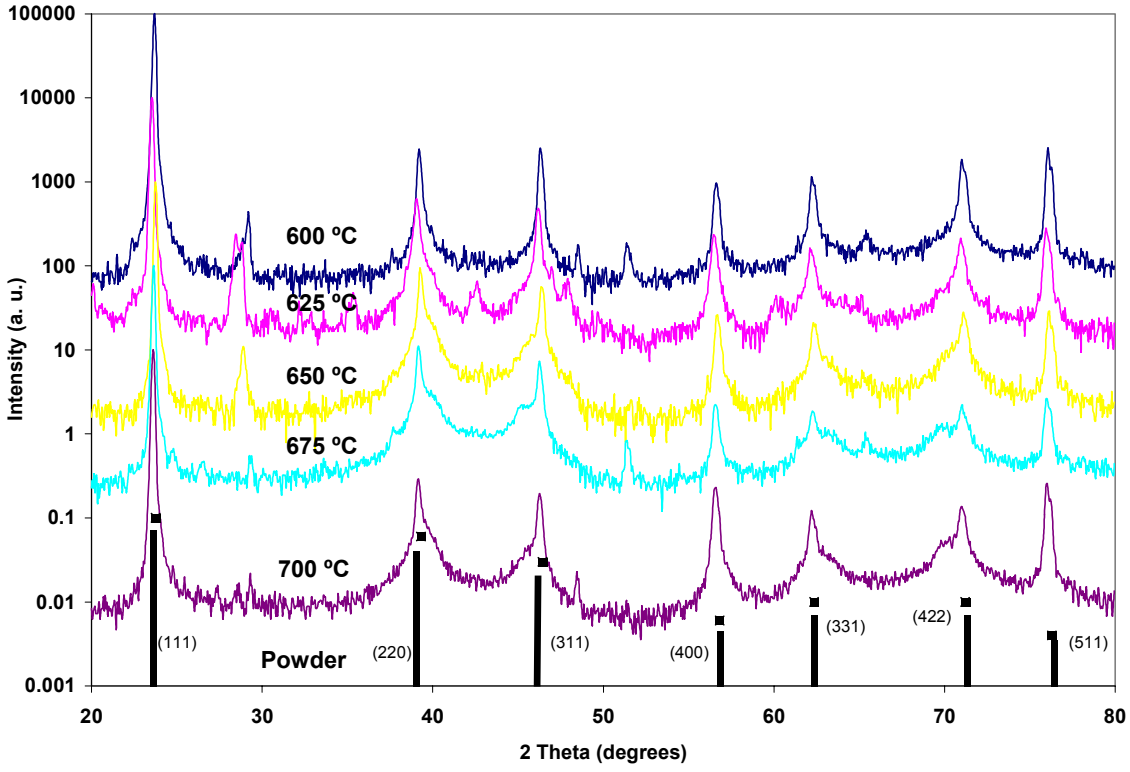


Figure 25: XRD pattern of JVD CdTe films as a function of source temperatures, Tsub = 400 ºC.

The XRD peaks from a powder pattern are shown for comparison purposes, and the computed texture coefficient values, C_i, are given in *Table 6*. The texture coefficient (C_i) values were determined as follows[25]:

$$C_i = \frac{I_i / I_{oi}}{(1/N)\sum_{i=1}^{N} I_i / I_{oi}}$$

where I_i is the intensity of a particular peak in the XRD pattern, I_{oi} the intensity of that peak in the powder standard, and N the total number of peaks included in the analysis (4 in our case). If C_i equals 1, the sample is randomly oriented. A value greater than 1 indicates the sample is preferentially oriented in that direction. Peak intensities were determined using peak height. With the exception of the Tsource = 700 ºC data, the C_i values indicate that the preferential (111) orientation weakens with increasing source temperature. It should be noted that the peak observed at 2*Theta = 28-29 degrees, is not attributed to cubic, hexagonal, or tetragonal CdTe. In addition, the peak doesn't match up with any peaks from a SnO_2 only measured pattern, or CdS, and is thus presently of unknown origin.

Table 6: C_i Values - Variable Tsource, Tsub = 400 ºC

Sample	Tsource	(111)	(220)	(311)	(400)
J68	600	3.110	0.128	0.261	0.501
J66	625	2.416	0.253	0.388	0.943
J62	650	2.250	0.354	0.420	0.976
J64	675	2.224	0.411	0.542	0.823
J69	700	2.682	0.130	0.163	1.025

The cross-sectional/top view SEM image from each of the samples is shown in Figure 26. In Figure 26, the samples are identified clockwise from the top left image as follows: Tsource = 710 ºC (estimated-sample is from a different series than the rest), 700 ºC, 675 ºC,650 ºC,625 ºC, and 600 ºC. Magnification and scale given in images. As can be seen in cross-sectional portion of the images, the through-film morphology changes as a function of source temperature. The lower source temperature grains appear more rounded, while the higher source temperature grains appears denser and more faceted.

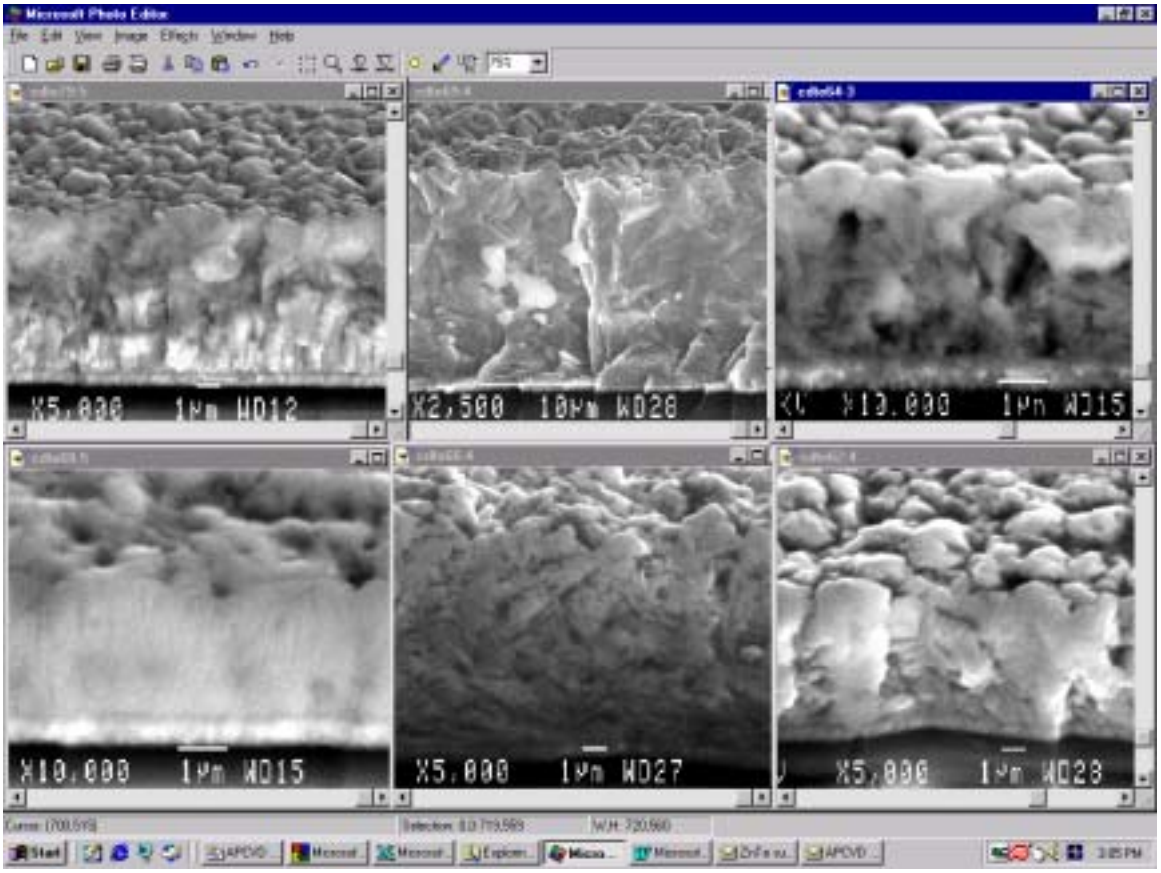


Figure 26: SEM images simultaneously showing cross-section and top surface of JVD CdTe films on CdS/SnO$_2$/Glass substrates, as a function of source temperature with Tsub constant (400 ºC). Clockwise from top left : Tsource = 710 ºC (estimated-sample is from a different series than the rest), 700 ºC, 675 ºC,650 ºC,625 ºC, and 600 ºC. Magnification and scale given in images.

The SEM images also indicate different top surface topographies. AFM was used to determine the surface roughness and a plot of surface roughness is shown in Figure 27. As one can see the surface roughness increased significantly as a function of deposition rate.

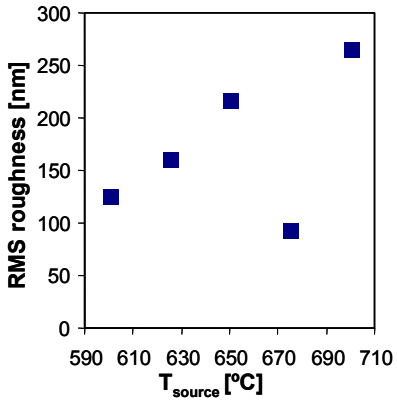


Figure 27: Surface roughness as a function of source temperature

7.2.2 The Influence of Substrate Temperature

The second variable examined was the substrate temperature. In this case the source temperature was fixed at approximately 700 ºC (depends on thermocouple location) and the substrate temperature was varied. Again deposition rate, XRD, SEM and AFM were employed to characterize the deposition. The results of deposition rate are shown in Figure 28 in an Arrhenius plot. There are two regimes indicated in Fig. 28. For relatively cold substrate temperatures (< 375 ºC), the deposition rate is constant at ~4.5 μm/min. As the substrate temperature is increased the rate drops exponentially, indicating that some resublimation is occurring. The apparent activation of resublimation is 11.3 kcal/mol. This behavior is not unexpected as one recalls that the chamber pressure of 0.4 torr is 1 – 2 orders of magnitude lower than that used for CSS processing.

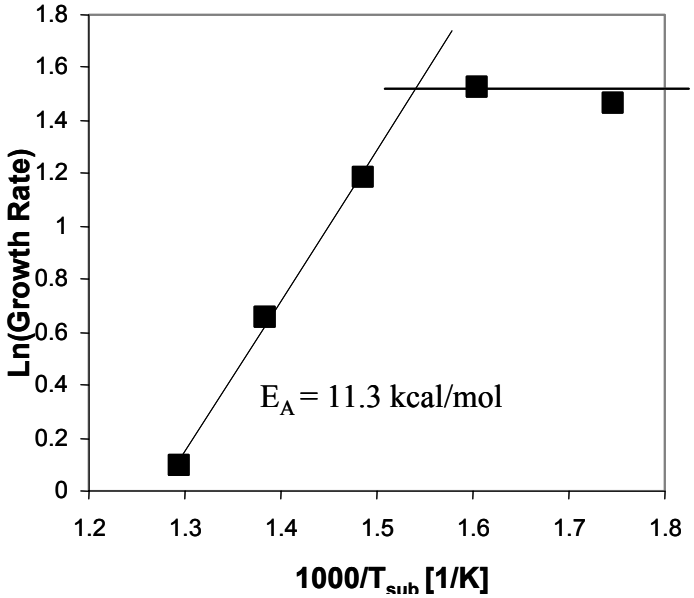


Figure 28: Arrhenius plot of deposition rate as a function of substrate temperature

The XRD patterns for these films are compared in Figure 29. Like their counterparts in Figure 25, the XRD patterns correspond to cubic CdTe with a (111) preferred orientation. The films at the lowest temperature, T_s = 300 ºC, still shows good crystallinity, relative to the (111) peak. This indicates that JVD made be well suited for low temperature deposition. However, there are large differences relative to the non-(111) peaks. The C_i values for four of the peaks in each sample are given in *Table 7* below. In this series, the C_i values for the predominate (111) peak are relatively constant, except for the Tsub = 500 C values, where the (111) Ci value drops by more than half its value at lower substrate temperatures, and the preferred orientation becomes (400). The homogeneity of these results was not tested.

Table 7: C_i Values - Variable Tsub, Tsource ≈ 700 ºC

Sample	Tsub	(111)	(220)	(311)	(400)
J92	300	3.430	0.130	0.219	0.221
J90	350	3.894	0.012	0.025	0.069
J79	400	3.666	0.005	0.008	0.321
J91	450	3.112	0.140	0.241	0.506
J93	500	1.458	0.076	0.334	2.132

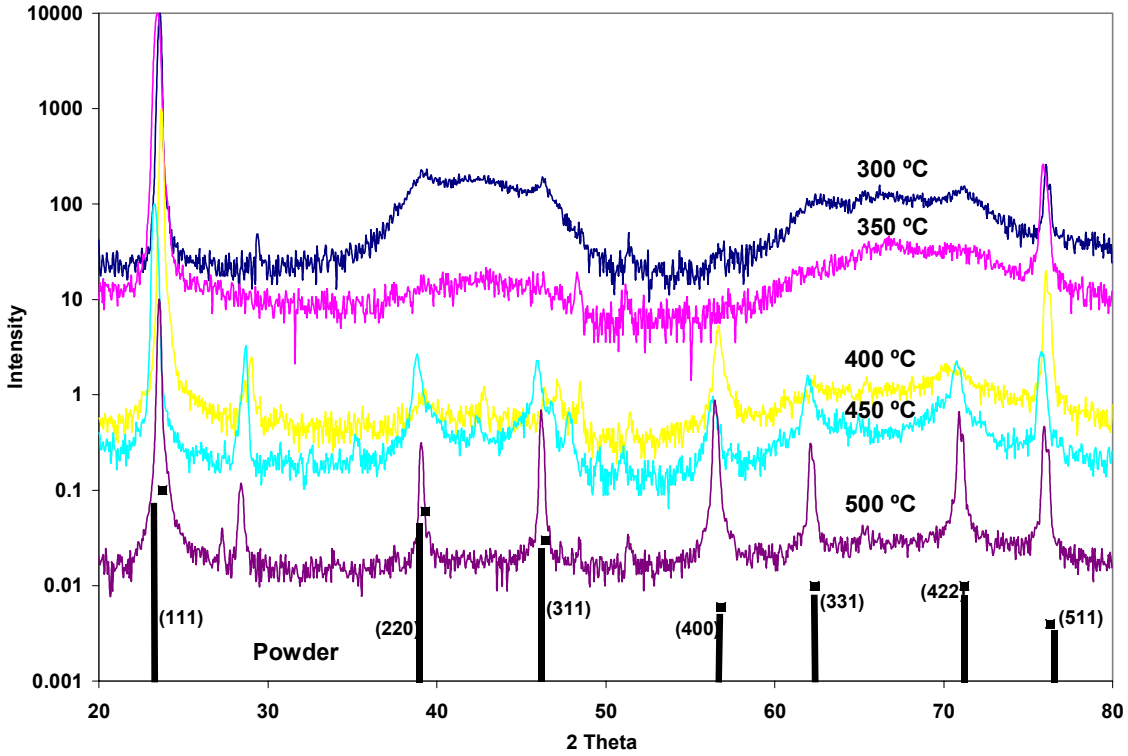


Figure 29: XRD pattern of JVD CdTe films as a function of substrate temperature, Tsource ≈ 710 ºC.

The cross-sectional/top view SEM image from each of the samples is shown in Figure 30. In Figure 30, the samples are identified clockwise from the top right image as follows: Tsub = 300 ºC, 350 ºC, 400 ºC, 450 ºC, and 500 ºC. Magnification and scale are given in images. As can be seen in cross-sectional portion of the images, the top surface and through-film morphology has a considerable variation as a function of substrate temperature. The lower substrate temperature grains appear more columnar, while the highest substrate temperature (500 ºC) grains appear denser and more faceted. The Tsub = 400 ºC image (bottom right) may depict the beginnings of resublimation as discussed above (refer to Fig. 28.).

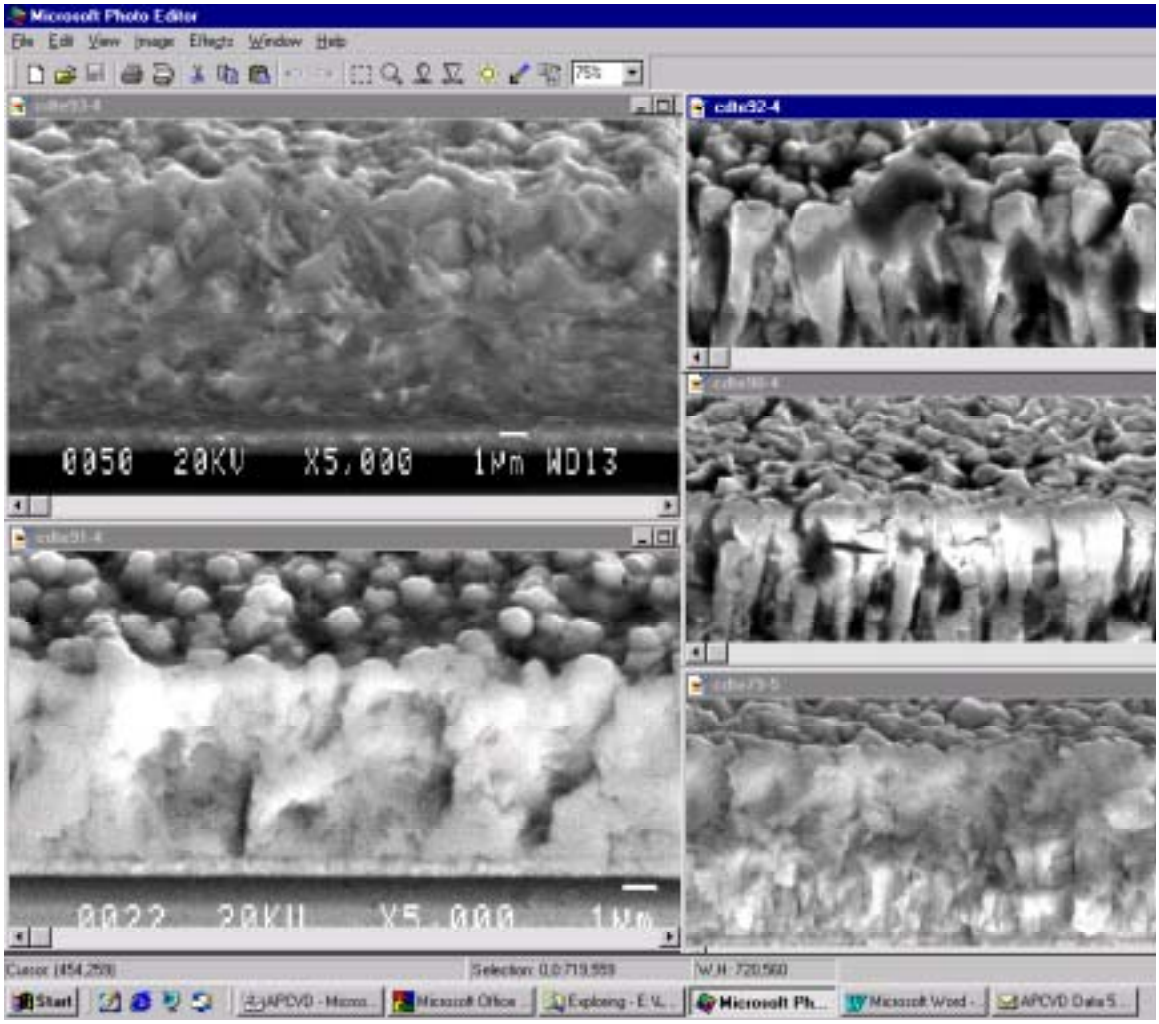


Figure 30: SEM images simultaneously showing cross-section and top surface of JVD CdTe films on CdS/SnO_2/Glass substrates, as a function of substrate temperature with Tsource constant (700 ºC). Clockwise from top right : Tsub = 300 ºC, 350 ºC, 400 ºC, 450 ºC, and 500 ºC. Magnification and scale are given in images. Magnification and scale given in images.

Again the sample surface roughness was determined by AFM, and Figure 31 shows a plot of the results. There was no clear trend displayed in this series of films. The film at T_{sub} = 400 ºC was relatively smooth, compared to the 450 ºC film. Further investigation is required to fully understand these results. It is interesting to note that the despite the apparent differences in surface morphology, all films display the same crystalline structure.

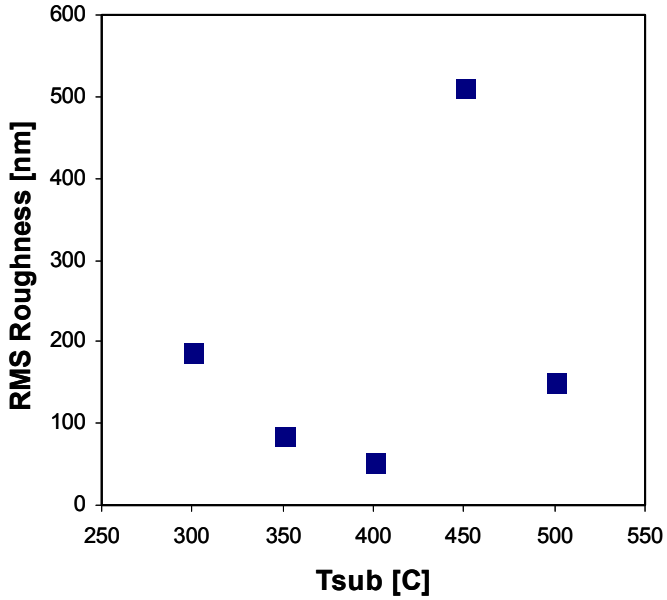


Figure 31: AFM surface roughness as a function of substrate temperature.

While the JVD system is not completely understood, the deposition process can begin to be compared with the APCVD deposition process.

- Pressure: JVD ~ 1 torr (JVD) vs. 600 torr (APCVD)
- Gas Flowrate: 140 sccm (JVD) vs. 20 scfm (APCVD). A >1000X reduction
- Growth Rates: 20 μm/min (JVD) vs. 0.2 μm/min (APCVD). A 100X increase.
- Dust Formation: None (JVD) vs. Extensive (APCVD)
- Materials Utilization: Difficult to quantify, but conservatively estimated to be at least one order of magnitude greater in the case of JVD
- Oxidation: No issues (JVD) vs. high susceptible to catastrophic oxidation (APCVD)

Future avenues of exploration to validate and expand the JVD program would focus on optimization of device fabrication for JVD material as well as further exploration of the low temperature synthesis capabilities. ITN is also interested in exploring deposition of films on moving substrates.

7.2.3 JVD CdTe First Device Results/Study of $CdCl_2$ Optimization

Several devices were fabricated from the early JVD CdTe films. All of these early films received the JVD CdTe with Tsub = 400 ºC, and Tsource is approximately in the range of 550 – 650 ºC. As stated earlier, the substrates were commercial TCO-coated glass coated with ~ 2000 Å of CdS deposited by chemical bath deposition. A small examination of $CdCl_2$ treatment was investigated on JVD CdTe films.

In the procedure at CSM, the $CdCl_2$ coated plates were fabricated by exposing them to a $CdCl_2$ mist for a set amount of time. The $CdCl_2$ plates were then mounted with CdTe plates in a CSS configuration and loaded into a quartz furnace for a given amount of time. In this study annealing time and temperature were the two primary variables. CdTe films of different thickness were examined to see if that influenced device performance. After $CdCl_2$ treatment and back contact formation, devices were finished by small area evaporated gold contacts on the back and using indium as the front contact to the TCO. Device performance was measured under AM1.5 illumination at CSM, and represents the first CdTe devices made with JVD material. The results are summarized below in *Table 8*, where the rows are color coded according to the approximate sample thickness. Although far from comprehensive, a few initial trends could be identified. For the JVD material, the best efficiency and Voc was obtained at combinations of lower temp and shorter time of the $CdCl_2$ treatment. In addition, the thinnest CdTe film yielded the best efficiency device. The light IV curve of the best device is given in Figure 32 below.

Table 8: Summary of $CdCl_2$ treatment study on JVD CdTe superstrate devices.

Sample	Thick-ness (μm)	Anneal Temp (°C)	Time of anneal	Eff.	Voc (mV)	Jsc (mA/cm2)	Fill Factor (%)
J20-E	4.3	<400	1x	8.8	757	19.1	61
J21-C	5.2	<400	3x	7.7	726	19.3	55
J20-C	6.6	<400	1x	8.3	758	19.9	55
J18-C	4.6	<400	1x	8.7	762	19.6	59
J24-S	5.6	>400	3x	7.5	531	24.4	58
J10-S*	7.4	>400	1x	8.0	585	23.1	59
J14-W*	7.9	>400	3x	7.4	612	20.3	60

*Higher growth rates during JVD of CdTe.

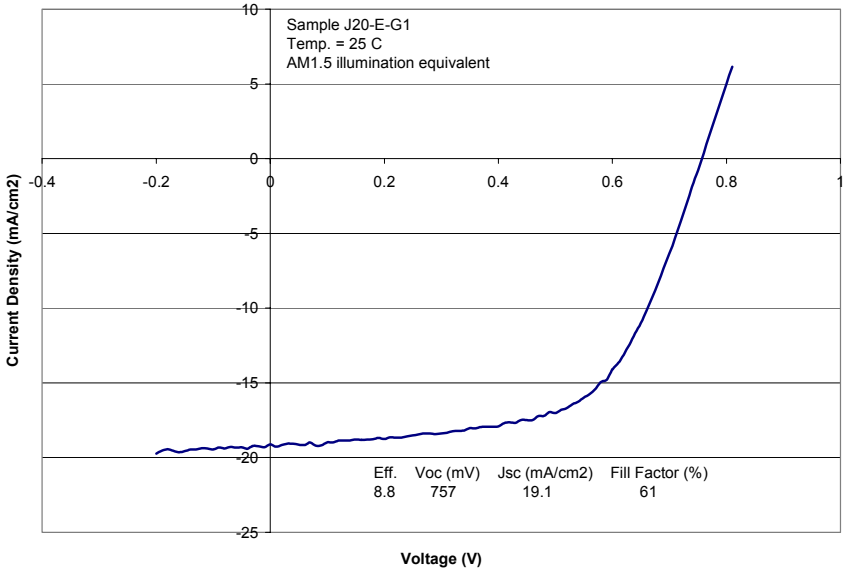


Figure 32: AM1.5 light IV of best JVD CdTe device in superstrate configuration.

7.2.4 Study of Substrate Configuration Devices

7.2.4.1 Background

The highest efficiency CdTe based photovoltaic devices are fabricated in the superstrate configuration. That is, the "substrate" forms the top surface of the device. Thus, the "substrate" must be transparent to visible light in the superstrate configuration when making photovoltaic devices. This requirement severely limits the possible "substrates", especially when thin flexible "substrates" are desired. Thin flexible substrates offer many advantages in terms of roll-to-roll processing, hence reduced manufacturing costs. On the other hand, devices fabricated in the *substrate* configuration have not come near the level of performance as the superstrate devices, albeit the quantity of research and development (R&D) on substrate devices has been relatively small in comparison. It is likely that reluctance to perform R&D on substrate type devices is due to the following:

1) Belief of increased lack of processing control over the formation of the "back contact" to CdTe, which is inherently difficult for p-type CdTe and consequently critical to device performance. In addition, the relationship between bulk CdTe Cu-content and formation of the back contact further increases the importance of back contact processing control.
2) Complications with the important $CdCl_2$ heat treatment relative to the heterointerface between CdS and CdTe, and the individual layer bulk properties. The importance of intermixing at the heterointerface may be an additional complication.
3) Success of superstrate device together with little previous interest in lightweight, flexible substrate modules.

Regarding the former, recent developments and increasing popularity of p-type ZnTe have raised interesting possibilities for forming a stable back contact to substrate CdTe devices. Regarding the second item, there has been relatively little optimization of the $CdCl_2$ heat treatment process and attempts to change the intermixing at the heterointerface with the substrate configuration devices. Regarding the latter, more and more markets are being identified for lightweight, flexible solar cells (as a-Si manufacturers can attest to) as well as the low-cost benefits of roll-to-roll processing.

Interest in JVD deposition of CdTe also stems from the interest in lightweight, flexible substrates. This is because non-metallic lightweight, flexible substrates require lower substrate temperatures (typically 400 ºC max.), and JVD may be able to supply extra energy to the thin film growth kinetics, which may be necessary to achieve high-quality CdTe films at lower substrate temperatures.

7.2.4.2 Back Contact Work

The substrate devices attempted herein, were fabricated on moly-coated sodalime glass substrates. The first attempt at substrate devices, focused on Cu-doped ZnTe back contacts, in addition to the moly only contact. Given the limited time that was left on the APCVD/JVD program, we decided to go with CSM's existing ZnTe room temperature deposition capability. Other possible options such as Cu-doped ZnTe source material and variable substrate temperature during the ZnTe deposition would have to wait for later exploration. As a part of the first set of samples, it was decided to try thin Cu depositions both before and after the ZnTe deposition. For the Cu on ZnTe, a high temperature anneal option would be tried in an effort to place most of the Cu doping in the ZnTe prior to the CdTe deposition.

Thus, the following back contacts were fabricated on 1.5" square moly/Na-lime glass substrates for a total of 24 back contact substrates (1x – one times film thickness, 2x – two times film thickness):

1) (2) No ZnTe (Moly only)
2) (2) No ZnTe/Cu
3) (4) ZnTe (No Cu)
4) (4) Cu/1x ZnTe
5) (4) Cu/2x ZnTe
6) (4) Cu/3x ZnTe
7) (2) 1x ZnTe/Cu (w/Anneal)
8) (2) 2x ZnTe/Cu (w/Anneal)

7.2.4.3 JVD CdTe Depositions

JVD CdTe depositions were attempted on all of the back contact configurations described above, and a total of 24 depositions were performed. The substrate temperature was 400 ºC and the source temperature was in the approximate range of 650 – 700 ºC. After the JVD CdTe depositions, it was found that the samples with ZnTe by itself as a back contact (item 3 above), did not adhere. In addition, the thickest ZnTe on Cu samples, (item 6 above), also lost adhesion after the JVD CdTe. Thus, this eliminated nearly half of the available ZnTe back contact substrates.

Further complications were experienced with the uniformity of the CdTe films. Visually, dark and light areas co-existed on the substrates, with the exception of the moly only substrates. This visual inhomogeneity occurred in spite of relatively uniform looking ZnTe prior to the CdTe deposition. In addition, some samples had small area "clumps" of CdTe that are believed to be a result of CdTe debris falling off of the shutter. Installing a new (clean) shutter piece later ameliorated this problem.

7.2.4.4 $CdCl_2$ Optimization and Post-JVD Device Processing

The $CdCl_2$ treatments were performed by the vapor technique using a glass tube furnace at Colorado School of Mines, and as previously described. Prior to the $CdCl_2$ treatment, the CdTe films had approx. 500 Å of chemical bath deposited CdS deposited on them. In a few select cases, a double coat of CdS was used to evaluate its effect on the $CdCl_2$ treatment and devices. Further sample attrition occurred during the CdS bath process, again due to poor adhesion at the ZnTe/moly interface. Two samples from the Cu/1x ZnTe group were lost (item 4 above), as well as all of the ZnTe with annealed Cu from the top (items 7 and 8 above). The non-uniform CdTe films and poor ZnTe adhesion discussed above, severely limited the number of samples available for $CdCl_2$ optimization during this first attempt at substrate devices. All of the moly only and moly/Cu samples remained, but only a few Cu/ZnTe samples were available. As a result only three different $CdCl_2$ treatments were attempted and are listed in the table below. Two different substrate temperatures and two different treatment times were accomplished, but there were insufficient identical substrate types to obtain a meaningful comparison, between all three processing conditions. Following the vapor $CdCl_2$ treatment, the devices received a sputter deposited TCO and grids for the top contact. Small area grids were used, and positioned to take advantage of areas where the CdTe was more visually homogeneous.

7.2.4.5 Device Results

The remaining devices were tested under AM1.5 illumination and the device processing conditions and best device results for each condition are given below in *Table 9*.

Table 9: Summary of back contact and $CdCl_2$ treatment study on JVD CdTe substrate devices.

Sample ID	ZnTe Thick-ness	Cu*	CdS Thick-ness	CdCl2a nneal Temp (°C)	CdCl2 Time of anneal	Eff.	Voc (mV)	Jsc (mA/cm^2)	Fill Factor (%)
711-B3	None	N	1.5x	<400	2x	0.7	208	12. 9	28
730-A1	None	N	1.5x	<400	2x	2.0	454	16.2	27
730-A2	None	N	1.5x	<400	1x	0.6	290	7.1	28
812-A1	None	Y	2x	<400	1x	3.1	588	15.6	34
812-A2	None	Y	1x	<400	1x	0.1	135	4.6	23
711-C1	1x	Y	1.5x	>400	1x	0.3	119	9.3	26
711-C4	1x	Y	1.5x	<400	1x	0.6	302	9.9	19
716-A1	2x	Y	1.5x	<400	1x	0.9	345	10.1	26
716-A2	2x	Y	1.5x	>400	1x	1.0	456	10.8	19
716-A3	2x	Y	1.5x	<400	2x	0.8	483	8.2	21
716-A4	2x	Y	1.5x	>400	1x	0.5	356	6.8	20

* N – No copper deposition, Y- Copper deposited on moly/glass substrate

Of the remaining fully processed devices, the best devices were obtained without a ZnTe layer. Of these, the device with a thin layer of copper on the moly, before JVD CdTe, and with 2x CdS, gave the best result. The light and dark IV curve of a small area device from this sample is given in Fig. 33 below. The best device with ZnTe, used a thicker ZnTe layer. With the limited data herein, there is no clear direction for optimizing the $CdCl_2$ heat treatment at this point.

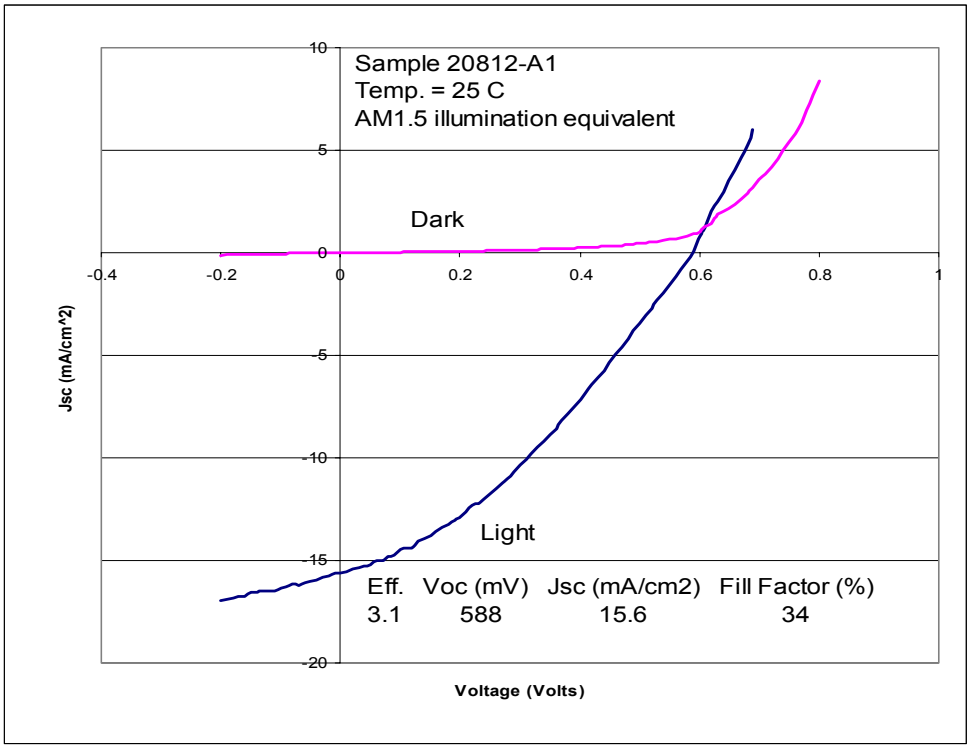


Figure 33: AM1.5 light IV of best JVD CdTe device in substrate configuration.

7.2.5 JVD CdTe Device Conclusions

Low substrate temperature (400 °C) JVD of CdTe has been implemented in the fabrication of thin-film photovoltaic devices. Both the more conventional superstrate type configuration, and more unconventional *substrate* type configuration have been fabricated, and an optimization of the $CdCl_2$ heat treatment has been attempted in each case. However, the results herein, represent only a first attempt at fabricating devices based on JVD CdTe. In the case of superstrate devices, the thinner CdTe films and the CdCl2 heat treatment with lower temperature and time gave the best results, and yielded an 8.8% efficient device with relatively little optimization. In the case of the substrate type devices, the best device results (3.1% efficient) were obtained with Cu deposited on the moly, but with no ZnTe as a part of the back contact. Poor adhesion at the ZnTe/moly interface severely limited the optimization of the back contact using ZnTe.

8 Summary

8.1 Project Summary

Activities during the third year and the extension of the APCVD program were directed toward improved design and testing of the APCVD reactor. High efficiency devices were fabricated with the second-generation reactor with the inclusion of SnO_x HRT buffer layer. A third generation, the split source reactor, was designed and built to overcome issues with both deposition rate and particle formation. Despite intensive investigation the limitations inherent to APCVD could not be overcome. Mathematical analysis was used to quantify the deficiencies of APCVD with respect to particle nucleation and mass transport. Based on this analysis the project direction was altered to pursue jet vapor deposition (JVD).

JVD maintains much of the geometrical similarities to APCVD, but it combination of sonic velocities and low pressure operation are expected to eliminate the problems encountered with APCVD.

Accomplishments during the Phase III include:

- Fabrication of APCVD CdTe PV devices with 10.6% (confirmed) efficiency
- Fabrication of APCVD CdTe PV devices with 14.6% (unconfirmed) efficiency
- Identification and quantitative analysis of deficiencies with APCVD technology
- Fundamental characterization of APCVD CdTe microstructure
- Identification of similarities & differences in APCVD vs. CSS
- Adoption, design and construction of a JVD reactor
- High rate deposition validating the promise of JVD
- Fabrication of low substrate temperature JVD CdTe PV devices with 8.8% (unconfirmed) efficiency
- Fabrication of low substrate temperature JVD CdTe PV devices in substrate configuration with 3.1% (unconfirmed) efficiency.

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13. ABSTRACT *(Maximum 200 words):* ITN's three-year project, Atmospheric Pressure Chemical Vapor Deposition (APCVD) of CdTe for High Efficiency Thin Film PV Devices, had the overall objectives of improving thin-film CdTe PV manufacturing technology and increasing CdTe PV device power-conversion efficiency. CdTe deposition by APCVD employs the same reaction chemistry as has been used to deposit 16%-efficient CdTe PV films, i.e., close-spaced sublimation, but employs forced convection rather than diffusion as a mechanism of mass transport. Tasks of the APCVD program center on demonstration of APCVD of CdTe films, discovery of fundamental mass-transport parameters, application of established engineering principles to the deposition of CdTe films, and verification of reactor design principles that could be used to design high-throughput, high-yield manufacturing equipment. Additional tasks relate to improved device measurement and characterization procedures that can lead to a more fundamental understanding of CdTe PV device operation, and ultimately, to higher device conversion efficiency and greater stability. Under the APCVD program, device analysis goes beyond conventional one-dimensional device characterization and analysis toward two-dimensional measurements and modeling. Accomplishments of the concluding year and extension of the APCVD subcontract included: incorporation of high-resistivity transparent buffer layers and achievement of 12.3%-efficient (NREL-measured, but not certified) devices by APCVD; analysis of scale-up issues related to APCVD, analysis of dust formation dynamics; demonstration of the inherent deficiencies of APCVD for CdTe manufacturing; modeling effects of CdSTe and SnO_x layers; and electrical modeling of grain boundaries; design and construction of a low-pressure jet vapor deposition (JVD) reactor; JVD CdTe film characterization as a function of substrate and source temperature; demonstration of high growth rates using JVD; and superstrate-type and substrate-type device fabrication using low-substrate-temperature JVD CdTe films.

14. SUBJECT TERMS: PV; atmospheric pressure chemical vapor deposition (APCVD); fundamental mass transport; manufacturing; jet-vapor deposition (JVD); thin-film solar cells; close-space sublimation (CSS); cathodoluminescence (CL); cross-sectional transmission electron microscopy (XTEM); impedance spectroscopy (IS); deep level transient spectroscopy (DLTS); back contact; CdTe; high resistivity transparent (HRT) buffer layer

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