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Subcontractor Report

Optimization of Processing and Modeling Issues for Thin Film Solar Cell Devices

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24 August 1998—23 October 2001

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SUMMARY

The overall mission of the Institute of Energy Conversion is the development of thin film photovoltaic cells, modules, and related manufacturing technology and the education of students and professionals in photovoltaic technology. The objectives of this 20 month NREL subcontract are to advance the state of the art and the acceptance of thin film PV modules in the areas of improved technology for thin film deposition, device fabrication, and material and device characterization and modeling, relating to solar cells based on $CuInSe_2$ and its alloys, on a-Si and its alloys, and on CdTe.

$CuInSe_2$-BASED SOLAR CELLS

Effect of Deposition Temperature on $Cu(InGa)Se_2$ Films and Devices

Lowering the $Cu(InGa)Se_2$ substrate temperature from 550 - 600°C, used for the highest efficiency devices can reduce processing costs associated with glass handling and thermal stress on the deposition system, and potentially enable polyimide substrates to be used. The effects of substrate temperature and evaporation sequence, with regard to Cu-rich film growth on $Cu(InGa)Se_2$, films and devices and to quantitatively determine the effect of grain size. $Cu(InGa)Se_2$ films were deposited by elemental evaporation of Cu, In, Ga, and Se using three flux versus time profiles to give depositions with: (1) Cu-rich flux, Cu/(In+Ga) > 1, at the start of the run, (2) Cu-rich flux in the middle of the run, and (3) uniform fluxes so that the films composition is never Cu-rich. The final composition of all devices was the same at the completion of the deposition. These depositions were each done with substrate temperatures (T_{SS}) = 400, 480, and 550°C. The grain size distribution and surface morphology of each $Cu(InGa)Se_2$ film was determined using atomic force microscopy and compared to the device behavior.

The highest efficiency devices in this study were 16.5% at 550°C and 14.1% at 400°C. Comparing different flux profiles, it was shown that at 400°C Cu-rich growth is necessary to achieve good performance. However, at higher T_{SS} the device performance is insensitive to the growth sequence allowing greater process flexibility. With the Cu-rich growth, the mean lateral grain area decreases from 1.8 to 0.3 μm^2 as T_{SS} is reduced from 550 to 400°C, but only at the highest T_{SS} does the grain size depend on the growth process. In general, lower device efficiency with lower T_{SS} cannot be simply described by changes in grain size, surface area or the availability of Na. Instead, the lower voltage and increased recombination current with lower temperature deposition indicate a greater density of intra-grain trap states in the $Cu(InGa)Se_2$ which can also lead to smaller minority carrier diffusion length and voltage dependent current collection.

In-line Evaporation of $Cu(InGa)Se_2$

In-line evaporation is a potentially effective means to achieve the high rate uniform deposition necessary for commercial-scale manufacture of $Cu(InGa)Se_2$ modules. In this process, the substrate is linearly translated over thermal sources from which the elemental materials are evaporated. An in-line evaporation system for the deposition of $Cu(InGa)Se_2$ films has been put into operation at IEC. The system's performance in terms of uniform deposition over large areas

at relatively high rates and in terms of device performance and reproducibility has been successfully demonstrated. The compositional uniformity across the 6-inch wide deposition zone is within the uncertainty limits of EDS measurements. A set of depositions with translation speeds ranging from 1 to 2.5 inches/min produced films with thicknesses from 2.1 to 0.9 μm thick. Devices from these runs had efficiencies from 13.2-14.5 %, for thickness > 1 μm, demonstrating the run-to-run reproducibility of the system. The best cell produced with $Cu(InGa)Se_2$ from this in-line system had 14.9% efficiency. Improvements to the design and control of in-line evaporation process included improved source design, source characterization, and *in-situ* AA modeling and characterization. Combined, these achievements allow a high degree of controllability over the incident fluxes at the substrate over extended runs.

The spatial flux distributions from each of the Cu, In, and Ga evaporation sources, and over a wide range of evaporation rates for the Cu source, were measured. In all cases the flux could be describe by a $\cos^n\theta$ approximation with n = 3.0. A source effusion model predicting film thickness, composition, and compositional gradients was developed using the flux distributions and tested. In conjunction with Auger depth profiles, the model and film results show that Cu diffuses freely through the film, while Ga and In maintain graded profiles consistent with their sequence of deposition.

Formation and Analysis of Graded $CuIn(SeS)_2$ and $CuGa(SeS)_2$ Films

The incorporation of sulfur into $CuInSe_2$ thin films was quantitatively investigated to establish a scientific and engineering basis for the fabrication of homogeneous and compositionally graded $CuIn(SeS)_2$ thin films. By reacting stoichiometric or slightly Cu-rich $CuInSe_2$ films in a flowing H_2S/Ar atmosphere, the films can be completely converted to $CuInS_2$ or converted to a graded $CuIn(Se_{1-y}S_y)_2$ film, depending on processing conditions. A phenomenological model of the reaction/diffusion process was developed wherein H_2S reacts with $CuInSe_2$ at the surface to form $CuInS_2$, releasing Se. The $CuInS_2$ and $CuInSe_2$ layers interdiffuse, resulting in a S/Se gradient in the structure. X-ray diffraction (112) line profiles of graded films are compositionally broadened due to continuously changing lattice parameters. The 3-dimensional sulfur distribution was calculated for measured grain size distribution using generated diffraction line profiles. These were fit to measured line profiles using bulk and grain boundary diffusion coefficients as fitting parameters, yielding diffusion coefficients and activation energies for bulk and grain boundary diffusion processes.

The effect of initial film composition and substrate in the sulfurization of $CuInSe_2$ was further investigated. $CuInSe_2$ films deposited on either soda-lime glass (SL) or Corning 7059 borosilicate glass (7059) substrates were reacted in flowing H_2S for times from 1 to 8 hours. Films with Cu-rich composition, Cu/In > 1, reacted for 1 hour, had nearly all the Se replaced by S. For Cu-poor films, the incorporation of S was significantly reduced. In addition, in Cu-poor films on SL glass, $CuInS_2$ and $NaInS_2$ were found at the film surface. These phases were not detected in films on 7059 substrates or in Cu-rich films. A phenomenological model has been proposed to explain the formation of segregated surface phases in Cu-poor films on SL substrates.

$CuInSe_2$ Team Participation and Collaborations

IEC was an active member of the following four sub-teams under the National CIS Team for the NREL Thin Film Partnership program:

Global Solar Energy. This team focused on helping GSE develop a low temperature process for the roll-to-roll deposition of $Cu(InGa)Se_2$. IEC has provided direct support through materials characterization and device fabrication and characterization on both glass and flexible substrates. In addition, IEC and GSE have collaborated on several issues related to the in-line and roll-to-roll deposition of $Cu(InGa)Se_2$. This included application of chemical surface deposited (CSD) CdS, as described in the CdTe section of this report. $Cu(InGa)Se_2$ devices, using absorber layers deposited at IEC and GSE, were fabricated with CSD CdS and shown to have comparable efficiency. The CSD process was shared with GSE.

ISET. IEC has assisting in the development of improved performance of ISET's CIS-based materials by investigating the use of sulfur incorporation to increase the voltages in devices and modules.

Siemens Solar Industries. This sub-team addressed reliability and transient effects in SSI's cells and modules. IEC provided device fabrication and characterization for other team members and supplying $Cu(InGa)Se_2$ films and devices for characterization.

UNISUN. IEC has provided detailed materials characterization, device fabrication and device characterization to support Unison's development of particle-based processes for deposition of $Cu(InGa)Se_2$.

In addition to these activities in support of the national CIS Teams, IEC has provided direct support to several other groups within the Thin Film Partnership. Some specific activities have included:

Florida Solar Energy Center. IEC has done detailed J-V and QE measurements and analysis of FSEC's $CuIn(SeS)_2$ devices.

University of Florida. IEC has provided $Cu(InGa)Se_2$ absorber layers, and fabricated and characterized solar cells using $In_x(OH,S)_y$ buffer layers deposited by chemical bath deposition at UF [1].

University of Illinois. IEC developed a process to fabricate solar cells on $Cu(InGa)Se_2$ epilayers grown on GaAs substrates at University of Illinois. This process includes a Pt back contact and takes advantage of the conductivity of the GaAs. The best cell to date on the epilayers had efficiency > 7%.

University of Oregon. IEC is collaborating with the University of Oregon to quantitatively characterize the defects in working $Cu(InGa)Se_2$ solar cells using admittance spectroscopy. IEC has provided device samples encompassing a range of different $Cu(InGa)Se_2$ parameters including Ga content, deposition temperature and process and JV behaviors. Initial results showed that high efficiency devices have both band tails and a deep defect band [2]

Washington State University. IEC has continued to fabricate and characterize devices using alternate window layers being developed at WSU, focusing on MOCVD grown ZnSe and ZnO buffer layers [3].

Si-BASED SOLAR CELLS

Several investigations concerning a-Si solar cells and hot wire chemical vapor deposition (HWCVD) films were conducted during this contract. In the area of a-Si solar cells, the deposition of more conductive μc-Si p- and n-layers based on silicon carbide and silicon oxide was studied. The dependence of various commercial SnO_2 substrates to thermal and H_2 treatments was also investigated. In addition, two novel methods to characterize the contact resistance and junction properties of the transparent conductive oxide (TCO)/p contact in active p-i-n devices were developed. A key result from this analysis was that ZnO does not result in a blocking or high resistance contact as was commonly assumed. This work was done in collaboration with Dr. Gautam Ganguly at BP Solar. Finally, we completed a comprehensive study of optical enhancement and losses in a-Si p-i-n solar cells, determining the effect of TCO texture, back contact reflectivity and i-layer thickness on the optical enhancement factor. We conclude from this that parasitic absorption in the textured SnO_2 is a major loss, in addition to parasitic absorption at the back contact.

Regarding HWCVD Si films, two papers, summarizing the results of the deposition and characterization of HWCVD Si films and the modeling of the HWCVD process, were published in the *Journal of Industrial and Engineering Chemistry Research*. Key results from this work are that polycrystalline Si films can be deposited by HWCVD with pure silane and that there is a critical value of the atomic hydrogen to silane radical ratio at which the transition from amorphous to polycrystalline films occurs. In addition, several approaches were also investigated to enhance the grain size of HWCVD films. Preliminary results of an *in-situ*, low temperature metal induced crystallization method appears to produce films with micron size grains and no contamination by Al in the Si layer as determined by EDS.

Microcrystalline p-layers Based on Silicon Carbide and Silicon Oxide

The focus of the a-Si research was on deposition of more conductive μc-Si based p-layers and characterizing properties of TCO layers following plasma exposure. The Si:C:H and Si:O:H p-layers were deposited by RF CVD. The effect of H_2, SiH_4, CH_4 and CO_2 flow rates, boron dopant source gas, and RF power on microcrystallinity and conductivity was studied. This work is motivated by the need for a wide bandgap highly conductive p-layer material to simultaneously increase V_{oc} and blue response of superstrate p-i-n solar cells.

The investigation of glow discharge deposited crystalline p-layers was conducted in two stages. First, we investigated the deposition and characterization of these types of films having a high level of CH_4 in the feed gas, which completed the investigation of carbon containing p-layers. The goal was to determine the feasibility of obtaining crystalline SiC phases in the films. Second, we investigated the deposition and characterization of films having CO_2 in the feed gas. The goal here was to obtain two-phase films of crystalline Si imbedded in a matrix of a–Si:O:H:C. The idea is that such films incorporated in p-i-n type devices could give high currents due to the transparency of the amorphous phase and high voltages due to the highly conductive

crystalline phase with a smaller junction surface. Also, the presence of CO_2 in the glow discharge plasma would tend to decrease the reducing effects of the plasma on the thin conductive oxide used as the front contact in superstrate devices.

The p-layers were deposited on 7059 glass and on SnO_2 substrates, and their crystallinity was determined by Raman spectroscopy. In-plane conductivity and activation energy measurements were also performed on most of the films deposited on glass substrates.

The main experimental variables were the hydrogen dilution and CH_4 or CO_2 content in the feed gases. The secondary parameters were discharge power density and doping gas (B_2H_6) level. Increasing hydrogen dilution reduces deposition rate even though silane partial pressure and gas residence time stay the same. This observation supports hydrogen etching of the film during growth. The observed increase in deposition rate with gas phase diborane concentration is related to the known ability of diborane in cracking silane molecules. Results also show that while the CO_2 level in the discharge does not seem to have an effect on the c-Si content in the case of glass substrates, it does, however, control crystallinity of the films deposited on SnO_2 substrates.

The only crystalline phase identified for films with CH_4 or CO_2 was silicon. Volume fraction of the crystalline phase was found to depend on hydrogen dilution but not on the discharge power. High silane partial pressures resulting in high deposition rates suppress the formation of the crystalline phase. High levels of crystallinity were obtained at very low power densities. Crystallinity in the films was found to decrease with increasing amounts of CO_2 in the discharge. The amount of crystalline phase in the films deposited on SnO_2 was consistently lower than in the films deposited on glass substrates. Raman spectra showed the existence of a two-phase mixture consisting of c-Si and amorphous silicon phases. Also, the film deposited on glass seems to have a higher amount of c-Si phase.

SIMS depth profiles indicate that the composition of the films are independent of the substrate, and the oxygen and carbon content in the films are, respectively, 10^{22} and $7x10^{20}$. Since the films have a c-Si and an amorphous phase, the latter must contain almost all the hydrogen, carbon and oxygen observed in the SIMS analysis. Thus, it can be concluded that the amorphous phase is essentially hydrogenated silicon oxide containing small amounts of carbon and boron.

It is found that the fraction of c-Si increases with increasing hydrogen dilution and decreases with increasing diborane level. However, this observation is complicated by the dependence on the film deposition rates. This is because bonding rearrangement on the surface of the growing film that favors c-Si formation will be more extensive for low deposition rates. Consequently, dependence of crystallinity on hydrogen dilution is only clear in the regions where deposition rates do not change appreciably. The deposition rate argument can also explain the difference in crystallinity between like substrates deposited at different diborane levels.

However, the difference in crystallinity between glass and tin oxide substrates for a given diborane level might also be controlled, in addition to deposition rate, by the possible difference in the initial nucleation rate of crystallites on glass and tin oxide surfaces. The difference in deposition rates between glass and SnO_2 substrates is most probably due to the voltage difference between substrate and the plasma. In the case of a conductive substrate, such as SnO_2, the

surface is grounded and the potential difference between substrate and plasma is the plasma potential. In the case of glass substrate, the potential difference is the floating potential which, in general, is substantially smaller than the plasma potential.

Increasing hydrogen dilution reduces the deposition rate even though silane partial pressure and gas residence time stay the same. This observation supports hydrogen etching of the film during growth. Finally, the observed increase in deposition rate with gas phase diborane concentration is related to the known ability of diborane in cracking silane molecules.

Interpretation of the measured conductivities and activation energies is problematic because of the two-phase nature of these films. However, it can be pointed out that measured activation energies of 0.07 eV are, within experimental errors, that of boron in silicon and, as such, confirm that in this respect silicon crystallites in the films behave like bulk silicon.

In order to characterize the structure of the films at thicknesses comparable to p-layer thicknesses in operational devices, we deposited 150Å thick films and determined their crystallinity. Deposition times for these films were estimated from the deposition rates measured on thicker films on SnO_2 substrates prepared under identical conditions. Raman analysis of the films showed that on SnO_2-coated substrates the films had all amorphous character. On glass substrates, however, substantial crystalline fractions were observed. Considering the fact that deposition rates on glass substrates are generally lower than on SnO_2, the data indicate that on glass substrates c-Si phase forms at film thicknesses considerably less than 150Å. It can then be concluded that lack of crystallinity on SnO_2 coated substrates is not simply due to the small film thickness.

To substantiate this observation we deposited the same films on the same substrates but coated *in-situ* with a very thin (≈10 Å) SiO_x layer. Raman spectroscopic analysis of the films indicates the presence of c-Si phase in all cases but with a smaller c-Si peak width than for the films deposited on glass without SiO_x. This could possibly indicate that SiO_x film thickness was thick enough to provide a base for c-Si nucleation but not thick enough to suppress totally the effect of the underlying substrate.

Microcrystalline n-layers

A limited investigation of the microcrystalline n-layers deposited from SiH_4, H_2, and CO_2 found that they contained P doped c-Si imbedded in a matrix of a-SiO_x:H:C. The c-Si volume fractions and conductivities are higher than what is observed in the B doped microcrystalline p-layers.

The sensitivity of three commercially available textured SnO_2 substrate materials to H_2 plasma or annealing in H_2/Ar from 100-400°C was investigated using optical transmission and Hall effect measurements. With both types of H_2 treatments, the mobility of the SnO_2 having the lowest carrier density (<2 x 10^{20} cm^{-3}) doubles from ~30 to ~60 cm^2/V-s while the mobilities of SnO_2 materials having a higher carrier density were unaffected. There was no systematic change in carrier density with either treatment for any SnO_2. The visible transmission degrades significantly with H_2 plasma at 200°C, but it is unaffected by H_2/Ar annealing up to 400°C. Thus, it is possible to decrease the resistivity of bare SnO_2 by a factor of 2 without any loss of transmission using H_2/Ar annealing. A 20 nm layer of sputtered ZnO is sufficient to protect the

SnO_2 from plasma-induced damage while still allowing the factor of two improvements in SnO_2 mobility. Annealing in H_2/Ar or Ar is comparable and more effective than air, showing that there is both a chemical and thermal component to the improvement in mobility.

Minimizing the resistance between the p-layer and TCO of superstrate p-i-n a-Si devices and modules is a critical issue for utilizing new TCO materials like ZnO and new p-layers like μc-SiC or μc-SiO. However, characterization of the TCO/p interface is difficult since it is in series with the dominant p-i-n junction. We have developed two new methods to characterize the TCO/p contact and the SnO_2 sheet resistance in a completed device structure. Both require a-Si devices deposited on scribed TCO having individual cell contacts placed on each TCO strip. These methods were applied to devices made at BP Solar on different types of SnO_2 (Asahi, AFG, and LOF), different p-layer recipes, and with a thin ZnO layer on the SnO_2. The junction and contact properties are obtained from analysis of dV/dJ from each of several devices on the strip of TCO. Analysis of temperature dependent JV measurements using this special configuration can be used to determine the activation energy of the TCO/p contact resistance.

There was no significant difference in $R_{TCO/P}$ between SnO_2 or ZnO substrates, or with H_2 plasma treatments. The reason for poor V_{oc} and FF with ZnO must be found elsewhere. Instead, our analysis showed that the diode factor and recombination current increases with ZnO, especially with certain pre-deposition treatments.

A unique feature of these methods is the direct measurement of the JV characteristic of the TCO/p contact. No evidence for a blocking contact, a photovoltaic junction or a high resistance was found. Instead, ZnO changes the p/i junction recombination. Values of the contact resistance (R_C) of 1 ± 0.5 Ω-cm^2 were found for a wide range of TCO and p-layer processing, including ZnO. Temperature dependence of R_C gave barrier height of 40-55 meV. Analysis of devices with a thin ZnO layer on SnO_2 and with different predeposition treatments indicates lower V_{oc}, and FF observed with ZnO is not due to the contact but to changes in the p/i junction recombination. The solar cell performance is very sensitive to the ZnO surface treatment, but R_C is not. No evidence was found for a blocking or high resistance ZnO/p contact. The "ZnO/p" contact problem is not really due to the ZnO/p contact resistance or a barrier but rather to an increase in recombination.

Optical enhancement in a-Si solar cells is a well-known technique to increase the absorption efficiency of weakly absorbed light, and is critical for improving the performance of single or multijunction p-i-n or n-i-p devices. Optical enhancement increases the optical path length so that the device has an effective optical thickness of ($\boldsymbol{m}$d) where d is the physical thickness of the i-layer. The parameter $\boldsymbol{m}$ represents the increase in absorption length and is a measure of the optical enhancement for weakly absorbed light due to both oblique scattering and multiple passes. We have developed a quantitative analysis of the QE and applied it to a wide range of a–Si p-i-n solar cell device structures. The measured QE data at long wavelengths is fit with a simple, analytical model having one adjusted parameter, $\boldsymbol{m}$, as a function of wavelength. The experimental variables investigated include the i-layer thickness, d, from 0.14 to 0.92 μm, the SnO_2 texture (lightly textured LTX or highly textured HTX), and the back reflector (BR) structure (Al, ZnO/Al, or ZnO/AG).

Values of ***m*** are generally less than 1.5 with Al contacts on the LTX or HTX substrates for all device thicknesses studied here. This indicates a strong reduction in multiple passes due to the Al BR regardless of how textured the SnO_2 is. But ***m*** increases significantly with ZnO/metal contacts on HTX SnO_2 , saturating at ***m*** ~ 3 - 4. We found that the ZnO/Ag BR enhances light trapping more in thin devices compared to thicker ones. These results confirm the critical importance of a ZnO (or any other TCO buffer layer) between the Si and metal layers for improving optical enhancement of the QE. Besides gains in QE due to optical enhancement, we also considered the losses due to parasitic absorption. By comparing absorption in different simplified test structures with and without back reflectors, we conclude that the textured SnO_2 is responsible for a very significant fraction of the parasitical absorption. Absorption of about 50% of the light is unaccounted for beyond 800 nm with the HTX SnO_2. The most likely parasitic loss, as at long wavelengths, is light absorbed in the textured SnO_2. Critical angle trapping inside the SnO_2 will lead to multiple internal reflections or light piping in the SnO_2. This suggests that in a solar cell, light that is reflected from the BR but not absorbed in the i-layer can be trapped in the SnO_2, remaining there instead of re-entering the i-layer.

The hot-wire CVD of uniform Si films onto 1 in^2 7059 glass substrates was investigated. We studied the effects of silane flow rate (4-60 sccm), filament temperature (1550-1850^oC), total pressure (25-1000 mTorr), substrate temperature (400-600^oC) and hydrogen dilution on the exit gas-phase composition, film growth rate and film crystalline fraction. Experiments show that the growth rate increases with silane flow rate and is independent of substrate temperature. The growth rate variation with pressure and filament temperature is observed to change with the axial position of the substrates. A transition from amorphous to polycrystalline silicon films is observed with increasing total pressure, filament temperature and substrate temperature, and with decreasing silane flow rate. The effect of hydrogen dilution is found to be equivalent to the effect of increasing gas pressure using pure silane.

To explain these results, a quantitative model of the deposition of silicon films by HWCVD was developed. The model equations describe a vacuum reactor in which silane cracks over a series of heated tantalum wire reacts further in the gas phase and deposits to form Si films on glass substrates. The model considers gas motion in the form of diffusion in the reactor and incorporates surface pyrolysis reactions on the hot wire, gas-phase reactions, and film growth reactions on the substrates. The model predictions of silane conversion and silicon film growth rate are in good agreement with the experimental results over the range of conditions studied. This study shows that a critical ratio of atomic hydrogen flux relative to the total flux of growth precursors is required at the film surface in order to effect a transition from amorphous to polycrystalline silicon films. The flux ratio of atomic hydrogen radical to growth precursors is controlled by the pressure, filament temperature and silane flow rate. For the conditions investigated, a flux ratio greater than 15 leads to the deposition of polycrystalline silicon films.

One of the critical issues in the development of thin film silicon devices is the grain size. Typically, films deposited by HWCVD exhibit grain sizes between 10-50 nm. It is expected that the excessive number of grain boundaries in such films will lead to considerable carrier recombination and poor device performance. During this contract, we have focused on the evaluation of various *in-situ* and post-treatment methods, which can be used to fabricate films with micrometer size grains. The core idea in all these approaches is the process of metal induced crystallization (MIC) by which a-Si undergoes crystallization when in contact with

metals such as Al, Ni and Sb at temperatures as low as 200°C. In one approach, we investigated the use of RTP MIC in collaboration with Ajeet Rohatgi at Georgia Institute of Technology. Although only preliminary, results in this study do not show grain enhancement in the films. We have also investigated the use of *in-situ* approaches, which leads to grain enhancement during the HWCVD process. The work has concentrated on the use of Al and Sb layers as the catalysts for grain enhancement and crystallization. We have studied two temperature regimes, i.e., temperatures above and below the Al-Si eutectic temperature 575°C. In the first case, films have a tendency to delaminate from the substrate. This is caused by poor wetting characteristics of the metal layer on the glass substrate at the processing temperature. For the lower temperature regimen, uniform films have been obtained. These films do not contain Al contamination and have a columnar structure with a diameter in the micrometer range. Characterization after polishing to reveal grain boundaries indicates the grains have a micrometer size width as far as the interface with the Al layer.

Si Team Participation

IEC is a member of the National a-Si Team under the Thin Film Partnership Program. Steve Hegedus had been the leader of the Multijunction Device sub-team for 8 years and stepped aside last year. The work on characterization of the TCO/p contact resistance was performed as part of the Teaming activities in collaboration with BP Solarex. Results from this work have lead BP Solarex to develop new TCO/p materials and processes. During this contract period, IEC collaborated with: Gautam Ganguly at Solarex, by characterizing the TCO/p contact resistance on their sub-modules having different textured SnO_2; Bhushan Sopori at NREL, by fabricating back reflector structures on textured TCO/a-Si substrates for analysis by PVOPTICS; Prof. Roy Gordon at Harvard University, by characterizing ZnO films deposited there by APCVD and fabricating a-Si pin devices on those films for comparison to standard SnO_2 substrates; and Prof. Eric Schiff at Syracuse University, by providing him with special TCO/i-n device structures for electroabsorption measurements. These teaming collaborations lead to co-authoring one publication at the Spring 2000 Materials Research Society Conference and two at the 28th IEEE Photovoltaic Specialists Conference.

CdTe-BASED SOLAR CELLS

CdTe-CdS Interdiffusion and Post-Deposition Processing

Chemical and kinetic aspects of thin-film CdTe/CdS solar cell processing have been analyzed and provide a framework for variation and failure analysis and control of large-area cells in modules. In particular, controlling CdS thickness and CdTe grain properties during growth or post-deposition treatments will become more critical as CdS and CdTe film thickness are reduced; the analysis shows that 'tolerant' processing windows exist for fabricating efficient cells in the low-limit of semiconductor film thickness.

The CdTe-CdS phase system has been quantitatively analyzed in thin-film structures and has been shown to conform to the equilibrium system for CdTe-CdS mixed crystals. The miscibility gap for the CdTe-CdS pseudobinary system was investigated in the temperature range used to process thin-film solar cells, i.e., from 360°C to 700°C. Metastable single-phase $CdTe_{1-x}S_x$ alloy thin films with composition near the middle of the alloy range, x~0.4, were deposited by thermal

evaporation. Thermal treatment in a kinetically enhancing ambient resulted in segregation of the equilibrium alloy phases. Analysis of the resulting x-ray diffraction patterns yielded precision lattice parameters, hence composition, of the Te-rich zincblende and S-rich wurtzite phases. The *T-x* phase boundaries were found to be asymmetrical and were modeled using non-ideal solution thermodynamics. The empirical and modeled phase boundaries provide the fundamental basis for investigation of interdiffusion between CdTe and CdS.

Analysis of superstrate and substrate CdTe/CdS structures with CdTe deposited at low temperatures has allowed chemical and thermal effects to be de-coupled. The effects of the observed phenomena on thin-film polycrystalline CdTe/CdS device operation can be summarized as follows. CdS diffusion into CdTe reduces the CdTe bandgap slightly, lowering the built-in voltage. This is offset by a slight increase in long wavelength quantum efficiency. CdS thickness is reduced, which increases light generated current due to greater absorption of short wavelength photons in CdTe. However, non-uniform CdS consumption can lead to poor overall junction behavior by the formation of a sufficient number of parallel junctions between CdTe/TCO and CdTe/CdS. This problem can be ameliorated by modifying the CdS growth habit and introducing high resistance oxide layers between CdS and the TCO. The effect of bandgap variations parallel to the junction interface is still not understood.

By comparing films deposited by different techniques used to obtain solar cell efficiencies in the 11 to 12% efficiency range, it is shown that film morphology *per se* is not an efficiency-limiting parameter for films with grains from 0.2 to < 2 microns in lateral dimension. We have shown that in PVD films, the $CdCl_2$ treatment causes grain growth by a coalescence process. However, it seems that devices with CdTe films having sub-micron grains can benefit from the growth of penetrating oxides which electrically passivate grain boundaries and kinetically reduce CdS consumption during treatment with $CdCl_2$ and O_2. High conversion efficiencies are still restricted to cells with CdTe deposited by CSS in oxygen-containing ambient. A negative consequence of oxide formation on the CdTe surface is the need for aggressive chemical treatments to allow low resistance contacts to be formed. Residual oxygen in grain boundaries may play a significant role in controlling grain boundary diffusion of contact-related species such as contaminants and dopants. The dependence of the limiting diffusivities for CdS diffusion into CdTe on temperature and ambient composition in thin-film couples have been determined, yielding activation energies for bulk and grain boundary diffusion processes. The bulk diffusion appears to be limited by the Cd self-diffusion, while the boundary diffusion is chemically limited. Intra-grain recrystallization proceeds more rapidly than grain growth, which proceeds more rapidly than CdS diffusion, even in films without oxides. The observed benefit of high temperature growth or high temperature anneal strongly suggests that grain quality is of paramount importance to obtaining high junction quality.

Window Layer Processing

Options for window layer processing were evaluated, with emphasis on development of high resistance transparent (HRT) oxide layers and improved CdS film quality. Resistive oxide SnO_2, In_2O_3, and Ga_2O_3 films were formed by oxidizing metal films, Sn, In, and Ga, respectively, in air at 400°C-500°C. Incorporation of these layers between the TCO and the CdS film allows junction quality to be similarly maintained for devices with d(CdS) < 100 nm.

A new method for chemically depositing CdS films with very high utilization of cadmium species was developed and has been submitted for patent review. The method, called chemical surface deposition (CSD), yields conformal CdS films with >70% cadmium utilization and low pinhole and particulate occurrence, contributing to process robustness. It was also demonstrated that CSD $Cd_{1-x}Zn_xS$ films may be used in lieu of a CdS/HR combination to simplify processing and retain junction quality while obtaining high photocurrent.

Contact Processing and Stress Analysis

At the beginning of this contract, it was already well established that the contacting of CdTe is problematic and the details of the contact were crucial to obtaining a high performance device. There were suggestions that the contact process and structure can influence the stability under accelerated stress conditions and that the electrical bias during stress was important to understanding the degradation. Therefore, we established a contact fabrication process which allowed us to separate and control various aspects of the contact process, such as removing oxides on the CdTe surface, formation of the Te layer, applying Cu and reacting it to form Cu-Te alloys, and forming a robust current carrying contact. We separated these features into the primary and secondary contacts. The primary contact may contain Cu-Te alloys and makes intimate contact to the CdTe. The secondary contact is typically a thick layer of C, Mo, Ni or Al and carries the current to the external connections. We also built a system for accelerated stressing of thin film PV devices under controlled atmosphere, temperature, bias, and light conditions, and used it to stress a large number of CdTe devices with a variety of contact structures. The glass/SnO_2/CdS/CdTe plates for these contacting and stress studies were obtained from First Solar, L.L.C.. The CdS and CdTe were evaporated. The 4 μm thick CdTe received a $CdCl_2$ treatment at First Solar. Thus, devices were fabricated using CdS/CdTe material from First Solar with back contact processing at IEC. Given the well known sensitivity of CdTe device performance and degradation to the back contact, these results on hybrid FS/IEC devices do not quantitatively reflect the behavior of First Solar devices with their own contact process.

CdTe cells have been stressed for 10-30 days at 60-100°C under ~1 sun light and in dark. Ambient conditions have included dry (bottled) air, H_2/Ar and Ar. Of critical importance is the bias applied to the cell during stress. Various bias points have been studied: short circuit (SC), maximum power (MP), open circuit (OC) as well as –1V and +2V. Variations in cell processing has included the Cu thickness (0-15 nm), wet or dry surface treatment, various secondary contacts (C paste, Ni, and Mo). In general, we focused on the effect of bias during stress and the effect of the contact process on initial and post-stress performance. A variety of JV analysis methods were applied to gain further insight into device mechanisms in the initial and degraded states.

We have shown that devices degrade in both illumination and dark conditions during stress, and even at temperatures as low as 60°C. Devices biased at SC, or 0V in the dark, were more stable than those at forward or reverse bias. This highlights a crucial observation which must be accounted for in developing a model, namely that the degradation is non-monotonic with bias. Degradation increases with increasing forward bias, at least up to 2.5V. Devices without Cu degrade much less, especially at forward bias. There is little difference between devices where the pre-contact treatment of the CdTe was a wet or dry process, providing that the Cu thickness

was optimized for each process. Considerable variability has been found for nominally similar devices under similar stress conditions. Devices stressed at 0V for 10 days at 100°C can degrade as little as 2-3% or as much as 20%. Given the excellent control over the stress conditions, we attribute the variability to unintentional differences in the CdS/CdTe starting material or the lack of reoptimization of the contact for different starting material properties.

Initial performance is very similar for devices with the wet or dry surface process, independent of Cu thickness. Initial V_{oc} was 0.80±0.02 V and initial FF was 69±2% for all devices except ones without Cu. After stress, devices without Cu having the wet contact have higher V_{oc} than devices with Cu, despite starting with a lower initial V_{oc}. But we found no strong dependence of either solar cell performance (V_{oc}, FF, J_{sc}) or device properties (A, J_o, space charge, R_s) on Cu concentration (2-15 nm) or the contact process. These results demonstrate significant degradation occurs independent of the amount of Cu for both of the contact processes. Although we observed that devices with the dry contact process tend to have less "roll over" or curvature in forward bias after stressing, they had no significant difference in FF. This suggests the wet contact enhanced the formation of the blocking contact despite its having consistently a slightly higher FF after stress. The two key differences between the dry and wet process are that the dry process leaves a thinner Te layer and is less penetrating along grain boundaries. It is not known yet how these differences are responsible for the differences in blocking contact formation.

The effect of the secondary contact was unexpectedly large. Mo and Ni required thicker Te layers (110 nm vs 10 nm) to achieve even moderate device performance. Thicker Te was collarated with better intial and degraded performance with all secondary contacts. Devices with C have higher initial J_{sc} and V_{oc} compared to devices with Mo or Ni. We have no explanation for this. All three secondary contacts were relatively stable without a Cu layer.

Analysis of the J(V) characteristics indicates that the junction recombination is a Schockley-Read-Hall (SRH) mechanism. Evidence includes A values between 1.5 and 2.0, $V_{oc}(T)$ values extrapolated to T = 0K equal to the CdTe bandgap, and the temperature dependence of J_o giving an activation energy near mid-gap of CdTe. This suggests that deep centers in the CdTe, whose concentration increases with stress are responsible for the recombination limiting V_{oc}.

Losses in V_{oc} and FF occur within the ~1 week stress time used in this study while stressing for longer times enhances the formation of the blocking contact. We developed a method to recontact devices after stress, and found that losses in V_{oc} and FF are independent and separable. Recontacting cells after stress may eliminate the roll-over and partially recover some of the FF loss but there is no recovery in V_{oc}.

Since even devices without any Cu layer show degradation, other non-Cu related degradation mechanisms must be identified and solved. Before stressing, low V_{oc} and FF result without Cu doping layer, consistent with our previous results using both SCI/FS CdTe material. Degradation in V_{oc} for these "Cu free" devices is much less (~0.06 V) than typically found for devices with Cu layer. The relatively smaller loss in V_{oc} after stressing is independent of the contact processing or surface etch. However, severe degradation in FF occurs even without Cu. Devices without the BDH etch show extreme distortion of the JV curve, suggesting formation of a blocking contact is suppressed with sufficient Cu or Te, consistent with maintaining a p+ surface. The changes in J-V behavior due to stress suggest changes in non-copper doping

sources such as oxygen, chlorine, and excess Te. Devices with insufficient Cu dopant will be more susceptible to presence of other doping species, which may be less well controlled.

We collaborated extensively with First Solar LLC, who provided most of the bare CdS/CdTe plates on which contact and stress analyses were conducted. Extensive collaborations were also conducted with BP Solar with respect to film morphology, structure and chemical composition. We performed stresses on their own completed devices to determine temperature and ambient dependence as well as assist them in evaluating stability of different back contact processes. In general, we found no dependence of stability on the ambient (air, H_2.Ar, or Ar). We found some dependence on temperature, with degradation increasing as the stress temperature increased from 60 to 100°C.

Teaming Activity

IEC researchers participated in the National CdTe R&D Team, attended and made presentations at team meetings. Collaborations within the team activity consisted of device fabrication, device stressing, performing electrical and physical characterization of films and devices, and exchange of technical progress. In addition, thin-film samples were provided to various team members. IEC participated in the First Solar focus group and provided film characterization, device analysis, and interpretation of SIMS measurements made at NREL. Direct interaction between IEC and BP Solar yielded a fruitful collaboration in which processing developments at IEC such as post-deposition treatments and incorporation of HR layers were successfully incorporated into the Apollo line, resulting in significant performance gains.

TRAINING AND EDUCATION

During the period of this subcontract (August 24, 1998 to October 23, 2001) IEC provided training and education for the following: 10 visiting professionals; 11 post-doctoral fellows/limited term researchers; 18 graduate students; and 16 undergraduate students. Names are given in the list of contributors.

PUBLICATIONS

As a result of research performed under this subcontract reporting period, IEC published 34 papers, as shown in Appendix 1.

ORGANIZATION OF THE REPORT

This report is organized into three technical sections: $CuInSe_2$-based solar cells, Si-based solar cells, and CdTe-based solar cells. Each section describes the progress made at IEC in addressing the critical issues discussed above during the period of this subcontract.

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1. INTRODUCTION

1.1 $CuInSe_2$-based Solar Cells

Most efforts to manufacture $Cu(InGa)Se_2$ or related thin films for commercial modules utilize formation of the $Cu(InGa)Se_2$ films by either multisource evaporation or selenization of metal precursor films in either Se or H_2Se. For either process to become a commercially viable technology, manufacturing costs must be reduced. In-line evaporation is a promising approach to reduce manufacturing costs by enabling uniform deposition over a large area with high substrate throughput and good composition control. The in-line process involves the linear translation of a heated substrate over an array of sequential evaporation sources, which are designed to give uniform deposition perpendicular to the direction of translation. However, the design and control of this process and its effect on the resulting thin films are not well documented.

Another means to reduce processing costs is by reducing the substrate temperature at which the $Cu(InGa)Se_2$ layer is deposited to make substrate handling simpler and reduce thermal stress on the entire deposition system. Soda lime glass is typically used as the substrate for high efficiency $Cu(InGa)Se_2$ solar cells, but it deforms at the temperatures used for the highest efficiency devices, 550 – 600°C. It is not well understood why the high processing temperatures are needed to process these cells. With temperature reduced to ~400°C alternative substrate materials, like a flexible polymer, could be utilized. These materials could then be incorporated into an in-line process using a roll-to-roll configuration.

$CuInSe_2$ has a bandgap of 1.0 eV and the devices typically have V_{oc} less than 0.5V. The highest efficiency cells have bandgaps of about 1.2 eV through the addition of gallium to form $Cu(InGa)Se_2$. It is desirable to further increase the bandgap to reduce module-related losses. The addition of sulfur and aluminum has also been used to increase the bandgap. In addition, sulfur could be used to form a $CuIn(SeS)_2$ layer with a graded bandgap near the device interface to increase V_{oc}. A fundamental scientific and engineering basis of sulfur incorporation into $CuInSe_2$ is needed for the fabrication of homogeneous and compositionally graded $CuIn(SeS)_2$ thin films.

1.2 a-Si:H-based Solar Cells

Amorphous silicon (a-Si) PV modules were the first thin-film PV modules to be commercially produced and are presently the only thin-film technology that has an impact on the overall PV markets. However, the efficiencies of these modules have not yet reached the levels that were predicted in the 1980s. To a significant degree this is due to the intrinsic degradation of a-Si under illumination. The amount of light-induced degradation can be limited to 20% in modules operating under prevailing outdoor conditions. The use of multijunction devices (allowing the use of thinner absorber layers in the component cells) and the use of light-trapping appear to be the most powerful device design schemes to improve stabilized device performance.

The US industry currently uses two approaches to build a-Si-based modules. The substrate type devices are built on stainless steel foil. The superstrate devices are built on glass coated with

TCO. Presently, all superstrate devices use an a-SiC p-layer while substrate devices use a "μc–Si" p-layer, which is, in fact, a mixture of a-Si and μc-Si phases. Fabricating devices with p-layers having wider bandgaps and higher conductivity is expected to lead to higher V_{oc} and higher blue response, hence J_{sc}. Further, such highly conductive and transparent layers will reduce electrical and optical losses at the n/p interconnect junction of multijunction devices. Thus, improvements in p-layers would benefit both superstrate and substrate device technologies, in either single or multijunction configurations.

Another approach to low cost Si-based PV modules involves the deposition of thin films (<20 μm) of large grain (>1 μm) polycrystalline Si on low cost substrates. This requires high growth rates and the ability to form large grains either directly or in post-deposition processing.

1.3 CdTe-based Solar Cells

Fabricating high efficiency CdTe/CdS superstrate devices when using ultra-thin CdS window layers presents a difficult technical challenge because of the coupled nature of the processing steps and of the interaction between CdS and CdTe films. We and others have shown that simply reducing CdS thickness to reduce parasitic absorption does not lead to the expected increase in performance, since the junction quality is found to progressively deteriorate (as measured by a loss in V_{oc} and FF) as final CdS thickness in the device is reduced below 100 nm. The extent of this phenomenon is: 1) process specific; 2) more serious for processes in which the CdTe layer is deposited at temperatures below 400ºC; and 3) related to consumption or even disappearance of a continuous CdS layer. In addition, reducing CdS thickness exposes the TCO/glass materials to interaction with the chemical treatment ambient, which can result in loss of adhesion or contamination. The loss of CdS due to diffusion into CdTe is dominated by the grain boundary diffusion. Incorporating S uniformly into the CdTe lattice at concentrations below the solubility limit does not have a deleterious effect on the junction quality. Improving the $CdTe_{(1-x)}S_x$/TCO junction quality for CdTe devices with ultra-thin CdS has been facilitated by use of a high resistance layer between the TCO and CdS films.

There are also serious problems to be solved at the other end of the device, namely the CdTe contact. The back contact consists of a primary contact, in intimate contact with the CdTe and often containing Cu-Te compounds, and a secondary contact, which is the external current carrying conductor. Prior to forming a low resistance primary contact to CdTe, the surface must be modified to remove oxides and residues and produce a Te-enriched layer. Nearly all contacting schemes follow this step with application of a copper-containing contact or copper layer and a heat treatment. Analysis of the resulting surface reveals that low resistance contact operation is facilitated by formation of a very thin Cu_2Te layer between CdTe and the secondary contact. Processing which allows for independent control and variations in the primary and secondary contact will be useful in identifying mechanisms of degradation.

2. $CuInSe_2$-BASED SOLAR CELLS

2.1 Effect of Deposition Temperature on $Cu(InGa)Se_2$ Films and Devices

2.1.1 Introduction

For $Cu(InGa)Se_2$ based solar cells to achieve their promise for low cost photovoltaic power generation, manufacturing costs need to be reduced while maintaining high yield, reproducibility, and performance. Lowering the processing temperature for the $Cu(InGa)Se_2$ can reduce costs and increase yield by decreasing the heat load and stress on the deposition system and by allowing faster heat-up and cool-down. The highest efficiency solar cells utilize $Cu(InGa)Se_2$ deposited at substrate temperatures (T_{SS}) greater than 550°C onto soda lime glass which softens at such temperatures. This could create significant problems when handling large area substrates for module manufacturing. In addition, if T_{SS} is reduced to ~400°C, high temperature polyimide could be used as a substrate enabling roll-to-roll processing with subsequent monolithic integration of cells to fabricate modules.

We have previously shown a decrease in $Cu(InGa)Se_2$ device efficiency from 16.4% to 14.1% due to decreasing the substrate temperature during evaporation from 550 to 400°C [4]. The most significant change in the $Cu(InGa)Se_2$ films deposited at lower T_{SS} was a smaller grain size. Other groups have also shown a simultaneous decrease in efficiency and grain size with lower T_{SS} using an in-line evaporation process [5] and with a three stage evaporation process which begins with an In-Ga-Se layer [6]. In this work, changes in $Cu(InGa)Se_2$ films and devices are characterized as a function of substrate temperature to determine the causes for the drop in device performance as T_{SS} is reduced.

2.1.2 Experimental Details

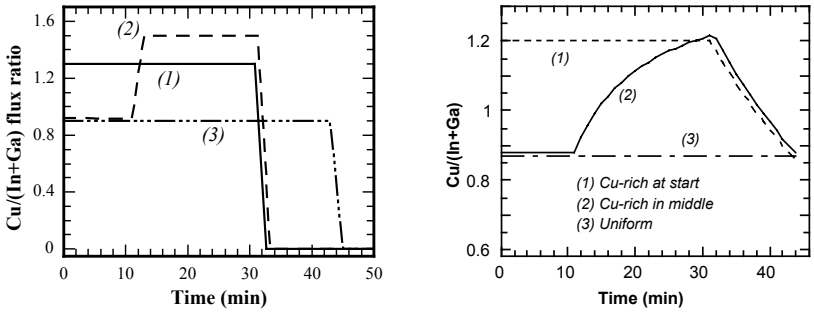
$Cu(InGa)Se_2$ films were deposited by thermal evaporation from independently controlled elemental sources for Cu, In, Ga, and Se. Three flux versus time profiles were used to give depositions with: (1) Cu-rich flux, Cu/(In+Ga) > 1, at the start of the run followed by only In, Ga, and Se fluxes to give the desired Cu-deficient final composition, (2) Cu-rich flux in the middle of the run, and (3) uniform fluxes so that the films composition is never Cu-rich. The Cu/(In+Ga) flux and integrated Cu/(In+Ga) ratios in the films as a function of time through the deposition are shown in Figure 1 for these three processes. This illustrates the fact that the endpoint compositions were the same in all cases. The process with the Cu-rich flux in the middle is intended to determine if the effects of Cu-rich growth specifically require the presence of a Cu_xSe_y phase during the initial nucleation of the film on the glass/Mo substrate. The In, Ga, and Se fluxes were kept constant throughout each deposition so there were no gradients in Ga content or bandgap, and were the same for each flux profile and substrate temperature. Auger electron spectroscopy depth profiles show that the composition is roughly uniform through the thickness of all the films. This is shown for films deposited by each of the three processes in Figure 2 at T_{SS} = 480°C. In each case, there is a small decrease in the relative Cu content near the surface which is probably due to the formation of a Cu-poor ordered vacancy phase.

The deposition time for all films was 44 min resulting in final film thicknesses of 2 - 2.5 μm. Film compositions, measured by energy dispersive x-ray spectroscopy (EDS), were Cu/(In+Ga) = 0.8 – 0.9 and Ga/(In+Ga) ≈ 0.3, giving a bandgap E_G = 1.2 eV. For this work, Cu(InGa)Se_2 films were deposited at T_{SS} = 400, 480, and 550°C with constant T_{SS} through each deposition. At 480°C the soda lime glass substrate is below all glass transition temperatures.

Film morphology was characterized by scanning electron microscopy (SEM) and atomic force microscopy (AFM). In addition to EDS, composition was characterized by Auger electron spectroscopy (AES) and secondary ion mass spectroscopy (SIMS). The AES and SIMS measurements were done at the National Renewable Energy Laboratory. Finally, x-ray diffraction (XRD) was used to measure crystallite orientation of the films.

Devices with a soda lime glass / Mo / Cu(InGa)Se_2 / CdS / ZnO:Al / Ni-Al grid structure, with no anti-reflection layer, were fabricated using IEC's baseline processing. In this processing, the substrate is 1.5 mm thick float soda lime glass coated on the non-Sn side with 0.7 – 1.0 μm thick Mo deposited by dc sputtering. The Mo film has sheet resistance R_{sq}= 0.15 – 0.2 Ω/sq. After Cu(InGa)Se_2 deposition CdS is deposited by chemical bath deposition with thickness ~ 40 nm. Then a bi-layer ZnO film is deposited by rf sputtering from a compound ZnO:Al_2O_3 target with 2% Al_2O_3 by weight. The first layer was deposited with a sputter gas composition of Ar/O_2(2%) to give a 50 nm thick layer with resistivity ρ ≈ 20 Ω-cm. This was followed by a layer deposited with a sputter gas composition of Ar/O_2(0.2%) to give a 500 nm thick layer with a sheet resistance of 15 Ω/sq or ρ ≈ 8x10^{-4} Ω-cm. Electron beam evaporation was used to deposit Ni/Al grids with ~4% shading loss. The devices did not have an anti-reflection layer. Cell areas were delineated by mechanical scribing to give individual cells with area 0.47 cm^2.

Characterization of the devices included the total area current-voltage (J-V) response measured at 25˚C under 100 mW/cm^2 AM1.5 illumination and quantum efficiency (QE) measured under white light bias as a function of voltage bias.



(a) (b)

Figure 1. Schematic representation of three temporal flux profiles (a) and integrated relative Cu concentration in films (b) during deposition with different Cu(InGa)Se_2 evaporation flux sequences.

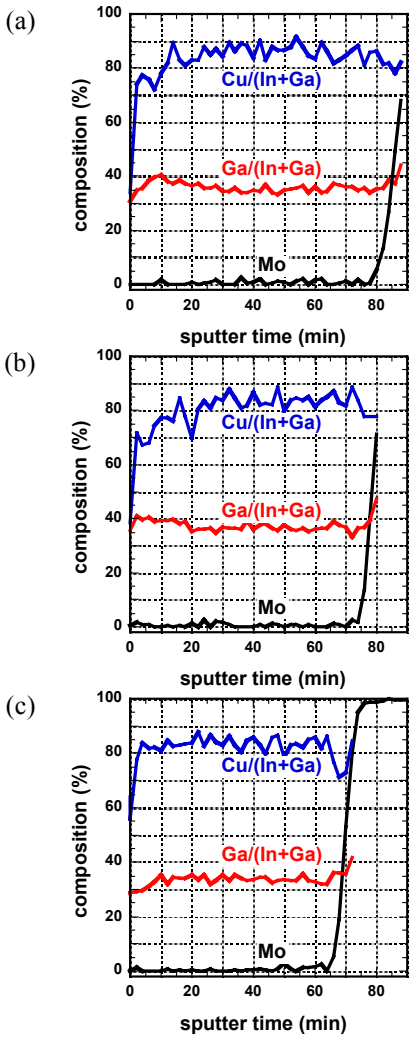


Figure 2. Compositional ratios Cu/(In+Ga) and Ga/(In+Ga) determined from AES depth profiles for films deposited at T_{ss} = 480ºC with, (a) Cu-rich flux in the beginning of the deposition, (b) Cu-rich flux in the middle of the deposition, and (c) uniform flux.

2.1.3 Results

2.1.3.1 Grain Size and Morphology

SEM cross-sectional micrographs of films grown with Cu-rich flux at the start and with uniform flux at T_{SS} = 400 and 550°C are shown in Figure 3. The films grown at T_{SS} = 550°C have larger grains than those grown at 400°C. At the lower temperature, the uniform flux process appears to give more columnar grains and a smoother surface. There are no apparent differences between films grown with the Cu-rich flux at either the beginning or middle of the deposition. In general, it is not possible to quantitatively characterize the grain size and morphology from these images.

For quantitative analysis, the films have characterized by AFM. The surface morphologies of films grown at T_{SS} = 400, 480, and 550°C with a Cu-rich flux at the beginning of the deposition

are shown by AFM images in Figure 4. The surface roughness appears to decrease as grain size gets larger with higher temperature.

AFM images of the top surface were used to determine the lateral grain size. These are shown in Figure 5 for the films grown with a Cu-rich flux at the beginning at each temperature. Again, the higher T_{SS} clearly gives larger grains, while the lower T_{SS} gives a more faceted morphology. The grain size is quantitatively characterized by the area of the grains observed in the AFM images for films deposited with the three processes described above and at the three substrate temperatures. This characterization uses contrast-enhanced AFM images of the planar view of the top surface to create a map of the grain boundaries [4] as shown in Figure 6. This map is then and the enclosed grain areas are determined using NIH Image software [7].

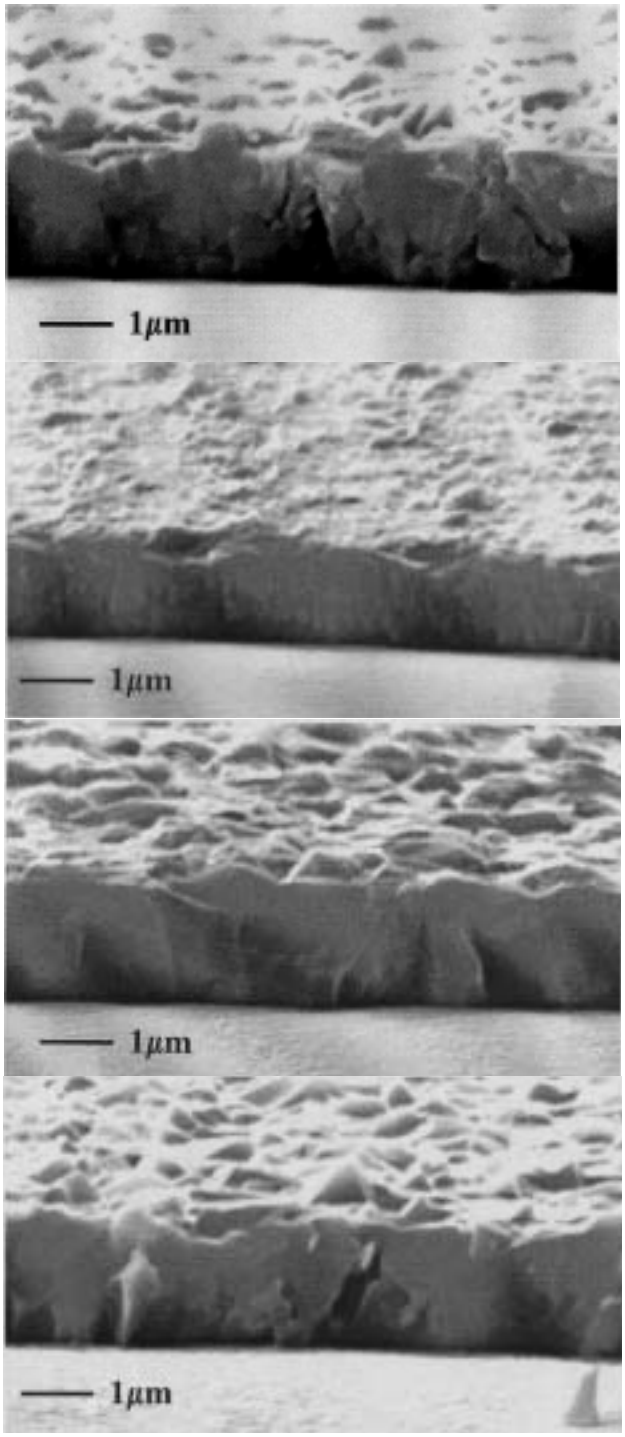
For each sample the lateral grain areas were determined over 3 randomly selected 100 μm^2 regions. In all cases the grain areas (A) are well described by a log-normal distribution, i.e., a normal distribution of the logarithm of A [8]:

$$f_n(lnA) = \frac{1}{\sigma(lnA)\sqrt{2\pi}} \exp\left[-\frac{(lnA - E(lnA))^2}{2\sigma(lnA)^2} \right], \quad (1)$$

where E(*ln*A) is the expected value or mean of *ln*A and σ(*ln*A) is the standard deviation of the distribution. The mean grain area, $\overline{A}$, and length, $\overline{d}$, are given by:

$$\overline{A} = E(A) = \exp\left[E(lnA) + \tfrac{1}{2}\sigma(lnA)^2\right] \quad \text{and} \quad \overline{d} = \sqrt{\tfrac{4}{\pi}\overline{A}} \ . \quad (2)$$

These are weighted grain size measures since the probability of finding grains of a given area is proportional to the relative area rather than just the number of grains. Figure 7 shows the measured grain area distributions and log-normal fits for the samples deposited at different T_{SS}. The parameters which describe the distribution, E(*ln*A), σ(*ln*A), and $\overline{A}$ are listed in Table 1 for all processes and temperatures along with $\overline{d}$ which can be compared to the length typically observed in cross-sectional electron microscope images.



400°C
Cu-rich at
beginning

400°C
Uniform deposition

550°C
Cu-rich at
beginning

550°C
Uniform deposition

Figure 3. Cross-sectional SEM micrographs of Cu(InGa)Se_2 films deposited with different flux profiles at T_{SS} = 400 and 550°C.

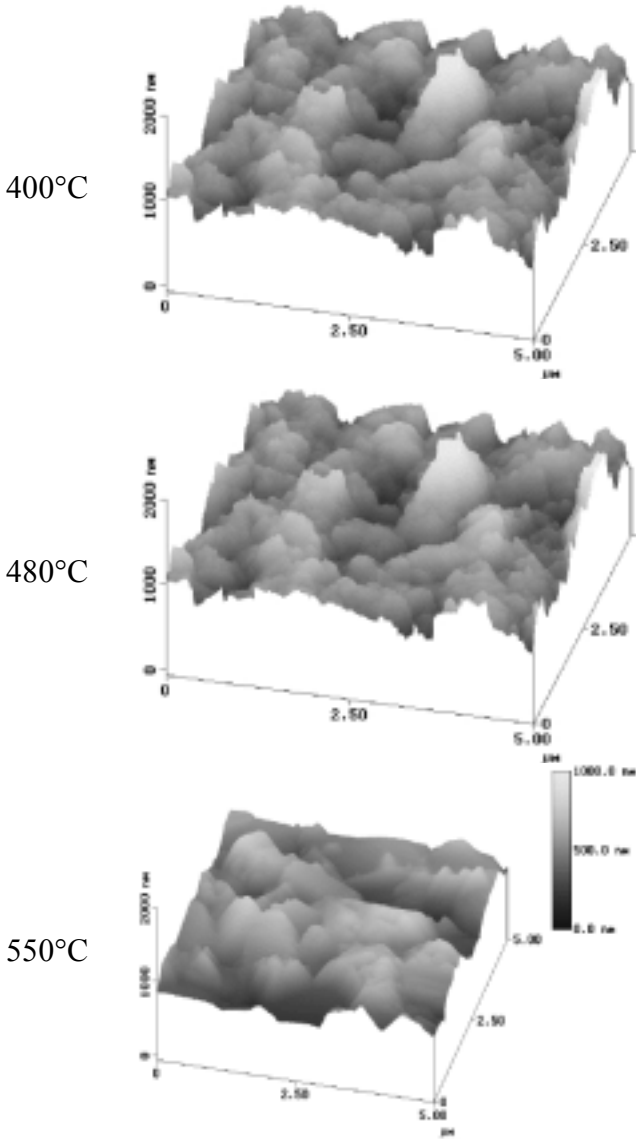


Figure 4. AFM images showing 5µm x 5µm areas of films deposited with Cu-rich flux at T_{SS} = 400, 480, and 550°C.

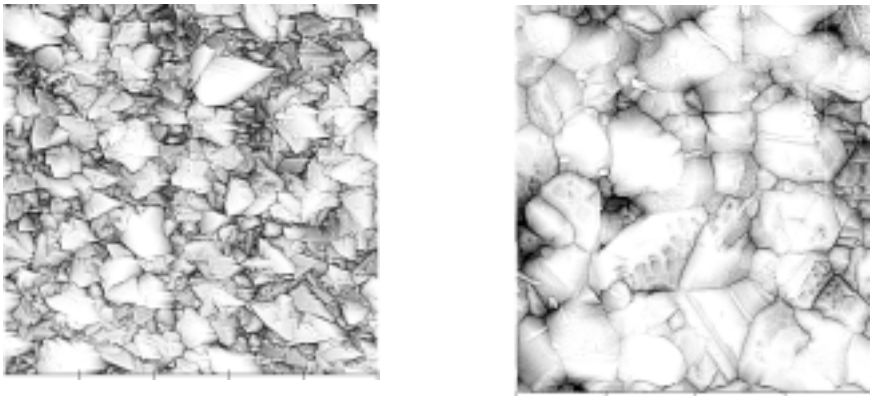


Figure 5. AFM images of the top surface of films deposited with a Cu-rich flux at the beginning of the deposition. Each figure shows a 10 µm x 10 µm area.

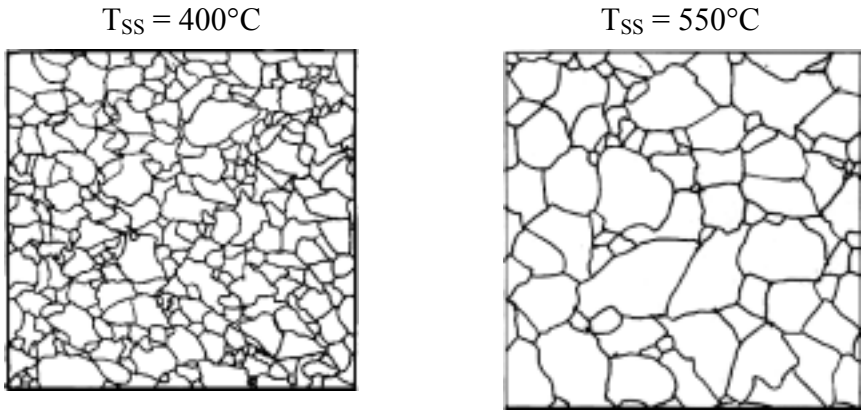


Figure 6. Grain boundary maps created from the AFM images in Figure 5.

In Figure 7 it can be seen that the median, or mid-point, of the log-normal distribution, is the same for the films deposited at the two higher temperatures. However, the film at 550°C has a larger mean area, 1.8 μm^2, due to the larger standard deviation and greater number of grains with $A > 1\ \mu m^2$ which dominate the distribution. For T_{SS} = 550°C, the mean area is larger with Cu-rich growth than with the uniform process. With T_{SS} = 400 and 480°C, the mean grain size is independent of the growth process.

The surface roughness is important because the open circuit voltage in a device is a function of junction area, as addressed below. The surface roughness is characterized by $\Delta A_{surf} = (A_{surf} - A_{\perp})/A_{\perp}$ where A_{surf} is the total surface area and $A_{\perp}$ the planar area. Experimentally, A_{surf} was determined from AFM measurements over an area $A_{\perp} = 100\ \mu m^2$. This is also listed in Table 1.

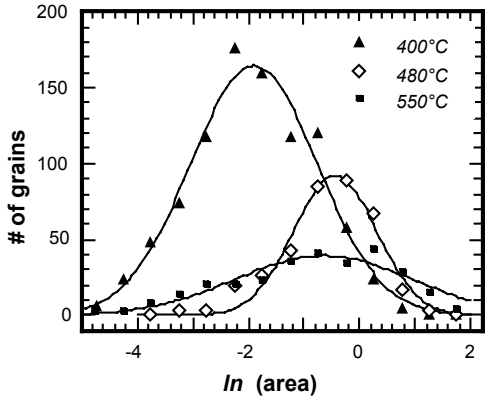


Figure 7. Grain size distributions for Cu(InGa)Se_2 films deposited with Cu-rich flux and log-normal fits to each distribution.

Table 1. Grain size and surface area with different deposition processes and temperatures.

T_{SS} (°C)	Process	E(*ln*A)	σ(*ln*A)	$\overline{A}$ (μm^2)	$\overline{d}$ (μm)	ΔA_{surf} (%)
400	Cu-rich at start	-1.9	1.1	0.3	0.6	54
	Cu-rich in middle	-1.9	1.2	0.3	0.6	76
	Uniform	-1.9	1.1	0.3	0.6	28
480	Cu-rich at start	-0.7	1.0	0.8	1.0	23
	Cu-rich in middle	-0.9	1.0	0.7	0.9	40
	Uniform	-0.4	0.7	0.9	1.0	32
550	Cu-rich at start	-0.7	1.6	1.8	1.5	26
	Cu-rich in middle	-0.6	1.2	1.2	1.1	33
	Uniform	-1.0	1.1	0.7	0.9	19

Finally, XRD measurements did not show any significant difference in the film orientation for different processes or temperatures. All the films had nearly random orientation, as has been found for films deposited on (110) oriented Mo films [9].

2.1.3.2 Sodium Incorporation

Depth profiles of the total Na content, measured by SIMS, are shown in Figure 4 for samples deposited at T_{SS} = 400 and 550°C using Cu-rich flux at the beginning or uniform flux. The films deposited at 400°C have greater average Na concentrations than those deposited at higher T_{SS}. Thus, improved device performance with increased T_{SS} cannot be explained by greater availability of Na.

Films with smaller grain size or a greater density of grain boundaries may have greater average Na concentration since nearly all the Na probably resides along those boundaries [10]. However, it is not clear why the films deposited at T_{SS} = 400°C with different processes but comparable grain size have the different Na concentrations shown in Figure 4.

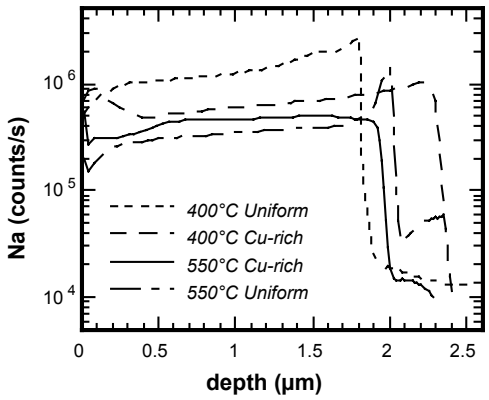


Figure 8. Sodium content measured by SIMS in Cu(InGa)Se_2 films deposited at T_{SS} = 400 and 550°C.

2.1.3.3 Device Results

Current-voltage (J-V) parameters for the best cells fabricated with T_{SS} = 400, 480, and 550°C and the three deposition processes are listed in Table 2. V_{OC} and FF increase with T_{SS} for all three deposition processes. The uniform deposition process gives poorer device performance at T_{SS} = 400°C than the Cu-rich growth processes despite the comparable grain sizes in the films. At higher temperatures, 480 and 550°C, there is no advantage to the Cu-rich growth even with increased grain size at 550°C.

The J-V curves under illumination and in the dark are shown in Figure 9 for the cells deposited with Cu-rich flux at the start. To further characterize the losses as T_{SS} is reduced, the J-V data was analyzed assuming a standard diode equation:

$$J = J_o \exp\left[\frac{q}{nkT}(V - R_S J)\right] - J_L \qquad (3)$$

The diode quality factor, n, and series resistance, R_S, were determined from the slope and intercept, respectively, of the derivative dV/dJ vs. $(J+J_{SC})^{-1}$ as shown in Figure 10. Then the recombination current, J_O, was determined from the intercept of $ln(J+J_L)$ vs. $V-R_SJ$. This plot is shown in Figure 11 for the data with T_{SS} = 400 and 550°C. With the lower T_{SS}, there is a difference between the data measured in the dark and the data under illumination which can be attributed to a voltage dependent light generated current collection [11]. There is much better agreement between the dark and light J-V curves for the sample with T_{SS} = 550°C. The device parameters R_S, n, and J_O determined from the dark J-V data for all temperatures are listed in Table 3. The devices have comparable values of n consistent with Shockley-Read-Hall recombination, but decreasing J_O with higher T_{SS} as expected for the decrease in V_{OC}.

Table 2. Device results with different substrate temperature and evaporation process.

T_{SS} (ºC)	Process	V_{OC} (V)	J_{SC} (mA/cm^2)	*FF* (%)	eff. (%)
400	Cu-rich at start	0.59	33	71	13.7
	Cu-rich in middle	0.60	33	71	13.8
	Uniform flux	0.56	29	69	11.3
480	Cu-rich at start	0.62	32	72	14.4
	Cu-rich in middle	0.63	30	71	13.4
	Uniform flux	0.60	32	72	14.0
550	Cu-rich at start	0.65	32	76	16.0
	Cu-rich in middle	0.65	32	75	15.5
	Uniform flux	0.65	33	74	15.9

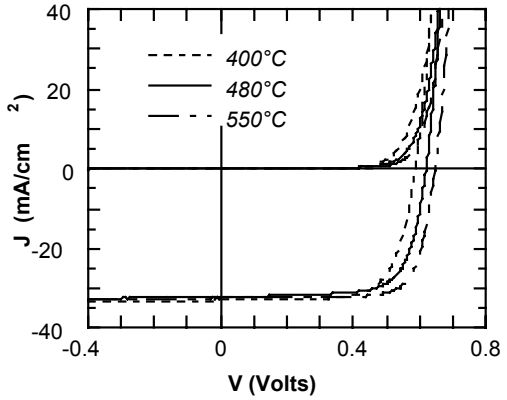


Figure 9. Current-voltage curves for devices with Cu(InGa)Se_2 deposited at different T_{SS} with Cu-rich growth at start.

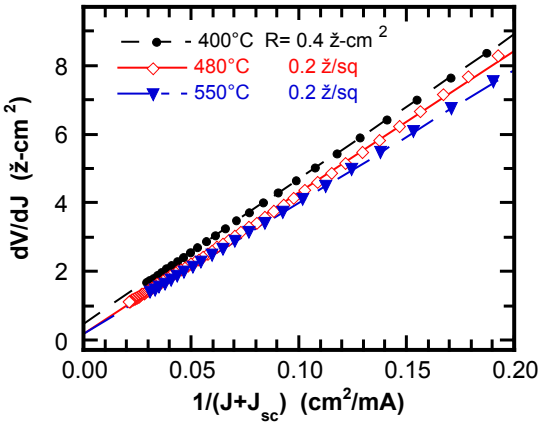


Figure 10. Derivative dV/dJ vs. $(J+J_{SC})^{-1}$ of the data in Figure 9 used to determine series resistance, R_S, from the intercept.

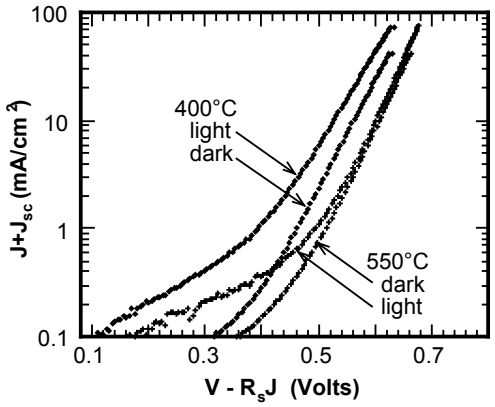


Figure 11. Logarithmic J-V behavior showing differences between light and dark curves for the 400°C case.

Table 3. J-V parameters with different substrate temperature.

T_{SS} (°C)	R_S (Ω-cm^2)	*n*	J_O (mA/cm^2)
400	0.4	1.8	14×10^{-6}
480	0.2	1.7	2×10^{-6}
550	0.2	1.6	0.9×10^{-6}

2.1.4 Cu(InGa)Se2 Deposition with In-Ga-Se Nucleation Layer

$Cu(InGa)Se_2$ films were also deposited using a deposition sequence that starts with an In-Ga-Se nucleation layer deposited at T_{ss} = 300°C, similar to the process used to produce high efficiency cells at NREL. This was followed by the delivery of a Cu-In-Ga-Se flux with Cu/(In+Ga) > 1 at T_{ss} = 550°C which proceeded until the total film composition had Cu/(In+Ga) ≈ 0.8 – 0.9.

The texture and grain size of these films were determined from XRD and AFM measurements, respectively. The XRD measurements show that the film growth from the In-Ga-Se layer gives a (220) preferred orientation. Films deposited with a Cu-In-Ga-Se layer at the start give a nearly random or slightly (112) preferred orientation. The mean grain area was found to be only 0.2 μm^2, smaller than the films deposited using a Cu-rich layer at the start of the run which give grain areas of 1.2 – 1.8 μm^2, as discussed above.

Finally, devices were fabricated from the films deposited with the In-Ga-Se nucleation layer using our baseline structure of glass/Mo/$Cu(InGa)Se_2$/CdS/ZnO/ITO. The best cell in this case had eff. = 15.0% with V_{oc} = 0.66V, J_{sc} = 32.5mA/cm^2, and FF = 70%. This result has comparable V_{oc} and J_{sc} to the best cells made with other processes using T_{ss} = 550°C, despite the different texture and small grain size. The cell has lower fill factor but the number of samples is too small to make general conclusions.

2.1.5 Discussion And Conclusions

By comparing different deposition sequences at fixed T_{SS}, it is clear that differences in grain size do not simply correlate to device efficiency. This can be seen at T_{SS} = 400°C where the uniform

deposition gives lower device efficiency but comparable grain size to the growth processes that incorporate a Cu-rich step. At T_{SS} = 550°C an increase in mean grain size with the Cu-rich growth does not result in an increased efficiency.

There are several other possible reasons for the lower V_{OC} that occurs with lower T_{SS}. An increase in surface area can result in a loss in V_{OC} since J_O is proportional to the surface area A_{surf}. With constant n and J_L, the change in V_{OC} with surface area can be written as

$$V_{OC}\left(A_{surf1}\right) - V_{OC}\left(A_{surf2}\right) = \frac{nkT}{q} ln\left(\frac{A_{surf2}}{A_{surf1}}\right) \quad (4)$$

For a 50% increase in surface area, with n = 1.7, the loss in V_{OC} is 18 mV. Thus, the decrease in ΔA_{surf} from 480 to 400°C reported in Table 1 can account for, at most, half of the decrease in V_{OC}. The films deposited at 480 and 550°C have comparable surface areas.

The increase in J_O suggests an increase in the density of intra-grain defects that act as deep trapping states to control the recombination current in the Cu(InGa)Se_2. These intra-grain defects can also cause the light generated current collection to become more voltage dependent by reducing the minority carrier diffusion length. Also, the J-V curves for devices made with T_{SS} = 400°C have hysterisis [4] which indicates long relaxation times associated with defect states in the devices.

In conclusion, the effect of reducing substrate temperature during multisource evaporation of Cu(InGa)Se_2 on grain size and surface area has been characterized and related to the decrease in device efficiency. Comparing different flux profiles, it was shown that at T_{SS} = 400°C Cu-rich growth, whether at the beginning of the deposition or later in the process, is necessary to achieve good performance. However, at higher T_{SS} the device performance is insensitive to the growth sequence allowing greater process flexibility. With the Cu-rich growth, the mean lateral grain area decreases from 1.8 to 0.3 μm^2 as T_{SS} is reduced from 550 to 400°C, but only at the highest T_{SS} does the grain size depend on the growth process. In general, lower device efficiency with lower T_{SS} cannot be simply described by changes in grain size, surface area or the availability of Na. Instead, the lower voltage and increased recombination current with lower temperature deposition indicate a greater density of intra-grain trap states in the Cu(InGa)Se_2 which can also lead to smaller minority carrier diffusion length and voltage dependent current collection.

2.2 Deposition of Cu(InGa)Se_2 Films by In-Line Evaporation

2.2.1 Introduction

Commercial manufacture of Cu(InGa)Se_2-based solar modules requires uniform deposition, control of composition, and high throughputs. These requirements can be met by continuous in-line evaporation, schematically shown in Figure 12, in which a heated substrate is linearly translated over sequential Cu, In, and Ga evaporation sources in a Se environment. The potential of in-line evaporation has already been demonstrated [12,13].

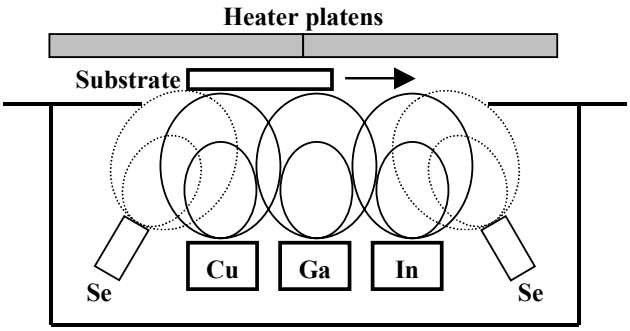


Figure 12. Schematic of elemental in-line evaporation.

The sequential nature of the incident elemental fluxes allows control of the composition and compositional gradients in the film. This allows the incorporation of Cu-rich growth transients, which have been shown to improve film properties [14], as well as grading the Ga/(Ga+In) ratio in the film, allowing the fabrication of graded-bandgap absorber layers.

In 1999, IEC began operation of a Cu(InGa)Se_2 in-line evaporation system to study issues relevant to the design and operation commercial-scale systems. These include broad issues such process modeling and control, as well as specific issues such as effusion source design and implementation of *in-situ* atomic absorption spectroscopy (AAS) for direct measurement of elemental effusion rates [15].

The primary design model for in-line evaporation is the description of the incident fluxes as the substrate translates through the deposition zone. The elemental incident fluxes depend on source geometry and temperature and determine the film's growth rate, composition, and uniformity. Models directly relevant to process control include prediction of the effusion rate based on temperature, and the atomic absorption of light by the effusing vapor.

The key requirement for long-term (> 8 hour) commercial deposition is stable effusion rates at high (> 1 ft/min) substrate throughput. This requires stable, reliable process components and sensors, regardless of the sophistication of the control algorithm. In addition to developing process models, an ongoing effort has and is being made to improve the reliability of various system components. These primarily include the effusion sources and the in-situ AAS hardware

2.2.1.1 System Description

The IEC in-line evaporation system, shown in Figure 13, is capable of deposition over a 12"-wide web at translation speeds up to 20"/min, though it is presently configured for 6" wide substrates. The chamber measures 64"L x 33"W x 27"H. The base pressure is $5x10^{-8}$ Torr, with a typical operating pressure of $2x10^{-5}$ Torr.

Each elemental effusion source has two nozzles spaced 4.6" apart. The sources are placed 3.5" apart in the sequence Cu-Ga-In, with the Ga source at the center of the deposition zone. The deposition zone is 15" long with the substrate at 9.25" above the sources.

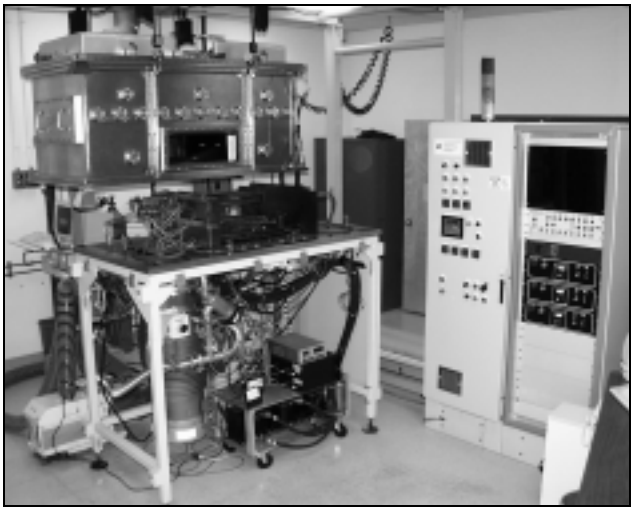


Figure 13. IEC in-line evaporation system.

The substrate is heated by two sequentially arranged, independently controlled heater platens. The platens measure 14" x 14", so that they are substantially wider and, taken together, longer than the deposition zone. The substrate temperature is monitored using a bare-junction thermocouple cemented to the substrate surface.

Temperature control is used for the heater platens and selenium source. Cu, Ga, and In sources are controlled by ATOMICAS™ AAS systems while source temperatures are monitored by thermocouples. Presently, all of the system components are being operated using independent PID control loops.

2.2.1.2 Film Characterization

The compositional uniformity across the 6" wide substrate (in the *cross-direction*) was characterized by EDS measurement. The data, shown in Figure 14, indicate uniform Cu/(Ga+In) and Ga/(Ga+In) ratios within the uncertainty of the EDS. Film thickness, however, decreases by 10-15% from center to edge due to the current system geometry.

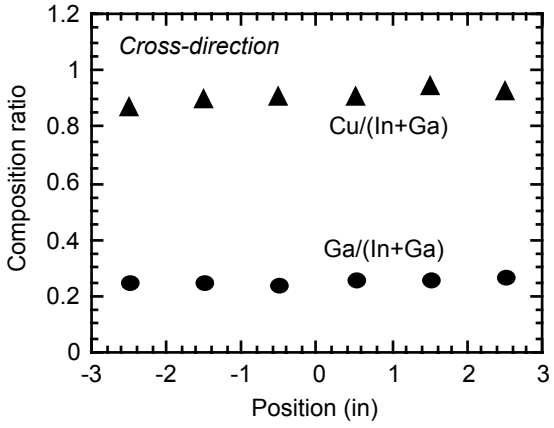


Figure 14. Compositional uniformity across the deposition zone.

Figure 15 shows the composition profile of a 2.3 μm film measured by Auger electron spectroscopy (AES) depth profiling. The film was deposited at 525 ºC at a translation speed of 1"/min. This particular deposition run produced the best device to date, with V_{OC} = 0.606 V, J_{SC} = 33.2 mA, FF = 74.3%, and eff. = 14.9% under 100mW/cm^2 AM1.5 illumination.

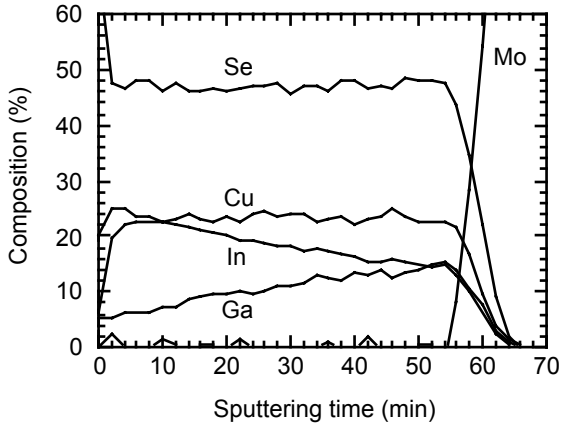


Figure 15. AES depth profile of Cu(InGa)Se_2 film deposited at 525ºC and 1"/min.

To study the effect of substrate throughput, films were deposited at different substrate translation speeds, from 1"/min to 2.5"/min. The source effusion setpoints were not varied, so that the films would vary in thickness but retain a fixed composition. Film composition was characterized by EDS, and the film quality by the performance of solar cells fabricated from them. Figure 16 indicates similar compositions for all of the translation speeds, as expected. The best solar cell result from each run is shown in Table 4, again good device quality over a 2.5x range of substrate throughput. It should be noted that, with respect to film thickness, the drop in performance for thickness < 1μm is consistent with the work of Negami et al. [16].

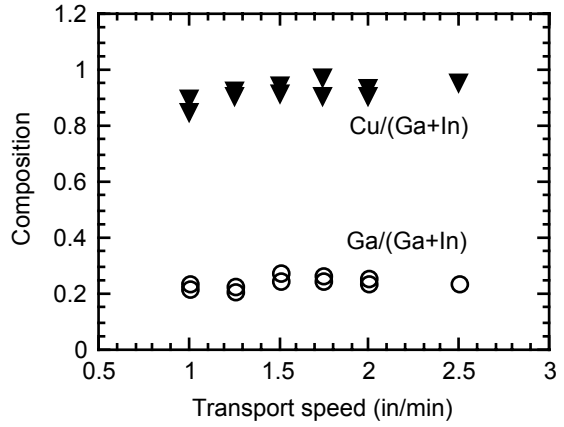


Figure 16. Film composition with varying substrate transport speed.

Table 4. Device performance with increasing translation speed.

Speed (in/min)	Thickness (μm)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Eff (%)
1	2.1	0.594	32.1	69.4	13.2
1.25	2	0.594	32.5	71.8	13.8
1.5	1.8	0.614	33.2	71.7	14.6
1.75	1.4	0.588	33.7	70.5	14.0
2	1.3	0.590	33.6	67.8	13.5
2.5	0.9	0.570	31.9	66.3	12.2

In summary, the system is capable of depositing compositionally-uniform, device-quality $Cu(InGa)Se_2$ films at deposition times from 8-15 minutes.

2.2.1.3 System Characterization

The motivations for system characterization are twofold. First, an accurate system characterization is critical to improve the science and engineering basis of the in-line process. For example, if elemental incident fluxes are accurately known, the effects of Cu-rich transients, or Ga-In interdiffusion can be quantitatively studied. Second, system characterization allows the development of process models that can be extrapolated to larger, commercial-scale systems.

2.2.1.3.1 Flux Characterization

The source geometry used for the model is shown in Figure 17 where the vector (ρ, θ) points from a source nozzle to a point on the substrate. The flux profile of the effusion source can be approximated using:

$$f(\rho,\theta) = \frac{F(n+1)}{2\pi\rho^2}\cos^n\theta \qquad (5)$$

where n is an empirical fitting parameter describing the collimation of the molecular beam. In the case of free-molecular flow, the molecular beam profile is solely a function of the nozzle aspect ratio (nozzle length divided by nozzle diameter) [17]. There are a number of references describing the effect of flow regime and nozzle aspect ratio on effusion flux profiles [18,19,20,21]. The accumulation rate, f^{dep}, at the substrate is obtained by multiplying Equation 5 by an additional cos θ correction to account for the angle of incidence. The deposition from multiple sources at a point on the substrate is calculated by simply summing the individual source contributions.

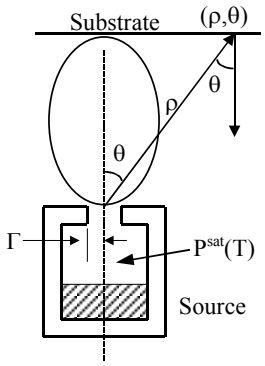


Figure 17. Variables used in effusion analysis.

IEC has previously reported flux profiling results for the in-line system [22]. However, during the past year, the source required re-characterization due to a design change of the effusion nozzles. Due to its thermal characteristics, the previous nozzle was prone to droplet condensation (at all effusion rates) and droplet ejection (at high rates). Nozzle condensation effectively collimates the flux profile, since vapor atoms hitting nozzle walls condense instead of scatter. This complicates the process design control if the condensation varies with time and from source to source. Ejected droplets pose a critical problem since many of them reach and adhere to the substrate. The improved nozzle design eliminated condensation and spitting, thereby allowing a more reliable characterization of the flux profile.

The apparatus used for measuring flux profiles is shown in Figure 18. Substrates are arranged in a semi-circle, at regular azimuthal angles, about one effusion nozzle. A shutter is used to prevent deposition during heat-up and cool-down of the effusion source. A shield is used to prevent deposition from the second source nozzle. Flux profiles at effusion rates ranging from 0.23 g/hr to 31 g/hr were measured for Cu. Flux profiles were measured for Ga and In at rates of 2.2 and 1.4 g/hr, respectively. *In-situ* AAS, as opposed to source temperature, was used to control the effusion rate during deposition.

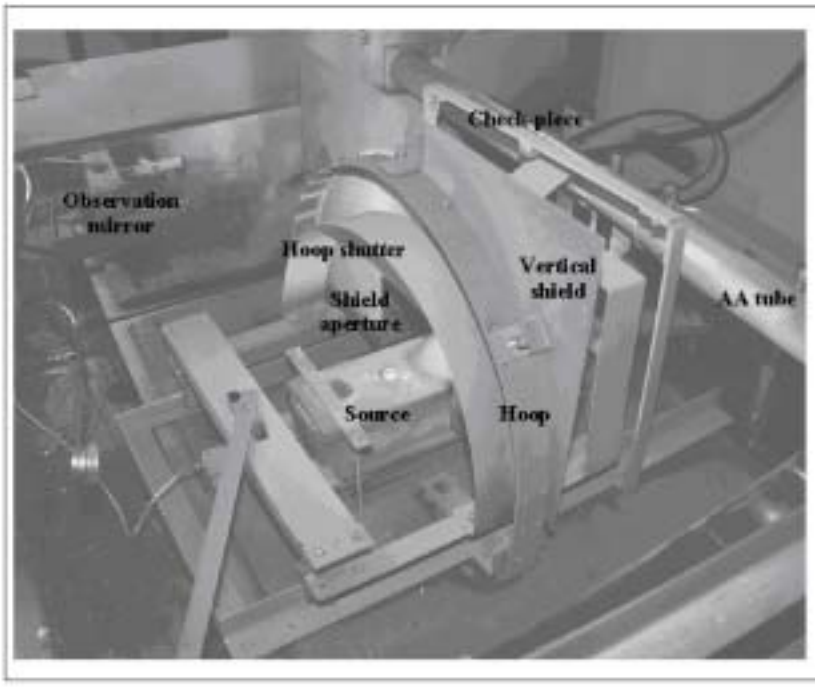


Figure 18. Apparatus for measuring flux distribution from a nozzle.

Data for Cu (low and high rates), In, and Ga are shown in Figure 19. Intermediate Cu effusion rates have been omitted for clarity. The data are well modeled by a $\cos^n\theta$ approximation with n = 3.0.

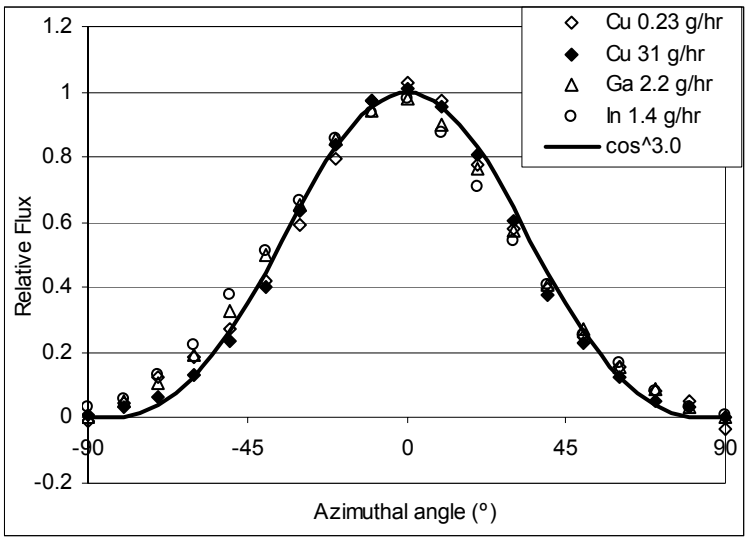


Figure 19. Effusion profile of IEC in-line evaporation sources.

The aforementioned literature indicates that the only factors influencing the flux profile are the nozzle geometry (aspect ratio = length ÷ diameter) and Knudsen number (mean free path ÷ diameter). The consistency in the Cu profiles over a wide range of rates (and hence Knudsen numbers) is due to the insensitivity of the flux to the Knudsen number *at the particular aspect ratio*. Given the similarity of the Cu results, the In and Ga results are not surprising.

These results are encouraging on two levels. First, they indicate that reliable effusion behavior has been achieved by the improved nozzle design. Second, they indicate that a simple model is applicable at all relevant effusion rates.

2.2.1.3.2 *In-situ* Atomic Absorption

In conjunction with the effusion characterization, significant effort was devoted to quantifying the atomic absorption. This included the development of a model incorporating system geometry, and experiments to determine element-specific absorption coefficients.

Modeling the beam absorption of a thermal evaporation source involves using the Lambert-Beer law to line-integrate the change in intensity, I, through a variable-density field (Figure 20):

Lambert-Beer:
$$\frac{dI}{I} = -K\rho_{vapor}(s)ds \qquad (6)$$

$$\ln\left(\frac{I}{I_0}\right) = \int_{\mathbf{S}}\left[-K\rho_{vapor}(s)\right]ds \qquad (7)$$

where s is the path variable, **S** is the beam path, **K** is the absorption coefficient, and $\rho_{vapor}(s)$ is the position-dependent vapor density.

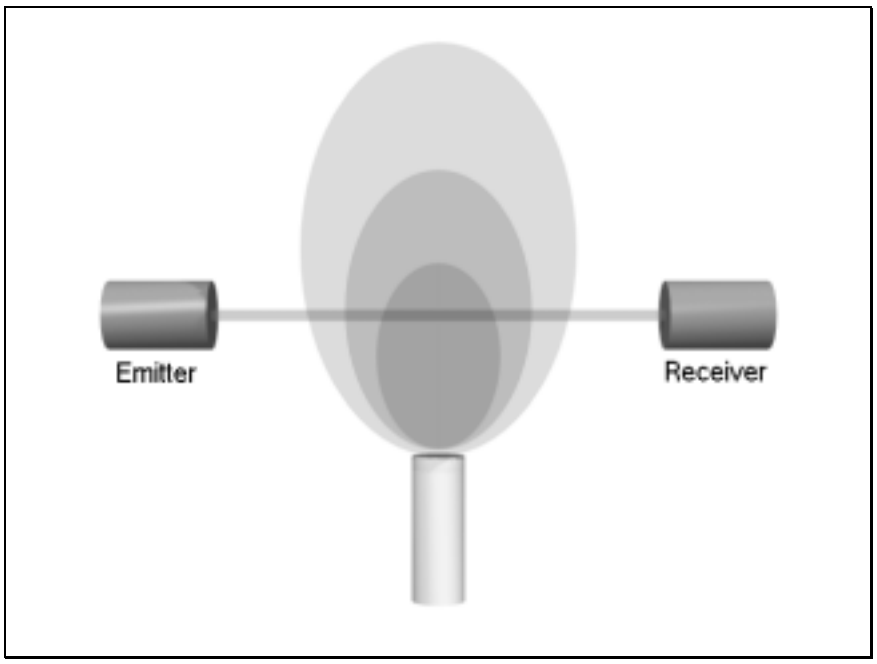


Figure 20. Illustration of AA beam passing through the variable-density effusion profile of an evaporation source.

Assuming straight-line atomic flight, ρ_{vapor} is simply related to the flux by

$$\rho_{vapor} = \frac{f}{\bar{c}} \tag{8}$$

where $\bar{c}$ is the atomic mean speed, and f is the flux, which is known from the flux characterization experiments. Thus, once the beam geometry and effusion rate are fixed, the absorbance can be predicted if K is known:

$$\ln\left(\frac{I}{I_0}\right) = \int_s K \frac{f(s)}{\bar{c}}\, ds \tag{9}$$

The determination of K is the fundamental experimental task of the AA characterization. Values for $\frac{K}{\bar{c}}$ were found to be 1.02×10^6, 4.5×10^5, and 2.9×10^5 cm-sec/g for Cu, In, and Ga, respectively, at typical evaporation rates for deposition onto a substrate translating at 1"/min.

2.2.1.4 Conclusion

Significant progress has been made to improve the design and control of in-line evaporation. This includes improved source design, source characterization, and *in-situ* AA modeling and characterization. Combined, these achievements allow a high degree of controllability over the incident fluxes at the substrate over extended runs. This effort provides the groundwork for future development on roll-to-roll, flexible substrate operation.

2.3 Formation and analysis of Graded $CuIn(SeS)_2$ and $CuGa(SeS)_2$ Films

Alloy materials based on $CuInSe_2$ are potential absorber layers for wide bandgap, Eg > 1.5 V, heterojunction solar cells. High performance, wide bandgap, solar cells could: 1) improve module performance and reduce module cost; and 2) provide the wide bandgap device needed for 'next generation' monolithic tandem devices. Graded bandgaps could be used to improve V_{oc} of present generation devices by allowing incorporation of graded bandgap structure into the junction region. The Cu-In-Ga-Se-S chalcopyrite materials system, $CuInSe_2 \Leftrightarrow CuInS_2 \Leftrightarrow CuGaSe_2 \Leftrightarrow CuGaS_2$, can be developed to yield bandgaps from 1.0 to 2.5 eV, since alloys of these compounds form continuous solid solutions. At present, substitution of Ga for In to form alloys has resulted in the highest performance devices, but at Ga/(Ga+In) > 0.5, with Eg > 1.3 eV, the device performance decreases [23]. Siemens Solar Industries utilizes a graded $Cu(InGa)(SeS)_2$ film structure where the junction region is alloyed with sulfur to increase V_{oc}, while the back contact region is alloyed with gallium [24].

Formation of $CuIn(Se_{1-y}S_y)_2$ alloy films has been addressed with respect to formation of graded structures and providing a quantitative basis for characterizing the film formation process. The experimental approach consists of reacting $CuInSe_2$ films in flowing H_2S/Ar atmosphere at 450°C to 525°C to convert films completely to $CuInS_2$, or to produce graded $CuIn(Se_{1-y}S_y)_2$ alloy films. A model of the reaction/diffusion conversion process was developed and a method to quantitatively analyze the process is presented that predicts the compositional distribution of the converted films. The methodology is similar to that reported for analyzing CdS/CdTe thin-film couples [25]. Finally, the reaction of sulfur with films of different starting composition has been characterized. This includes comparison of $CuInSe_2$ and $CuGaSe_2$ films and of Cu-rich and Cu-poor films. This work was presented at the E-MRS 200 Sprint Meeting, Strasbourg, France, May 30–June 2, 2000 (Appendix 1, Ref. 24).

The effect of initial film composition and substrate in the sulfurization of $CuInSe_2$ was further investigated. $CuInSe_2$ films deposited on either soda-lime glass (SL) or Corning 7059 borosilicate glass (7059) substrates were reacted in flowing H_2S for times from 1 to 8 hours. Films with Cu-rich composition, Cu/In > 1, reacted for 1 hour, had nearly all the Se replaced by S. For Cu-poor films, the incorporation of S was significantly reduced. In addition, in Cu-poor films on SL glass, $CuInS_2$ and $NaInS_2$ were found at the film surface. These phases were not detected in films on 7059 substrates or in Cu-rich films. A phenomenological model has been proposed to explain the formation of segregated surface phases in Cu-poor films on SL substrates. This work was presented at the 2001 MRS Spring Meeting, San Francisco, CA, April 16–20, 2001 (Appendix 1, Ref. 21).

3. Si-BASED SOLAR CELLS

3.1 Microcrystalline Silicon Carbide p-layers

3.1.1 Introduction

During the present contract, the investigation of glow discharge deposited crystalline p-layers was conducted in two parts. In the first part, we have investigated the deposition and characterization of these types of films having high level of CH_4 in the feed gas which completed the investigation of carbon containing p-layers. The goal was to determine the feasibility of obtaining crystalline SiC phases in the films. The second part of the work deals with investigation of the deposition and characterization of films having CO_2 in the feed gas. The goal here was to obtain two phase films of crystalline Si imbedded in a matrix of a-Si:O:H:C. The idea is that Si:C:H or Si:O:H:C p-layers incorporated in p-i-n type devices could give high currents due to the transparency of the amorphous phase and high voltages due to the highly conductive crystalline phase with a smaller junction surface. Also, the presence of CO_2 in the glow discharge plasma would tend to decrease the reducing effects of the plasma on the thin conductive oxide used as the front contact in superstrate devices.

3.1.2 Experimental Approach

The p-layers were deposited on 7059 glass and on SnO_2 substrates, and their volume fraction crystallinity (X_c) and deposition rates were determined by Raman spectroscopy [26] and by profilometry. In-plane conductivity and activation energy measurements were also performed on most of the films deposited on glass substrates. X_c was determined both on glass and SnO_2 substrates for many of the deposition conditions.

The main experimental variables were the hydrogen dilution and CH_4 or CO_2 content in the feed gases. The secondary parameters were discharge power density and doping gas (B_2H_6) level. Preliminary experiments comparing B_2H_6 and $B(CH_3)_3$, or TMB, as dopants found that TMB reduced X_c. All other groups use B_2H_6 or BF_3 for doping μc-Si p-layers. We speculate that TMB suppresses nucleation or crystallization, similar to the effect of CH_4. All p-layers reported here use B_2H_6.

In designing experiments and interpreting results, normalized flows rather than the actual gas flows were used. These normalized flows were defined as,

$$c = f(CH_4) / [f(SiH_4) + f(CH_4)] \quad (10)$$

$$h = f(H_2) / [f(SiH_4) + f(CH_4)] \quad (11)$$

$$b = 2 \times f(B_2H_6) / [f(SiH_4) + f(CH_4)] \quad (12)$$

for the deposition of carbon containing p-layers, and

$$o = f(CO_2) / [f(SiH_4) + f(CO_2)] \quad (13)$$

$$h = f(H_2) / [f(SiH_4) + f(CO_2)] \quad (14)$$

$$b = 2 \times f(B_2H_6) / [f(SiH_4) + f(CO_2)] \quad (15)$$

for the deposition of oxygen containing p-layers.

For all depositions substrate temperature was kept at 150°C. Except in few cases discharge pressure, SiH_4 partial pressure and residence times were also kept constant throughout the study by introducing He to the discharge as a buffer gas. The deposition system is a 13.5 MHz RF plasma enhanced CVD (RF-PECVD).

3.1.3 Results and Discussion

3.1.3.1 Films Deposited from CH_4 Containing Discharges

3.1.3.1.1 Effect of CH_4 on Crystallinity

In order to determine the effect of CH_4 on the crystallinity of the films a series of undoped films were deposited at different normalized CH_4 flow keeping all other parameters constant, including SiH_4 partial pressure P_s. Again, these deposition parameters are the ones that yielded high crystalline fraction for non-carbon containing films. Table 5 gives the deposition conditions and critical material parameters of the films. The data indicates the steep decline of the c-Si fraction with the increasing amount of CH_4 in the gas phase.

Table 5. Deposition conditions and characteristics of films with different normalized CH_4 flows.

Normalized Flow		Power	P_s	Thickness	E_a	σ_d	c-Si
C	h	(W)	(mT)	(μm)	(eV)	(S/cm)	(%)
0	100	50	9.9	0.11	0.38	$5x10^{-6}$	85
0.33	100	50	9.9	0.33	0.67	$3x10^{-10}$	38
0.43	100	50	9.8	0.34	0.75	$2.5x10^{-12}$	0
0.5	100	50	9.8	0.36	0.82	$2.1x10^{-13}$	3

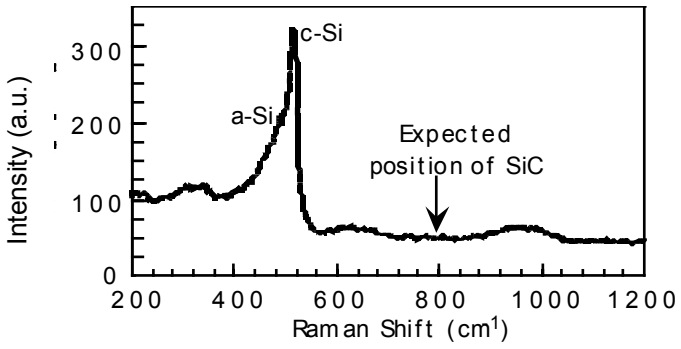


Figure 21. Raman spectrum of a μc-Si film deposited with CH_4 normalized flow of 0.33.

Raman spectra of these films showed only the presence of c-Si and a-Si phases, as can be seen in a typical spectrum in Figure 21. No carbon containing species, such as SiC, were identified in these samples. This observation leads us to conclude that all the carbon in the film is located within the amorphous phase.

3.1.3.1.2 Effect of RF Power

The effect of RF power was investigated in the range of 10 to 50W, corresponding to power density range from 84 to 420 mW/cm^2. For this set of experiments normalized flows of H_2, CH_4, B_2H_6 and SiH_4 partial pressure were kept constant at 300, 0.33, 0.02 and 2.2 mT levels. Raman spectra showed that, as before, only c-Si and a-Si phases are present in the films. The activation energies were measured to be around 0.05 eV for all the films, which indicates that in-plane c-Si phase controls in-plane electrical transport.

Figure 22, where room temperature dark conductivity and the c-Si volume fraction is plotted against discharge power, shows that for SiH_4 partial pressure of 2.2 mT, crystallinity is independent of power while conductivity decreases with increasing power. This decrease in conductivity cannot be explained with the available data.

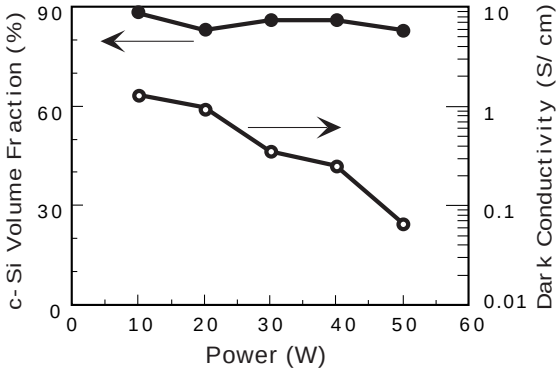


Figure 22. c-Si volume fraction and dark conductivity as a function of discharge power.

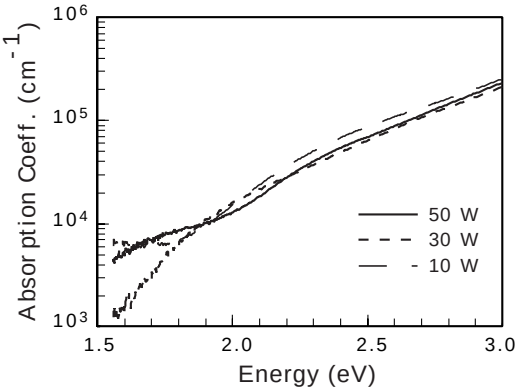


Figure 23. Absorption coefficient as a function of energy at three different discharge power levels.

Optical analysis of the films is displayed in Figure 23 in the form of absorption coefficient *vs* energy. Within experimental errors absorption at high energies is independent of power, suggesting that the amount of carbon in the amorphous phase is also independent of the discharge power.

3.1.3.1.3 Effect of Hydrogen Dilution

Next, we investigated the flow ranges of $0.5 \leq c \leq 0.94$, $5 \leq h \leq 227$, and $b = 2 \times 10^{-3}$. SiH_4 partial pressure and total pressure were kept constant at 2.2 mT and 1 Torr levels, respectively. Table 6 gives the deposition parameters of a set of films deposited with c = 0.5.

Table 6. Deposition parameters of microcrystalline p-layers with c = 0.5 and discharge power density of 168 mW/cm^2. R is the deposition rate and c-Si is the amount of crystalline Si phase in the films as determined by Raman spectroscopy.

Gas Flows (sccm)					h	Glass Substrate		SnO_2 Substrate (1)	
SiH_4 (90% H_2)	CH_4	B_2H_6 (99.8% H_2)	H_2	He		R (Å/s)	c-Si (Vol%)	R (Å/s)	c-Si (Vol%)
10	1	1		445	5	0.38	0		NA
10	1	1	70	380	40	0.22	1		0
10	1	1	140	310	75	0.18	61		0
10	1	1	290	170	150	0.07	84		28
10	1	1	445		227	0.04	100		74

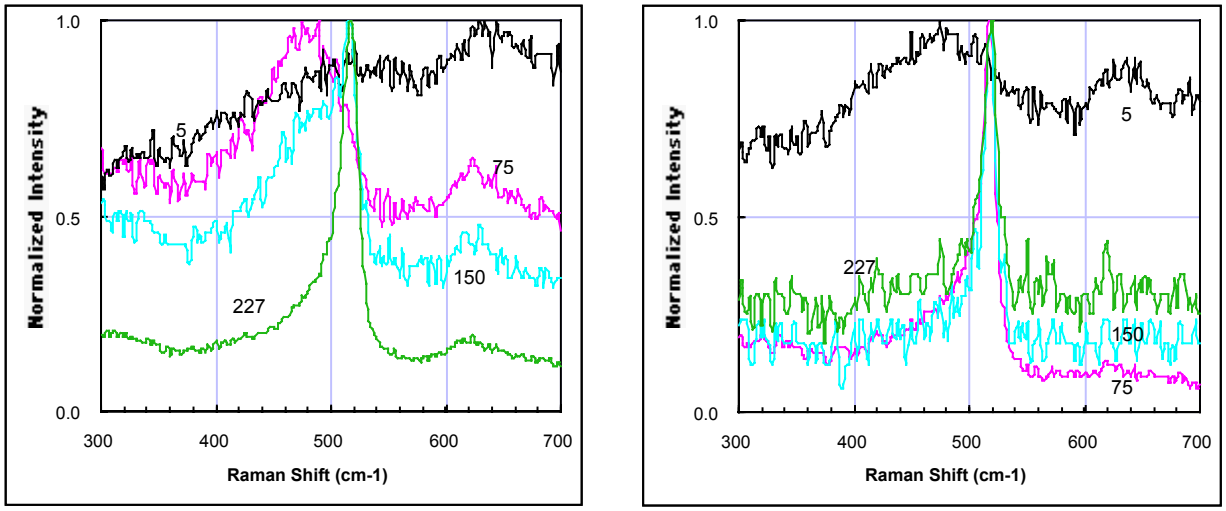
(1): Film thicknesses could not be measured due to textured surface.

No crystalline SiC phase (peak at 800 cm^{-1}) was observed in the Raman spectra of these films.

The spectra from 300 to 700 cm^{-1} are given in Figure 24. Films deposited on SnO_2 have no identifiable structure for h = 5 and, as h is increased, change gradually from a-Si:C:H (broad peak at 480 cm^{-1}) to a mixture of a-Si:C:H and c-Si H (peak at 520 cm^{-1}). On glass, however, they start being a-Si:C:H at h = 5 but become entirely c-Si at hydrogen dilution of 227.

As can be seen from Table 6, while the onset of crystallinity on glass substrates is at hydrogen dilution of 40, on SnO_2 substrates it is between 75 and 150.

Table 6 also shows that the increase in hydrogen dilution h not only increases crystalline silicon volume fraction but also results in the decrease of deposition rate. Consequently, it is difficult to ascribe the change in crystallinity uniquely to changes in hydrogen dilution. However, at least for $40 \leq h \leq 75$ crystallinity is mainly controlled by hydrogen dilution since deposition rate shows a relatively small change within this range.



(a) Glass/SnO_2 substrate (b) Glass substrate

Figure 24. Raman spectra of the films deposited c = 0.5 at a power density of 160 mW/cm^2. The labels give hydrogen dilution levels.

Analysis of films deposited under identical conditions but at 84 mW/cm^2 power density gave qualitatively similar results in terms of changes in crystallinity and deposition rate with hydrogen dilution. More quantitatively, however, deposition rates and crystalline Si volume fractions were found to be lower for the same hydrogen dilution. The results are shown in Table 7.

A number of films were also prepared at hydrogen dilution of 75 with c = 0.83 and 0.94 and with power densities from 168 to 420 mW/cm^2. Raman spectra of all these films were found to be featureless, lacking any of the characteristic peaks for crystalline or amorphous phases of interest.

Table 7. Deposition rate and crystallinity of the films deposited with power density of 84 mW/cm^2. All other parameters are the same as films of Table 6.

h	Glass Substrate		SnO_2 Substrate (1)	
	R (Å/s)	c-Si (Vol%)	R (Å/s)	c-Si (Vol%)
5	0.32	0		0
40	0.18	3		0
75	0.13	54		0
150	0.06	67		60
227	0.00 (2)	68 (2)		42

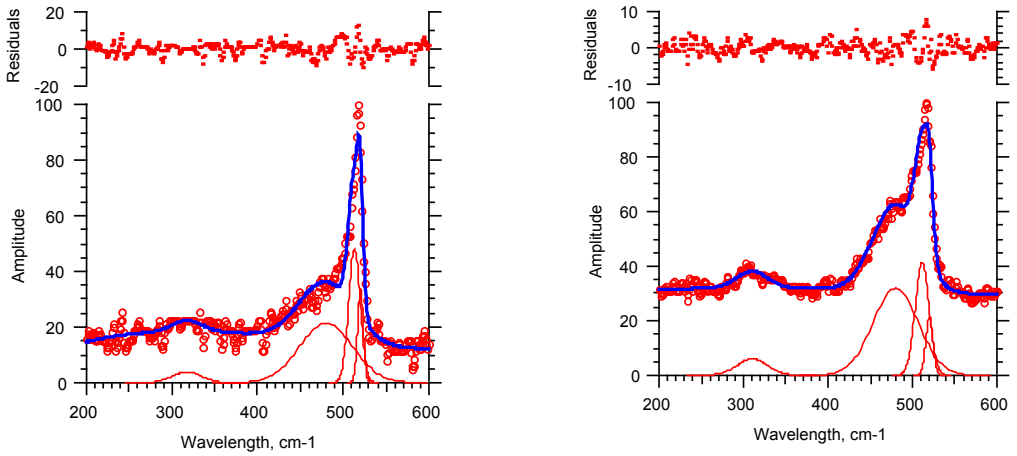
(1) Film thicknesses could not be measured due to textured surface.
(2) No deposition at the center of the substrate, Raman spectrum taken at the edge.

3.2 Microcrystalline Silicon Oxide p-layers

3.2.1 Effect of Substrates

As a first step, we have performed a deposition under conditions that favor crystallinity in films with CH_4 for the purpose of evaluating crystallinity and carbon and oxygen incorporation into the film (Run #4847). The conditions chosen were: f(SiH_4) = 20 sccm; Power Density = 420 mW/cm^2; Pressure = 1 Torr; h = 154; o = 0.23; b = 1.5x10^{-3}.

Raman spectra of the films (Figure 25) show the existence of a two-phase mixture consisting of c–Si and amorphous silicon phases. Also, the film deposited on glass seems to have higher amount of c-Si phase (45% *vs* 35%).



Glass substrates Glass/SnO_2 substrate

Figure 25. Raman spectra of the films from run #4847 deposited with CO_2 discharge on glass and glass/SnO_2.

3.2.2 SIMS Analysis

SIMS depth profile of the films shown in Figure 26 indicate that:

1) the composition of the films are independent of the substrate,
2) oxygen and carbon content in the films are respectively 10^{22} and $7x10^{20}$.

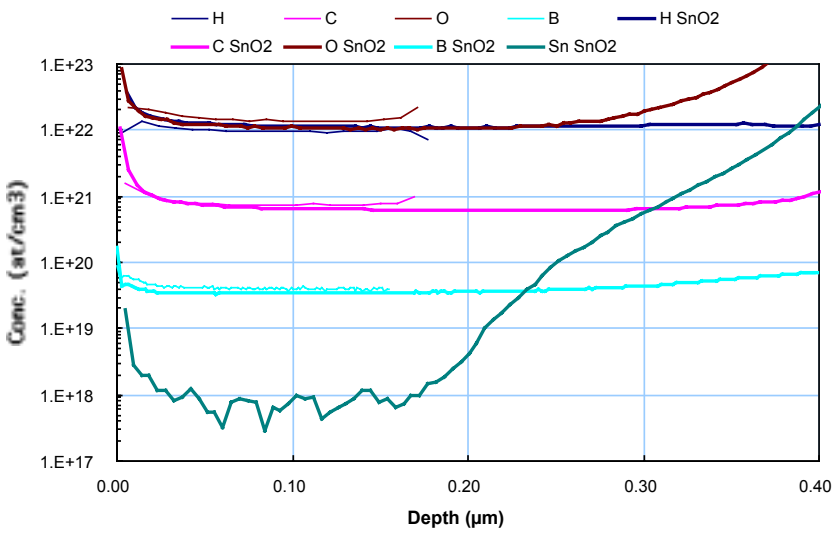


Figure 26. SIMS depth profiles of the films from run 4847. Thinner lines are the film on glass while thicker lines are the film on SnO_2.

It is important to note that since the films have a c-Si and an amorphous phase, the latter must contain almost all the hydrogen, carbon and oxygen observed in the SIMS analysis. Thus, it can be concluded that the amorphous phase is essentially hydrogenated silicon oxide containing small amounts of carbon and boron.

3.2.3 Effect of Diborane Level in Discharge

In the next step, films deposited at two different diborane dilutions "b" for a range of hydrogen dilution "h" were investigated for their crystallinity by Raman spectroscopy. The deposition rates were determined by profilometric measurements. Total pressure, silane partial pressure and discharge power density were, respectively, 5 mT, 1 Torr and 168 mW/cm2. Table 8 summaraizes deposition conditions and the measured film properties.

First thing to note is that for the diborane concentration of b = 0.0015, the c-Si phase is observed at remarkably low hydrogen dilutions of h = 23 and 50, respectively, for 7059 glass and tin oxide substrates, even at such a low power density utilized here.

More generally, it is found that fraction of c-Si increases with increasing hydrogen dilution and decreases with increasing diborane levels. However, the degree of validity of this observation depends on the film deposition rates. This is because bonding rearrangement on the surface of the growing film that favors c-Si formation will be more extensive for low deposition rates. Consequently, dependence of crystallinity on hydrogen dilution is only clearly in the regions where deposition rates do not change appreciably. The deposition rate argument can also explain the difference in crystallinity between like substrates deposited at different diborane levels.

Table 8. Deposition conditions and measured characteristics of films deposited at two different diborane concentrations in the plasma for a range of hydrogen dilutions.

Gas Flows (sccm)							Glass Substrate				SnO_2 Substrate	
SiH_4 (90% H_2)	CO_2	B_2H_6 (99.8% H_2)	H_2	He	b	h	R (Å/s)	σ_d (S/cm)	E_a (eV)	c-Si (Vol%)	R (Å/s)	c-Si (Vol%)
20	0.6	10	0	370	$1.5x10^{-2}$	11	0.46	$3.8x10^{-08}$	0.54	1	0.63	0
20	0.6	10	75	295	$1.5x10^{-2}$	40	0.47	$4.7x10^{-08}$	0.54	5	0.63	0
20	0.6	10	145	225	$1.5x10^{-2}$	67	0.38	$1.3x10^{-04}$	0.15	13	0.63	0
20	0.6	10	232	138	$1.5x10^{-2}$	100	0.44	$1.2x10^{-03}$	0.10	13	0.49	0
20	0.6	10	368	0	$1.5x10^{-2}$	152	0.31	$1.7x10^{-01}$	0.06	42	0.47	16
20	0.6	1	0	380	$1.5x10^{-3}$	7	0.47	$5.0x10^{-11}$	0.70	0	0.76	0
20	0.6	1	40	338	$1.5x10^{-3}$	23	0.24	$1.8x10^{-05}$	0.23	10	0.49	0
20	0.6	1	72	305	$1.5x10^{-3}$	35	0.28	$7.2x10^{-03}$	0.11	36	0.44	0
20	0.6	1	110	270	$1.5x10^{-3}$	50	0.25	$1.3x10^{-01}$	0.07	58	0.42	22
20	0.6	1	150	230	$1.5x10^{-3}$	65	0.21	$1.5x10^{-01}$	0.07	62	0.33	25
20	0.6	1	190	187	$1.5x10^{-3}$	80	0.28	$1.4x10^{-01}$	0.07	67	0.35	43
20	0.6	1	240	138	$1.5x10^{-3}$	100	0.17	$3.1x10^{-01}$	0.06	74	0.28	47
20	0.6	1	381	0	$1.5x10^{-3}$	154	0.11	$2.3x10^{-01}$	0.07	71	0.22	50

However, the difference in crystallinity between glass and tin oxide substrates for a given diborane level might also be controlled, in addition to deposition rate, by the possible difference in the initial nucleation rate of crystallites on glass and tin oxide surfaces.

The difference in deposition rates between glass and SnO_2 substrates is most probably due to the voltage difference between substrate and the plasma. In the case of a conductive substrate such as SnO_2 the surface is grounded and the potential difference between substrate and the plasma is the plasma potential. In the case of glass substrate, the potential difference is the floating potential which, in general, is substantially smaller than the plasma potential. Also affecting the deposition rate are hydrogen dilution and diborane levels in the discharge. Increasing hydrogen dilution reduces deposition rate even though silane partial pressure and gas residence time stay the same. This observation supports hydrogen etching of the film during growth. Finally, the observed increase in deposition rate with gas phase diborane concentration is related to the known ability of diborane in cracking silane molecules.

As to the interpretation of the measured conductivities and activation energies, because of the two-phase nature of these films, the in-plane measurements of these characteristics do not provide much useful information. However, it can be pointed out that measured activation energies of 0.07 eV are, within experimental errors, that of boron in silicon and, as such, confirm that in this respect silicon crystallites in the films behave like bulk silicon.

3.2.4 Effect of Hydrogen Dilution

A number of films were deposited at different levels of hydrogen dilution for four different CO_2 levels, with $b = 1.5x10^{-3}$. All other deposition parameters were the same as given in Table 8. The c-Si content in these films is given in Figure 27 for glass and SnO_2 substrates. The data

show that while CO_2 levels in the discharge do not seem to have an effect on the c-Si content in the case of glass substrates, it does, however, control crystallinity of the films deposited on SnO_2 substrates. Also, as previously noted, increasing hydrogen dilution increases crystallinity and SnO_2 substrates give a lower c-Si fraction than glass substrates. The onset of crystallinity as a function of hydrogen dilution is also different for the two substrates, typically $h \leq 23$ for glass and $h \leq 50$ for SnO_2.

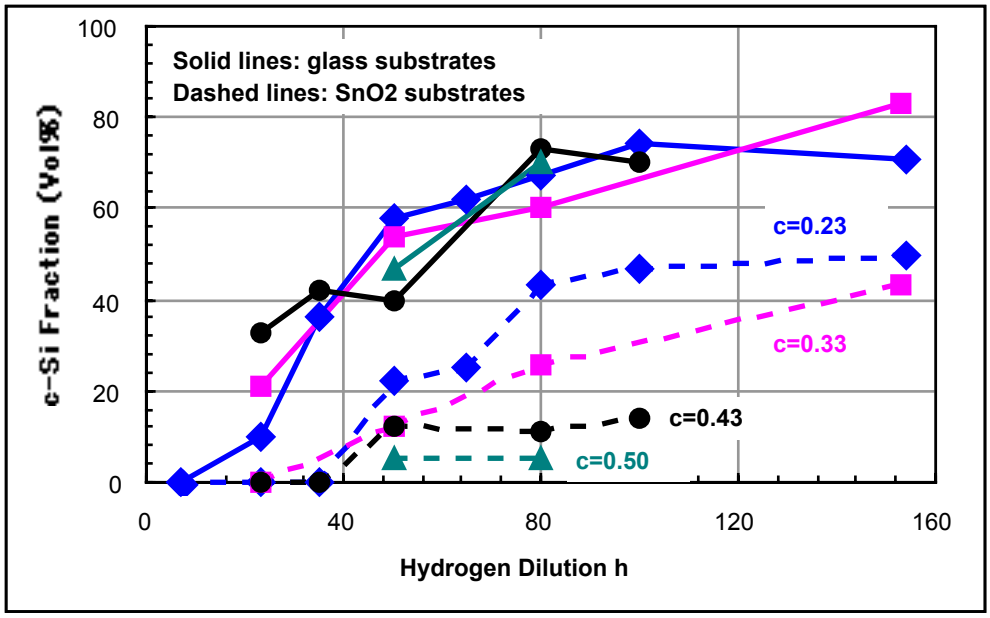


Figure 27. Volume fraction of c-Si as a function of hydrogen dilution for different levels of CO_2 in the discharge.

3.2.5 Crystallization in Ultra-thin Films

In order to characterize the structure of the films at thicknesses comparable to p-layer thicknesses in operational devices, we deposited 150Å thick films and determined their crystallinity. In this case, two CO_2 levels of 0.33 and 0.5 were investigated with a hydrogen dilution of 50. Other deposition parameters were kept the same as before. Deposition times for these films were estimated from the deposition rates measured on thicker films on SnO_2 substrates prepared under identical conditions. Raman analysis of the films showed that on SnO_2 coated substrates the films had all amorphous character.

On glass substrates, however, substantial crystalline fractions were observed for both CO_2 levels. Considering the fact that deposition rates on glass substrates are generally lower than on SnO_2, the data indicate that, on glass substrates, a c-Si phase forms at film thicknesses considerably less than 150Å. It can then be concluded that lack of crystallinity on SnO_2 coated substrates is not simply due to the small film thickness.

To substantiate this observation we deposited the same films on the same substrates but coated *in-situ* with a very thin (≈ 10 Å) SiO_x layer. Raman spectroscopic analysis of the films indicates

the presence a c-Si phase in all cases. In the case of c = 0.43, numerical analysis of the data gives a c-Si volume fraction of 20% and 35%, respectively, for glass and SnO_2 substrates in c = 0.43. For c = 0.33, the analysis gives c-Si volume fractions of 44% and 34%, respectively, as shown in Figure 28. For both CO_2 dilutions we observed that deconvolution of the data gives smaller c-Si peak width for the films deposited on glass. This could possibly indicate that the SiO_x film thickness was thick enough to provide a base for c-Si nucleation but not thick enough to suppress totally the effect of the underlying substrate.

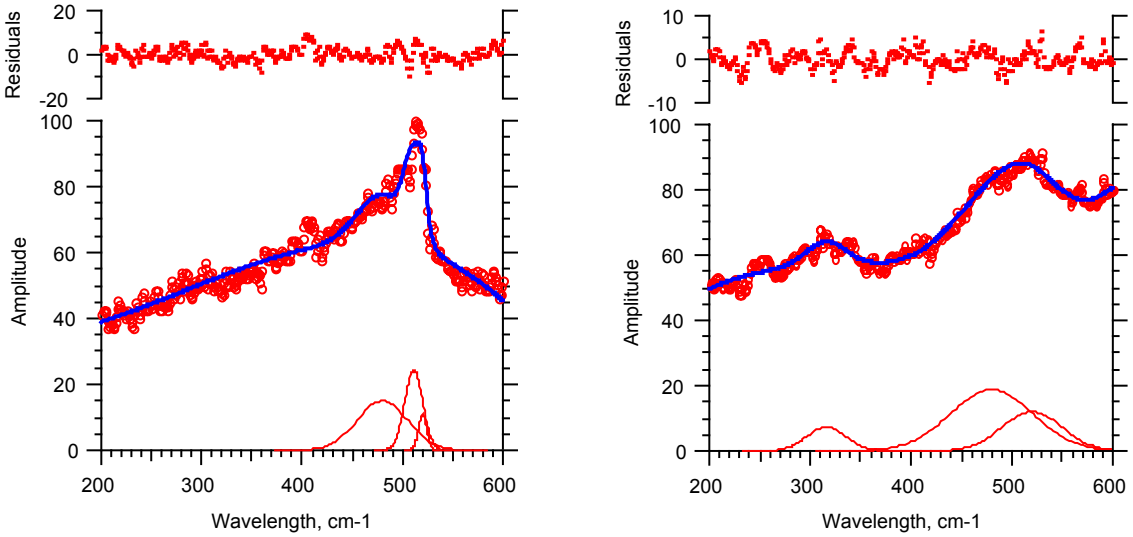


Figure 28. Raman spectra of ultra-thin films (≈ 150Å) deposited on an interlayer of ≈10Å SiO_x.

3.2.6 Conclusions Regarding Silicon Oxide p-layers

In the present work we have demonstrated the deposition, by RF-PECVD, of two phase films of B doped c-Si imbedded in a matrix of a-SiO_x:H:C for potential use as p-layers in a-Si:H based p-i-n solar cells. Structural and electrical properties of these films have been investigated as a function of SiH_4, CO_2 and B_2H_6 gas flows. Compositionally, the amorphous phase in the films contains an order of magnitude more oxygen than carbon, insuring high transparency. Low power density used for the deposition coupled with presence of CO_2 and He buffer gas in the discharge lowers the risk of chemically reducing the conductive oxides, such as SnO_2, during the deposition. At low film thicknesses similar to the p-layers in the p-i-n devices, nucleation of c-Si phase requires ≈ 10Å thick SiO_x base layer which should be operationally benign in the solar cell.

3.3 Microcrystalline silicon oxide n-layers

The n-layers deposited from SiH_4, H_2 and CO_2 were investigated similar to the procedure described earlier for the p-layers, albeit less extensively. The dopant was PH_3 with the normalized flow given by $p = f(PH_3) / [f(SiH_4) + f(CO_2)]$. Substrate temperature was 175°C.

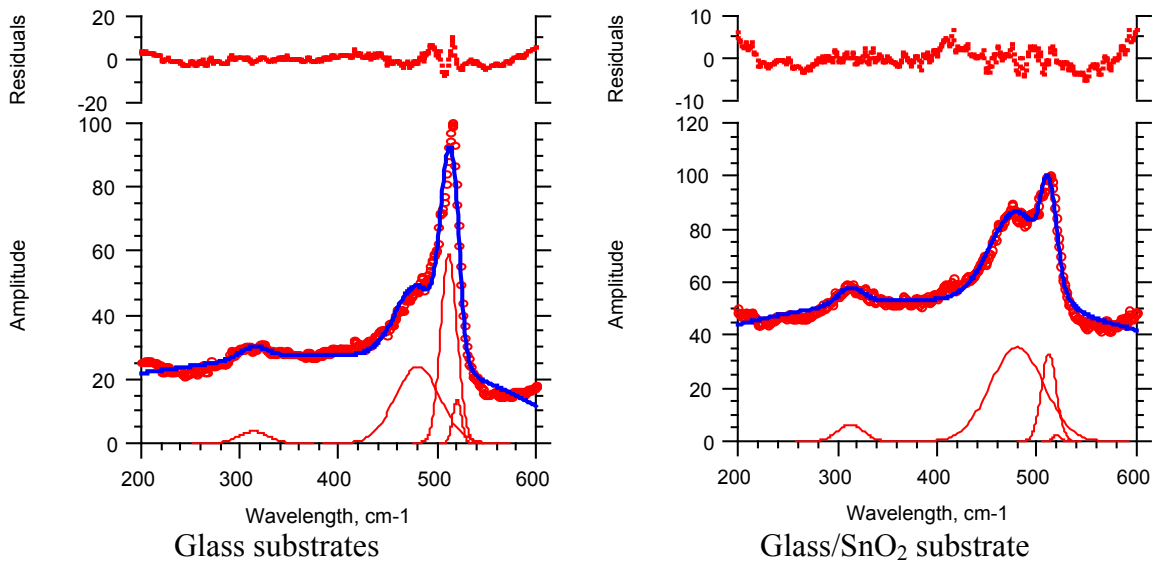


Figure 29. Raman spectra of microcrystalline n-layers deposited from CO_2 containing discharge.

Raman spectra of Figure 29 illustrate the mixed crystalline/amorphous structure of the films deposited on glass and on SnO_2 coated glass for a deposition where the reduced parameters were: f(SiH_4) = 2 sccm; Power Density = 420 mW/cm^2; Pressure = 1 Torr; h = 50; o = 0.43; p = 10^{-2}. The analysis gives c-Si volume fraction of 53% and 23% for glass and glass/SnO_2 substrates, respectively.

Characteristics of the films deposited at various CO_2 levels in the discharge for three different power densities are given below in Table 9. In these experiments total pressure, silane partial pressure, and hydrogen dilution were, respectively, 1 Torr, 9.9 mT and 50.

Table 9. Characteristics of the microcrystalline n-layer films deposited at various CO_2 levels in the discharge for three different power densities P_w.

Gas Flows (sccm)							P_w	Glass Substrate			SnO_2 Substrate	
SiH_4 (90%H_2)	CO_2	PH_3 (99.8% H_2)	H_2	He	p	c	(mW/ cm^2)	R (Å/s)	σ_d (S/cm)	c-Si (Vol%)	R (Å/s)	c-Si (Vol%)
20	0	10	73	100	0.01	0	420	0.64	16	76	0.58	63
20	1	15	117	50	0.01	0.33	420	0.50	7	58	0.61	34
20	1.5	18	140	23	0.01	0.43	420	0.39	3	53	0.39	23
20	0	10	73	100	0.01	0	253	0.50	27	66	0.53	30
20	1	15	117	50	0.01	0.33	253	0.39	14	67	0.42	38
20	1.5	18	140	23	0.01	0.43	253	0.36	5	41	0.36	23
20	2	20	163	0	0.01	0.5	253	0.28	4	66	0.31	22
20	1	15	117	50	0.01	0.33	168	0.39	19	52	0.33	33
20	1.5	18	140	23	0.01	0.43	168	0.22	12	50	0.28	23
20	2	20	163	0	0.01	0.5	168	0.22	5	49	0.28	22

Comparing these results with the p-layer results, it is found that:

3) the conductivities are significantly higher,
4) c-Si volume fractions, both for glass and glass/SnO_2 substrates, are also higher,
5) the differences in the deposition rates and in the c-Si volume fractions between glass and glass/SnO_2 substrates are smaller.

Higher discharge power densities favor the formation of the c-Si phase but the trend is not a strong one. For a given power, the c-Si volume fraction is weakly dependent on the CO_2 levels in the discharge.

The effect of the phosphine level in the discharge was estimated by comparing the film deposited at $P_w = 168$ mW/cm^2, c = 0.5, p = 0.01 to a film deposited under the same conditions but at p = 0.005. The film deposited at a lower phosphine level had similar properties except for the conductivity, which was measured to be 3 S/cm. It seems that, for this limited case, the effect of the phosphine in the discharge is limited to controlling the carrier concentration in the c-Si phase.

3.4 Effect of H_2 Treatments on Optical and Electronic Properties of SnO_2 Substrates Used for a-Si Solar Cells

3.4.1 Background

SnO_2-coated glass is the leading transparent conductive oxide (TCO) substrate for commercial fabrication of amorphous silicon (a-Si) p-i-n solar electric modules. PECVD is the most common a-Si deposition technology for these modules. It has been well known for over 15 years that exposure of SnO_2 films to H-rich plasmas, as occur in the deposition of a-Si by plasma CVD, can lead to degradation in the SnO_2 optical transmission under some plasma conditions. The SnO_2 is chemically reduced, leaving a thin but highly absorbing Sn-rich layer [27,28,29]. Incorporation of Sn or O_2 contaminants during subsequent a-Si solar cell deposition can lead to a

decrease in junction performance. This sensitivity of SnO_2 to H_2 plasma is a barrier to development of high performance p-layers which may require highly H_2 diluted plasmas.

It has been reported that degradation can be minimized or even eliminated by using low substrate temperatures [29,30], faster a-Si growth rates [30], or by covering the SnO_2 with a thin protective layer of sputtered ZnO [30,31,32]. The ZnO properties are relatively inert to reduction in H_2 plasma [29,30] although the H_2 penetrates several hundred Angstroms into the ZnO [30,33,34] and increases its bandgap [33,35]. However, there are conflicting reports saying that ZnO is also reduced by the plasma [35] or that it fails to protect the underlying SnO_2 layer [36,37]. Differences in the plasma conditions, substrate temperature and time, and in the ZnO thickness makes resolution of these opposing conclusions difficult.

One of the leading SnO_2 manufacturers, Asahi Glass, had shown that the optical transmission of their SnO_2 is not degraded by H_2 plasma over the range from 100 to 300°C [38], in direct contradiction to results from other groups, as well as their own later work [31]. They found that the electronic properties, primarily the mobility, were improved and concluded that optimization of SnO_2 properties using H_2 plasmas required a delicate balance between enhancement of electrical properties and simultaneous degradation in optical properties. Smaller improvements were reported with annealing SnO_2 in H_2 gas without the plasma but they only explored up to 200°C [38].

Therefore, we have studied the influence on the SnO_2 optoelectronic properties of the substrate temperature during H_2 plasma exposure or H_2/Ar annealing at higher temperatures using SnO_2 from several commercial suppliers. H_2 plasma exposures greater than a few minutes are probably not relevant to understanding a-Si TCO/p-i-n solar cells because the TCO is typically covered with a ~20 nm thick p-layer by that time, which shields it from the H_2 plasma. Typical temperatures for p-layer depositions in devices are 150-200°C. We used these practical limits in designing our experiments. We also evaluated whether the sputtered ZnO layer could simultaneously protect the SnO_2 from damage during plasma exposure yet still allow the improvement in electronic properties. Finally, the effect of depositing a thin μc-Si layer was investigated.

3.4.2 Experimental Techniques

The textured SnO_2 substrates were made by Asahi Glass Co. (Asahi Type U), AFG Industries (AFG PVTCO), or Libbey Owen Ford (LOF Tec 8). Initial sheet resistances (R_{SH}) were ~13, 10, and 8 Ω/sq and thicknesses were 0.8, 1.0, and 0.55 μm, respectively. Samples of area 2.5 x 2.5 cm^2 were cut from much larger plates (~900 cm^2). The H_2 plasma conditions were 30 Watts, 100 sccm of H_2 at 1 Torr for 1 minute. The substrate temperatures were 100, 150 and 200°C. These conditions are similar to those used in the study by Asahi [38] and similar to those that might lead to microcrystalline Si growth with the addition of SiH_4 [39,40]. The H_2/Ar annealing conditions (no plasma) were 1 atmosphere of forming gas (2% H_2) at 200, 300, and 400°C for 30 minutes. Some samples were also annealed in 1 atmosphere of air or Ar at 300°C for 30 minutes to compare to the H_2/Ar treatment. The Si deposition was under conditions which have yielded >80% crystallinity at similar thickness on glass: 50 Watts, SiH_4/H_2 = 20/200 sccm at 1 Torr, 150°C, for 2 minutes. The Si growth rate is ~ 0.2 Å/s.

Some SnO_2 substrates were coated with 20 and 60 nm sputtered ZnO layers before H_2 exposure. The ZnO thicknesses were chosen to evaluate the protective abilities based on published H profiles [30,33,34] in sputtered ZnO due to plasma exposure. A 60 nm ZnO layer would reduce the H penetration into the SnO_2 by 1-2 orders of magnitude compared to a 20 nm layer. The 60 nm ZnO has ~2% optical absorption so any film thicker than 60 nm would add unacceptable absorption losses to an a-Si superstrate solar cell. The sheet resistances of the 20 and 60 nm ZnO films were 900 and 250 Ω/sq, respectively. They were rf sputtered from Al doped ZnO targets onto unheated Asahi SnO_2 substrates at 3 mT in an Ar/O_2 atmosphere. Four substrates were placed in each H_2 plasma exposure or Si deposition: Asahi SnO_2 with 0, 20 or 60 nm ZnO protective layers, and a piece of AFG PVTCO. For the H_2/Ar treatments, a piece of LOF Tec 8 was also included.

Total transmission was measured using a Perkin Elmer Spectrophotometer with an integrating sphere. Hall effect measurements were made with magnetic fields of 10-15 kG and currents of 20-40 mA using Ag paste contacts on the corners. Results at several different currents and fields were averaged. Based on repeated measurements on multiple samples (typically 2 or 3 per treatment), and initial sample-to-sample variation, we feel that a 10% error bar should be applied to the electrical measurements.

3.4.3 Results

3.4.3.1 Bare SnO_2 Substrates

Figure 30(a) and Figure 30(b) show the optical transmission of the Asahi and AFG samples, respectively, following H_2 plasma exposure at 150 and 200°C. For both brands of SnO_2, H_2 plasma exposure at 100°C (not shown) or 150°C resulted in no change to the transmission while plasma exposure at 200°C caused losses in the visible transmission. This strong temperature dependence in this range is consistent with results of others [29,40]. The decrease in transmission is attributed to increased absorption by the Sn-rich layer formed by chemical reduction of the SnO_2 [27]. Losses are much greater for the AFG SnO_2 compared to the Asahi SnO_2. Figure 30(c) compares the transmission of the Asahi and AFG SnO_2 after annealing at 400°C in H_2/Ar. The transmission decreased ~1% between 400 and 600 nm. In comparison to the H_2 plasma exposure, there was essentially no change in transmission with the H_2/Ar treatments. From Figure 30(a-c), we conclude that the threshold for damage to SnO_2 in a H_2 plasma is between 150 and 200°C, but that no significant degradation occurs with annealing in H_2/Ar up to 400°C. Note that 150-200°C is in the range of substrate temperatures reported for μc-Si p-layer growth in highly H_2-diluted plasmas [39,40]. Results for the LOF Tec 8 material were similar.

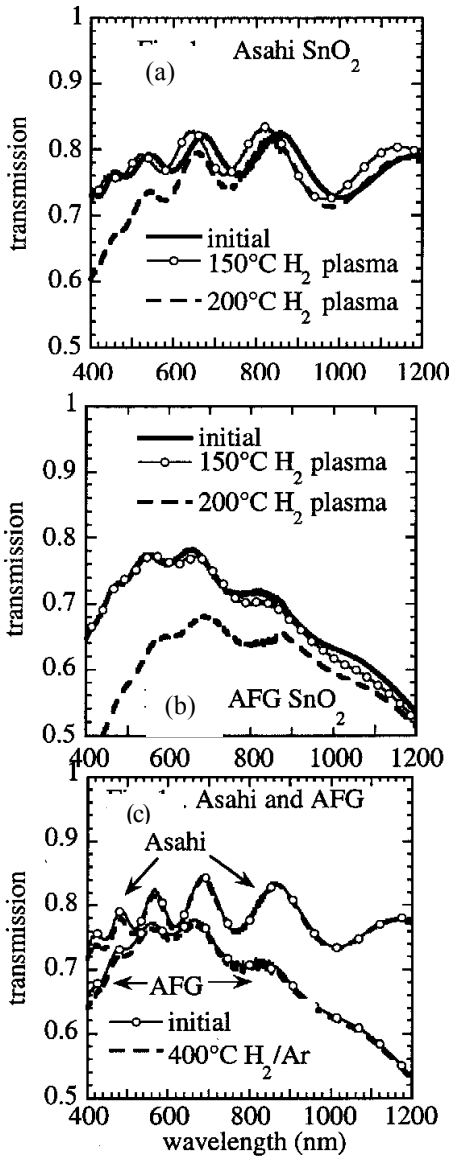


Figure 30. Transmission of SnO_2 films before and after various H_2 treatments: (a) Asahi SnO_2 after H_2 plasma treatments at 150 or 200°C; (b) AFG SnO_2 after H_2 plasma treatments at 150 or 200°C; (c) Asahi and AFG SnO_2 after 400°C H_2/Ar treatment.

The effect of substrate temperature during H_2 plasma or H_2/Ar anneal on SnO_2 sheet resistance, mobility and carrier concentration are shown in Figure 31(a), (b), and (c), respectively. All three properties from the AFG and Tec 8 SnO_2 were essentially unchanged by any of the treatments, as indicated by the straight horizontal lines. In contrast, the Asahi SnO_2 electrical properties improve with increasing substrate temperature for both types of H_2 treatment. Figure 31(a) shows that R_{SH} for Asahi SnO_2 decreases from an initial value of ~13 down to 7-8 Ω/sq with H_2 plasma or H_2/Ar treatments. However, different temperatures are required to achieve this lower value. For example, at 200°C, R_{SH} for the Asahi SnO_2 has decreased from ~13 to ~8 Ω/sq with

H_2 plasma treatment but only to ~12 Ω/sq with the H_2/Ar anneal. Figure 31(b) shows that the Hall effect mobility for Asahi SnO_2 increases with increasing substrate temperature during the plasma treatments, nearly doubling from ~30 to ~60 cm^2/V-sec. This is a substantial increase, and similar to those reported by Asahi and attributed to a reduction in grain boundary barrier height [38]. H_2/Ar annealing requires temperatures of 400°C to achieve the same increase in mobility, but this is achieved without the optical degradation which occurs in the plasma, as seen by comparing the Asahi transmission in Figure 30(a) and Figure 30(c). Figure 31(c) shows that, within the experimental error, the carrier density is unaffected by the treatments on all SnO_2 samples, indicating that the H_2 plasma doesn't change the defect density or doping in the SnO_2. Also note that the AFG and LOF SnO_2 have a higher carrier density than the Asahi.

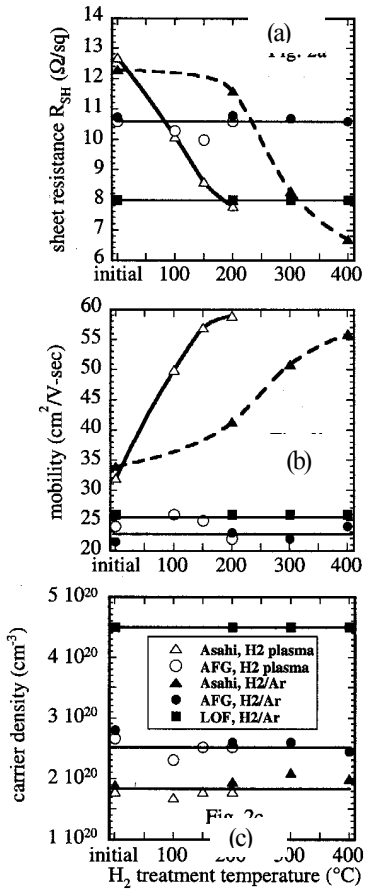


Figure 31. Electronic properties of Asahi, AFG and LOF SnO_2 before and after H_2 plasma treatments at 100, 150 and 200°C, and H_2/Ar treatments at 200, 300 and 400°C: (a) sheet resistance; (b) mobility; and (c) carrier density.

3.4.3.2 SnO_2/ZnO Substrates

Pieces of Asahi SnO_2 were covered with 20 or 60 nm of sputtered ZnO to determine whether the ZnO layer, while protecting the SnO_2 from optical degradation, would still allow the H_2 treatments to improve the SnO_2 mobility. Only Asahi SnO_2 was included in this portion of the

study since it was the only material to show improvements in the mobility with H_2 or H_2/Ar treatments. Figure 32 shows the transmission of the Asahi SnO_2 with 20 nm ZnO following a 200°C H_2 plasma treatment or 400°C H_2/Ar treatment compared to the as-deposited bilayer. They are all essentially the same. Below 600 nm, the 200°C H_2 plasma caused significant degradation to the transmission of *bare* SnO_2 (Figure 30(a) and 400°C H_2Ar caused slight, <2%, degradation to the transmission of *bare* SnO_2 (Figure 30(c) but the 20 nm ZnO successfully protects the SnO_2 from both treatments. The transmission of pieces with 60 nm ZnO were also unaffected by H_2 plasma at 200°C. Thus, 20 nm of ZnO is sufficient to protect the SnO_2 from damage in agreement with others [30,31].

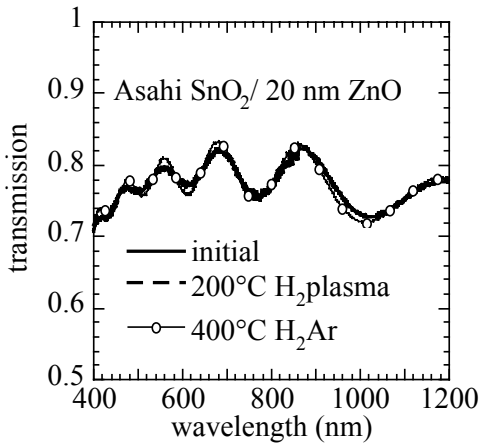


Figure 32. Transmission of Asahi SnO_2 with 20 nm ZnO layer following H_2 plasma or H_2/Ar treatments as shown.

The resistivity and mobility of the Asahi SnO_2 with 0, 20 or 60 nm of ZnO are shown in Figure 33(a) and Figure 33(b), respectively, as a function of the same H_2 treatment conditions as in Figure 31(a-c), i.e., H_2 plasma or H_2/Ar anneal. Deposition of the ZnO appears to cause a small but repeatable decrease in R_{SH} , from 13 to 12 Ω/sq, even before H_2 treatment, compared to the bare SnO_2, for reasons which are not understood. (Even larger decreases in R_{SH} for ZnO-coated SnO_2 can be seen in Reference 31.) With H_2 plasma or H_2/Ar treatments, R_{SH} decreases nearly the same, independent of the ZnO layer. Figure 33(b) shows that the reason for the decrease in R_{SH} is an approximately factor of 2 increase in mobility, same as for bare SnO_2. Thus, 20 or 60 nm thick ZnO layers allow the same improvement in SnO_2 electronic properties as no ZnO layer while preventing the degradation in optical properties.

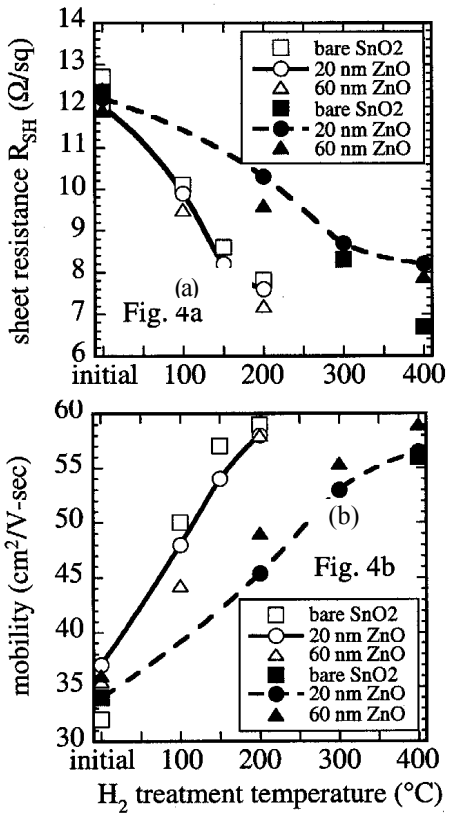


Figure 33. Electronic properties of Asahi SnO_2 with 20 or 60 nm ZnO layers before and after H_2 plasma treatments at 100, 150, and 200°C (open symbols), and H_2/Ar treatments at 200, 200, and 400°C (closed symbols): (a) sheet resistance; and (b) mobility.

3.4.3.3 Effect of Ambient During Heat Treatment

Having established that H_2/Ar was effective in doubling the mobility, we also investigated Ar and air treatments at 300°C for 30 minutes. The results are shown in Table 10. Treatments in H_2/Ar or air were approximately equivalent, increasing the mobility of Asahi SnO_2 from 30 to 50 cm^2/V-sec, while those in air were less effective. This shows it is not the H_2 *per se* which is responsible for the improved mobility but rather the exposure to heat in a non-oxidizing atmosphere. This suggests that the increase in mobility is due to a decrease in trapped O_2 or O_2-related species which escape during the thermal treatment, and is discussed further in section 3.4.4. There were no changes in the AFG or LOF SnO_2 with any ambient.

Table 10. Effect of treatments in H_2/Ar, Ar, or air at 300°C for 30 minutes on Asahi and AFG SnO_2, and on Asahi SnO_2 with 20 nm ZnO layer.

Sample	Condition	R_{SH} (Ω/sq)	Mobility (cm^2/V-sec)
Asahi	initial	13	31
	H_2/Ar	8	51
	Ar	7	52
	Air	9	40
AFG	Initial	11	24
	H_2/Ar	11	23
	Ar	11	24
	Air	11	24
Asahi/ZnO	Initial	12	34
	H_2/Ar	8	53
	Ar	n/a	n/a
	air	n/a	n/a

3.4.3.4 Effect of μc-Si deposition

A ~2 nm μc-Si film was deposited at 150°C on Asahi SnO_2 with 0, 20 and 60 nm thick ZnO layers, and on AFG SnO_2. There is no degradation in transmission on any of the substrates, similar to the situation where the SnO_2 was exposed to just H_2 plasma at 150°C as in Figure 30(a). The Si layer was so thin that it had negligible absorption itself.

Table 11gives R_{SH} and mobility for samples before and after μc-Si deposition or H_2 plasma exposure at 150°C for Asahi SnO_2 with and without ZnO layers, and for AFG SnO_2. The electrical properties of the Asahi SnO_2 improve with the μc-Si deposition, i.e., mobilities increase from ~30 to ~45 cm^2/V-sec. Within the 10% experimental uncertainty and sample-to-sample variation, the H_2 plasma and the μc-Si film deposition had comparable effect. This suggests that the Asahi SnO_2 electronic properties will improve during deposition of an a-Si p–I–n solar cell if the p-layer has a highly diluted plasma. If the deposition is below 200°C, this may be accomplished without optical losses. The mobility of the AFG SnO_2 showed no improvement with the μc-Si deposition, consistent with its behavior in a H_2 plasma (Figure 31(b)).

Table 11. Effect of 150°C μc-Si layer deposition (2 minutes) or H_2 plasma (1 minute) on Asahi and AFG SnO_2, and on Asahi SnO_2 with 20 nm ZnO layer.

Sample	Condition	R_{SH} (Ω/sq)	Mobility (cm^2/V-sec)
Asahi	Before μc-Si	13	32
	After μc-Si	9	44
	After H_2 plasma	8	57
AFG	Before μc-Si	11	24
	After μc-Si	10	25
	After H_2 plasma	10	25
Asahi/ZnO	Before μc-Si	12	35
	After μc-Si	8	45
	After H_2 plasma	8	54

3.4.4 Discussion

There are several points worth noting regarding the effect of H_2 treatments on the bare SnO_2. First, substantial improvements in mobility are possible even at 150°C (Figure 31(b) with the H_2 plasma or μc-Si deposition, which is below the threshold for optical degradation (Figure 30(a)), which indicates that the beneficial action of the plasma occurs below the damage threshold. Thus, the degradation and enhancement mechanisms are different. Second, improvements in mobility only occurred for SnO_2 films with carrier densities below ~ 2 x10^{20} cm^{-3} , which is very consistent with the results from Asahi [38]. Our results are more general since they were obtained on SnO_2 films from different manufacturers. Third, the improvement in Asahi SnO_2 electronic properties occurs at lower temperatures for the H_2 plasma compared to the H_2/Ar or Ar anneals, suggesting that plasma, containing excited H or atomic H, is a more effective reducing environment. Fourth, pieces of SnO_2 obtained from different batches from each of the manufacturers over the more than a four year period have all responded similarly, indicating that these results are not unique to a single lot of SnO_2 from any source. Fifth, annealing in air increased the mobility although less than in Ar or H_2/Ar. And sixth, the improvement in electronic properties with H_2 plasma was stable over two years. Samples whose R_{SH} and mobility had changed by a factor of two following H_2 plasma or H_2/Ar treatments were remeasured after two years of storage in air at room temperature and had the same low sheet resistance and high mobility as was found immediately after the H_2 treatments.

Next, we discuss the electronic mechanisms to explain these results by establishing that the mobility is limited by scattering at grain boundaries, not impurity scattering in the grains, and that desorption of oxygen trapped in the grains is responsible for the annealing results reported here. There is disagreement in the literature whether the transport-limiting scattering occurs at grain boundaries due to the energy barrier, or in the grains due to ionized or neutral impurity scattering. It is claimed [41], based on general analysis of transport in polycrystalline materials, that for moderate values of bulk grain carrier density, i.e., $N < 10^{18}$ cm^{-3}, the mobility should be governed by the barrier height of the grain boundaries, while for higher carrier density, i.e., $N > 10^{20}$ cm^{-3}, as in the films measured here, the mobility should be dominated by carrier scattering within bulk grains since the barrier width becomes negligible at such high N [42]. But

other groups [43,44,45] conclude that grain boundary scattering dominates even at values of $N > 10^{20}$ cm^{-3}. For ionized impurity scattering, mobility should vary as $N^{-2/3}$, yet the mobility is independent of N in this range [42,43,45], providing further confirmation that the mobility is limited by a scattering at the grain boundary potential barrier, not by impurity scattering. Perhaps the strongest evidence for grain boundary scattering is that single crystal SnO_2 has mobilities of ~90 cm^2/V-s, which are higher than those reported for as-deposited polycrystalline SnO_2, typically ~20-30 cm^2/V-s.

Sato *et al.* [38] measured the activation energy for the mobility as a function of carrier density and found that the H_2 plasma treatments reduced the barrier from 20 to 10 meV for the low N films ($< 3x10^{20}$ cm^{-3}) but had no effect on the barrier for $N > 4x10^{20}$ cm^{-3}. They speculated that the negatively charged trap density at the grain boundary decreases via neutralization by a proton from the plasma. However, we have shown here that the mobility increases equally with Ar annealing, implying that H_2 passivation or proton formation is *not* the dominant mechanism in the H_2 plasma treatments and, in fact, is not even required. Shanthi *et al.* [46] showed in 1980 that annealing in vacuum resulted in increased mobility similar to annealing in Ar, N_2 or H_2. But annealing in pure O_2 resulted in decreased mobility and the effects were reversible between O_2 and vacuum annealing. The activation energy for the mobility *increased* from 20 to 50 meV upon O_2 annealing [46]. Combined with the *decrease* in barrier upon H_2 annealing from Sato [38], this clearly identifies desorption or absorption of O_2 as responsible for the changes the grain boundary barrier height and hence for the changes in mobility. As in our study, Shanthi [46] found no change in N for any of the annealing ambients, confirming that the changes in O_2 do not affect the ionized impurities in bulk grains since oxygen vacancies are donor defects.

Thus, the grain boundary barrier is strongly influenced by O_2 or O_2-related species physically trapped at the grain boundaries. We speculate that thermal treatment in a reducing atmosphere, which includes Ar or vacuum, eliminates oxygen-related defects, which form at grain boundaries during SnO_2 growth at atmospheric pressure in air. The fact that H plasma was more effective than H_2 is consistent with the known ability of reactive H plasma to "clean" surfaces, especially of oxides. Additionally, the plasma treatments were at 1 T while the H_2/Ar treatments were at 1 atmosphere. The lower pressure of the plasma treatments gave an even greater driving force for out-diffusion of oxygen-species from the grain boundaries, effectively combining a H_2 exposure with low-pressure anneal.

If O_2 desorption is responsible for the increase in the mobility, why did the mobility increase for the Asahi films annealed in air? Shanthi [46] proposed that O_2 is absorbed and desorbed at different rates. At a given temperature, a dynamic equilibrium is established based on these rates and the ambient O_2 partial pressure. The result could be a net loss or gain of O_2. The increase in mobility was about half as large as with annealing in a reducing atmosphere, consistent with the above discussion. It is likely that the Asahi films annealed in air still had a net decrease in O_2, although smaller than for H_2/Ar or Ar.

Further circumstantial evidence that desorption is affecting grain boundaries is the speed at which the reaction must occur. Both this work and Reference 38 used 1 minute H_2 plasma exposures. Changes in film properties over such short treatment times and relatively low temperatures are consistent with diffusion along grain boundaries not into the grain bulk.

The AFG and LOF films studied here behaved like the high carrier density films in References 38 and 42, i.e., their mobilities were unaffected by the plasma or annealing treatments because they were limited by ionized impurity scattering within the grain, not at the grain boundary.

How can ZnO protect the SnO_2 from H_2 plasma damage while at the same time allowing improved mobility? As already mentioned, ZnO is much more resistant to reduction than SnO_2 under the conditions used here. The 20-60 nm ZnO layers allow the beneficial elimination of SnO_2 grain boundary scattering centers by desorbing O_2 but prevents direct interaction of the SnO_2 with the excited H radicals which chemically reduces the SnO_2. While the ZnO is shielding the SnO_2 from some deleterious types of H radicals, the ZnO is porous enough to allow trapped O_2-related species to escape. The small but repeatable increase in mobility discussed in Section 3.4.3.2 with the application of ZnO at room temperature (even larger increases are shown in Reference 31) may be due to O_2 desorption under the vacuum (2 mT) during ZnO sputtering.

These results suggest a strategy for developing an optimum SnO_2 product for superstrate a-Si device fabrication. The SnO_2 should be deposited with a low carrier density, < 2 x1020 cm^{-3}, then H_2/Ar or Ar treatments performed at 300-400°C. This will provide a lower SnO_2 sheet resistance without increased absorption losses which normally accompany higher doping or the H_2 plasma degradation. Alternatively, a 20 nm ZnO layer could be sputtered to protect the surface, but this is undesirable for two reasons. First, it requires another costly processing step, and second, problems with making high quality devices with SnO_2/ZnO bilayer substrates are commonly reported [47].

Finally, we did not try to optimize the H_2 plasma or H_2/Ar treatments to maximize improvements in mobility. The Asahi group achieved a R_{SH} of 5 Ω/sq and a mobility of 70 cm^2/V-sec, using plasma exposure of a ZnO coated SnO_2 substrate at 300°C for 1 minute [31]. This is close to our best result obtained at 200°C for 1 minute of a R_{SH} of 7 Ω/sq and a mobility of 60 cm^2/V-sec. But the SnO_2 films had different values of initial R_{SH} and thickness so closer comparison is not warranted.

3.5 Characterization of the SnO_2/p and ZnO/p Contact Resistance and Junction Properties in a-Si p-I-n Solar Cells and Modules

TCOs are critical to the optical and electrical performance of a–Si based solar cells. This is especially true for superstrate a-Si p-i-n solar cells which are deposited on a glass/TCO substrate. Electrically, the TCO must have low lateral sheet resistance since there are no grids and low contact resistance with the p-layer. The TCO must be robust, inert to subsequent chemical and thermal device processing and also must be able to be laser scribed with high yield.

Minimizing the resistance between the p-layer and TCO of superstrate p-i-n a-Si devices and modules is a critical issue for utilizing new TCO materials like ZnO and new p-layers like μc–SiC or μc–SiO. Compared to SnO_2, ZnO typically gives higher short circuit density (J_{SC}) due to lower absorption losses but poorer electrical performance commonly attributed to the ZnO/p interface, forming a non-Ohmic contact. Various schemes to improve the ZnO/p electrical contact have been discussed. However, characterization of the TCO/p interface is difficult since it is in series with the dominant p-i-n junction.

We have developed two new methods to characterize the TCO/p contact and the SnO_2 sheet resistance in a completed device structure. One method requires having two adjacent TCO regions, e.g., strip A and strip B. The p-I-n device on strip A is biased to have standard current flow through its TCO/p contact and TCO region while the voltage is measured on the adjacent TCO pad B which is electrically floating. We call this the V_{AB} method. This procedure can be applied to scribed sub-modules having individual cell contacts placed on each strip. It was applied to devices made at BP Solar on different types of SnO_2 (Asahi, AFG, and LOF) and was presented at the Material Research Society Symposium, San Francisco, CA, April 5–10, 1999 (Appendix 1, Ref. 1). A second method does not require electrical contacting of the adjacent TCO strip, only a single isolated strip of TCO/pin/contact cell structures. The junction and contact properties are obtained from analysis of dV/dJ from each of several devices on the strip of TCO. But the analysis to obtain the TCO/p contact resistance is essentially the same. The dV/dJ method was applied to a series of devices made at BP Solar having different p-layers as well as ZnO protective layers on the SnO_2. Analysis of temperature dependent JV measurements using this special configuration can be used to determine the activation energy of the TCO/p contact resistance. This technique was presented at the 28th IEEE PVSC in Anchorage, AK, September 15-22, 2000 (Appendix 1, Ref. 16).

Table 12 lists the values of $R_{TCO/p}$ obtained from the analysis of the dark JV curves as described in two papers, the dV/dJ method from the 28th IEEE PVSC paper (Appendix 1, Ref. 16) and the V_{AB} method (Appendix 1, Ref. 1) from the 1999 MRS Symposium. The good agreement verifies the two approaches. The dV/dJ method is simpler to implement but does allow the JV curve of the TCO/p contact to be obtained explicitly as in the V_{AB} method. Also listed are the V_{oc}, J_{sc} and FF for the best device on each piece. This table compares devices with and without the ZnO protective layer. Regarding the SnO_2 samples, there was little difference between the 30-minute or 15-hour bakeout, but the 3–minute H_2 plasma degraded all parameters, presumably due to chemical interaction between the plasma and the SnO_2 (see Section 3.4). Note that this resulted in the lowest J_{sc} and $R_{TCO/P}$, consistent with formation of a metallic Sn layer on the surface. The ZnO substrates had very low V_{oc} and FF with the 30-minute bakeout. Significant improvement in V_{oc} and somewhat less in FF occurred with the longer bakeout. FF continued to improve with the H_2 plasma treatment, opposite to the change in devices on the SnO_2 substrates. However, the crucial conclusion from Table 12 is that there was no significant difference in $R_{TCO/P}$ for SnO_2 or ZnO substrates. The reason for poor V_{oc} and FF with ZnO must be found elsewhere. As described in the 28th IEEE PVSC paper (Appendix 1, Ref. 16), it is the diode factor and recombination current which increases with ZnO, especially with certain treatments.

Table 12. R_C from 2 methods for devices on SnO_2 and ZnO/SnO_2 with different predeposition treatments. Also shown are device performances: (a) dV/dJ method (Appendix 1, Ref. 16); and (b) V_{AB} method (Appendix 1, Ref. 1).

TCO	Treatment (Ar bakeout or H_2 plasma)	(a) $R_{TCO/p}$ (Ω-cm^2)	(b) $R_{TCO/p}$ (Ω-cm^2)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)
Asahi	30 min Ar	1.3	1.0	0.89	13.3	70
ZnO/Asahi	30 min Ar	1.4	1.3	0.70	13.2	56
Asahi	15 hr Ar	0.8	0.6	0.90	12.5	71
ZnO/Asahi	15 0hr Ar	0.6	n/a	0.86	13.0	60
Asahi	30 min Ar then 3 min H_2 pl.,	0.4	0.3	0.79	9.3	58
ZnO/Asahi	30 min Ar then 3 min H_2 pl.,	1.3	n/a	0.83	12.0	64

A crucial result of this work is that the ZnO layer does not contribute to a higher contact resistance or a blocking diode, as is commonly believed. Using the MRS method, the JV characteristic of the TCO/p contact can be measured directly. No evidence for a blocking contact, a photovoltaic junction or a high resistance was found. Instead, ZnO changes the p/i junction recombination. A brief summary of the other key conclusions follows.

Values of the contact resistance (R_C) of 1 ± 0.5 Ω-cm^2 were found for a wide range of TCO and p-layer processing including ZnO. Temperature dependence of R_C gave barrier height of 40-55 meV. Analysis of devices with a thin ZnO layer on SnO_2 and with different predeposition treatments indicates that the lower V_{oc} and FF observed with ZnO is not due to the contact but to changes in the p/i junction recombination. The solar cell performance is very sensitive to the ZnO surface treatment, but R_C is not. No evidence was found for a blocking or high resistance ZnO/p contact. The "ZnO/p" contact problem is not really due to the ZnO/p contact resistance or a barrier, but rather to an increase in recombination.

3.6 Analysis of QE to Determine Optical Enhancement

Optical enhancement in a-Si solar cells is a well-known technique to increase the absorption efficiency of weakly absorbed light, and is critical for improving the performance of single or multijunction p-i-n or n-i-p devices. Optical enhancement increases the optical path length so that the device has an effective optical thickness of $\boldsymbol{m}$d where d is the physical thickness of the i-layer. The parameter $\boldsymbol{m}$ represents the increase in absorption length, and is a measure of the optical enhancement for weakly absorbed light due to both oblique scattering and multiple passes. The theoretical thermodynamic upper limit is $\boldsymbol{m}$~$4n^2$ where n is the index of refraction of the absorber. With n~4 for a-Si, the upper limit for $\boldsymbol{m}$ is ~60, but this decreases rapidly to ~10-20 with even a few percent losses due to parasitic absorption at the interfaces.

There are two methods to increase the optical enhancement, or light trapping, and both must be achieved simultaneously to gain the full benefit. First, the substrate must be textured, which increases the path length by scattering the normally incident light at an angle away from normal.

Second, the back surface must be textured and have high reflectivity so that a large fraction of photons reaching that back contact are reflected and scattered back into the i-layer without losses.

Studies of optical enhancement and light trapping in a-Si solar cells typically fall into one of two categories: 1) use of changes in the short circuit current (J_{SC}) or the long wavelength quantum efficiency (QE) as an empirical measure of the optical enhancement; or 2) use of an optical model based on detailed calculations of the reflection, absorption, transmission, and scattering at each interface using either coherent wave theory or geometric ray optics treatment to characterize the optical behavior of the multilayer structure.

We have developed an approach which bridges the gap between the empirical and the theoretical approaches by presenting a quantitative analysis of the QE of a wide range of a-Si p-i-n solar cell device structures. The measured QE data at long wavelengths is fit with a simple, analytical model having one adjusted parameter, ***m***, as a function of wavelength. All other optical characteristics of the device are measured separately and incorporated in the analysis. The experimental variables investigated include the i-layer thickness, d, from 0.14 to 0.92 μm, the SnO_2 texture (lightly textured LTX or highly textured HTX), and the back reflector (BR) structure (Al, ZnO/Al, or ZnO/Ag). A full report of this work has been accepted by *Progress in Photovoltaics* for publication in 2001 (Appendix 1, Ref. 34). A summary of the results is given below.

Figure 34 shows ***m*** for four devices having a very thin i-layer, d = 0.14 μm. The SnO_2 textured substrate and back reflector is different for each piece, as indicated in the figure. There is little optical enhancement with the Al BR for either the LTX or HTX SnO_2 for either the thinnest or thickest i-layer. Values of ***m*** are generally less than 1.5 with Al contacts on the LTX or HTX substrates for all device thicknesses studied here. This indicates a strong reduction in multiple passes due to the Al BR regardless of how textured the SnO_2 is. But ***m*** increases significantly with ZnO/metal contacts on HTX SnO_2, saturating at ***m***~3-4. We found that the ZnO/Ag BR enhances light trapping more in thin devices compared to thicker ones. These results confirm the critical importance of a ZnO (or any other TCO buffer layer) between the Si and metal layers for improving optical enhancement of the QE.

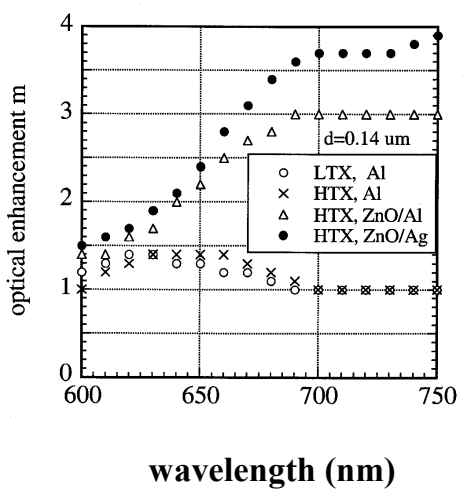


Figure 34. Enhancement *m* for devices with all 4 combinations of SnO_2 with d = 0.14 μm.

We found that for a given device structure, ***m*** decreases at a given wavelength with increasing thickness. This suggests that ***m*** depends on the product αd, not just d. With decreasing αd, ***m*** continues to increase, then saturates for very weakly absorbed light, αd < 0.1. The peak value of ***m*** increases with increasing reflectivity of the BR.

Besides gains in QE due to optical enhancement, we also considered the losses due to parasitic absorption. The effect of the substrate texture and back contact on parasitic absorption is seen in Figure 35 which shows the total absorption for samples with the 3 different BRs used in this study along with bare a-Si (no BR). There are three different substrates represented; smooth glass, LTX SnO_2, and HTX SnO_2. Each has 0.5 μm a-Si layer. The structure was glass/ (LTX or HTXSnO_2) / 0.5 μm a-Si i-layer / BR or air. Some samples had no BR other than air. Comparing first the samples with air as the BR (no contact) beyond 800 nm, absorption in the i–layer on smooth glass is <1%, absorption of the sample on LTX SnO_2 is about 25%, while HTX SnO_2 is greater than 50%. This indicates that the textured SnO_2 is responsible for a very significant fraction of the parasitical absorption. The absorption of the samples with a BR is greater than 70%. Figure 35 shows that large parasitic absorption losses occur at the textured Al/Si interface and that ZnO/Al reduces the absorption compared to Al, confirming the importance of a dielectric buffer. There is only a slight difference between ZnO/Ag and ZnO/Al, as expected. However, even with no BR, absorption of about 50% of the light is unaccounted for beyond 800 nm with the HTX SnO_2.

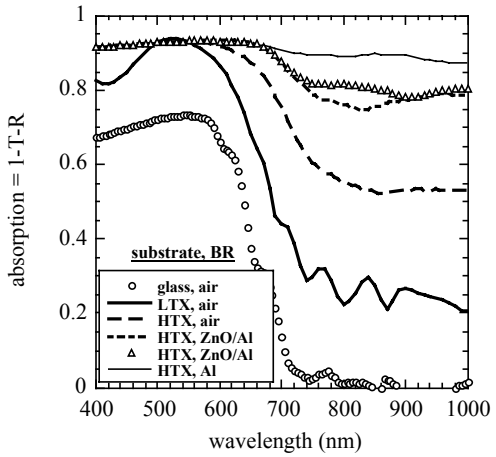


Figure 35. Absorption (A = 1-T-R) in glass/HTX/a-Si/BR, glass/LTX/a-Si (solid line) or glass/a-Si (open circles) structures. The a-Si was 0.5 µm. Devices without BR contact listed as having "air" as BR.

Where is this light being absorbed? The most likely parasitic loss as at long wavelengths is light absorbed in the textured SnO_2. Critical angle trapping inside the SnO_2 will lead to multiple internal reflections or light piping in the SnO_2. The weakly absorbed light will "bounce around" until it is either reflected out of the glass, absorbed in the SnO_2, or absorbed at the back contact. The LTX SnO_2 had less of this effect consistent with having less texture, hence light trapping. This suggests that in a solar cell, light which is reflected from the BR but not absorbed in the i–layer can be trapped in the SnO_2, remaining there instead of re-entering the i-layer.

3.7 HWCVD of Silicon Films and Reactor/Reaction Analysis and Modeling of HWCVD

During the period of this contract, two papers, which summarize our work on the deposition of silicon films by HWCVD and the modeling of this process, were published in the *Journal of Industrial and Engineering Chemistry Research*. The first of these papers, titled "Hot-Wire Chemical Vapor Deposition of Silicon from Silane: Effects of Process Conditions," (Appendix 1, Ref. 30) describes the hot-wire chemical vapor deposition and characterization of silicon. The second paper, titled "Reactor and Reaction Model for Hot-Wire Chemical Vapor Deposition of Silicon from Silane," (Appendix 1, Ref. 33) describes a reactor/reaction model of the HWCVD process.

3.8 Grain Enhancement of HWCVD Films

3.8.1 Post-Deposition Grain Enhancement of HWCVD Si Films

One of the critical issues in the development of thin film silicon devices is the grain size. Typically, films deposited by HWCVD exhibit grain sizes between 10-50 nm. It is expected that the excessive number of grain boundaries in such films will lead to considerable carrier recombination and poor device performance. During this contract period, our focus has been to

evaluate various *in-situ* and post-treatment methods, which can be used to fabricate films with micrometer size grains.

To this end, a set of amorphous Si films were deposited on Al-coated 7059 glass and provided to Professor Ajeet Rohatgi at the Georgia Institute of Technology to study the process of metal induced crystallization (MIC) by RTP. Table 13 below summarizes film properties before annealing.

Table 13. a-Si samples deposited for RTP MIC.

Sample ID	Film thickness (nm)	Crystalline fraction (%)	Metal layer thickness (nm)
HW159-11	2000	0	5
HW159-12	2000	0	10
HW159-13	2000	0	50
HW159-32	2000	0	100
HW159-22	2000	0	500

RTP experiments were performed on these samples at temperatures of 400, 450, 500, 550 and 600^{o}C for a period of 3 minutes at each temperature. Of all the samples, only HW159-22 became crystalline after RTP at the highest temperature (see Figure 36). The XRD patterns for one of the samples which did not undergo MIC (HW159-32) are shown in Figure 37.

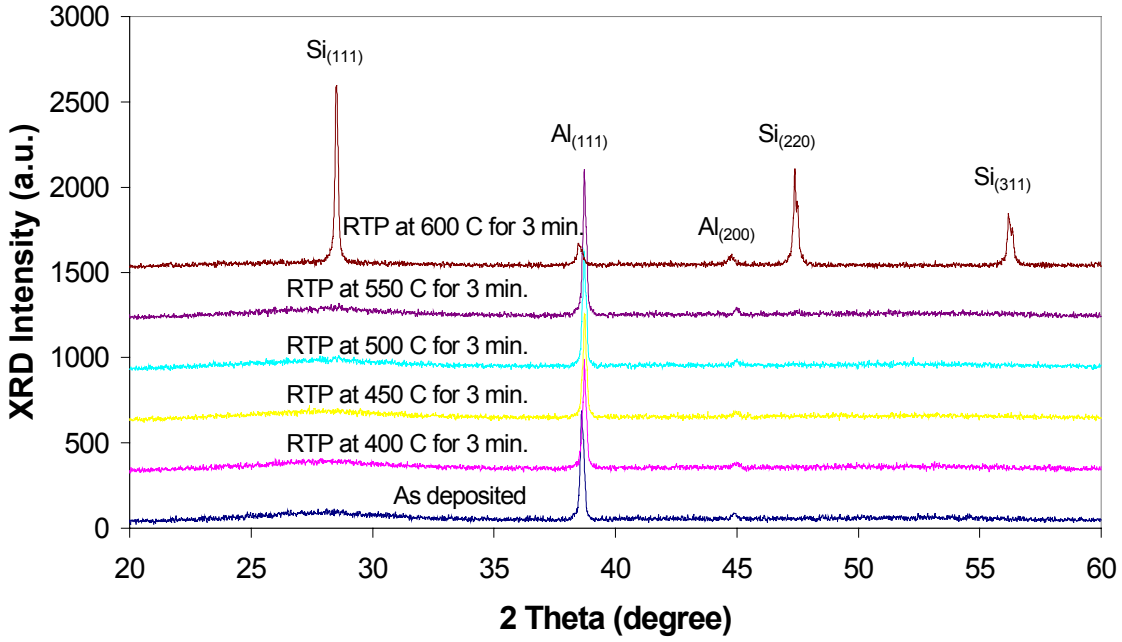


Figure 36. XRD patterns of HW159-22 before and after RTP.

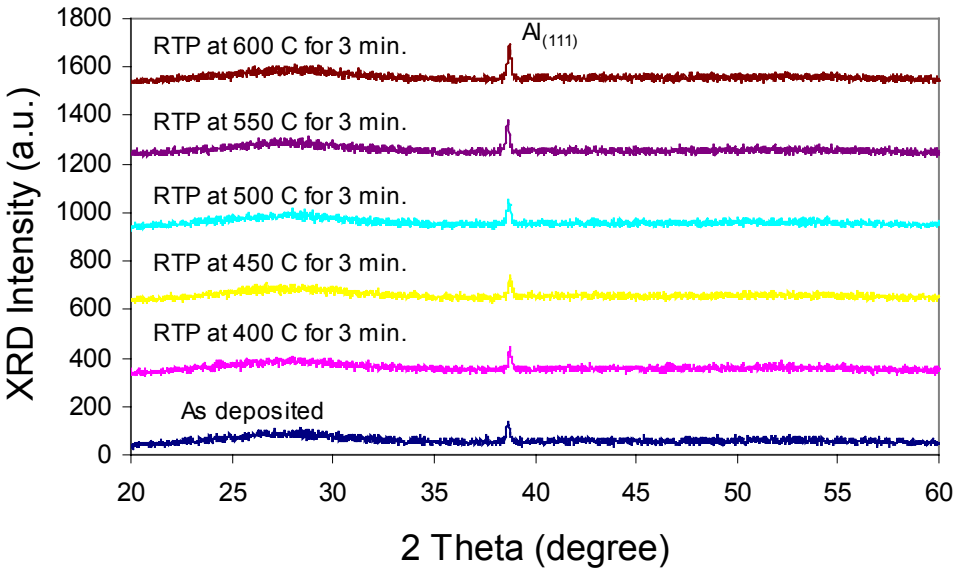


Figure 37. XRD patterns of HW159-32 before and after RTP.

These results lead to the conclusion that for the RTP conditions used, 500 nm is the minimum Al layer thickness necessary for MIC to occur. MIC at lower temperatures, therefore, requires thicker Al layers. The grain size calculated from the broadening of the (111) peak of sample HW159-22 after crystallization was 60 nm.

A second set of samples was also sent to Professor Rohatgi to study the effect of RTP on HW Si films of varying crystalline fraction. The substrate in all cases was 7059 glass without a metal layer. Table 14 summarizes the film properties. The samples were annealed at 600, 700, 750 and 800^{o}C for a period of 3 min at each temperature. For sample HW92-13, crystallization occurred at the highest temperature (see

Figure 38). The grain size obtained from the broadening of the (111) peak was 24 nm. Both polycrystalline samples (HW115-33 and HW118-32) did not exhibit grain enhancement upon annealing. Their grain size remained unchanged at 22 nm. The XRD patterns for sample HW115-33 are shown in Figure 39 for illustration.

Table 14. HW-Si samples deposited for RTP.

Sample ID	Film thickness (nm)	Crystalline fraction (%)	Metal layer thickness (nm)
HW92-13	4400	0	0
HW115-33	2200	45	0
HW118-32	3200	85	0

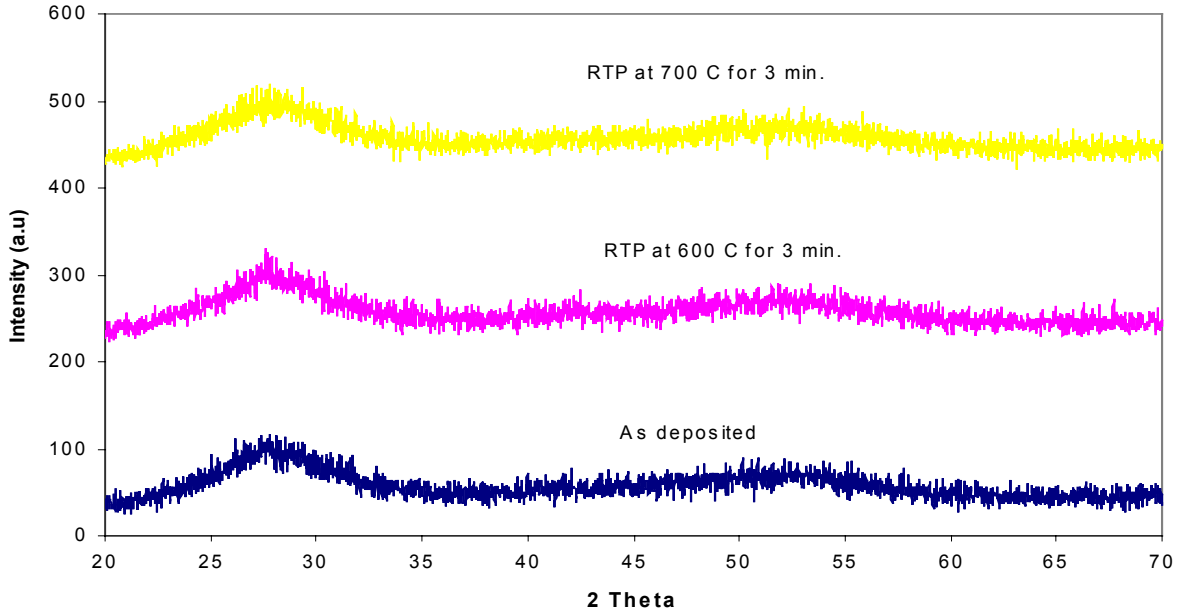


Figure 38. XRD patterns of HW92-13 before and after RTP.

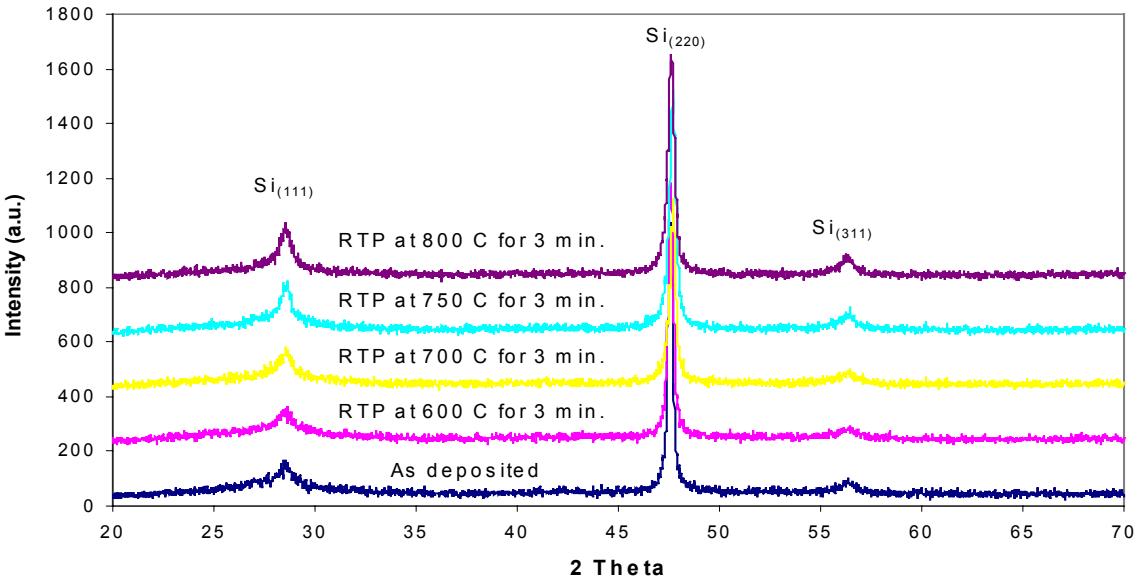


Figure 39. XRD patterns of HW115-33 before and after RTP.

A third set of samples was also provided to Professor Rohatgi to study the crystallization of HW Si films by RTP with UV radiation. Sample properties are given in Table 15. Difficulties with temperature and motion control in the UV-RTP set-up limited processing to only 600^{o}C and

2 minutes for both samples. After annealing, neither sample exhibited change in crystalline fraction or grain size.

Table 15. HW-Si samples deposited for UV-RTP.

Sample ID	Film thickness (nm)	Crystalline fraction (%)	Metal layer thickness (nm)
HW133-13	2700	10	0
HW131-13	3300	78	0

3.8.2 *In-situ* Grain Enhancement of HWCVD Films

Investigation of various *in-situ* grain enhancement approaches was also carried out. These approaches seek to combine the fast deposition rates of HWCVD with the ability to nucleate micron-sized grains. The first approach considered was variation of Vapor-Liquid-Solid (VLS) growth. In this method, very thin metal layers are deposited on the glass substrates. These layers are then heated to temperatures above the metal-Si eutectic. As the Si deposition proceeds, thermodynamics dictates the formation of a liquid phase. Therefore, we have termed this approach molten-metal or eutectic-promoted HWCVD. Further addition of Si to the system leads to precipitation of Si from the supersaturated liquid solution. Alternatively, precipitation of Si can be accomplished by quenching the metal-Si liquid solution below the eutectic temperature. Increased grain sizes are expected due to the reduced nuclei density that results from enhanced mobility in the liquid medium.

Preliminary experiments of this technique were performed using Al and Sn to increase silicon film grain size. The metals were deposited on Corning 7059 type glass substrates by electron beam evaporation. These samples were subsequently transferred to the HWCVD reactor for Si deposition. Since Al layers oxidize quickly at room temperature, an atomic hydrogen treatment was performed for samples with Al layers (MM1) just before Si deposition to reduce the Al_2O_3. The operating conditions during the treatment were 50 sccm hydrogen flowrate for 10 minutes with substrate and filament temperatures of 400ºC and 1850ºC, respectively. The total reactor pressure was kept at 20 mTorr. Thermodynamically, it is expected that atomic hydrogen should reduce Al_2O_3 since the Gibbs free energy of the associated reaction is negative (see below).

$$Al_2O_{3(s)} + 6\ H_{(g)} \Rightarrow 2\ Al_{(s)} + 3\ H_2O_{(g)} \qquad \Delta G_{rxn} = -283\ kJ/mol \qquad (16)$$

However, the effectiveness of the hydrogen treatment was not verified by characterization.

Silicon depositions were performed immediately after the hydrogen treatment. Since the objective of the experiments was to produce a very thin layer (<1 μm) with large grains (>1 μm), deposition conditions were adjusted so that approximately 1 μm thick Si films were obtained after 60 minutes of deposition ($T_{filament}$ = 1850ºC, $P_{reactor}$ = 25 mTorr, F_{silane} = 4.5 sccm, $T_{substrate}$ = 620ºC).

For the samples with Sn layers (MM2), no hydrogen treatment was performed. An accurate temperature control was not possible with Sn samples because of radiative heating from the filament, which doesn't occur with the Al samples. The substrate temperature was set to 250ºC

(T_m = 232ºC for Sn) but during deposition it increased to 400ºC. All other deposition conditions were the same as with the samples with Al layers (MM1 set). The thicknesses of the films were determined by the net weight gain after deposition. Most of MM2 samples peeled off after deposition.

The films were characterized by X-ray diffraction (XRD), Raman spectroscopy, atomic force microscopy (AFM) and scanning electron microscopy (SEM). Basic properties of the samples are shown in Table 16. The crystallinities of the samples were determined by Raman spectroscopy. Since the beam size is much smaller than the sample area, measurements were made at several places on the film. Percent crystallinity of a sample is given as a range of the minimum and maximum values found, which is also a measure of uniformity. Grain size and preferential orientation of the samples were determined by XRD. Figure 40 shows the XRD pattern of the sample listed in Table 16 deposited on glass and on glass with 50 nm of Al, compared to the random powder pattern for Si. The XRD spectra of films with 50 and 100 nm Al was very similar to the unmetallized sample in Figure 40.

Table 16. Basic properties of HW Si samples deposited on various metallized substrates.

Sample	Metal	Metal Thickness (nm)	Orientation	Grain Size (A)	Crystallinity, %
MM1-23	N/A	N/A	(220)	430	78-79
MM1-12	Al	5	(220)	380	61-76
MM1-21	Al	10	(220)	314	75-77
MM1-32	Al	50	(111)	439	81-94
MM2-22	Sn	10	(220)	330	75-77

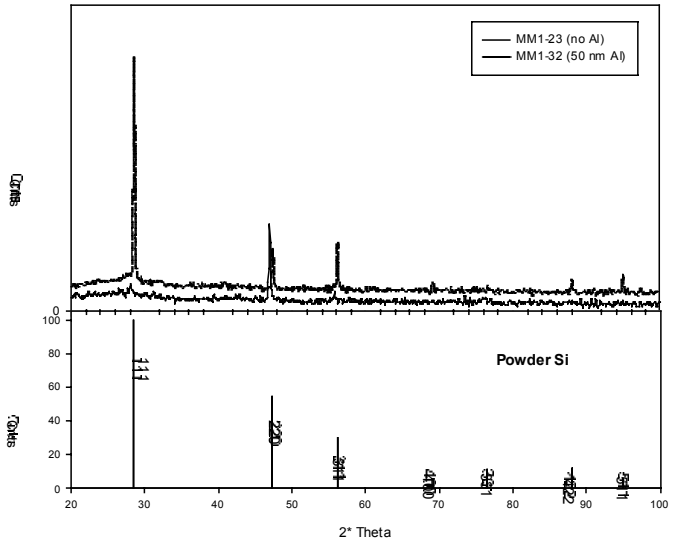


Figure 40. XRD pattern of Si film grown on glass (no Al), on glass/50 nm Al (top), and powder Si (bottom).

In Figure 41, the (111) and (220) peaks of all the patterns in Figure 40 are plotted on an expanded scale to facilitate the following discussion. In the powder silicon pattern, the (111) and (220) peaks are located at 28.442º and 47.302º, respectively. For the Si films deposited on bare glass, these peaks are clearly shifted to the lower angle side, indicating the presence of stress in the films. However, stress was not observed on the films deposited on Al layers. An Al-Si alloy layer formed at the interface may act to reduce the stress in the films. However, the major peak for Al-Si alloy, which is around 36º for (220) orientation, was not observed possibly because such a layer is too thin to be measured by XRD. On the other hand, the tails of (220) peaks of all metallized samples suggest that films are still under stress, though not as much as films deposited on bare glass. The stress may be due to the difference between the thermal expansion coefficient of Al (25×10^{-6} C^{-1}) and poly-Si (2.6×10^{-6} C^{-1}) and/or high growth rate (1 μm/hr). Peeling observed in Si films deposited on Sn may be the result of the difference between thermal expansion coefficient of Si and Sn (2.0×10^{-6} C^{-1}) as well as de-wetting of Sn during deposition. It has been shown that addition of wetting agents significantly improves the uniformity of the metal layer and Si films. In addition, the substrate temperature during deposition was well above the melting point of Sn, unlike deposition of MM1 samples where the substrate temperature was kept close to the melting temperature of Al.

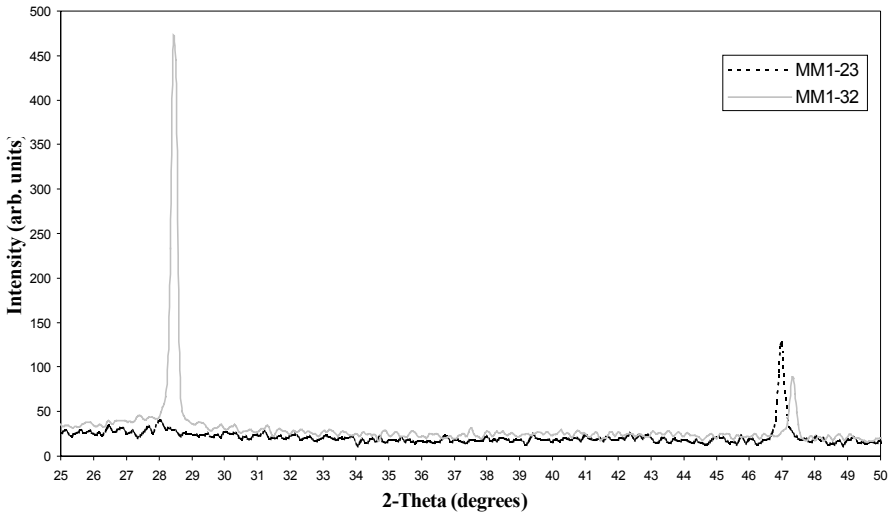


Figure 41. XRD pattern of selected samples in detail, (111) and (220) peaks.

After initial characterization of the samples, a heat treatment process was carried out in an attempt to further reduce the stress and increase the grain size. Samples were kept at 350ºC for 45 minutes in the HWCVD reactor at 2.8×10^{-8} Torr background pressure. Figure 42 shows the (111) and (220) peaks of the same two samples, MM1-23 (deposited on bare glass) and MM1-32 (deposited on 50 nm Al layer), before and after heat treatment. It is expected that an oxide layer is formed on top of the Si layer when the heat treatment is not carried out under inert atmosphere. However, the XRD pattern showed no peaks other than silicon, indicating a very thin or negligible oxide layer on the films. After heat treatment, the peak positions for the sample deposited on bare glass shifted almost half a degree to a two-theta value close to that expected for the random powder pattern indicating a reduction of stress in the films. For the sample deposited on Al layers, the shift in the peak positions was less than 0.02º. The grain size did not change in any of the samples.

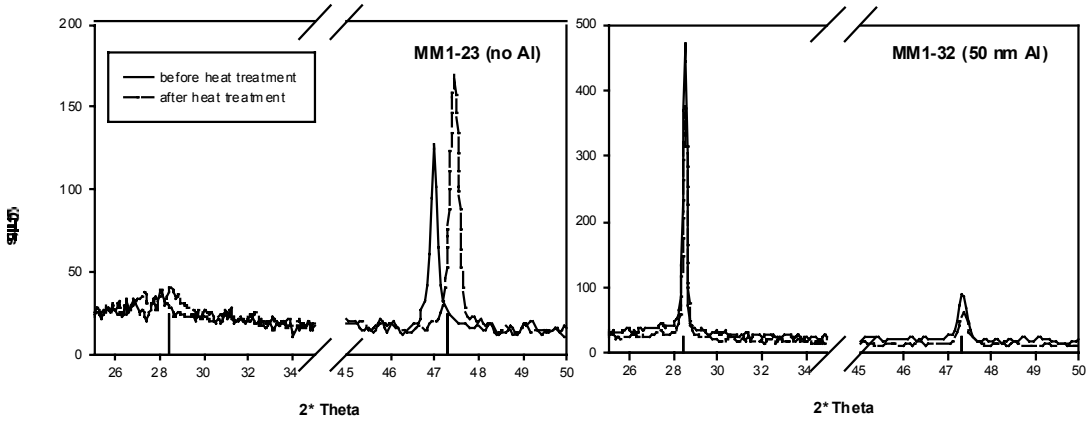


Figure 42. Effect of heat treatment on samples.

It was also observed that the film orientation is affected by the thickness of the Al layer. In the random powder pattern, the ratio I(220)/I(111) is 0.55, as seen in Figure 40. For the sample with 50 nm Al (MM1-32), the preferred orientation of the film was (111). This change in orientation with the thickness of the Al layer has been reported previously in our work on MIC. The ratio of metal layer/Si layer thickness is expected to be an important parameter for this grain enhancement approach. The effect of this ratio on the grain size for the experiments discussed is not clear since Al layers were too thin. There may exist an optimum metal/Si ratio with respect to grain size and other deposition conditions. Future work will include the use of thicker metal layers to investigate the effect of metal/Si ratio on the grain size of the films.

SEM analysis of the films showed large structures as well as smaller needle-like features on the surface of Sn-Si films. Similar features, with sizes between 1-15 μm, were observed on most samples. Their composition measured by EDS was 95-98% Si with oxygen accounting for the balance. Needle-like features seen on films deposited on Sn resemble whisker structures reported in the literature. EDS measurements did not yield accurate data since the films were very thin. The signal coming from the glass substrate (which contains Si, Al, and Ba) contributes to the signal from the films and did not allow an accurate determination of the atomic percentages of Si, Al and Sn in the film.

After these preliminary experiments, we proceeded to investigate the effect of substrate temperature on the grain enhancement process. Primarily, we were interested in understanding the differences between the grain enhancement process at temperatures above and below the Al-Si eutectic temperature. It is known from the literature that a-Si crystallizes when in contact with Al at temperatures greater than 200°C. This is the basis for the process of Metal Induced Crystallization (MIC). However, MIC is typically carried out by depositing the a-Si and Al layers at temperatures below 100°C. Under these conditions, the Si layer remains amorphous during deposition. These layers are then annealed at temperatures between 200 to 600°C to achieve crystallization. In the experiments that follow, Si films were deposited at 400 and 600°C, respectively. At these temperatures, it is expected that the Si film would crystallize immediately upon deposition. The substrate temperature plays an important role in grain enhancement processes since it determines the mechanism of crystallization. For depositions

below the Al-Si eutectic temperature (575°C), crystallization follows a pattern similar to that of conventional MIC. This is the basis for the second approach being considered, i.e., *in-situ* MIC-HWCVD. On the other hand, at temperatures above the eutectic temperature, the mechanism of crystallization is expected to be different since a liquid phase forms.

In the first experiment (MM3), Si films were deposited on Al coated glass substrates under the conditions in Table 17.

Table 17. MM3 deposition conditions.

Substrate Temperature (^oC)	600
Wire Temperature (^oC)	1850
Reactor Pressure (mTorr)	25
SiH_4 Flowrate (sccm)	22.5
Deposition Time (min)	60

The thickness of the Al and Si layers was 1 and 5 μm, respectively.

Figure 43 indicates that the resulting films are highly crystalline with a slight (200) preferred orientation.

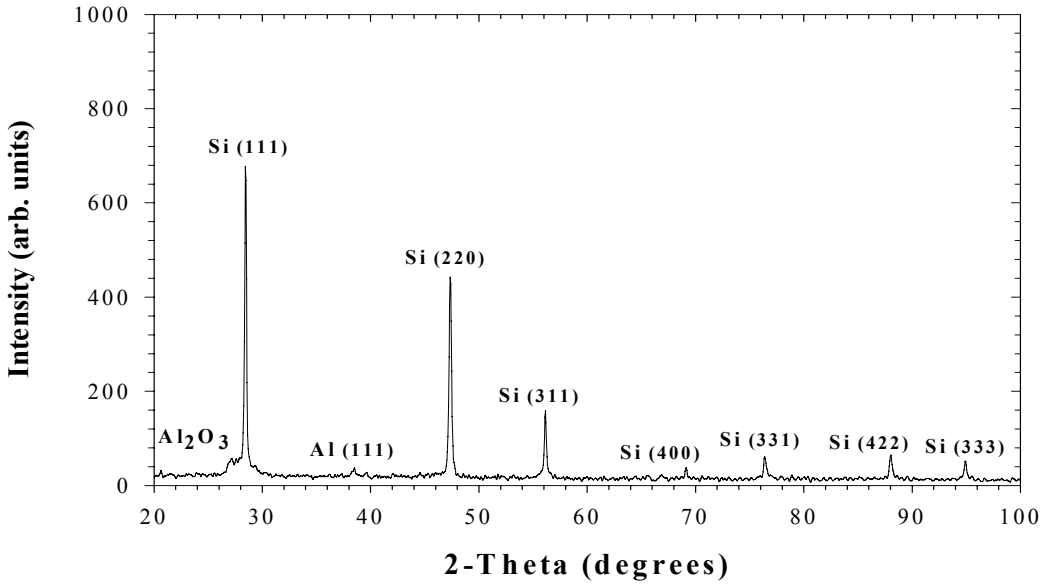


Figure 43. XRD pattern of Si film MM3-11.

Figure 44 is a set of SEM images of the film surface. The film is composed of 10-100 μm features decorated by 1 μm needle like objects. The composition of the larger objects measured by EDS was 98% Si and 2% Al. On the other hand, Al was not detected on the needle shaped

objects. It is not clear at this point that the large features are individual grains. Further characterization will be done to determine the grain size.

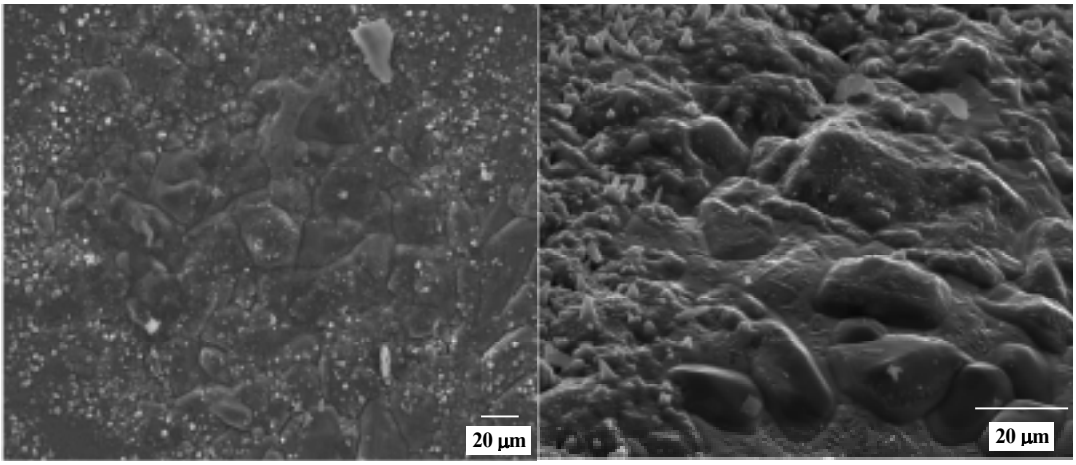


Figure 44. SEM images of Si film MM3-11.

In the second experiment (MM4), Si films were deposited on Al coated glass substrates under the conditions in Table 18.

Table 18. MM4 deposition conditions.

Substrate Temperature (ºC)	400
Wire Temperature (ºC)	1850
Reactor Pressure (mTorr)	25
SiH_4 Flowrate (sccm)	22.5
Deposition Time (min)	60

The thickness of the Al and Si layers was 1 and 5 μm, respectively. The XRD pattern for sample MM4-22 is shown in Figure 45. The broad background near the vicinity of 28 and 50 degrees two-theta, where the dominant peaks for Si lie, indicates that the films were only partially crystallized. This may also explain the strong reflections from the thinner Al layer. Figure 46 shows the microstructure of the films. The observed features are highly columnar and several micrometers in diameter. Al could not be detected by EDS in the films. In order to determine whether the surface features represented individual grains, a sample was polished down to 1 μm in thickness (Figure 47). Close examination of Figure 47 shows that the underlying microstructure appears to be composed of grains several micrometers in size. The surface morphology seems to then evolve from this basal structure. Characterization by TEM and selective etching is planned to confirm these observations.

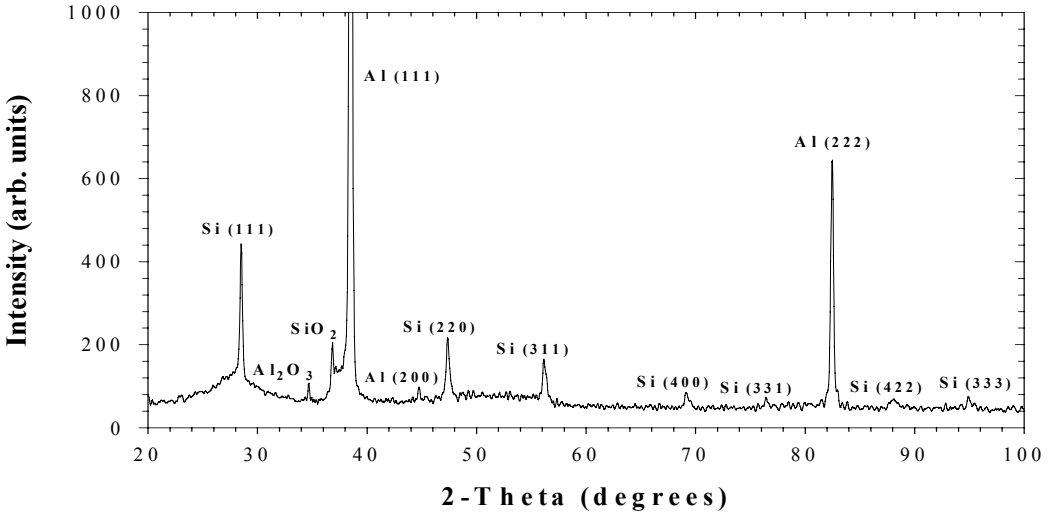


Figure 45. XRD pattern of Si film MM4-22.

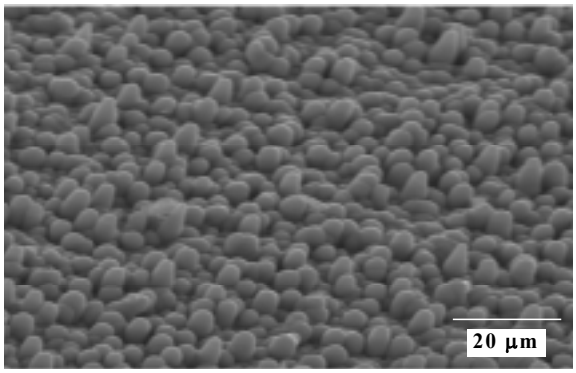


Figure 46. SEM image of as-deposited Si film MM4-22.

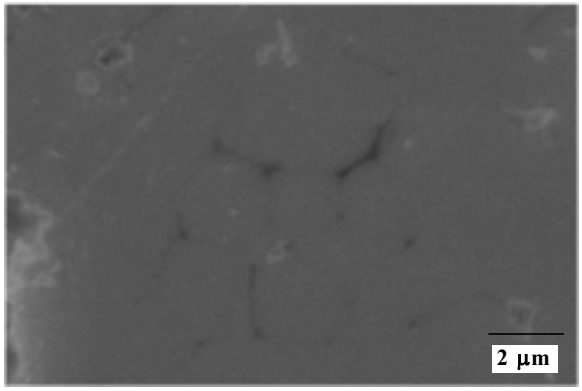


Figure 47. SEM image of polished Si film MM4-22.

Further experiments are planned to study the effect of Al and Si thickness on the grain enhancement process. The preliminary results of the above experiments seem to indicate that substrate temperatures below the Al-Si eutectic temperature can lead to grain enhancement

without measurable invasion of the Si film by Al. The fact that the films were only partially crystallized at the lower temperature can be overcome by decreasing the Si film growth rate. This would allow for a longer deposition time and additional annealing of the film sub-layers. The effect of substrate temperature and additional post-deposition annealing will be studied in more detail.

4. CdTe-BASED SOLAR CELLS

The goal of this sub-task is quantification of the effects of critical processing steps on performance and stability in CdTe thin-film polycrystalline solar cells. Experiments with CdTe films deposited by different methods, coupled with systematically varied post-deposition and contact processing, provides a generalized basis for understanding thin-film CdTe/CdS solar cells. This in-turn has resulted in development of alternative processes for higher performance, simplified processing, and greater stability. These options have been transferred to manufacturing groups, where gains in module performance have already been demonstrated. This report summarizes progress towards: 1) fundamental understanding of the chemical and kinetic behavior of CdTe-CdS thin-film system under a wide range of deposition and post-deposition processing conditions; 2) development of window layer options for high performance and large area manufacture; 3) identifying the relation between contact processing, device operation, and stability; and 4) transfer of processing technology and fundamental understanding to the PV manufacturing community. Reference will be made to the three annual reports for Phases I, II, and III.

4.1 CdTe-CdS Interdiffusion

4.1.1 Introduction

Processing highly efficient CdTe thin-film solar cells in the superstrate configuration includes exposure of CdTe/CdS couples to high temperature, T > 500°C, and reactive chemical species, in particular $CdCl_2$ and O_2 [48]. Although the role of the $CdCl_2$ and O_2 on the electronic operation of devices is not quantitatively understood, it is well-known that small-area cells with conversion efficiency, η, exceeding ~13% can be obtained using CdTe deposited by different conditions and using different thermal sequences with $CdCl_2$ and O_2. However, obtaining the *highest* efficiencies, greater than 15%, is achieved by depositing CdTe by one specific method, close-space sublimation, at temperatures near 600°C in an O_2 partial pressure [49,50]. In spite of the beneficial effects of the high temperature deposition, these devices still require $CdCl_2$ treatment for optimal performance. Typical values for open circuit voltage and short circuit current in CSS devices are V_{oc} ~ 830 mV and J_{sc} ~ 25 mA/cm^2. Similar V_{oc} can be obtained in cells with CdTe deposited at low temperature, but with an added high temperature anneal step [51].

Cell performance is sensitive to relatively subtle processing deviations. For example, to obtain J_{sc} > 25 mA/cm^2 under AM 1.5 illumination requires CdS thickness less than 80 nm in the operating device. Obtaining high V_{oc} with the high J_{sc} in the same device requires lateral continuity in the CdS film to avoid occurrence of parallel junctions between CdTe and the underlying transparent oxide (TO). This is because CdTe/TO junctions exhibit higher dark diode current, J_o, than CdTe/CdS junctions, and a surprisingly low area density of CdS voids, < 0.01%, reduces V_{oc} of the entire device by ~100 mV. Manipulation of the window layer, by addition of a high-resistance interlayer, modified CdS deposition, and modified CdTe/CdS post-deposition treatment, can be employed to reduce J_o of CdTe/TCO junctions and reduce the fractional area of CdS voids.

A key challenge is thus minimizing CdS thickness while maintaining CdS integrity during critical thermal and chemical processing steps: CdTe deposition, post-deposition treatment and contact formation. This mandate has enormous impact for process control when fabricating large-area CdTe/CdS cells at high efficiency. This section presents the relationship between the CdTe-CdS-$CdCl_2$-O_2 chemical system, film deposition and treatment processes, and film structure and diffusion. The impact of processing variations on electrical device operation and implications for stability and large area manufacture are addressed.

4.1.2 Approach

As a materials problem, separating the effects of deposition and post-deposition processing on the thin-film microstructure is complicated by the polycrystallinity of the film and the chemical reactivity and miscibility of the components, CdTe, CdS, $CdCl_2$, and O_2. The problem was approached in three steps: 1) systematic analysis of species distribution in thin film devices made by different methods to determine general processes, 2) kinematical modeling of measured quantities to quantify these processes, and 3) determination of activation energies and diffusion coefficients and their dependence on chemical and structural conditions. To provide the highest degree of generality, CdTe/CdS samples were prepared in superstrate and substrate configurations. In most cases, CdTe films were deposited by physical vapor deposition. However, superstrate samples using CdTe deposited by electrodeposition and close space sublimation were also utilized. Polished single crystal CdTe substrates were coated with CdS films to obtain CdTe/CdS couples on defect-free CdTe for determination of bulk diffusivity. In selected studies, superstrate devices were fabricated on Si substrates to provide mechanically stable cross-section specimens for transmission electron microscopic (TEM) analysis. In selected cases, a semi-transparent Au contact was applied to comparably processed samples on glass and Si. Similar backwall device operation in structures on glass and Si provided the validation needed for collateral observations.

CdTe and CdS films were thermally evaporated from 99.9999% purity CdTe crystals and CdS powder onto indium-tin oxide (ITO) coated Corning 7059, tin-oxide (TO) coated 7059, or polished Si wafers. The CdS deposition temperature was 220°C for all samples, and CdTe deposition temperature was typically 300 to 340°C. In addition, CdS films were deposited by a modified form of chemical bath deposition, referred to as chemical surface deposition (CSD) and is described in Section 4.2 below. CdTe films were also deposited by close-space sublimation at 600°C at 1 Torr with O_2 partial pressure of 0.1 Torr. Electrodeposited CdTe films were supplied by BP Solar.

A high-temperature anneal, from 450°C to 600°C, was carried out in a quartz-lined tube furnace with Ar and O_2 carrier gases. $CdCl_2$ treatments were carried out in controlled Ar:O_2 ambient using a reactor to deliver $CdCl_2$ vapor to the surface of the CdTe. The partial pressure of $CdCl_2$ was controlled by the temperature of a hollow susceptor heated with quartz halogen FCM-type lamps and is described more fully in reference and shown in Figure 48. This method of treatment is referred to as 'vapor' $CdCl_2$ treatment. A United States patent was awarded with respect to this development [52]. In selected cases, samples were coated with a saturated solution of $CdCl_2$ in CH_3OH and dried to form a ~0.5 μm thick coating of solid $CdCl_2$ prior to heating. This is referred to as 'wet' $CdCl_2$ treatment.

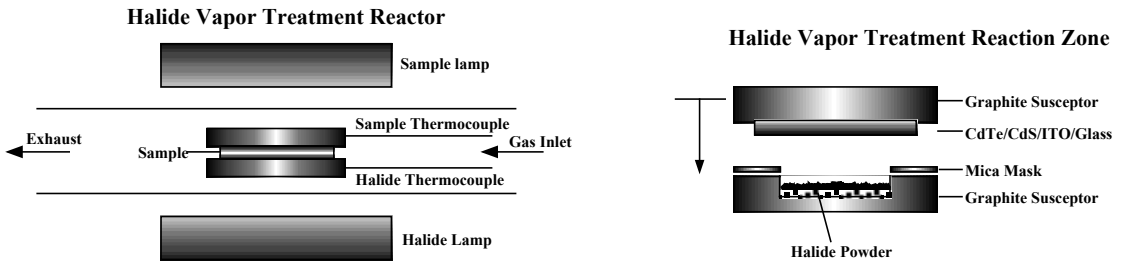


Figure 48. Schematic views of halide vapor treatment reactor.

Measurements were made to provide structural, chemical and optical properties. Surface morphology was characterized using scanning electron microscopy (SEM), atomic force microscopy (AFM) in tapping mode, and scanning transmission electron microscopy (STEM). For SEM and AFM, minimal sample preparation was necessary since vapor treatments produced negligible residue. For STEM, cross-sections were prepared by cleaving the samples, mounting on TEM grids, and thinning with Ar^+ ion beam. Grain size and surface morphology were typically determined by atomic force microscope (AFM) analysis. In most cases, grain boundaries were easily detected and quantified without surface modification. In selected cases, grain boundaries were enhanced by etching the CdTe surface in 0.01 wt% Br_2:CH_3OH, followed by topotaxial conversion to Cu_2Te by reaction in aqueous CuCl solution, then etching the Cu_2Te away in aqueous KCN solution. This procedure was only employed on samples after all other necessary treatments and measurements had been made.

Lattice parameter distributions, crystalline phases and grain orientation were measured by symmetric x-ray diffraction (XRD) in Bragg-Brentano para-focusing beam geometry using Cu-k_α radiation. The x-ray diffraction pattern contains sufficient information to determine accurate volume fraction distributions of $CdTe_{1-x}S_x$ alloy and secondary phase components, although it does not yield the spatial arrangement of these phases. To separate thin crystalline surface phases, glancing-incidence x-ray diffraction (GIXRD) was employed, at fixed incident beam angles from 0.5 to 5° in parallel-beam geometry using Cu-k_α radiation. To determine three-dimensional $CdTe_{1-x}S_x$ alloy distribution, a method for analyzing x-ray diffraction line profiles of CdS/CdTe thin-film couples was developed. This yielded bulk and grain boundary diffusion coefficients and their sensitivity to temperature and $CdCl_2$ and O_2 concentration during treatments. The solution of Gilmer and Farrell [53] for bulk and grain boundary diffusion was applied to measured grain size distributions to yield three-dimensional alloy volume fractional contribution to diffracted beam intensity. The line profile of the $CdTe_{1-x}S_x$ (511)/(333) reflection was then modeled by convoluting the generated compositional distribution with the Pearson VII function and accounting for beam attenuation in the sample. The (511)/(333) reflection was selected on the basis of its high Bragg angle, hence resolution in lattice parameter. Since it is an order of the basal plane (111) reflection, which is the most intense in the random pattern, it is typically the strongest reflection in as-deposited films. It should be noted that earlier work established that all reflections exhibit the same lattice parameter distribution [54]. Modeled line profiles were refined by comparison with measured profiles, using only the bulk and grain boundary diffusion coefficients as fitting parameters. Measured profiles were obtained from

both superstrate and substrate configurations. Verification of the bulk coefficient was obtained by Auger depth profile analysis of treated CdS/CdTe couples using single crystal CdTe substrates.

Solar cells were fabricated by formation of primary and secondary contacts to the CdTe. This is described more fully in Section 4.3. Typically, primary contact to CdTe, Cu_2Te, was obtained in two steps: by vapor treatment of the CdTe surface at ~100°C to remove oxides and to produce Te excess, then electron beam evaporation of copper metal followed by heat treatment at 200°C. Acheson carbon ink was used to form the secondary, or current-carrying, conducting back contact pad, and devices were electrically isolated by scribing through the $C/Cu_2Te/CdTe$.

Optical transmission and reflection were used to determine the transmittance of oxide layers, CdS thickness, and CdTe absorption. For CdS films deposited on similar TCO or HR/TCO combinations, the normalized optical transmission, T/(1-R), provided a routine means to determine CdS film thickness for films as thin as 5 nm. The accuracy of this method, checked for films from 10 to 100 nm thick by step profilometry, was ±10%. Current-voltage and quantum efficiency-wavelength measurements were used to characterize device operation and determine final CdS thickness in working devices.

4.1.3 Results

4.1.3.1 CdTe-CdS Alloy System

Since the 1970's, it has been known that the mixed-crystal CdTe-CdS system exhibits a miscibility gap at temperatures below ~750°C, and that the mixed thin-film system CdTe-CdS system can be prepared over a continuous compositional range, if deposited at sufficiently low temperature. Such phases are kinetically limited and thus do not constitute an equilibrium condition. When these films are heated in a kinetic-enhancing atmosphere, such as vapor containing halide and oxygen, phase segregation occurs, producing Te-rich $CdTe_{1-x}S_x$ and S-rich $CdS_{1-y}Te_y$ alloy components. The limiting compositions at the equilibrating temperature correspond to the miscibility gap and are thermodynamically limited by the mixing free energy. In phase-segregating structures, or binary couples, these compositions are the boundary conditions for diffusion wherever an interface exists. Therefore, it is critical to determine the low-temperature phase diagram for the CdTe-CdS system.

The solubility limits and mixing energies of the two-phase CdTe-CdS system were established for the temperature range normally used to fabricate high efficiency CdTe/CdS solar cells. Previous works [55,56.57] have determined the *T-x* phase relations for CdTe-CdS mixed crystals at temperatures above 625°C, which exceeds the temperatures typically used to deposit and process thin-film CdTe/CdS structures. However, $CdTe_{1-x}S_x$ alloy films deposited at temperatures from 120°C to 200°C exist as metastable single-phase, with a continuous compositional range [58,59,60,61,62,63]. Heating these films above 300°C induces phase segregation in general accordance with the miscibility gap reported for mixed CdTe-CdS crystals at higher temperature. The segregated films exist in two crystallographic forms: zincblende (F-43m) structure on the Te-rich side and wurtzite ($P6_3mc$) structure on the S rich side. To accelerate the transition from the metastable to the equilibrium state at low temperatures, films

are typically treated in a vapor ambient containing relatively *low* concentrations of $CdCl_2$ and O_2, which do not measurably shift the solubility limits of the CdTe-CdS system in the 650°C to 700°C range.

Single phase $CdTe_{1-x}S_x$ films with x ~ 0.4 were heat treated at 360°C to 700°C in an inert ambient containing low concentrations of $CdCl_2$ vapor and O_2 to induce phase segregation. X–ray diffraction was used to determine the composition of the segregated phases by measuring the d-spacings of multiple lattice plane reflections and using these to calculate the lattice parameter. From this, the composition was determined by assuming a linear relationship between composition and lattice parameter, and using data for pure CdTe and CdS powders as end points [64]. The treatments were carried out incrementally until no detectable change in lattice parameter between consecutive treatments was found. The precision lattice parameters in $CdTe_{1-x}S_x$ and $CdS_{1-y}Te_y$ phases were taken to represent the equilibrium compositions at the temperature used to treat the films. By convention, x and y represent the minority components S in $CdTe_{1-x}S_x$ and Te in $CdS_{1-y}Te_y$, respectively.

The CdTe-CdS system was modeled using two component solution thermodynamics, a common approach used for alloy systems [65]. Deviations from ideal solution behavior in the system were expressed in terms of the excess free energy of mixing. These parameters were regressed from a fit of the model to experimentally determined solubility data.

$CdTe_{1-x}S_x$ films 2 microns thick were evaporated at 250°C on Corning code 7059 glass coated with 200 nm of polycrystalline indium-tin-oxide (ITO). The ITO facilitated adhesion of the films and served as an internal standard for x-ray diffraction analysis. CdTe and CdS were co-evaporated from separate boron nitride effusion sources onto the radiatively heated substrates at a growth rate of ~8 Å/sec using 99.999% pure CdTe and CdS powders. Films with composition (x) from 0.4 to 0.5 were obtained by depositing the CdTe and CdS at an effusion rate ratio (r_{CdS}/r_{CdTe}) of 1.5. A ratio greater than unity was needed to overcome the lower sticking coefficient of CdS. For the source configuration used, this corresponded to source temperatures, T_{CdS} = 900°C and T_{CdTe} = 760°C.

Treatment of the $CdTe_{1-x}S_x$ films in $CdCl_2$:O_2:Ar ambient was carried out in the previously described reactor. The uncertainty in temperature was ± 2°C.

Independent temperature control established a constant $CdCl_2$ partial pressure for different film treatment temperatures. In these experiments, the $CdCl_2$ source and the CdTe/CdS thin films were heated simultaneously to their respective temperatures. The $CdCl_2$ source was maintained at 400°C, which corresponded to a $CdCl_2$ partial pressure of approximately 3×10^{-3} Torr, or concentration of 8×10^{-5} μmol/cm^3 at the film surface. Heat-up times from room temperature to 400°C were 40 seconds for the samples and 20 seconds for the $CdCl_2$ susceptor. Treating $CdCl_2$ as a polar diffusing species, the characteristic diffusion time of $CdCl_2$ vapor in Ar from source to film surface was ~2 sec. Therefore, the rate-controlling step for films to reach equilibrium is not gas-phase diffusion, but heating susceptors to the treatment temperatures. Oxygen partial pressure was fixed at ~120 Torr by flow rate control. All treatments were conducted in flowing Ar:O_2 at a total flow rate of 0.94 L/min at atmospheric pressure.

Wide-angle XRD measurements yielded lattice parameter (a_{hkl}) which was calculated for each observed reflection by the equations

$$a_{hkl} = d_{hkl}\sqrt{h^2 + k^2 + l^2} \qquad \text{(cubic)} \qquad (17)$$

$$a_{hkl} = d_{hkl}\sqrt{\frac{4}{3}\left(h^2 + hk + k^2\right) + \left(\frac{1}{c_{hkl}}\right)^2} \qquad \text{(hexagonal)} \qquad (18)$$

where h, k, and l are the Miller indices of a given reflection. In the hexagonal case, a_{hkl} was solved iteratively by refining c/a from an initial estimate. The set of observed lattice parameters were reduced to a precision lattice parameter (a_f) by extrapolation on a plot of a_{hkl} versus the Nelson-Riley-Sinclair-Taylor function (F_{NRST}) to the function's zero point; $F_{NRST} = 0.5[(\cos^2\theta/\sin\theta)+(\cos^2\theta/\theta)]$, where θ is the Bragg angle of the peak centrum [66]. The alloy composition (x) was determined using the equation

$$x = 1.508(a_o - a_f) \qquad (19)$$

where x = [CdS]/([CdS]+[CdTe]) in $CdTe_{1-x}S_x$ and a_O = lattice parameter of pure CdTe = 6.481Å. Narrow-angle x-ray diffraction scans of high order (*hkl*) reflections such as (511/333) and (531) were made to verify that a single composition had been reached after treatment on the basis of symmetrical peak shape. All diffraction patterns and profiles were stripped of the $k\alpha_2$ component using the Rachinger correction prior to analysis.

4.1.3.1.1 *Heat Treatment of $CdTe_{0.6}S_{0.4}$ Films*

The XRD pattern of a $CdTe_{0.6}S_{0.4}$ film on ITO/7059 glass before and after the $CdCl_2$:Ar:O_2 vapor treatment at 415°C is shown in Figure 49. Before treatment, the film exhibits strong preferential (001) orientation of the wurtzite alloy phase, with few other resolved peaks, making detailed XRD analysis inaccurate. The broad feature near 2θ = 69° (d~1.36Å) corresponds to poorly nucleated surface grains having wurtzite (105) orientation. Glancing incidence x-ray diffraction with incident beam angle of 1° resolved the (105) reflection into a more discrete intense peak, indicating that the terminating layer contains a high grain population with (105) texture.

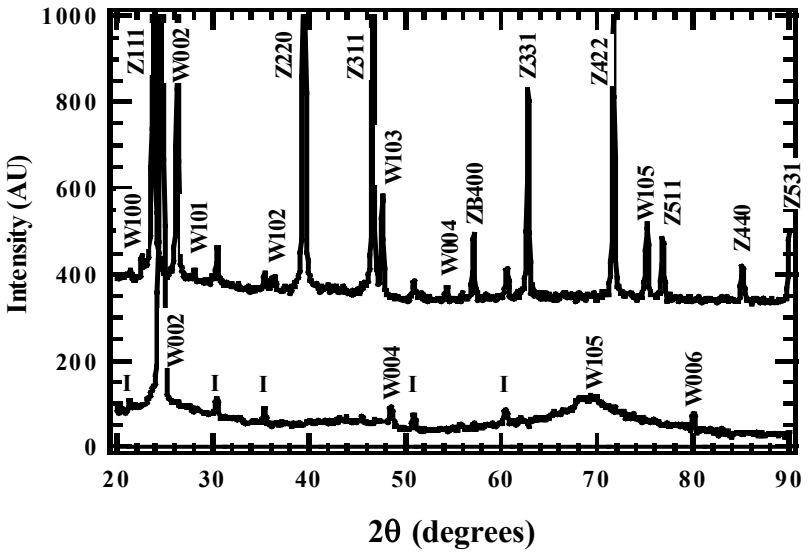


Figure 49. XRD patterns for $CdTe_{0.4}S_{0.4}$ as deposited (lower) and after treatment at 415°C in $CdCl_2$:Ar:O_2 for 60 minutes. ITO substrate is indicated by "I". Zincblende and wurtzite phases and corresponding (hkl) are indicated by "Zhkl" and "Whkl", respectively.

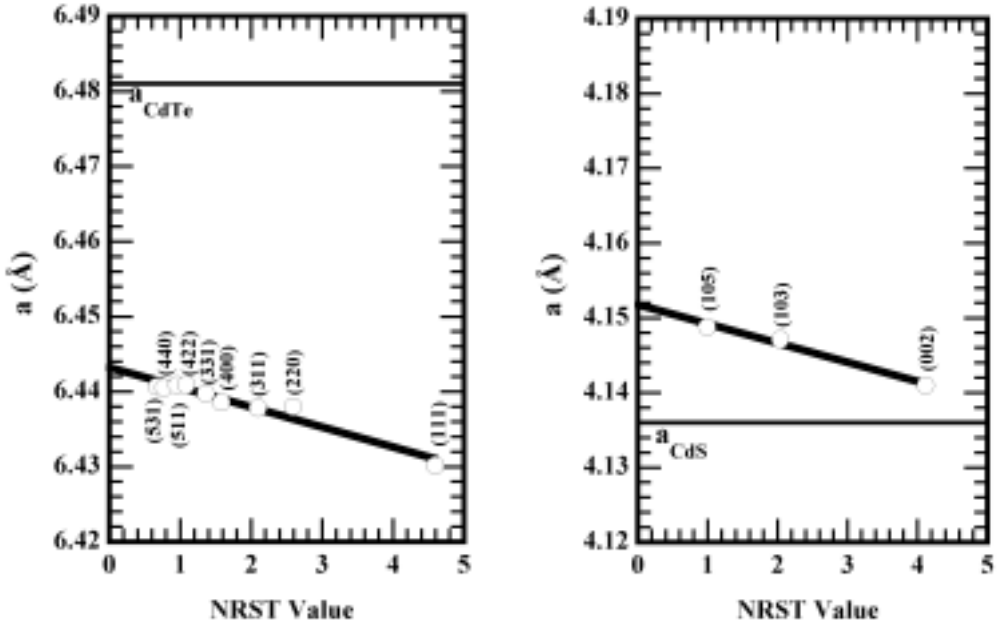


Figure 50. Lattice parameter versus NRST function value for zincblende and wurtzite phases of film shown in Figure 49 for $CdTe_{0.6}S_{0.4}$ after treatment. Horizontal lines indicate the lattice parameter values for pure CdTe and CdS.

Upon heat treatment, two phases are detected, each exhibiting multiple (hkl) reflections, indicating phase segregation and randomization of grain orientation with respect to the substrate. The NRST plots for this film corresponds to the zincblende and wurtzite components are shown in Figure 50. For each phase, the lattice parameters derived from each reflection fell onto a

straight line on the NRST plots, indicating that the treated films are free of any orientation-specific perturbations such as strain. Similar results were obtained at the higher temperatures.

The equilibrium compositions of zincblende and wurtzite phases and the time to reach equilibrium over the range from 360°C to 700°C are shown in Table 19, including data for samples treated at 625°C and 700°C in argon ambient only. For 625°C rates, the composition is identical regardless of ambient, demonstrating that the role played by $CdCl_2$ and O_2 is purely kinetic. The data of Table 19 are graphically represented in a pseudobinary phase diagram (Figure 51). The miscibility gap is bounded by asymmetrical solubility limit curves.

Table 19. Summary of final compositions for different treatment temperatures, and approximate time needed to reach equilibrium for fixed $CdCl_2$ and O_2 concentrations.

T °C, (K)	Ambient	Time (min)	x ± 0.003	y ± 0.005
360, (633)	$CdCl_2$:Ar:O_2	2700	0.041	0.020
415, (688)	$CdCl_2$:Ar:O_2	60	0.058	0.030
445, (718)	$CdCl_2$:Ar:O_2	60	0.066	0.035
480, (753)	$CdCl_2$:Ar:O_2	60	0.078	0.050
525, (798)	$CdCl_2$:Ar:O_2	30	0.095	0.070
570, (843)	$CdCl_2$:Ar:O_2	30	0.110	0.070
625, (898)	$CdCl_2$:Ar:O_2	10	0.140	0.100
625, (898)	Ar	40	0.140	0.100
700, (973)	Ar	15	0.185	0.180

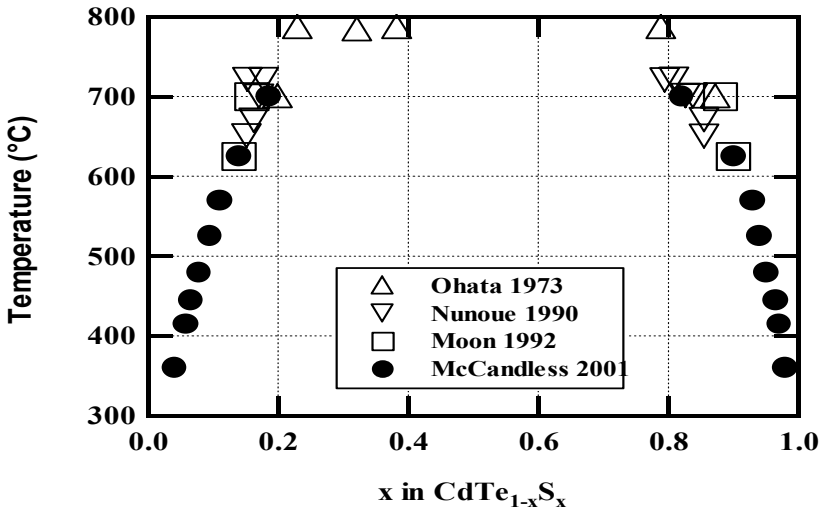


Figure 51. CdTe-CdS pseudobinary phase diagram with data of present work and others: Ohata, *et al.* [55], Nunoue, *et al.* [56], and Moon, *et al.* [57].

4.1.3.1.2 Miscibility Gap Modeling

The first step in mixture analysis is to express the free energy of the system as a function of the molar quantities of it components. Next, the change in free energy as a component is added to the mixture and is determined by the derivative of the free energy with respect to that component. This derivative is referred to as the partial molar free energy. The requirement for

equilibrium is that the partial molar free energy of each component be equal in all phases. The total free energy for a single phase containing two components (1 and 2) is:

$$G^{mix} = N_1 \underline{G}_1 + N_2 \underline{G}_2 + RT\left[N_1 \ln\left(\frac{N_1}{N_1 + N_2} \right) + N_2 \ln\left(\frac{N_2}{N_1 + N_2} \right) \right] + (N_1 + N_2)\Delta \underline{G}^{EX}_{mix} \qquad (20)$$

where N_i is the number of moles of the ith component, $\frac{N_i}{N_1 + N_2}$ is the mole fraction of the ith component, $\underline{G}_i$ is the free energy of the pure ith component, and $\Delta \underline{G}^{EX}_{mix}$ is the excess free energy of mixing. The excess free mixing energy is zero at the endpoints, $N_1 = 0$ and $N_2 = 0$, and is a maximum at $N_1 = N_2$. In Equation 20, the first two terms are the pure species free energies, i.e., the independent free energies of the components before mixing. The second term represents the ideal entropy of mixing. The last term quantifies the departure from ideality, and is called the excess free energy of mixing. All the non-ideal behavior of the mixture is contained in this term, which can be a function of temperature and composition.

The simplest expression of the excess energy of mixing is the two-suffix Nargules equation which is the zero-order term of a Redlich-Kister expansion for a binary mixture:

$$\Delta \underline{G}^{EX}_{mix} = \left(\frac{N_1 N_2}{(N_1 + N_2)^2} \right) \Omega \qquad (21)$$

where

$$\Omega = a - bT . \qquad (22)$$

The parameters a and b are regressed values that fit the model behavior to the experimental data. Each phase may be expected to have its own value of a and b, thus allowing for asymmetrical T^x dependence. In cases where the data shows the miscibility gap to be asymmetrical, different Ω's are used to characterize the mixing energies of each phase. It is difficult to ascribe physical significance to these constants, though they are based on fundamental thermodynamic principles.

Determining the partial molar free energies from Equation 20 is accomplished by differentiating with respect to the molar quantity N_i. The result is:

$$\underline{\mu}_1 = \frac{\partial G^{mix}}{\partial N_1} = \underline{G}_1 + RT \ln\left(\frac{N_1}{N_1 + N_2} \right) x + \Omega \left(\frac{N_2}{N_1 + N_2} \right)^2 . \qquad (23)$$

Then by symmetry,

$$\underline{\mu}_2 = \frac{\partial G^{mix}}{\partial N_2} = \underline{G}_2 + RT \ln\left(\frac{N_2}{N_1 + N_2} \right) + \Omega \left(\frac{N_1}{N_1 + N_2} \right)^2 . \qquad (24)$$

The condition for 2-component, 2-phase equilibrium is:

$$\mu_1^W = \mu_1^{ZB} \tag{25}$$

$$\mu_2^W = \mu_2^{ZB} \tag{26}$$

where the zincblende $CdTe_{1-x}S_x$ and wurtzite $CdS_{1-y}Te_y$ phases are denoted by the superscripts ZB and W, respectively. For the CdS/CdTe system, Equation 25 states that the partial molar free energy of CdS (W) in the CdS-rich phase (W) is equal to the partial molar free energy of CdS in the CdTe-rich phase (ZB).

Making Equations 23 and 24 phase-specific by using $x = \frac{N_1}{N_1 + N_2}$ for CdS in CdTe and $y = \frac{N_2}{N_1 + N_2}$ for CdTe in CdS and substituting into Equations 23 and 24 yields:

$$RT\ln(1-y) + \Omega^W y^2 = RT\ln x + \Omega^{ZB}(1-x)^2 \tag{27}$$

$$RT\ln y + \Omega^W (1-y)^2 = RT\ln(1-x) + \Omega^{ZB}x^2 \tag{28}$$

Note that the values x and y are the minority component mole fractions in the $CdTe_{1-x}S_x$ and CdS_{1-y} Te_y phases. Equations 27-28 are linear with respect to Ω^W and Ω^{ZB}, and are simultaneously solved for Ω^W and Ω^{ZB} at each (*x, y, T*) data point. The parameters a and b are then regressed using Equation 22 from these (*T,* Ω^W and (*T,* Ω^{ZB}) data. Solving Equations 27-28 for Ω^W and Ω^{ZB} shows that Ω is much more sensitive to the concentration of the dilute species. A change in the dilute species from 1% to 0.1% has a much greater effect on Ω than a change of 99% to 99.9% of the predominant species.

4.1.3.1.3 Parameter Regression

The miscibility gap data in Table 20 were used to calculate Ω as a function of temperature and composition. Plots of Ω^W and Ω^{ZB} are shown in Figure 52.

Recalling Equation 22, it is apparent that a linear fit for Ω as a function of temperature would appear to work well for either Ω^W or Ω^{ZB}. The values obtained by the linear regression are:

a^W 23325 J/mol

a^{ZB} 14750 J/mol

b^W 3.71 J/mol/K

b^{ZB} 4.90 J/mol/K

The drawback to the above modeling approach is that a closed form solution for x and y is not possible. It is therefore not suitable as a correlation. For expediency, it is appropriate to fit a

simple polynomial to the calculated curves. For CdS in CdTe, this is well approximated by a cubic fit:

$$x = (4.717e-2) + (-3.104e-4)T + (9.543e-8)T^2 + (-3.687e-10)T^3 \quad (29)$$

$$y = (-1.684e-1) + (1.172e-3)T + (-2.639e-7)T^2 + (2.348e-10)T^3 \quad (30)$$

where T is in ºC. The regression was performed for the range 400ºC -700ºC. The data, model, and empirical fits are shown in Figure 4.6. The empirical fit is in excellent agreement with the calculated solubility curves over the regression range, but the model is unreliable above 750ºC.

The miscibility gap for the CdS-CdTe system has been experimentally demonstrated and quantitatively modeled in the low temperature regime (400ºC - 700ºC). There are a number of factors explaining the unfavorable mixing thermodynamics that give rise to this miscibility gap.

An interesting feature in CdS-CdTe system is the structure difference between CdS (wurtzite) and CdTe (zincblende). The low-temperature data presented here show the limited ability of wurtzite CdS to incorporate zincblende CdTe, and vice versa. The high-temperature data of Ohata *et al*. [55], however, indicate that the wurtzite lattice can exist in either CdTe-rich, CdS-rich, or continuous compositions. In the temperature range 775ºC to 875 ºC, the wurtzite phase segregates into CdS- and CdTe-rich compositions. Above 875ºC, the wurtzite phase exists in a continuous $CdTe_{1-x}S_x$ composition of $0.25 < x < 1$. In contrast, the CdTe-rich zincblende phase exists over a limited composition range of $0 < x < 0.25$. These results indicate that the wurtzite lattice is much more tolerant to the opposite species at higher temperatures. This is consistent with our regressed free energy parameter *b*. If we visualize b as an excess entrophy coefficient of mixing, then the positive value for the wurtzite phase, b^W, reduces the excess free energy as the temperature increases, thereby eliminating the wurtzite-wurtzite miscibility gap at sufficiently high temperatures. Conversely, the negative excess entropy of the zincblende phase, b^{ZB}, makes CdS incorporation more unfavorable as the temperature is increased. An interesting footnote is that metastable $CdTe_{1-x}S_x$ films demonstrate a zincblende to wurtzite transition at x = 0.3, consistent with that observed in the high temperature phase data.

Table 20. CdS/CdTe solubility limits and calculated departure from ideal behavior for the temperatures of Table 19.

T ºC, (K)	x	y	Ω^W, J/mol	Ω^{WB}, J/mol
360, (633)	0.041	0.020	21244	18176
415, (688)	0.058	0.030	21024	18183
445, (718)	0.066	0.035	21143	18389
480, (753)	0.078	0.050	20346	18473
525, (798)	0.095	0.070	20187	18675
570, (843)	0.110	0.070	20875	19021
625, (898)	0.140	0.100	20298	19061
700, (973)	0.165	0.160	19253	19500

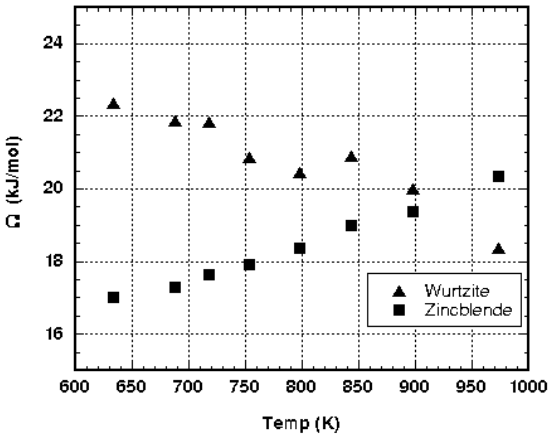


Figure 52. Excess free energies of mixing for CdS/CdTe system.

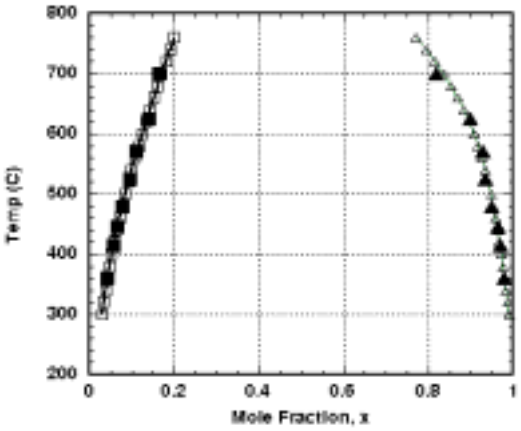


Figure 53. Measured [solid], modeled [open], and empirical fit [line] of CdTe and CdS solubility limits.

At higher reactant concentrations it is also important to consider the CdTe-$CdCl_2$ system. For CdTe-$CdCl_2$, the occurrence of a eutectic at ~490°C suggests that enhanced surface mobility can be expected in situations of $T > 490$°C and high $CdCl_2$ concentration due to liquid Cd(TeCl). Note that the solubility limit for $CdCl_2$ in CdTe is < 0.1 wt% at 490°C. At lower temperatures and low $CdCl_2$ concentration in the presence of O_2, chemical reaction at the surface and in grain boundary between $CdCl_2$, O_2, CdTe and CdS is expected. For treatments where solid $CdCl_2$ is in physical contact with CdTe in air ambient, the favored solid phase reaction is:

$$CdCl_2(s) + O_2(g) + CdTe(s) <=> TeCl_2(g) + 2CdO(s),\ \Delta G_{rxn}(400°C) = -32.9 \text{ kcal/mol.} \quad (31)$$

For vapor $CdCl_2$:O_2:Ar treatments, in which $CdCl_2$ condensation is prevented by maintaining the CdTe/CdS at a higher temperature than the $CdCl_2$ source, the favored reaction between gas phase $CdCl_2$ and O_2 and solid CdTe is:

$$CdCl_2(g) + O_2(g) + CdTe(s) <=> TeCl_2(g) + 2CdO(s),\ \Delta G_{rxn}(400°C) = -49.3\ \text{kcal/mol}. \quad (32)$$

Both cases are thermodynamically favored; in the former case, it is important to recognize the significant partial pressure of $CdCl_2$ obtained at the 400°C reaction temperature = 10 mTorr. For vapor treatments, the $CdCl_2$ partial pressure can be varied over a wide range by controlling the source temperature. Analogous reactions exist for CdS-$CdCl_2$-O_2:

$$CdCl_2(s) + O_2(g) + CdS(s) <=> SCl_2(g) + 2CdO(s),\ \Delta G_{rxn}\ (400°C) = -10.5\ \text{kcal/mol} \quad (33)$$

and

$$CdCl_2(g) + O_2(g) + CdS(s) <=> SCl_2(g) + 2CdO(s),\ \Delta G_{rxn}\ (400°C) = -12.6\ \text{kcal/mol}. \quad (34)$$

In these reactions, a volatile VIB-VIIA species is generated and a solid CdO phase is produced. This reaction scenario was verified experimentally for treatments of both CdTe and CdS powders and films. The CdO has halite (Fm3m) structure, is thermally stable up to 900°C, has the highest ionicity value in the Cd-VIB system (0.78), and is insulating. In the above reactions, the formation of volatile VIB-VIIA species provides a mechanism for enhanced surface mobility. In the presence of O_2 alone, CdTe forms a native oxide according to

$$CdTe(s) + 1.5\ O_2(g) <=> CdTeO_3(s),\ \Delta G_{rxn}\ (500°C) = -66.3\ \text{kcal/mol}. \quad (35)$$

This oxide lies on the TeO_2-CdO pseudobinary tie-line and is the equilibrium native thermal oxide of CdTe, has cubic structure and is electrically insulating. Although it will be shown later that oxides are found in the grain boundaries of thin film solar cells and may 'passivate' the boundaries, their presence on the CdTe surface hinders formation of low resistance contacts and, in the case of CdO, shifts the electronic equilibrium towards Cd-rich, n-type conductivity.

4.1.3.2 Evidence of CdTe Diffusion in to CdS

The CdS layer does not contribute to the photocurrent in thin-film CdTe/CdS solar cells, resulting in optical absorption loss at wavelengths below the CdS bandgap. Since about 1991, quantum efficiency analyses have shown that additional loss in photocurrent is incurred in cells receiving $CdCl_2$ treatment, in the region from the CdS bandgap to ~650 nm [67,68]. We showed that this additional loss originates from formation of $CdS_{1-y}Te_y$ alloy during the $CdCl_2$ treatment, due to CdTe diffusion into CdS. The most compelling evidence for this was obtained by selectively removing the CdTe film and directly analyzing the chemical composition, lattice parameter, and optical transmittance of the remaining CdS film. The exposed CdS film was found to contain an average of ~ 1 wt% Te, exhibit a higher lattice parameter, and exhibit optical transmission that matched the device spectral response from 400 nm to 650 nm. The loss in transmission was consistent with formation of $CdS_{1-y}Te_y$ alloy, having high absorption coefficient at wavelengths above the CdS bandgap. It was further shown that the alloy formed on the CdS side of the junction could be minimized by treatment of the CdS film in $CdCl_2$ vapor in air at 400°C for several minutes prior to deposition of CdTe. This treatment promotes dramatic grain growth in the CdS film and renders it tolerant to further processing with respect to diffusion of CdTe. For superstrate cells in the present study, all the CdS films were treated in

$CdCl_2$ vapor prior to CdTe deposition, which corresponds to the procedure used to fabricate optimized devices, simplifying interpretation of the interdiffusion process.

4.1.3.3 Evidence of CdS Diffusion into CdTe

Diffusion of CdS into CdTe during post-deposition cell processing was first proposed by Birkmire, *et al*. [69] in 1989 to explain anomalous shifts in long-wavelength quantum efficiency and CdTe lattice parameter in PVD CdTe/CdS devices. The quantity of CdS required to produce the observed changes was negligible, corresponding to an equivalent CdS film thickness of ~40 nm, which was not then considered to be a significant matter for devices with CdS films >200 nm thick. Subsequent compositional and precision lattice parameter analysis by IEC of devices made by numerous methods revealed that all moderate to high efficiency CdTe/CdS thin-film devices exhibited $CdTe_{1-x}S_x$ alloy within the structure [70].

Lacking in the earlier studies was determination of the $CdTe_{1-x}S_x$ alloy distribution and its dependence on processing variables. Clearly, its presence in the device did not seem to be destructive to the CdTe/CdS junction [71], but its formation caused CdS consumption, which is a serious issue for high-performance devices in which the parasitic CdS optical loss is simply designed-out by reducing the CdS thickness. For a given post-deposition process, IEC showed that there is a critical CdS thickness below which the device junction performance suffers, due to non-uniform loss of CdS. It was, therefore, critical to quantify the CdS loss process and find window layer options to ameliorate non-uniformities in the CdS film after processing.

In a polycrystalline thin-film CdTe/CdS couple, two paths exist for diffusion of CdS species into the CdTe film: across the grain interface, "bulk diffusion", and via grain boundaries. STEM measurements with spot EDS analysis of the CdTe film after cell processing provided evidence for grain-boundary enhancement of CdS diffusion (Figure 54). The CdS film in the as-deposited structure was ~220 nm thick, and the CdTe grains were ~200 nm wide, as shown in reference [72]. After treatment, the CdS film was reduced to half its initial thickness. EDS analysis parallel to the interface found increased S at grain boundaries. EDS analysis normal to grain boundaries found a decrease in S content towards the CdTe film surface. The central portion of grains contained the lowest S content. In some regions at the original CdS-CdTe interface, the triangular region lying at the apex of the CdTe grain boundary was found to be highly defective and was thinned faster by the ion milling process. In some cases, the regions were found to be milled completely away. This suggests a correlation between disorder and diffusivity, although the causality is not obvious.

Near the surface, sub-micron 'precipitates' were detected, containing elevated Cl levels suggesting incorporation of $CdCl_2$ or other products. Otherwise, Cl was detected at ~1 at% in grain boundaries near the surface and decreased monotonically towards the CdTe-CdS interface. The apparent anti-correlation between the spatial distribution of S and Cl levels reflects the source-sink aspect of the structure due to diffusive transport along grain boundaries. No data was obtained for O levels in these structures.

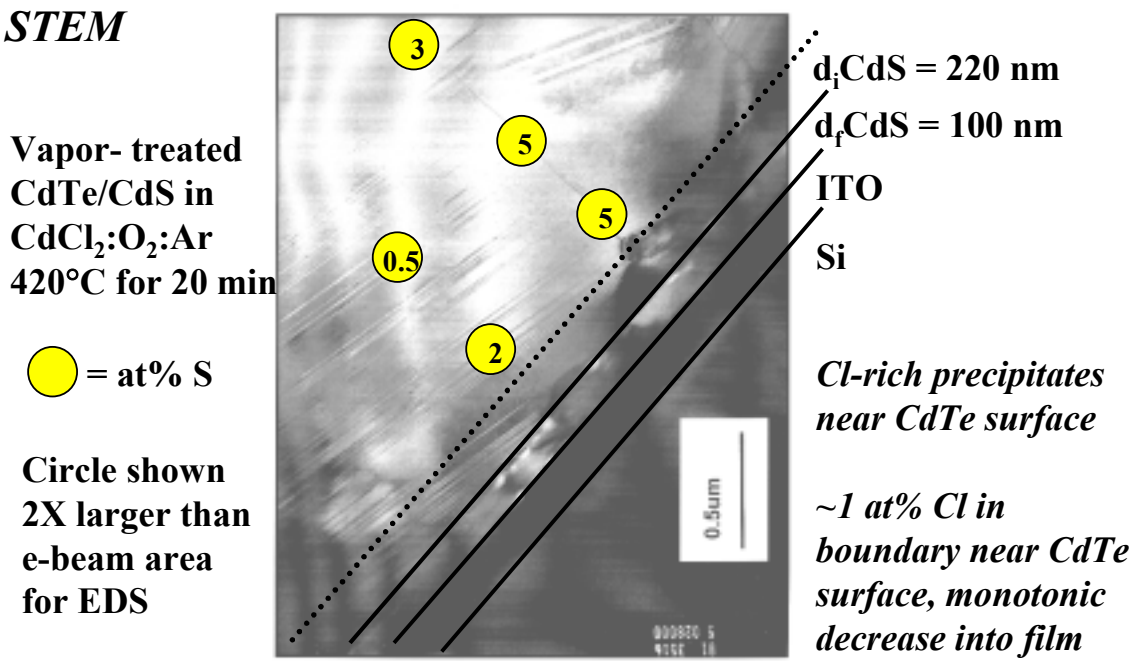


Figure 54. STEM and EDS analysis of near-junction region of CdTe grain and grain boundary.

4.1.3.4 Simulation of XRD Line Profiles and AES Depth Profiles

A full description of the diffusion model used to generate diffraction line profiles and Auger depth profiles is given in the Phase III annual report for this contract and in reference [73]. Success in modeling time-progressive diffusion afforded unique solutions to the alloy volume fraction distribution and was only possible by considering the actual grain size distribution in the structure. This fact immediately illustrated the importance of the grain boundary diffusion process, which supplies additional S species for bulk diffusion into CdTe grains. As described above, substrate and superstrate CdTe/CdS thin film couples were analyzed. For the substrate case, CdS/CdTe/CuTe/Mo/glass structures were used, and the grain size distribution remained constant over the entire treatment temperature and time range explored. The time-progressive diffraction pattern for a substrate film couple treated in $CdCl_2$:O_2 vapor at 440°C is shown in Figure 55.

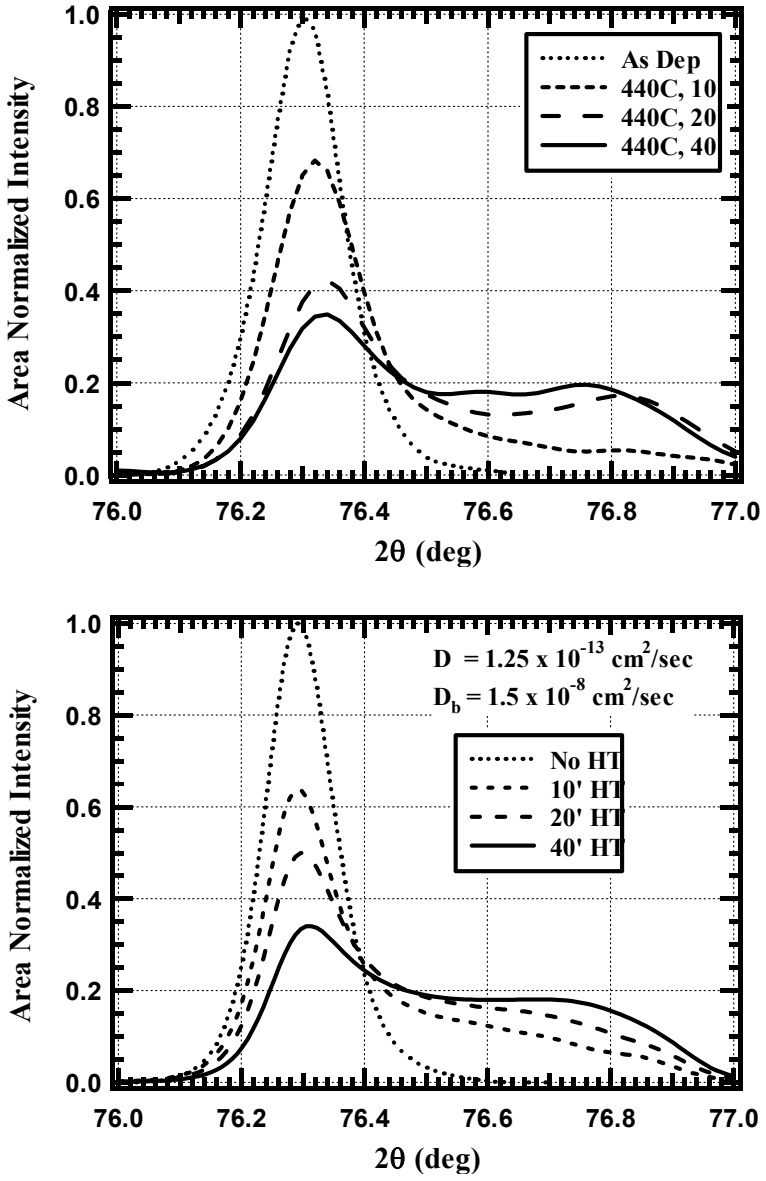


Figure 55. XRD (511)/(333) line profiles for substrate configuration. Measured (top) and modeled (bottom) x-ray diffraction line profiles: as-deposited and after treatment in $CdCl_2$:O_2:Ar vapor at 420°C for 10, 20 and 40 minutes with p($CdCl_2$) = 9 mTorr and p(O_2) = 150 torr.

For the superstrate configuration normally employed to make solar cells, the grain size distribution is observed to change with treatment during the first few minutes. This is particularly significant in devices where the CdTe is deposited at temperatures below ~400°C and the CdTe deposit is heteroepitaxially coordinated to the CdS film. The line profiles of these samples were thus modeled by taking this into account. Figure 56 shows time-progressive diffraction pattern for a superstrate film couple treated in $CdCl_2$:O_2 vapor at 420°C.

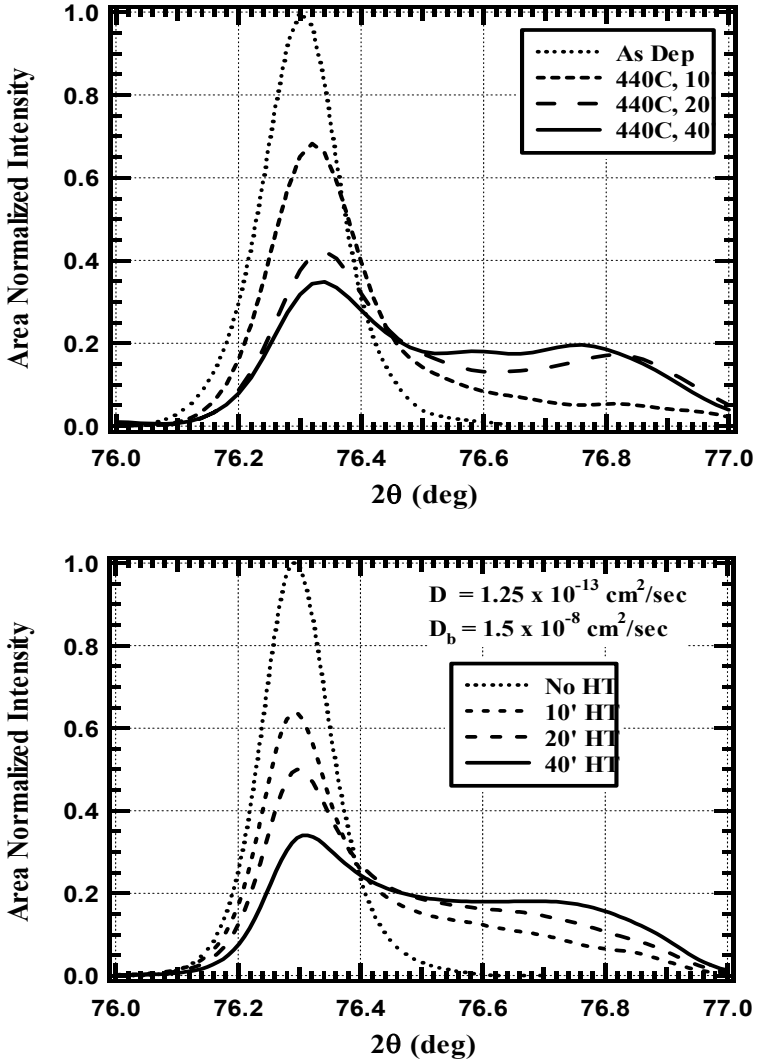


Figure 56. XRD (511)/(333) line profiles for superstrate configuration. Measured (top) and modeled (bottom) x-ray diffraction line profiles: as-deposited and after treatment in $CdCl_2$:O_2:Ar vapor at 420°C for 10, 20 and 40 minutes with p($CdCl_2$) = 9 mTorr and p(O_2) = 150 torr.

4.1.3.5 Dependence of Diffusion on Processing Parameters

Performing the above analysis at different temperatures allowed the activation energies of the diffusion processes to be determined. The treatments were conducted at *fixed* $CdCl_2$:O_2:Ar vapor concentration. Comparative values for the bulk diffusion coefficients were obtained by Auger electron depth profiles of sulfur distribution in single crystals compared to the XRD results of substrate and superstrate film samples. The combined bulk diffusion coefficient data is shown in Figure 57, yielding an activation energy of 2.8 eV for bulk diffusion of CdS into CdTe. This activation energy is the same as has been reported for the self diffusion of Cd in CdTe attributed to formation of singly-ionized Cd interstitials [74]. For the films, the grain boundary diffusion coefficient obtained at the three temperatures is shown in Figure 58, yielding an activation energy of 2.0 eV.

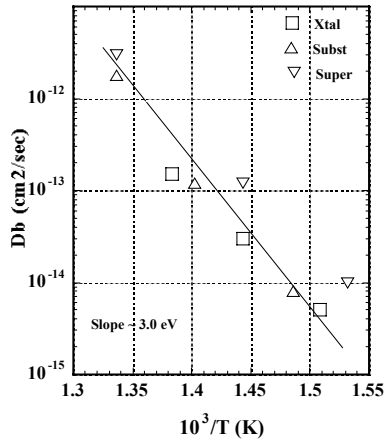


Figure 57. Arhennius plot of bulk diffusion coefficients vs inverse of treatment temperature for values obtained by modeling XRD line profiles of thin-film CdTe/CdS samples and from AES depth profiling of S distribution in CdTe single crystal.

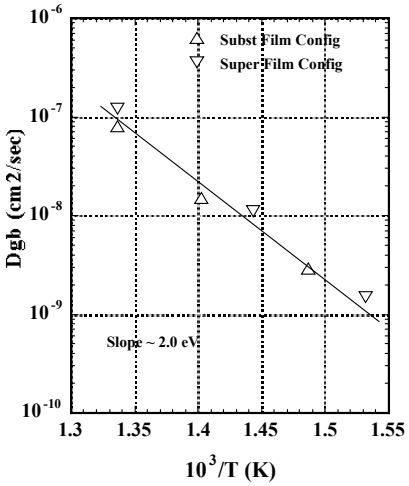


Figure 58. Arhennius plot of grain boundary diffusion coefficients vs inverse of treatment temperature for values obtained by modeling XRD line profiles of thin-film CdTe/CdS samples.

The activation energy for grain boundary diffusion has not been ascribed to a single defect or mechanism, but is likely due to the chemical reactions in the grain boundaries leading to formation of volatile species. The estimated value (2.0 eV) is the magnitude as that found for the reactions between CdTe and $CdCl_2$ and O_2 vapors (2.1 eV) and implies a dependence of the grain boundary diffusion coefficient on the concentration of the kinetic-enhancing species. The same diffusion model was used to estimate D_b and D_{gb} for CdTe/CdS couples treated at fixed temperature, $T = 420°C$, in vapor ambient having different $CdCl_2$ and O_2 concentrations. As with prior studies, time-progressive treatments were employed to ensure uniqueness of the estimated diffusion coefficients. The effect of ambient concentrations on the measured line profiles for

treatments at 420°C and 20 min are shown in Figure 59. The corresponding diffusion coefficients obtained by modeling time-progressive treatment data are shown in Figure 60.

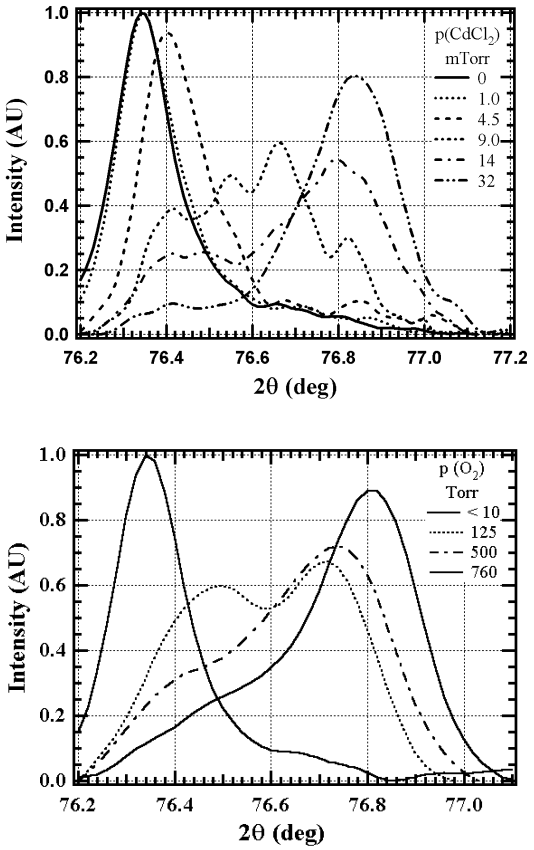


Figure 59. XRD (511)/(333) line profiles for superstrate configuration. Measured data for reactions in $CdCl_2$:O_2 at 420°C and 20 min with constant $p(O_2)$ = 125 Torr and varying $p(CdCl_2)$ (top) and constant $p(CdCl_2)$ and varying $p(O_2)$ (bottom).

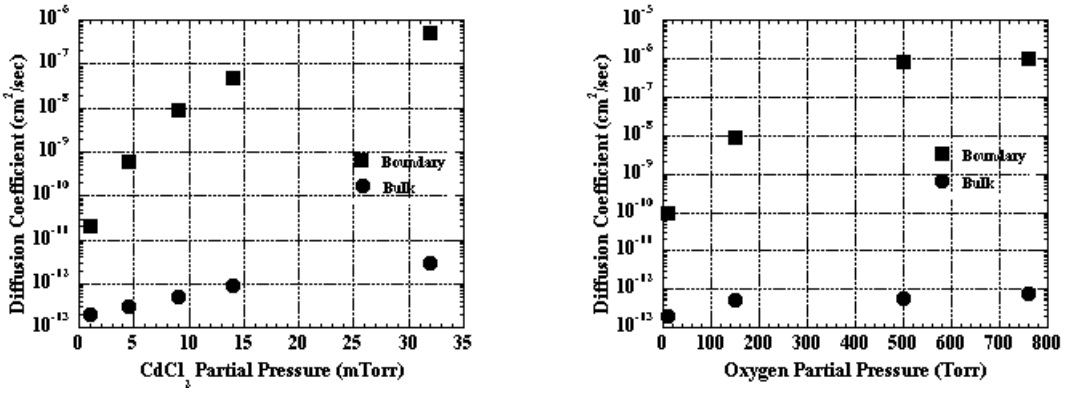


Figure 60. Sensitivity of bulk and grain boundary diffusion coefficients to $pCdCl_2$ at constant pO_2 ~ 125 Torr (left) and to pO_2 at constant $pCdCl_2$ = 9 mTorr (right), at T = 420°C.

The grain boundary diffusion coefficient depends strongly on the concentration of $CdCl_2$ and O_2 in the vapor ambient and varies over 4 orders in the concentration ranges examined. The saturation of the grain boundary diffusion coefficient at very high pO_2 is easily understood as the effect of creating excess oxide species in the grain boundaries, which suppresses further diffusion. Not surprisingly, the bulk diffusion coefficient is weakly dependent on either $CdCl_2$ or O_2 concentration in the vapor ambient. At very low $pCdCl_2$ and O_2, D_{gb} approaches D_b, and in such cases, a one-dimensional diffusion model can account for the measured XRD line profiles

4.1.3.6 Control of Diffusion by Manipulation of Microstructure and Chemistry

Having shown the overall diffusion process is enhanced by the grain boundaries in PVD CdTe films, it is necessary to determine how the grain structure varies with deposition conditions and to find ways of retarding the grain boundary component. For evaporated CdTe at a fixed incident flux, substrate temperature controls grain size and crystallographic defect density. In the present deposition system, substrate temperatures exceeding 350°C are achievable, at a growth rate of 0.2 um/min. CdTe films deposited at elevated temperatures exhibit progressively larger grain size as shown in the histograms of Figure 61 and the AFM images of Figure 61, for 4 micron thick CdTe films deposited on CdS/ITO/soda-lime glass. Note that CdTe depositions below 300°C exhibit mean grain size less than 0.3 micron. The texture coefficient [75], p(111), before and after $CdCl_2$ treatment at 420ºC for 20 minutes is listed in Table 21 for CdTe films deposited on CdS at 5 different substrate temperatures.

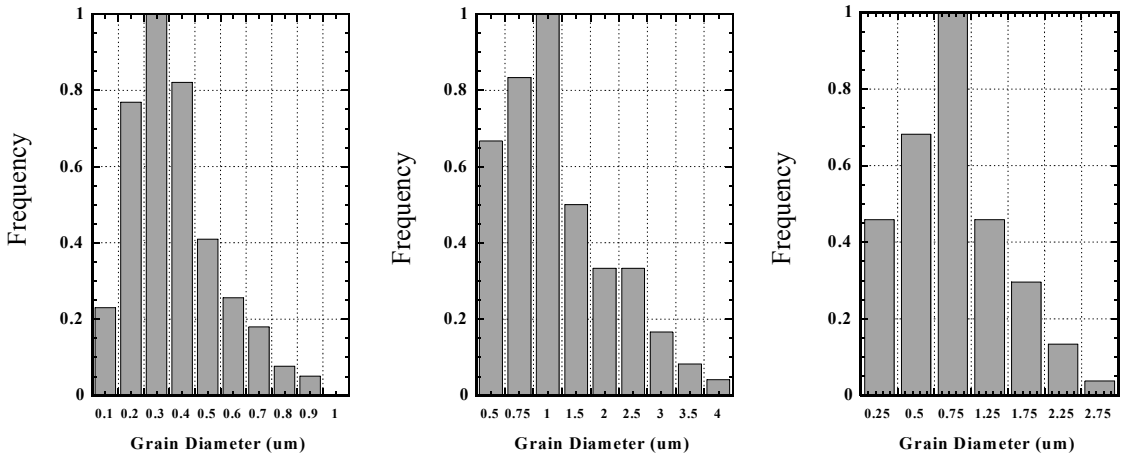


Figure 61. Effect of deposition temperature on grain size distributions for 275°C (left), 350°C (middle), and 400°C (right).

Table 21. Texture coefficient and mean grain size of 4 micron thick CdTe films deposited at different substrate temperatures on CdS/ITO/soda-lime glass before and after $CdCl_2$ vapor HT at 420ºC for 20 minutes.

Tsub (C)	As Dep p(111)	HT TC(111)	As Dep Grain Size (μm)	HT Grain Size (μm)
250	5.3	1.0	0.2	1.2
275	4.5	1.5	0.2	1.3
325	3.6	1.8	0.7	1.4
340	2.5	1.6	0.9	1.8
350	2.5	1.5	1.3	2.0

After $CdCl_2$ treatment, the texture coefficients are similar for films deposited at all substrate temperatures. However, the mean grain size doubled for films deposited above 300°C and quadrupled for films deposited below 300°C. Note that in the report for Phase I under this contract, the coalescence of sub-micron grains into larger grains was shown to occur on a time-scale of ~ 1 minute[76]. From Table 21 it can be seen that films deposited at higher temperature undergo significantly less structural change during $CdCl_2$ vapor treatment, with maximum lateral grain size on the order of the film thickness.

Comparing this data with that of films deposited at much lower temperature, such as by electrodeposition (ED), and at much higher temperatures, such as by CSS, it is possible to establish a framework linking the deposition process to the effects of post-deposition processing on the structure and interdiffusion within the structure.

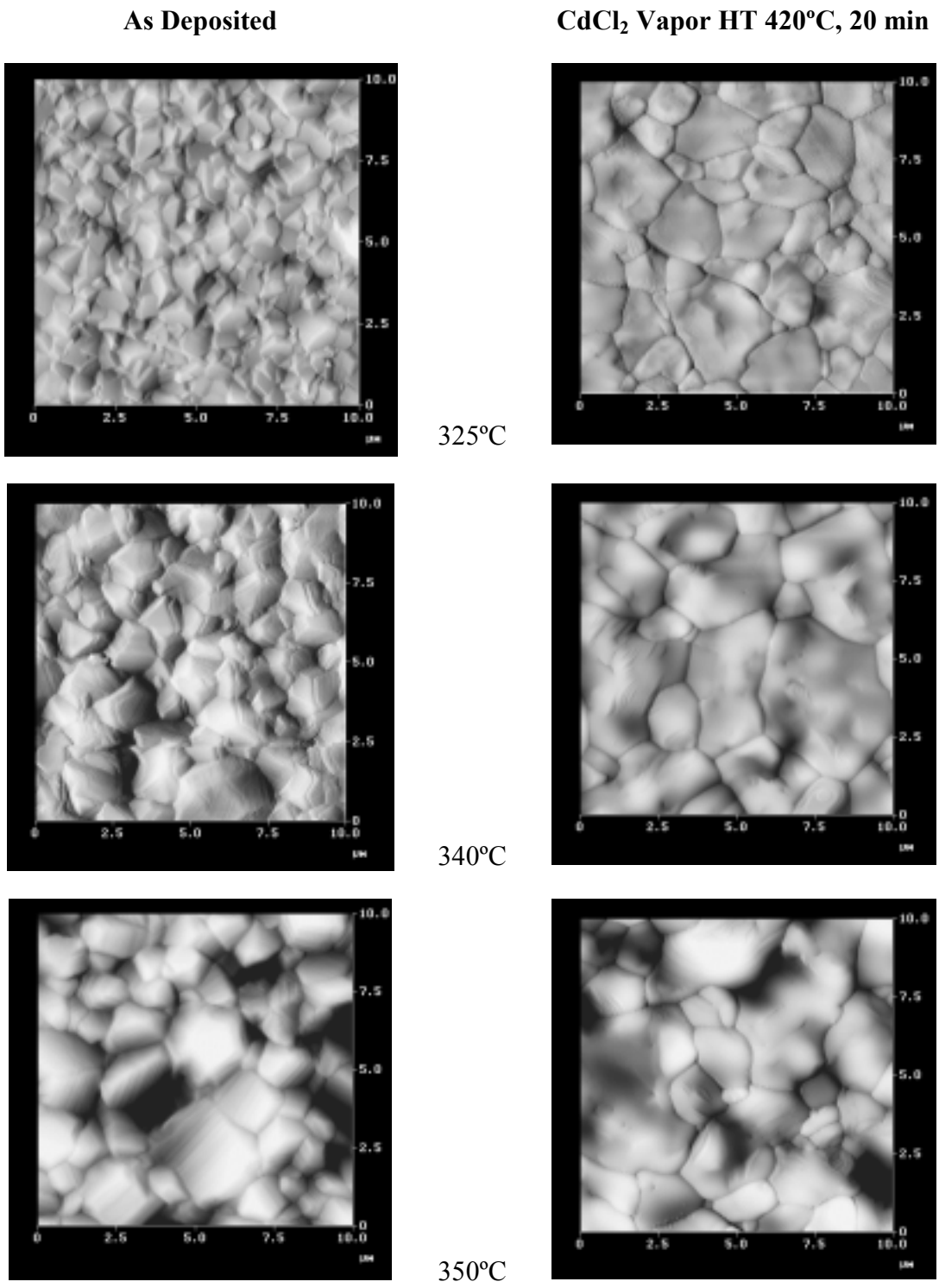


Figure 62. Tapping AFM images of the CdTe surface for as deposited (left) and $CdCl_2$ treated films (right) for films deposited at fixed incident Cd, Te flux but different substrate temperatures.

A comparison of as-deposited and treated materials properties and device results for three CdTe/CdS cell fabrication processes is shown in Table 22. The surface morphology for these samples is shown in Figure 63. The most notable result is that similar performance was achieved in structures with vastly differing thermal history, grain size, and composition. For the electrodeposited sample, the post-deposition anneal and treatment in $CdCl_2$:O_2:Ar only marginally increased grain size, but did promote intra-grain recrystallization, evidenced by the loss of (111) texture. The treatments also formed a significant quantity of $CdTeO_3$ and CdO on the CdTe surface and within the film, presumably along grain boundaries. In contrast, the CSS sample exhibited no grain growth, no recrystallization, and negligible oxide products. To a first order, the surface roughness was unchanged in all the samples examined.

Table 22. Comparative treatments and properties used to obtain specified cell performance. 'Mean Grain Dia' ≡ mean diameter of grains found over a 10 x 10 μm survey, 'RMS' ≡ root-mean-square surface roughness, 'p' ≡ penetrating, and 'w' ≡ weak.

State	Processing Conditions	Grain Orientation	Mean Grain Dia and RMS μm, nm	Surface Phases	V_{oc} (mV)	Eff (%)
As-Dep						
ED	85°C, aqueous	(111)	0.15, 25	CdTe	-	-
PVD	300°C, 10^{-6} Torr	(111)	0.50, 50	CdTe	-	-
CSS	600°C. 1 Torr	Random	1.5, 100	CdTe	-	-
Treated						
ED	Anneal + $CdCl_2$ HT	Random	0.20, 30	p.$CdTeO_3$, p.CdO	800	11
PVD	Anneal + $CdCl_2$ HT	Random	2.0, 70	$CdTeO_3$, CdO	820	12
CSS	$CdCl_2$ HT	Random	1.5, 100	w.$CdTeO_3$, w.CdO	810	12

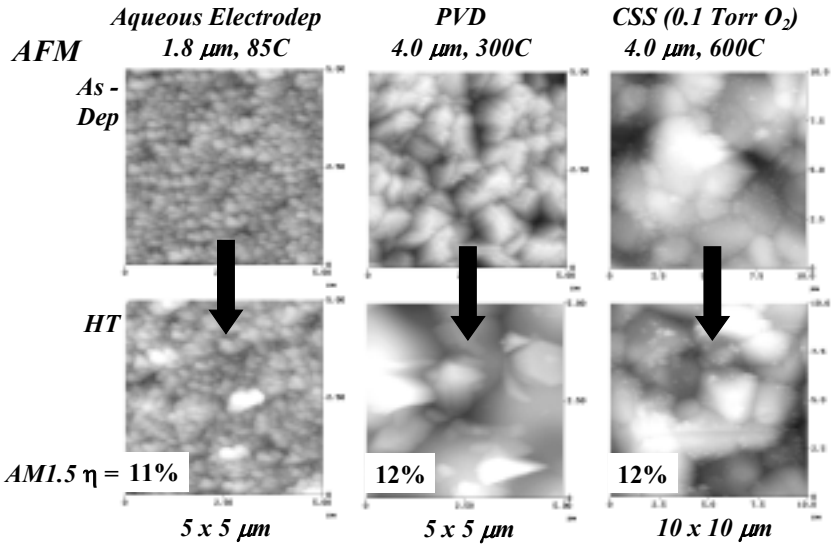


Figure 63. AFM images of CdTe films deposited by electrodeposition, physical vapor deposition and close-space sublimation. Top: as-deposited; Bottom: after cell processing treatment sequences as described in Table22.

The PVD samples are considered in more detail. As with ED films, (111) texture was lost after thermal treatment; this intra-grain effect occurs more rapidly than grain growth, in a manner similar to primary and secondary recrystallization in cold-worked metals. The as-deposited PVD grain size was intermediate to the ED and CSS cases and increased after annealing and again after treatment in $CdCl_2$:O_2:Ar. A detailed AFM study of CdTe surface morphology evolution with treatment time in $CdCl_2$:O_2:Ar showed that grain growth occurs by coalescence of small-grain clusters and often results in bimodal grain size distributions [19].

The progression is shown in XRD line profiles and SEM and STEM images for a different sample (Figure 64 and Figure 65). Precision lattice parameters of the films reveal that as-deposited PVD films exhibit in-plane compressive stress that is relaxed during anneal at 600°C. Additional treatment in $CdCl_2$:O_2:Ar at 420°C for 20 minutes reduces the lattice parameter slightly, due to alloying between the CdTe film and CdS. The SEM image after treatment in $CdCl_2$:O_2:Ar shows considerable rounding of the grain edges. The STEM cross-section image in Figure 65 allowed the depth of the curved grain boundary to be estimated, extending less than ~200 nm into the film from the CdTe surface, which consistent with the root-mean square (rms) values measured over the entire surface. The STEM image also shows a low density of crystallographic defects in the CdTe grains for PVD films receiving both anneal and $CdCl_2$:O_2:Ar treatments, consistent with earlier work [77]. Oxide formation on PVD samples was intermediate to that observed on ED and CSS samples. The phases CdO and $CdTeO_3$ were observed by GIXRD on all PVD samples treated in $CdCl_2$:O_2:Ar. The intensity of these reflections was correlated with the pO_2 during the $CdCl_2$:O_2:Ar treatment.

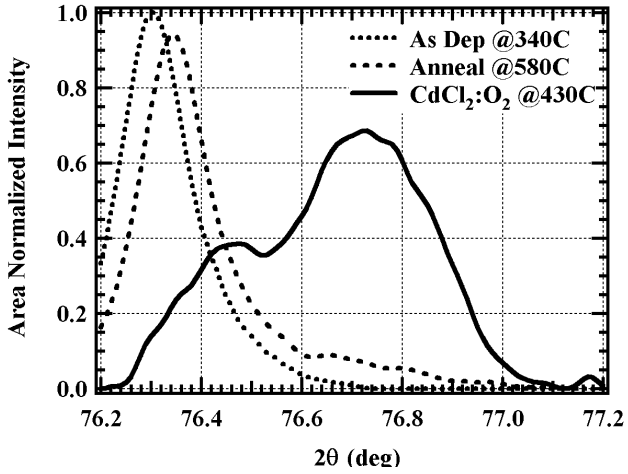


Figure 64. (511)/(333) x-ray diffraction line profile for the superstrate structures: after deposition at 340°C, after annealing at 580°C for 15 minutes; after treatment in $CdCl_2$:O_2:Ar vapor at 430°C for 20 minutes.

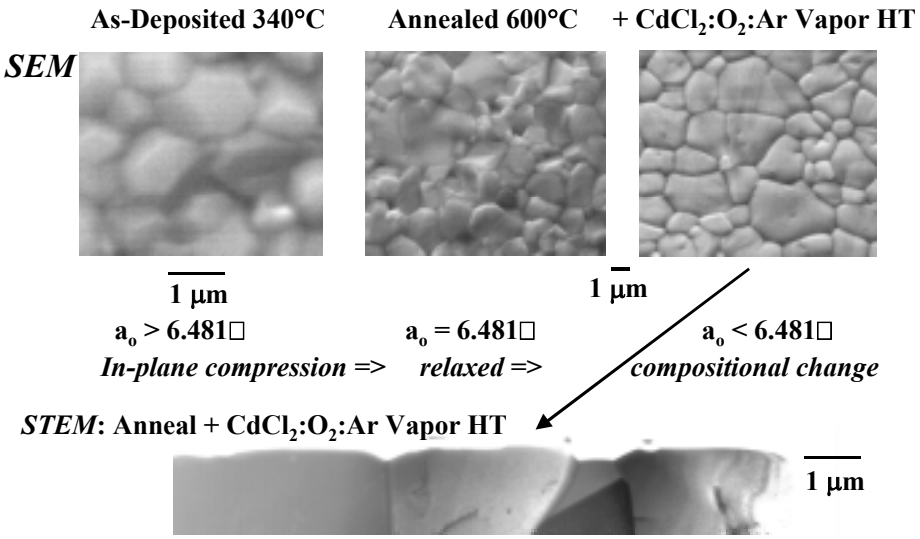


Figure 65. SEM surface and STEM cross-section images and precision lattice parameter (a_o) of PVD CdTe film at different processing stages.

Another method for reducing grain boundary diffusion in small-grain CdTe films is by performing a moderate-temperature treatment at 400°C to 450°C in oxygen-containing atmosphere to form penetrating native oxides in the CdTe film. These oxides, detected using GIXRD, consist primarily of $CdTeO_3$, are relatively stable during subsequent $CdCl_2$:O_2:Ar vapor treatment and retard grain boundary diffusion of CdS as seen by the near elimination of the $CdTe_{1-x}S_x$ alloy tail in x-ray diffraction line profiles. During $CdCl_2$ treatment, CdO is also formed as a result of chemical interaction between the CdTe and the treatment ambient. Controlling the degree of oxide formation and interdiffusion with thin CdTe layers depends on optimizing the pre-anneal steps, the vapor composition and reaction temperature used during the $CdCl_2$ treatment.

Figure 66 compares the $CdTe_{1-x}S_x$ XRD (511/333) line profiles after treatment in $CdCl_2$:O_2:Ar vapor for different pre-treatments of 1.3 micron thick CdTe/CdS. The line profiles have been normalized to the same area and show that a sample with argon pre-anneal at 580°C for 5 minutes exhibits significantly less $CdTe_{1-x}S_x$ alloy, hence CdS consumption, than the sample with no pre-anneal (data on left). The pre-annealed sample contains an equivalent CdS thickness of 13 nm, compared to 53 nm for the non-annealed sample. In the right figure, 450°C air pre-anneal is also shown to retard CdS diffusion, resulting in equivalent CdS consumption of 45 nm for 10 minutes and 35 nm for 20 minute pre-anneal treatment.

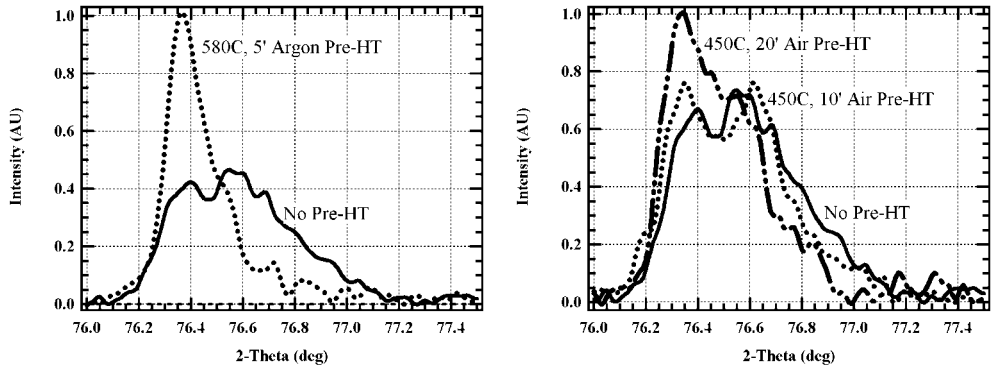


Figure 66. X-ray diffraction line profiles of $CdTe_{1-x}S_x$ (511/333) of CdTe/CdS films treated at 420°C in $CdCl_2$:O_2:Ar vapor with and without pre-anneal (pre-HT) step. Left: argon pre-HT; Right: air pre-HT.

To further illustrate the retarding effect of air pre-treatment, the diffusion process was modeled for ED samples with and without pre-treatment in air at 450°C. Figure 67 shows XRD line profiles of 1.8 μm thick ED films treated for different times at 420°C at $pCdCl_2$ = 9 mTorr and pO_2 = 150 Torr, corresponding to films having *sub-micron* grains, with and without penetrating $CdTeO_3$, formed by annealing in Ar:O_2 ambient. With no $CdTeO_3$, D_{gb} of ~1.5 x 10^{-8} cm^2/s leads to complete conversion of the CdTe film to the equilibrium alloy composition of $CdTe_{0.95}S_{0.05}$, with significant CdS consumption.

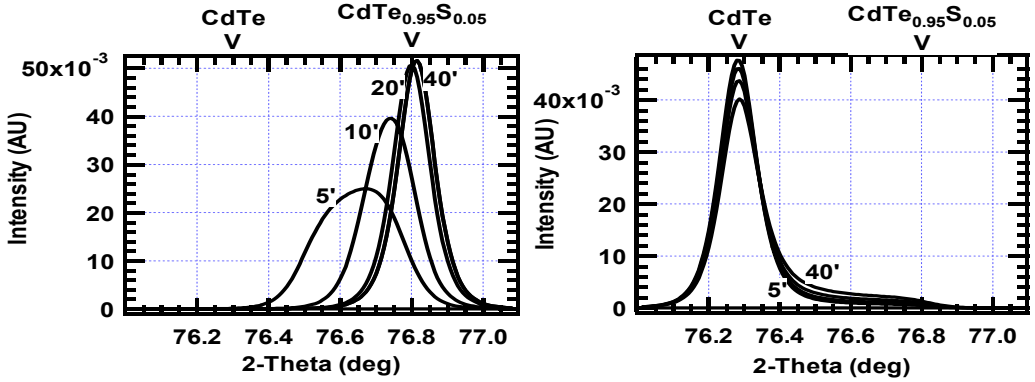


Figure 67. Modeled time-progressive XRD line profiles for 0.2 μm diameter grains in 1.8 μm thick CdTe films for fixed D_b = 1.25 x 10^{-13} cm^2/s and D_{gb} = 1.5 x 10^{-8} cm^2/s (left) and reduced boundary diffusion D_{gb} = 1.5 x 10^{-11} cm^2/s (right).

With penetrating oxides, D_{gb} is reduced to 1.5 x 10^{-11} cm^2/s and a trace diffusion tail is observed, similar to 1-dimensional bulk diffusion. In addition to representing ED films containing oxides, the line profiles in the right box of Figure 67 also correspond to measured CSS films *deposited* in relatively low pO_2 ambient, ~ 0.1 Torr and treated in $CdCl_2$:O_2:Ar at 420°C for 20-40 minutes. Although no $CdTeO_3$ phases are detected in the CSS films, the D_{gb} is negligible. This suggests that oxygen during growth can inhibit interdiffusion during subsequent treatments in $CdCl_2$:O_2, by either producing oxides at levels below the detection limit for the XRD methods (< 1 wt%) or by reducing the grain boundary width.

4.1.4 Summary and Conclusions

The CdTe-CdS phase system has been analyzed in thin-film structures. The miscibility gap for the CdTe-CdS pseudobinary system was investigated in the temperature range used to process thin-film solar cells, i.e., from 400°C to 625°C. Metastable single-phase $CdTe_{1-x}S_x$ alloy thin films with composition near the middle of the alloy range, x~0.4, were deposited by thermal evaporation. Thermal treatment in a kinetically enhancing ambient resulted in segregation of the equilibrium alloy phases. Analysis of the resulting x-ray diffraction patterns yielded precision lattice parameters, hence composition, of the Te-rich zincblende and S-rich wurtzite phases. The *T-x* phase boundaries were found to be asymmetrical and were modeled using non-ideal solution thermodynamics. The empirical and modeled phase boundaries provide the fundamental basis for investigation of interdiffusion between CdTe and CdS.

Analysis of superstrate and substrate CdTe/CdS structures with CdTe deposited at low temperatures has allowed chemical and thermal effects to be de-coupled. The effects of the observed phenomena on thin-film polycrystalline CdTe/CdS device operation can be summarized as follows. CdS diffusion into CdTe reduces the CdTe bandgap slightly, lowering the built-in voltage. This is offset by a slight increase in long wavelength quantum efficiency. CdS thickness is reduced, which increases light generated current due to greater absorption of short wavelength photons in CdTe. However, non-uniform CdS consumption can lead to poor overall junction behavior by the formation of a sufficient number of parallel junctions between CdTe/TCO and CdTe/CdS. As will be shown in the next section, this problem has been addressed empirically by improving CdS growth habit and introducing high resistance oxide layers between CdS and the TCO. The effect of bandgap variations parallel to the junction interface is still not understood.

Grain size is not an efficiency-limiting parameter for films with grains from 0.2 to < 2 microns in lateral dimension in the 11 to 12% efficiency range. We have shown that in PVD films, the $CdCl_2$ treatment causes grain growth by a coalescence process. However, it seems that CdTe films having sub-micron grains can benefit in the device from the growth of penetrating oxides which electrically passivate grain boundaries and kinetically reduce CdS consumption during treatment with $CdCl_2$ and O_2. High conversion efficiencies are still restricted to cells with CdTe deposited by CSS in oxygen-containing ambient. A negative consequence of oxide formation on the CdTe surface is the need for aggressive chemical treatments to allow low resistance contacts to be formed. Residual oxygen in grain boundaries may play a significant role in controlling grain boundary diffusion of contact-related species such as contaminants and dopants. The dependence of the limiting diffusivites for CdS diffusion into CdTe on temperature and ambient composition in thin-film couples have been determined, yielding activation energies for bulk and grain boundary diffusion processes. The bulk diffusion appears to be limited by the Cd self diffusion, while the boundary diffusion is chemically limited.

Intra-grain recrystallization proceeds more rapidly than grain growth, which proceeds more rapidly than CdS diffusion, even in films without oxides. The observed benefit of high temperature growth or high temperature anneal strongly suggests that grain quality is of paramount importance to obtaining high junction quality. The role of intra-grain properties such as defect density, doping, and bandgap on recombination needs to be investigated to facilitate development of cells with V_{oc} beyond 900 mV and efficiency beyond 20%.

The chemical and kinetic aspects described here for processing thin-film CdTe/CdS solar cells provide a framework for failure and variation analysis and control of large-area cells in modules. In particular, controlling CdS thickness and CdTe grain properties during growth or treatments will become more critical as CdS and CdTe film thickness are reduced by design. This analysis suggests that 'tolerant' processing windows exist for fabricating efficient cells in the low-limit of semiconductor film thickness. Methods of sensing film morphology and chemical composition during growth and treatment can allow timely feedback to process controls in a manufacturing environment.

4.2 Window Layer Processing

4.2.1 Introduction

As described in Section 4.1, optical absorption in the CdS layer is the largest potential source of photocurrent loss, making CdS film thickness in the device a critical control parameter. This naturally assumes that the glass and TCO have appropriate properties to serve as low-absorption window layers. Maintaining junction quality in superstrate structures with $d_{CdS} < 100$ nm depends on maintaining a uniform interface throughout the processing to avoid formation of parallel junctions between CdTe and the TCO. From the CdS perspective, this condition depends on the CdS growth habit and film density, and the change in CdS thickness with subsequent processing. From the TCO perspective, reducing the forward diode current in CdTe/TCO junctions reduces the effect of parallel junctions on V_{oc}.

Materials measurements of the interfacial region in high efficiency cells verify that the interface consists of $CdTe_{1-x}S_x/CdS_{1-y}Te_y$, alloys, where the interfacial values of x and y correspond to the solubility limits in the CdTe-CdS system at the device processing temperature. Although the alloy *distribution* throughout the cell is not at equilibrium, due to diffusion-limiting processes, the interface is at chemical equilibrium and establishes the boundary condition for interdiffusion. The $CdTe_{1-x}S_x$ and $CdS_{1-y}Te_y$ alloys form via diffusion across the interface during CdTe deposition and post-deposition treatments and have significant effects on photocurrent and junction behavior. Formation of the $CdS_{1-y}Te_y$ alloy on the S-rich side of the junction reduces the bandgap and increases absorption, reducing photocurrent in the 500 to 600 nm range. Formation of the $CdTe_{1-x}S_x$ alloy on the Te-rich side of the junction reduces the absorber layer bandgap, due to the optical bowing parameter of the CdTe-CdS alloy system. This increases the long wavelength spectral response and thus photocurrent by $J_L \sim 0.5$ mA/cm^2, but is nearly offset by small reduction in $V_{oc} \sim 25$ mV.

Other significant effects of this alloy formation shown in Section 4.1 include spatially non-uniform consumption of the CdS layer, penetration of CdS into the CdTe film grain boundaries, and relaxation of lattice strain between CdTe and CdS. Non-uniform consumption of CdS leads to parallel junctions between $CdTe_{1-x}S_x$/ $CdS_{1-y}Te_y$ and $CdTe_{1-x}S_x$/ ITO (or SnO_2), resulting in a net increase in J_o, which reduces V_{oc}. Penetration of S-rich species into the CdTe grain boundaries can produce a three-dimensional junction, which increases the actual junction area, also reducing V_{oc}. The grain boundary penetration of CdS in CdTe is accelerated by $CdCl_2$ and O_2 chemical activity during the post-deposition treatment and is extremely sensitive to the physical and chemical state of the CdTe film prior to the treatment. Evidence is mounting that suggests grain boundaries play a dominant role in controlling dark diode current, photocurrent

collection, and stability, and processing techniques which control grain boundary properties should aid controlling film properties over the large areas required for module manufacturing.

An effective window layer must overcome all these issues. Maintaining good junction performance in cells with ultra-thin CdS requires: 1) lateral control of CdS film thickness and 2) reducing J_o of the CdTe/ITO junction. CdS film uniformity in cells is affected by coverage during CdS deposition and diffusion during thermal processing. Reduced J_o in CdTe cells with thin CdS is obtained by the inclusion of a high resistance, HR, 'buffer' layer between CdTe and ITO78. A wide range of oxides has been demonstrated as effective buffer layers for CdTe/CdS devices with ultra-thin CdS layers. The oxides include un-doped and Cd-doped SnO_2, In_2O_3, Ga_2O_3, and Cd_2SnO_4, representing a range of electrical resistivity from 10^1 to 10^5 Ω-cm, suggesting that composition and electrical conductivity are not critical parameters. This aspect allows buffer layer selection to be based on criteria of optical transmittance, ease of manufacture, etc. The effect of high resistivity In_2O_3 and Ga_2O_3 layers on as-deposited CdS film coverage and grain size was investigated. The beneficial effect of incorporating a high resistance interlayer between the TCO and CdS was investigated in devices, showing that V_{oc} and FF can be maintained as CdS thickness is reduced, yielding PVD cells with efficiency >13%. It has been shown that the composition of the high resistance layer is less important than its resistivity, and results are given for devices with In_2O_3, SnO_2, Ga_2O_3 buffer layers fabricated by oxidation of metal precursors deposited onto ITO/glass substrates. It is shown that the grain size and coverage of CdS films are significantly improved when deposited on buffer layers as thin as 50 nm.

The critical properties of the oxide buffer layers are wide bandgap and low conductivity, and it is essential that the CdS film is deposited conformally onto the HR layer. In the previous phase of this contract, we showed that larger CdS grains and superior coverage are obtained for chemical bath deposited (CBD) CdS films on In_2O_3 buffer layers. In this phase, Ga_2O_3 is introduced as a suitable material for HR buffer layers. Table 24 compares the crystallographic and optical properties of Ga_2O_3 to other candidate binary oxides.

The CdS deposition method appears to be increasingly critical as the CdS thickness is reduced. A new chemical bath CdS deposition technique was developed that yields a low density of pinholes and particulates and has >90% utilization of cadmium species, CdS/CdTe adhesion can be a problem during some post-deposition treatments. For cells with ITO, crystallization of the ITO layer prior to CdS growth improves CdS/CdTe adhesion and reduces reaction of different glasses with $CdCl_2$.

Another path for improved processing tolerance and performance evaluated in this report is $Cd_{1-x}Zn_xS$ window layers. Alloying CdS with ZnS to form $Cd_{1-x}Zn_xS$ alloy shows promise for device optimization by relaxing the thickness required to obtain a specified photocurrent. The gains in light generated current, J_L, obtainable by widening window layer bandgap in superstrate CdTe solar cells using $Cd_{1-x}Zn_xS$ and the $Cd_{1-x}Zn_xS$ film thickness required to achieve similar J_L for given, thinner, CdS film thickness were estimated. The light generated current, J_L, was calculated by integration of interpolated global AM 1.5 spectrum [79] with quantum efficiency (QE) curve synthesized from CdS, $Cd_{1-x}Zn_xS$, and ZnS optical absorption data [80,81,82] and normalized long wavelength spectral response of a high efficiency CdTe cell. Calculations were

performed for *no* glass/TCO losses and for measured 7059/ITO absorption losses with 4% panchromatic reflection

As Table 23 shows, for a specified photocurrent, e.g. ~26 mA/cm^2, using $Cd_{1-x}Zn_xS$ alloy with x ~ 0.3 would enable the thickness to be increased from 25 nm to >50 nm. For fixed window film thickness, e.g. 100 nm, nearly 2 mA/cm^2 can be gained by using $Cd_{1-x}Zn_xS$ alloy with x ~ 0.3 instead of pure CdS. Recent calculations showing an increase in valence band offsets in Zn-VI semiconductors suggest that addition of Zn to the interface may also translate to higher Voc83.

Table 23. J_L estimates for different window layer thicknesses with glass/TCO absorption and 4% panchromatic reflection loss.

Thickness (nm)	J_L (mA/cm^2)		
	CdS	$Cd_{0.7}Zn_{0.3}S$	$Cd_{0.5}Zn_{0.5}S$
0	27.3	27.3	27.3
10	26.7	27.0	27.2
25	**26.1**	26.7	27.0
50	25.1	**26.2**	26.9
75	24.4	25.8	26.7
100	23.8	25.5	26.6
150	22.9	25.0	**26.5**

It is important to emphasize the optical loss that can be incurred in the CdS layer if it reacts with the CdTe layer as a result of interdiffusion. Formation of $CdS_{1-y}Te_y$ alloy on the S-rich side of the junction is minimized or is measurably eliminated by heat treating the CdS layer in $CdCl_2$:O_2:Ar vapor at 400°C prior to CdTe deposition, which increases grain size, sharpens the CdS optical transmission edge, and forms oxides, which reside on grain surfaces and penetrate grain boundaries. The oxide-producing reaction between $CdCl_2$ vapor and O_2 vapor and CdS is:

$$CdS\ (s) + CdCl_2\ (v) + O_2\ (v) \Leftrightarrow SCl_2\ (g) + 2CdO\ (s), \qquad (36)$$

with free energy of reaction at 400°C of -12.5 kcal/mol. An analogous reaction occurs between CdTe in $CdCl_2$:O_2 ambient. Confirmation of this chemistry was obtained by detection of cadmium oxide phase in heat treated powder mixtures and films, using glancing incidence x-ray diffraction. As the stable equilibrium reaction product for the halide-air ambient, CdO is expected to behave as a barrier to subsequent reaction and diffusion of Te and Cd species from the CdTe layer into the window layer material. As an insulating oxide, CdO may also electrically passivate grain boundaries and surfaces and may not have a deleterious effect on junction behavior in the thin-film if confined to the grain boundaries.

4.2.2 Experimental Approach

4.2.2.1 TCO Structure

The critical properties of the oxide buffer layers are wide bandgap, high transparency and low conductivity. Table 24 compares the crystallographic and optical properties of candidate binary

oxides. All of these can be easily fabricated by reaction of the metal with oxygen in a method described by Chopra [84].

Table 24. Crystallographic and optical properties of selected oxides. The index of refraction, n, is given at 800 nm.

Material	Structure (space group)	Structure Type	ρ (gm/cm^3)	n	E_g (eV)
α-Ga_2O_3	R-3c (167)	Corundum	6.46	1.93	4.4
β-Ga_2O_3	C2/m (12)	Fluorite	5.94	1.93	4.4
SnO_2	$P4_2/mnm$ (136)	Rutile	6.99	1.99	4.0
α-In_2O_3	I213 (199)	pseudo-Fluorite	7.12	2.00	3.6
ZnO	$P6_3mc$ (186)	Wurtzite	5.67	2.03	3.3
CdO	Fm3m (225)	Aluminum	8.24	2.49	2.3

A promising candidate material is Ga_2O_3, having high optical bandgap, with full transmittance at wavelengths greater than 280 nm. The index of refraction is close to that of the two TCO materials commonly employed in cells and will not disrupt the index-matching properties of present cell designs. α-Ga_2O_3, β-Ga_2O_3 and α-In_2O_3 have related crystallographic structures corresponding to the two known types associated with all group III sesquioxides; Al_2O_3 and Ga_2O_3 of the corundum and In_2O_3 and Tl_2O_3 of the fluorite structure [85]. Therefore, α forms of Ga_2O_3 and In_2O_3 are not isostructural. However, Ga_2O_3 undergoes α to β phase transition at 600°C, corresponding to a change from the corundum to fluorite structure and may result in intermixing during treatments or depositions at temperatures above 600°C.

As with other HR layers, Ga_2O_3 films can be prepared by oxidation of the metal precursor. The reaction proceeds according to:

$$2Ga + 1.5O_2 <-> Ga_2O_3 \ (\Delta G_{rxn} = -258 \text{ kcal/mol}). \quad (37)$$

Ga melts at 29.8°C and undergoes a small density increase, from 5.91 g/cm^3 in the solid, to 6.09 g/cm^3 in the liquid. Conversion to α-Ga_2O_3 yields a final film density of 6.46 g/cm^3 and to β-Ga_2O_3 yields a final film density of 5.94 g/cm^3. Unlike the other oxides in Table 24, α-Ga_2O_3 has a higher density than its metal precursor.

4.2.2.2 CdS Characterization and Deposition

CdS films were deposited by vacuum evaporation (< 80 nm) at 220°C and chemical surface deposition (CSD) at 75-80°C. Chemical surface deposition (CSD) consisted of flowing aqueous solution containing cadmium sulfate, thiourea, and ammonia onto preheated superstrates. The net deposition rate was ~10 nm/min and utilization of Cd species was > 80%, in contrast to conventional CBD deposition, with <10% utilization of Cd species. A United States Patent was applied for with respect to this development.

All CdS films were vapor treated in $CdCl_2$:Ar:O_2 at 400°C for 10 minutes to increase grain size and reduce formation of S-rich CdS_yTe_{1-y} alloys in the CdS film. After treatment, all CdS films

were overcoated with 20 nm of CSD CdS to allow unambiguous comparison between "baseline" thickness, $d_f > 100$ nm evaporated CdS, and all-PCBD CdS films, with $d_f < 100$ nm. CdTe films were deposited by vacuum evaporation at 300 to 350°C and growth rate of 3 nm/sec at a base pressure of 2×10^{-6} Torr. Uniform CdTe films having thickness from 0.6 μm to 5.5 μm were obtained by varying deposition time. Different post-deposition treatments were employed to control CdS diffusion into CdTe. Prior to treatment in $CdCl_2$:Ar:O_2 vapor, the CdTe/CdS/TCO/glass structures were annealed, either in air at 450°C, or argon at 580°C. The requisite treatment in $CdCl_2$:Ar:O_2 was carried out at 420°C at p($CdCl_2$) from 5 to 9 mTorr and p(O_2) from 10 to 150 Torr. Contact to CdTe was obtained by vapor treatment of the CdTe surface at ~100°C to remove oxides and to produce Te excess. Cuprous telluride was formed by electron beam evaporation of copper metal followed by heat treatment at 200°C. Acheson carbon ink was used to form the current-carrying conducting back contact pad, and devices were electrically isolated by scribing through the C/Cu_2Te/CdTe.

Film morphology and structure was characterized by tapping atomic force microscopy (AFM) and symmetric x-ray diffraction (XRD). In some cases, surface phases were identified using glancing incidence x-ray diffraction (GIXRD). Optical transmission and reflection were used to determine the transmittance of oxide layers, CdS thickness, and CdTe absorption. Current-voltage and quantum efficiency-wavelength measurements were used to characterize device operation and determine final CdS thickness.

4.2.3 Results

4.2.3.1 High Resistance Buffer Layers

SnO_2, In_2O_3, and Ga_2O_3 films were formed on specular ITO or tin oxide films on Glaverbel soda-lime glass or Corning 7059 glass superstrates. The ITO films exhibited r.m.s. surface roughness less than 0.5 nm, indicating atomic-level film planarity as shown in Figure 68. Selected film structures were analyzed by glancing incidence Ω/θ x-ray diffraction. For Cu-kα radiation incident at Ω = 0.2°, the sampling depth, s, for the In_2O_3 and Ga_2O_3 phases is very different due to different mass absorption coefficients: s(Ga_2O_3) = 80 nm and s(In_2O_3) = 20 nm. Also, the atomic scattering factor for Ga is much lower than for In. Thus, although the Ga_2O_3 film is entirely sampled in both cases, its contribution to the GIXRD pattern is expected to be relatively weak. For tin oxide HR layers on tin oxide TCO, no distinguishing phase characteristics could be detected.

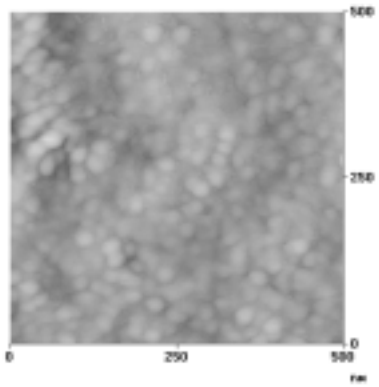


Figure 68. Tapping AFM image of surface of 200 nm thick ITO film on 7059 glass. The r.m.s. roughness is <0.5 nm.

Figure 69 shows diffraction patterns for structures with no gallium oxide, ~40 nm and ~60 nm thick gallium oxide films on 200 nm thick ITO/7059. The calculated pattern for β-Ga_2O_3 (monoclinic, space group C2/m, ρ = 5.943 gm/cm^3) is also shown. Contributions from In_2O_3 (222) and (400) reflections are clearly visible on all three measured patterns. For samples with gallium oxide, the peaks at 30.5° and 35.5° are shifted towards low angle and a new peak appears at 31.6°. The shifted peaks and new peak are consistent with the simulated random powder pattern for β- Ga_2O_3. The ITO film intensities are reduced by primary beam attenuation in the Ga_2O_3 layer.

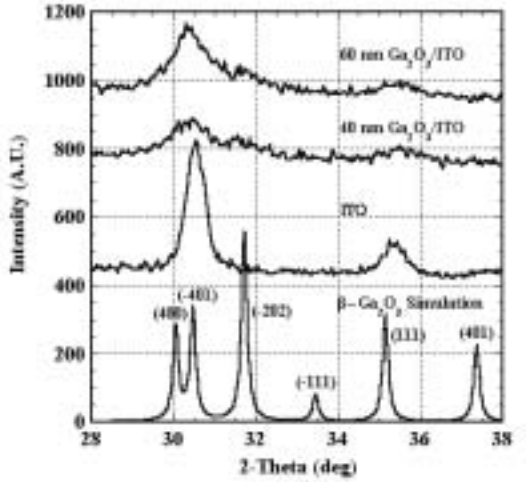


Figure 69. Simulated and measured diffraction patterns. β-Ga_2O_3 simulation for random pattern and instrument FWHM = 0.2°. Measured patterns for films on 7059 glass taken at Ω = 0.2°, step size = 0.05°, and 6 second dwell per step.

Figure 70 shows AFM images for a series of Ga_2O_3 films of increasing thickness on the same ITO/7059 superstrates of Figure 68. The images show well-defined grains with increasing size as thickness increases and low r.m.s. roughness, indicating good planarity in all cases. The optical transmission spectra for the 40 nm thick and 60 nm thick Ga_2O_3 layers, normalized for

reflection, T/(1-R), are nearly indistinguishable from that of the ITO/7059 base structure, and is shown in Figure 71. The Ga_2O_3 films exhibit smaller grain size and more planar structure than In_2O_3 films, and are compared in Figure 72.

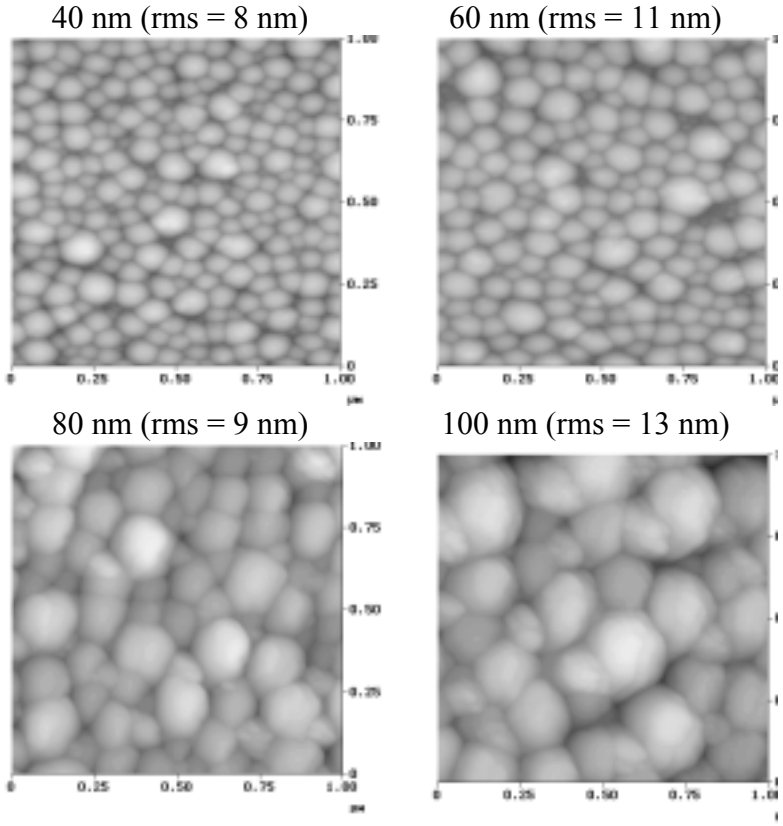


Figure 70. Tapping AFM images of Ga_2O_3 films with thicknesses and r.m.s. roughness indicated.

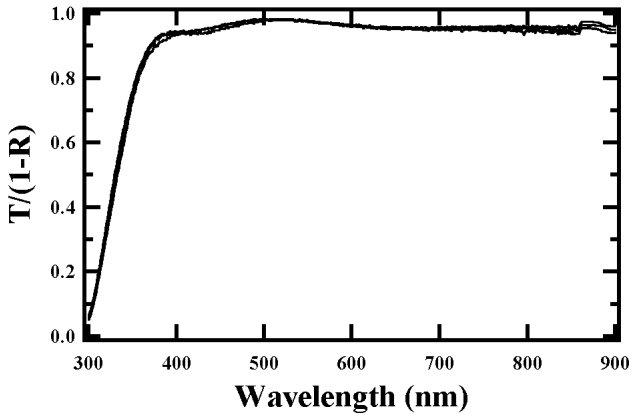


Figure 71. Optical transmission, T/(1-R), of 200 nm ITO/7059 coated with O, 40 nm and 60 nm thick Ga_2O_3 films.

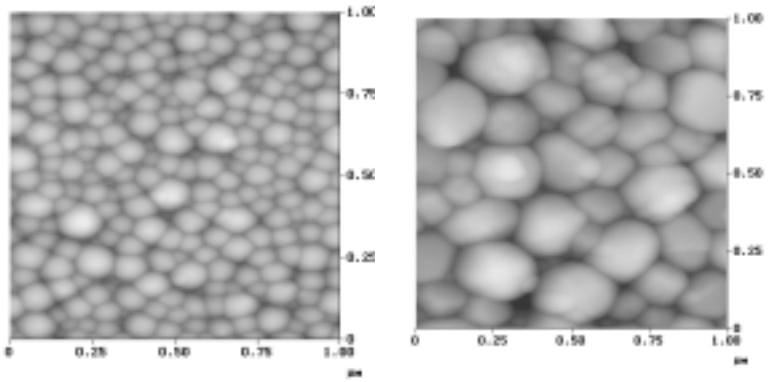


Figure 72. Tapping AFM images of 40 nm thick Ga_2O_3 film (left) and 50 nm thick In_2O_3 film.

Chemically, Ga_2O_3 films are more resistant to $CdCl_2$ species than In_2O_3:

$$Ga_2O_3 + 3CdCl_2 \Leftrightarrow 2GaCl_3 + 3CdO \ (\Delta G_{rxn} = +102.6 \text{ kcal/mol}) \quad (38)$$

$$In_2O_3 + 3CdCl_2 \Leftrightarrow 2InCl_3 + 3CdO \ (\Delta G_{rxn} = +60.5 \text{ kcal/mol}). \quad (39)$$

Thus, no delamination or changes in appearance were detected during processing of the ultra-thin CdS layers with $CdCl_2$ vapor treatments. Devices were fabricated with ~100 nm thick CdS window layers and 4 micron thick CdTe absorber layers deposited at 340°C. A high-temperature anneal at 590°C for 10 minutes followed by a 20 minute

Device results for structures with ultra-thin CdS and different buffer, or HR, layers are shown in Table 25. This includes a device made with 50 nm thick $Cd_{0.95}Zn_{0.05}S$ films deposited by chemical bath deposition, exhibiting demonstrably higher V_{oc} and *FF* than those with 50 nm or more of pure CdS with no buffer layer between the TCO and CdS.

Table 25. AM1.5 J-V results (28°C) for devices with 7059/ITO, 7059/ITO/50nm $Cd_{0.95}Zn_{0.05}S$, 7059/ITO/In_2O_3/CdS, and 7059/SnO_2/SnO_2/CdS window layers and evaporated CdTe. All processed with 580°C, 5 min pre-anneal and 420°C, 15 min $CdCl_2$:Ar:O_2 treatment.

TCO	HRT nm/ type	d_f(CdS) nm	V_{oc} mV	J_{sc} mA/c m^2	FF %	Eff %
ITO	None	0	440	25.0	47	5.0
ITO	None	50	590	23.9	47	6.6
ITO	None	110	790	20.3	70	11.3
ITO	None	30 CdZnS	750	23.2	62	10.8
ITO	20 In_2O_3	30	652	23.9	52	8.1
ITO	50 In_2O_3	< 20	754	26.2	60	11.9
ITO	50 In_2O_3	100	790	21.8	70	12.0
ITO	40 Ga_2O_3	40	760	24.0	62	11.4
SnO_2	None	0	440	18.0	46	3.5
SnO_2	None	90	753	22.8	63	10.8
SnO_2	50 SnO_2	< 20	790	26.0	68	13.8

Table 25 demonstrates that different HR layers can be employed to maintain junction characteristics for evaporated CdTe devices with final d(CdS) < 100 nm and processed with the same $CdCl_2$ vapor treatment. Further gains in efficiency are expected by optimizing both post-deposition and CdS processing for a given HR/TCO combination. Junctions between CdTe and the HR/TCO structure also need to be electrically analyzed.

4.2.3.2 CdS Films

The CSD films exhibit dramatically different growth habit than conventional CBD CdS films, typified by more conformal coverage to the oxide superstrate and a reduced level of surface particulates. Figure 73 shows AFM images of the surface morphology of as-deposited conventional CBD CdS films on ITO/7059 and CSD CdS films on ITO/7059 and In_2O_3/ITO/7059 superstrates.

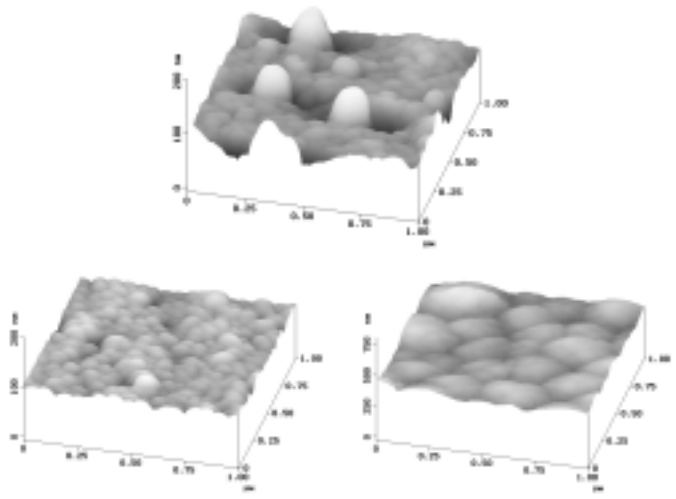


Figure 73. Tapping AFM images of conventional CBD CdS (top) and CSD CdS (lower, left and right) films. The CBD and left CSD films are on specular ITO/7059 glass. The right CSD film is on In_2O_3/ITO/7059.

The grain size of the CSD deposits replicate that of the underlying substrate. For samples with the HR oxide layers, grain size is larger, and the CdS film surfaces are significantly smoother. This may be due to better wetting of the liquid layer on the HR materials, although this has not yet been proven. Figure 74 and Figure 75 present a series of three thicknesses of CSD CdS films deposited on bare ITO and on In_2O_3-coated ITO, respectively. The figures show that ultra-thin CSD CdS films exhibit very little variation in grain size for thickness from ~5 nm to 50 nm, with conformal coverage when deposited on the In_2O_3 HR layer.

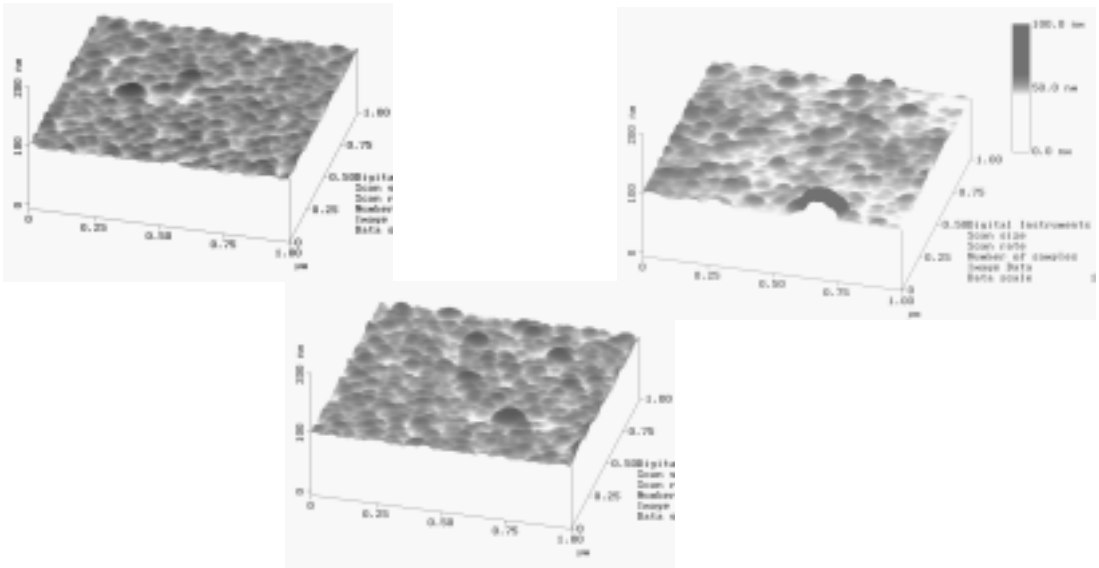


Figure 74. Tapping AFM images of as-deposited CSD CdS on specular ITO/7059. CdS film thickness from left to right are 6 nm, 22 nm and 45 nm.

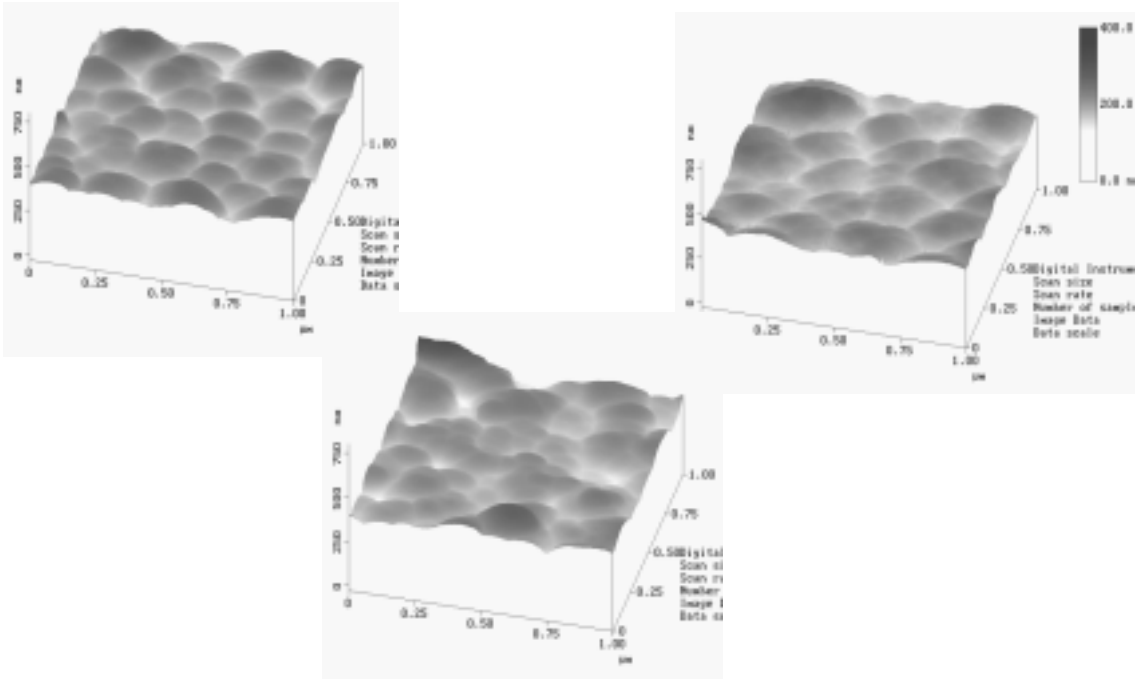


Figure 75. Tapping AFM images of as-deposited CSD CdS on In_2O_3-coated specular ITO/7059. CdS film thickness from left to right are 3 nm, 20 nm and 50 nm.

Cross-film conductivity measurements were made of 40 nm thick CSD CdS and $Cd_{0.95}Zn_{0.05}S$ films deposited onto ITO/7059 glass structures with a 175 μm wide gap. Table 26 shows dark and light, ~80 mW/cm^2 ELH, conductivity results for films before and after treatment in $CdCl_2$:O_2 vapor at 400°C for 10 minutes. The dark measurement was made prior to the light since the films were found to exhibit higher (2X) dark conductivity after exposure to the light. The original dark conductivity was obtained after relaxation on the order of 30 minutes. All the films exhibit photoconductivity. For CdS films, the dark and light conductivity increased after the treatment, but the photoconductivity decreased. For the $Cd_{0.95}Zn_{0.05}S$ films, treatment increased dark and light conductivity proportionally.

Table 26. Dark and light (~80 mW/cm^2 ELH) conductivity of 40 nm thick CdS and $Cd_{0.95}Zn_{0.05}S$ films deposited by CSD before and after treatment in $CdCl_2$:O_2 vapor at 400°C for 10 minutes.

Sample	Treatment	σ_d (S/cm)	σ_l (S/cm)	σ_l/σ_d
CdS	as-deposited	1×10^{-5}	9×10^{-4}	90
CdS	$CdCl_2$ HT	3×10^{-4}	7×10^{-3}	23
$Cd_{0.95}Zn_{0.05}S$	as-deposited	4×10^{-4}	3×10^{-2}	75
$Cd_{0.95}Zn_{0.05}S$	$CdCl_2$ HT	7×10^{-4}	5×10^{-2}	71

4.2.3.3 Device Analysis

Below, Table 27 summarizes the TCO layer structure and CdS thickness, measured J-V parameters, and extracted diode parameters for selected cells with different TCO configurations and CdS thickness. The J-V curves were analyzed by graphing dV/dJ vs ($1/J+J_{sc}$) to obtain R_s and A, and log ($J+J_{sc}$) *vs* ($V-JR_s$) to obtain diode parameters A and J_o. In general, good fits were obtained with the dark J-V, while poorer fits were obtained with the light J-V. The A-factors in the dark were near 2, except in the case of very low V_{oc}. The A-factor from the dark J-V curve was about half the value from the light, and J_o from the dark J-V is typically 3-5 orders of magnitude lower than from the light. This is commonly seen in cells with large voltage dependent collection (like a-Si). In this case, the apparent slope of log ($J+J_{sc}$) is not only due to the forward diode current but has other voltage dependent influences. Thus "J_o" and "A" obtained from the *light* should not be interpreted as diode parameters and are not included here. Values of R_s were always smaller in the light, typically less than 3 Ω-cm^2. The only devices with evidence of blocking contacts were the two from group E, having very thin (either 0 or 30 nm) final CdS, resulting in slight curvature in the light J-V, high R_s and large light-to-dark-crossover.

In Table 26, series A and B use ITO while series C, D, and E use SnO_2 as the TCO layer. Previously, with standard sputtered ITO of 200 nm thickness, the V_{oc} and FF would have been ~300 mV and 40%, respectively, for devices with initial CdS thickness of 100 nm. Series A shows the effect of CdS thickness on in-house ~0.5 μm ITO, which is 2X the previously used thickness. Note the decrease in V_{oc} as CdS is reduced from 140 to 80 nm but the improved performance compared to previous results. Piece 41082.12 represents a control since it has relatively thick ITO and thick bi-layer CdS. Series B compares the effect of H_2-heat treatment and CdS thickness using in-house standard ITO. Comparing results from series A to series B shows that V_{oc} is strongly degraded by decreasing CdS thickness with thin ITO (200 nm) or by decreasing ITO thickness with thin CdS (60-80 nm). The FF is less affected than V_{oc}. Crystallizing the thin ITO with a H_2 heat treatment restores V_{oc} despite the thin CdS layer.

Series C shows the significant gain in V_{oc} and FF with the addition of a thin high resistance in-house SnO_2 layer obtained by oxidizing a tin film. In both C and D, the devices with the high resistance SnO_2 bi-layer actually have much lower R_s but higher A and J_o. For example, 41082.13 having *undoped* ITN SnO_2 has poor FF not because of high R_s but very high A (~6) and J_o (2E-1 mA/cm^2). Pieces 41082.23 and .21 having Cd or Zn doped ITN SnO_2 have much lower A (~2) and J_o (~1E-5 mA/cm^2) but higher R_s. Thus, even though these pieces had 110 nm of starting CdS, the TCO resistivity affected the junction properties not the resistance. Series D compares ITN deposited SnO_2 layers (undoped and Zn and Cd doped) on LOF SnO_2. The Cd and Zn doped SnO_2 bi-layers had equivalent device performance and diode parameters. Series E compares very thin CdS on the Zn-doped SnO_2 from ITN. These both represent improvements in V_{oc} over what has been obtained with such thin CdS on ITO indicating improved junction behavior with the new SnO_2 materials. However, the two cells in series E have low FF due to high R_s.

To separate effects of CdS processing from post-deposition processing, future work will repeat some of these device structures using as-deposited CdS with and without high-temperature annealing. In addition, devices will be fabricated and characterized using CdTe and $CdTe_{(1-x)}S_x$

absorber layers, deposited by PVD at substrate temperatures > 350°C onto TCO bi-layers with and without ultra-thin CdS coatings to characterize and compare $CdTe_{(1-x)}S_x$/TCO junctions made by 1) diffusing CdS into CdTe and 2) co-deposition of CdS and CdTe.

Table 27. Results from analysis of IEC CdTe pieces having different TCO materials and CdS thickness. Series resistance R_s, diode factor A, and recombination current J_o from analysis of dark J-V data. All CdS layers treated with $CdCl_2$ heat treatment prior to CdTe deposition.

Series	Piece #	Window Contact	Final CdS thick (nm)	R_s (Ohm/ sqcm)	A factor	J_o (mA/ sqcm)	V_{oc} (mV)	J_{sc} (mA/ sqcm)	FF (%)
A	41083.12	550 nm ITO	60	5.0	1.2	2.6e^-7	630	22.0	63
	41082.12	540 nm ITO	120 bilayer	2.5	2.2	1.2e^-5	790	21.4	64
B	41042.23	200 nm ITO	80	5.3	1.7	4.8e^-5	590	17.8	61
	41082.22	200 nm ITO with H_2 HT	90	3.8	2.1	2.4e^-5	750	23.3	63
	41078.21	200 nm ITO	40	2.36	1.6	1.1e^-3	400	24.0	55
C	41072.12a	Slx SnO2	45	18	2.4	3.4e^-4	500	19.9	37
	41082.32	Slx SnO2 +Sn layer	55	0.5	3.0	8.4e^-5	780	27.1	65
D	41082.13	Undoped SnO2**	90	0.6	6.2	0.18	700	18.7	52
	41082.21	Cd doped SnO2**	90	2.5	1.9	1.3e^-5	730	22.1	65
	41082.23	Zn doped SnO2**	90	4.7	2.0	8.0e^-6	720	22.5	64
E	41077.23	Zn doped SnO2**	0	28.3	hyst.	hyst.	520	23.8	50***
	41077.32	Zn doped SnO2**	<10	17.8	1.9	7.2e^-6	700	22.3	49***

**SnO_2 bilayers deposited at ITN on LOF SnO_2.
***Slight curvature in J-V beyond V_{oc}, large light-to-dark crossover.

4.2.4 Summary and Conclusions

Options for window layer processing have been evaluated. Resistive oxide films formed by oxidizing metal films allow junction quality to be maintained for devices with d(CdS) < 100 nm. Conformal CdS films deposited by CSD have high Cd utilization and have low pinhole and

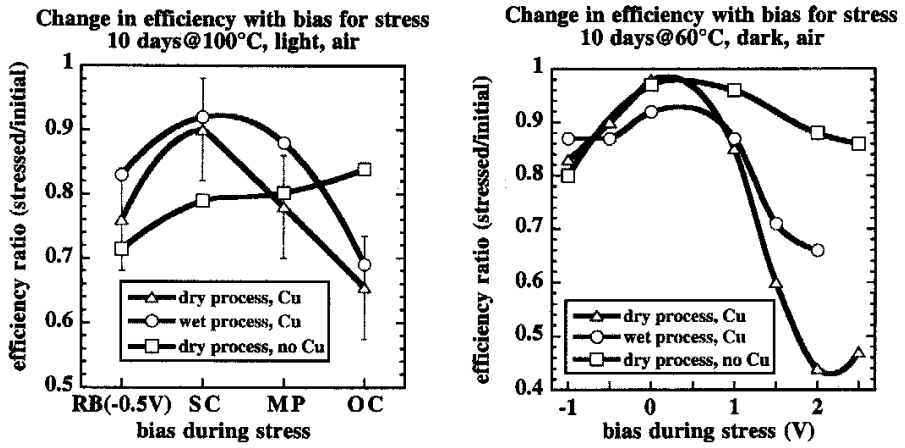
particulate occurrence, contributing to process robustness. It is demonstrated that CSD $Cd_{1-x}Zn_xS$ films may be used in lieu of a CdS/HR combination to simplify processing and retain junction quality while obtaining high photocurrent.

4.3 Contacts and Accelerated Stressing

4.3.1 Introduction

At the beginning of this contract, it was already well established that the contacting of CdTe is problematic and the details of the contact were crucial to obtaining a high performance device. There were suggestions that the contact process and structure can influence the stability under accelerated stress conditions and that the electrical bias during stress was important to understanding the degradation [86]. Therefore, we established a contact fabrication process which allowed us to separate and control various aspects of the contact process, such as removing oxides on the CdTe surface, formation of the Te layer, applying Cu and reacting it to form Cu-Te alloys, and forming a robust current carrying contact. We separate these features into the primary and secondary contacts. The primary contact may contain Cu-Te alloys and makes intimate contact to the CdTe. The secondary contact is typically a thick layer of C, Mo, Ni or Al and carries the current to the external connections. We also built a system for accelerated stressing of thin film PV devices under controlled atmosphere, temperature, bias, and light conditions, and used it to stress a large number of CdTe devices with a variety of contact structures. The glass/SnO_2/CdS/CdTe plates for these contacting and stress studies were obtained from First Solar, LLC. The CdS and CdTe were evaporated. The 4 μm thick CdTe received a $CdCl_2$ treatment at First Solar. Thus, devices were fabricated using CdS/CdTe material from First Solar with back contact processing at IEC. Given the well known sensitivity of CdTe device performance and degradation to the back contact, these results on hybrid FS/IEC devices do not quantitatively reflect the behavior of First Solar devices with their own contact process.

Figure 76(a) and (b) shows the salient behavior of devices we have stressed. This figure is a summary of our results as well as a motivation for studies described in this section. Devices in Figure 76(a) were stressed for 10 days at 100°C under ~1 sun light in dry air at various bias points: short circuit (SC), maximum power (MP), and open circuit (OC). Devices in Figure 76(b) were stressed for 10 days at 60°C in the dark in dry air at various applied bias from –1 to +2.5 V. Cells with Cu having wet or dry surface preparation are compared to cells without Cu having the dry process. The vertical axis is the efficiency after stress normalized by the initial value. The initial efficiencies were 10-12% for devices with Cu in the contact and 7-8% for those without Cu. These figures show the effect of electrical bias and illumination during stress, and the presence of Cu and back contact processing.



(a) **(b)**

Figure 76. Change in efficiency (normalized to initial value) with stress at 10 days, at (a) 100°C in light in dry air and (b) 60°C in dark in dry air, for devices with different contact. The x-axis is the bias during stress (reverse bias, short circuit, maximum power or open circuit).

Clearly, devices degrade in both illumination and dark conditions during stress, and even at temperatures as low as 60°C. In both cases, devices biased at SC or 0V were more stable than those at forward or reverse bias. This highlights a crucial observation which must be accounted for in developing a model, namely that the degradation is non-monotonic with bias. Degradation increases with increasing forward bias, at least up to 2.5V. Devices without Cu degrade much less, especially at forward bias. The bias dependence and effect of Cu are similar to results reported by others [87]. There is little difference between devices where the pre-contact treatment of the CdTe was a wet or dry process, providing that the Cu thickness was optimized for each process as discussed in Section 4.3.5. The error bars indicated on Figure 76(a) are indicative of the wide range of behavior we observed for nominally similar devices and stress conditions. Devices stressed at 0V for 10 days at 100°C can degrade as little as 2-3% or as much as 20%. Given the excellent control over the stress conditions, we attribute the variability to unintentional differences in the CdS/CdTe starting material or the lack of reoptimization of the contact for different starting material properties. In the following sections, we focus on the effect of bias during stress and the effect of the contact process on initial and post-stress performance.

4.3.2 Contacting (Wet, Dry, Primary, Secondary, Cu-Te Formation)

The contact process consisted of four steps following $CdCl_2$ treatment in air: 1) chemical removal of deleterious surface residues such as oxides and chlorates; 2) formation of Te excess; 3) deposition of Cu and reaction with Te to form the primary contact; and 4) deposition of the secondary contact to serve as the current carrying conductor. Two approaches, based on wet and dry chemical reactions, were employed for the surface preparation and Te excess formation. The

"wet" process used a three-step sequential reaction of the CdTe film in **b**romine-methanol, aqueous **d**ichromate, and **h**ydrazine (BDH). Bromine methanol removes surface residues and a thin layer of CdTe, leaving a terminating layer of Te ~2 nm thick. The dichromate solution produces a considerable oxide, which is then converted to a 30 nm thick Te layer by reaction in hydrazine. The dichromate and hydrazine steps are extremely penetrating. Thus the time in these liquids depends on the CdTe thickness and grain size and is a critical process parameter. The solutions and conditions used for 4 to 5 μm thick CdTe are as follows:

bromine-methanol:	0.15 g Br_2 in 100 cc CH_3OH; 25°C; 5-10 s
dichromate:	Fisher-brand Dichrol used at full strength; 25°C; 1 s
hydrazine:	98% N_2H_4 in H_2O; 40°C, 60 s.

The "dry" process achieves a similar result by reaction of the CdTe surface in H_2 and Te vapor at total pressure of 1 atmosphere. The gas phase composition is controlled by flowing 4% H_2 in Ar through a reactor in which the CdTe film is suspended directly over a Te source heated to 380°C, which establishes a Te partial pressure of ~2 mTorr. The reaction is carried out for 1 to 2 minutes, during which the CdTe temperature reaches 180°C to 200°C. A Te layer ~10 nm thick is formed on the CdTe surface. This process is not considered to be penetrating and thus the same process has been used on CdTe films with thickness from 1.3 to 7 μm.

The primary contact is completed by deposition of Cu layers from 2 to 15 nm thick by electron beam evaporation and *in-situ* treatment at 200°C for 30 min. Measurements with fixed incident beam x-ray diffraction of CdTe films at different stages of processing showed:

1) predominant surface residue after $CdCl_2$:O_2 treatment is CdO;
2) wet and dry processes leave elemental Te;
3) Cu-Te phases depend on Cu to Te ratio, in general accordance with the published phase diagram.

Secondary contact was made by application of Acheson 505SS carbon ink followed by a drying step at ~40°C for 30 min. An alternative approach to expedite processing was deposition of Cu, application of the secondary contact, then treatment at 200°C for 30 min. Alternative contacts such as Mo or Ni were deposited by electron beam evaporation immediately after depositing the Cu layer.

4.3.3 System for Accelerated Stress Studies

During this contract period a new stress testing system (Figure 77) was assembled and became operational. The system has 4 vacuum-compatible chambers for exposing devices to various controlled atmospheres, temperature, illumination intensity and electrical bias while monitoring the electrical performance. The chambers are pumpable down to 20 mT prior to stress. Then they are backfilled with the appropriate atmosphere. This is repeated several times to reduce moisture and O_2 content before raising the temperature and beginning the stress study. Stressing can occur in an atmosphere of dry air, Ar, 2% H_2 in Ar, or vacuum. The chambers are 5 inches high and 6 inches in diameter and have two 6-inch diameter glass windows. Temperatures of 60-120°C are achieved with two 100W halogen floodlamps mounted outside the chamber, one below providing solar cell illumination and one above providing additional heat if needed.

Typically, we have adjusted the position of the bottom lamp to provide a J_{sc} of 1.2 suns for CdTe devices, which heats the devices to about 70-80°C. Accurate temperature control is obtained without affecting the solar cell illumination intensity by adjusting of the power to the top lamp. Devices can be electrically biased from reverse bias through the active power quadrant into forward bias. Bias in the power quadrant is provided using a bipolar source-sink power supply along with a variable series resistance (0-100 Ohms). Analysis of a large number of stressed and unstressed devices found that the ratio of V_{mp} to V_{oc} ranges from 0.70 to 0.78. Therefore, we have selected to define "stressing at maximum power" as having an applied bias of 0.75 times V_{oc}. This is adjusted during stress as V_{oc} degrades.

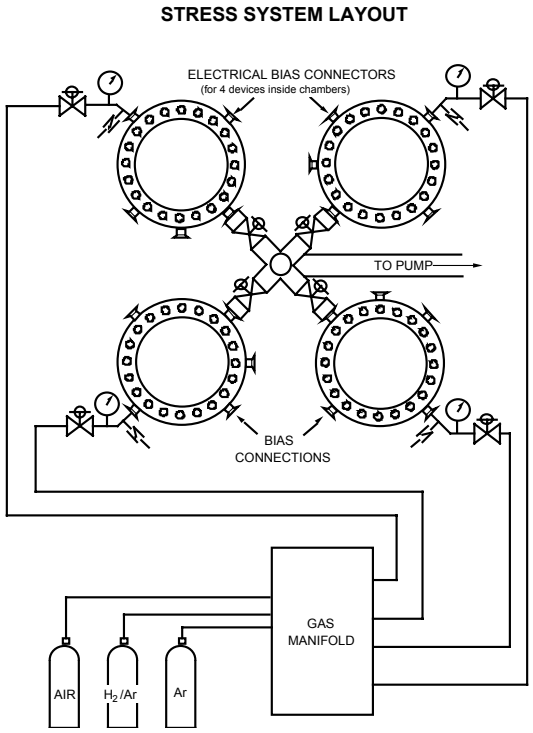


Figure 77. Diagram of IEC's stress system.

Each chamber can have up to four 1" x 1" pieces and four cells under bias. Unbiased cells are at V_{oc} by default. Thus, 16 cells can be biased and stressed at a time, with 4 each under 4 different conditions, if desired. A computer controlled switching matrix has been interfaced to standard solar cell test hardware to allow *in-situ* J(V) sweeps during stress without removing the cells from the stress chamber.

All results of stressing discussed in Sections 4.3.5 through 4.3.8 were obtained using the new stress system.

4.3.4 Stress of Partially Completed Devices and Recontacted Devices

Recognizing that fully completed CdS/CdTe/contact device structures degrade under accelerated stress, it was decided to investigate at what point in the device fabrication that degradation become operable. Was it inherent in the CdS/CdTe semiconductor layers? Did it occur only

after the Cu layer was deposited? Could it be eliminated with a second application of a new Cu layer after initial stressing with the first layer? We sought to answer these questions by stressing partially completed devices, then completing their fabrication and testing them. Contacts were removed or otherwise re-applied after stress in some cases.

We stressed CdS/CdTe structures without any contact under the same conditions as used to stress devices. After stressing at open circuit at 100°C, standard wet or dry contact processing, followed by Cu and C layers, was used to complete the devices. When tested, they had J(V) characteristics comparable to unstressed (as-deposited) devices including V_{oc} ~ 0.80V. CdS/CdTe structures were also stressed with a 6 nm Cu layer but no C contact at 100°C. After stress, some of these devices received a second Cu layer while all received the C contact. The completed devices had V_{oc} ~ 0.65V, including those with the double Cu layer. Subsequent restressing of these completed devices resulted in no further loss in V_{oc} but a loss in FF and the appearance of a current limiting blocking contact. This indicates that the current-carrying secondary conductor is responsible for the contact degradation. Together, these three experiments suggest that (1) the CdS/CdTe junction is intrinsically stable, (2) the presence of Cu during stress is correlated with junction (V_{oc}) degradation, (3) reapplying a fresh Cu layer does not immunize the device from further degradation nor does it restore a degraded device, and (4) the presence of the C conductor secondary contact is responsible for contact degradation.

We developed a method to remove the C contact after stress and reapply fresh C in order to separate contact and junction behavior. A CdS/CdTe solar cell with the wet process and 15 nm Cu, having an initial efficiency of 11.8% and V_{oc} of 0.82V, was stressed at open circuit at 100°C for 6 weeks (not the 6 days as devices in sections above) in air at 2 suns by Prof. Sites' group at Colorado State University. This reduced the efficiency to 7.2% and V_{oc} to 0.73V. J(V) results and diode parameters are given in Table 28 for the initial, stressed and recontacted states. Figure 78 shows light and dark J(V) curves in all three states, while Figure 79 shows log J(V) for the 3 dark curves. After stress, Table shows that J_o increased by 30X with no change in A-factor (~1.6), suggesting that the magnitude of recombination changes but not the mechanism (bulk recombination). Figure 78 also shows that curvature develops after stress in both light and dark JV curves at forward bias, most likely due to a blocking contact. After stressing, the original carbon contact was removed, the CdTe surface was re-etched in weak bromine-methanol, and a new C contact was applied with no additional Cu layer. The efficiency increased to 9.1%, the blocking contact disappeared and the FF increased significantly with no change in V_{oc}, J_o and A. This clearly demonstrates that the curvature in forward bias is associated with the back contact.

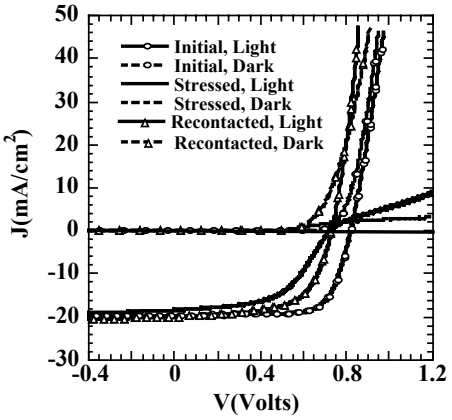


Figure 78. Light and dark JV curves for CdS/CdTe device: initial, 6-weeks stress at 100°C and OC; and following recontacting.

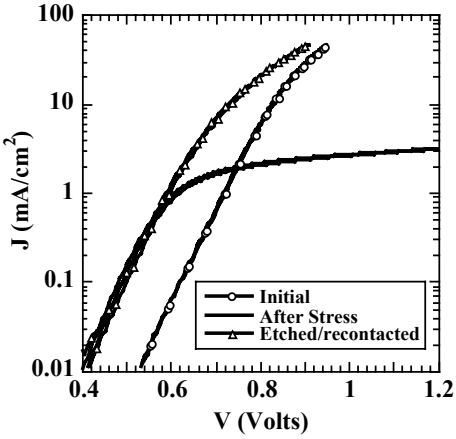


Figure 79. Log JV of dark curves from Figure 78.

Taken together, experiments described in this sub-section allow association of different parts of the contact process with the different mechanisms responsible for junction and contact degradation, i.e., Cu during stress causes V_{oc} loss, and C contact during stress degrades the CdTe contact electrical behavior.

Table 28. Cell performance measured in initial, stressed and recontacted states. R_{oc}, J_o and A determined from analysis of dark JV curves.

Condition	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Eff. (%)	R_{OC} (Ω-cm^2)	J_O (mA/cm^2)	A
Initial	0.82	19.6	73	11.8	4.4	3E-8	1.6
Stressed	0.73	18.4	54	7.2	20.2	8E-7	1.6
Recontacted	0.73	19.9	62	9.1	4.7	8E-7	1.6

4.3.5 Effect of Wet *vs* Dry Process, and Cu Thickness (OC stress, 100°C)

This subsection describes an extensive study of the effect of contact process and Cu thickness. Detailed analysis of JV curves was performed including temperature dependence to identify how Cu and stress influence the recombination and diode properties.

4.3.5.1 Sample Description and Measurements

All devices discussed in this subsection were processed from the same plate (20632) cut from a production module although devices on other plates yielded similar results. CdS/CdTe solar cells were fabricated using the wet process (BDH etch leaving ~30 nm Te layer) or the dry process (leaving ~10 nm evaporated Te layer) to prepare the CdTe surface prior to evaporation of Cu layers from 2 to 15 nm thick. Following the Cu evaporation, C ink was applied and the completed device was heated for 30 minutes at 200°C in air to dry the ink and to fully form the Cu_2Te layer. A more complete description of the contact chemistry is given in the preceding sections. After characterization of current voltage (JV) performance in the initial state, some devices were exposed to accelerated stress conditions. We used conditions of 100°C in air for 6 days at ~1 sun illumination. Devices were at open circuit (V_{oc}) during stress. This can be the most stringent stress condition depending on the details of the contact formation. It should be mentioned that results presented here are not necessarily indicative of those that would be obtained at First Solar with their proprietary contact processing, since published data suggests that the contact has a stronger impact on stability than the CdS/CdTe material. However, these results give important insight into the effect of specific process variables on initial and post-stress performance that can be generalized to devices made with similar contact processing on other CdTe/CdS layers. J(V) characteristics were measured at 28°C in light and dark using an Oriel Xe arc lamp solar simulator calibrated to 100 mW/cm^2 (AM1.5), and as a function of temperature from –50 to 80°C at several intensities with GE-ELH type lamps. The data was analyzed as described below.

Starting with the basic diode relation including series resistance,

$$J = J_D - J_L = J_O \exp\left[(qV/AkT)-1\right] - JL \quad (40)$$

$$J_O = J_{OO} \exp\left(q(\phi/AkT)\right), \quad (41)$$

where J_D is the diode current, J_L is the light generated current ($J_L \sim J_{SC}$ where J_{SC} is the short circuit current), J_{OO} is the saturation recombination current density, A is the diode factor, R_S is

the lumped series resistance, and ϕ is the barrier height or activation energy for the recombination mechanism. For Schockley-Read-Hall (SRH) type of recombination [88], $\phi = E_g$, which is the bandgap of the region where the recombination is occurring, and A ~ 2. More generally, it is found that $\phi/A = Eg$ for a range of values of A and device structures. The external voltage V is related to the actual voltage across the internal junction V_J by correcting for the series resistance losses as

$$V = V_J + (J*R_S). \quad (42)$$

From Equations 40 and 41, the open circuit voltage V_{oc} is when J = 0 or

$$V_{OC} = AkT/q \left[\ln (J_L/J_D \right] = \phi/q - AkT/q \ln (J_{OO} / J_L). \quad (43)$$

From Equations 40 and 42, the derivative dV/dJ is

$$dV/dJ = R_S + AkT/q (J + J_L) - 1. \quad (44)$$

Data was analyzed by plotting V_{OC} *vs* T, whose intercept gives ϕ/A; by plotting log (J_{SC}) *vs* V_{oc} or log (J) *vs* V_J whose intercept gives J_O and slope gives A (in the light or dark, respectively); and by plotting dV/dJ *vs* $1/(J + J_L)$ whose intercept give R_s and slope gives A.

4.3.5.2 General Results of Cu Thickness

Figure 80 and Figure 81 summarize the dependence of V_{oc} and FF on Cu layer thickness before and after stressing for the wet and dry contact processes. V_{oc} and FF are sensitive to the junction properties and series resistance of the device, which in turn are most strongly affected by contact process and stressing (3). Initial performance is very similar for the two processes independent of Cu thickness for Cu > 2 nm. Initial V_{oc} was 0.80 ± 0.02 V and initial FF was 69 ± 2% for all devices except the one without Cu. Note that the device without Cu having the wet contact has the highest V_{oc} after stressing, despite having the lowest V_{oc} before stressing. It degraded only 0.04 V compared to ~0.15 V for all the other devices. Figure 80 shows that the piece with the dry contact (thinner Te) and thickest Cu layer (15 nm) had the highest V_{oc} after stressing of any device with Cu. Conversely, the highest FF after stressing was on the piece with wet contact (thicker Te) and thinnest Cu layer (2 nm). This suggests that there is an optimum Cu thickness depending on the surface properties of the CdTe following a given contact process. There is also considerable scatter in the results, especially after stress, from nominally identically processed devices, as shown for example with 15 nm Cu. We believe this is due to the complexity of processing steps and their interaction, and to the multiple degradation mechanisms. Further, we speculate that much of the initial and post-stress results are due to grain boundary activity which would introduce a statistical variation. But these results also demonstrate that to first order, significant degradation occurs independent of the amount of Cu for both of the contact processes. Insight into the device behavior which leads to these trends is presented in the following sections based on detailed device analysis.

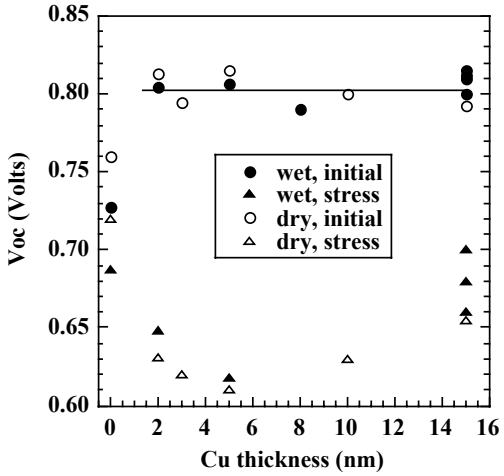


Figure 80. V_{oc} *vs* Cu thickness for devices with wet and dry contact before and after stress at 100°C in air at OC.

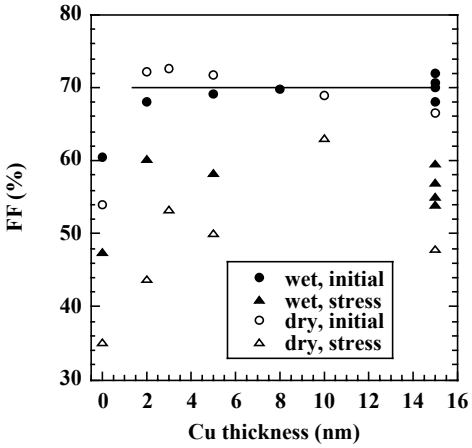


Figure 81. FF *vs* Cu thickness for devices with wet and dry contact before and after stress at 100°C in air at OC.

4.3.5.3 Initial JV Performance and Analysis

Figure 82 shows the dark J(V) curves of devices having the wet contact process with Cu thicknesses from 0 to 15 nm before any stressing occurred. The dark curves show a clear trend of increasing forward current conduction with increasing Cu. Only the device with Cu = 15 nm has a "normal" highly conducting dark current characteristic at forward bias. In contrast, the light J(V) curves in Figure 83 show typical diode behavior for all devices with Cu. Comparing Figure 82 and Figure 83 indicates a large light-to-dark crossover (LDXO), where the forward bias diode current in the light is much higher than in the dark, for devices with Cu = 0, 2 and 5 nm. The LDXO has been widely reported in polycrystalline Cu_2S/CdS solar cells and shown to be due to Cu-enhanced photoconductivity of the CdS layers [89,90]. Figure 82 and Figure 83 show the opposite effect, namely the device with the most Cu has essentially no LDXO. Several

recent papers analyze LDXO in CdTe solar cells in terms of light-generated minority carrier current flow at the CdTe contact [91,92] which is a very different mechanism from photoconductive CdS.

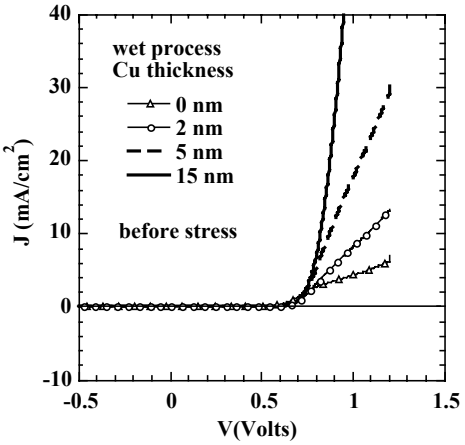


Figure 82. Dark JV curves for device with wet contact process before stress.

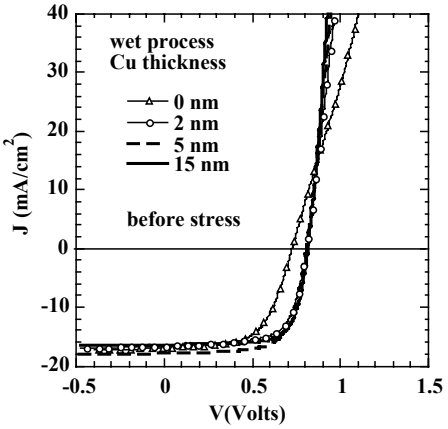


Figure 83. Light JV curves for device with wet contact process before stress.

Figure 84 shows the light and dark JV curves for a device having the dry contact with only 2 nm Cu. Also shown is the device from Figure 82 and Figure 83 with 15 nm Cu and the wet contact. Both are well formed J(V) curves and essentially identical. Thus, the dry contact process requires much less Cu to achieve an Ohmic contact and high current conduction in the dark compared to the wet contact.

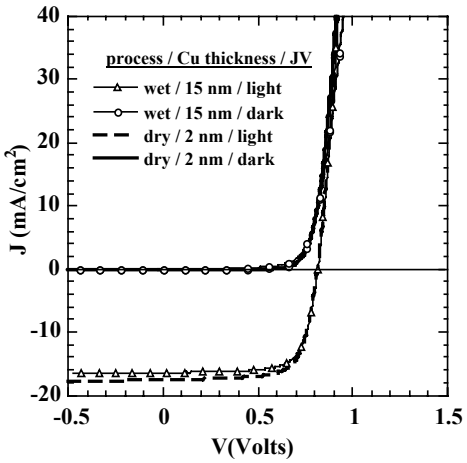


Figure 84. Light and dark JV curves for devices with wet (15 nm Cu) and dry (2 nm Cu) contact process.

Figure 85 plots dV/dJ *vs* 1/J for the two dark curves in Figure 84 using Equation 44 with $J_L = 0$. The data shown spans from J = 2 to 50 mA/cm^2. The A-factors and series resistances are very similar between the two devices and confirms that with the appropriate level of Cu at the back contact, equivalent device behavior results with either contact process. Figure 86 plots log J *vs* (V-JRs) for the same two dark curves. The terminal voltage V is corrected for series resistance losses giving the actual voltage across the junction. This linearizes the data at higher J where series resistance losses reduce the current at a given voltage. Again, both curves have the same diode saturation currents J_o = 8E-8 mA/cm^2. This value is 2-6 times larger than that reported for very high efficiency ~ 14% CdTe devices [93] but similar to values reported for similar efficiency (~10%) devices [93,94]. Note the increased current at low bias for the device with 150Å. This may be due to slight shunting of the CdS/CdTe junction due to excessive Cu diffusion down grain boundaries. The primary conclusion of Figure 84 through Figure 86 is that the junction properties of devices with wet or dry contact with Cu are equivalent and similar to those reported in the literature for CdS/CdTe devices of comparable efficiency.

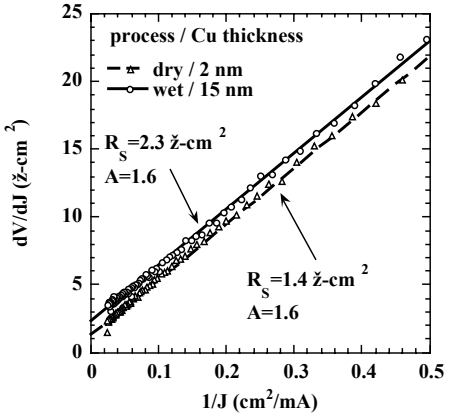


Figure 85. dV/dJ *vs* 1/J for dark JV curves of devices in Figure 84.

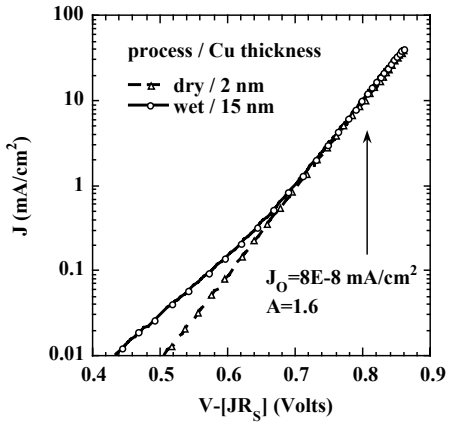


Figure 86. Log (J) *vs* junction voltage V-JRs for dark JV curves of devices in Figure 84.

However, given the large amount of LDXO in some of these devices, it is more appropriate to analyze the light J(V) characteristic to determine the junction properties relevant to photovoltaic performance, especially what determines V_{oc}. We do this using the intensity dependence of V_{oc} by plotting log (J_{sc}) *vs* V_{oc}. From Equation 43, the slope gives the A-factor, and the intercept is J_o under illumination. This method avoids problems due to blocking contacts and characterizes the junction under illumination and bias conditions near V_{oc}. Figure 87 shows log J_{sc} *vs* V_{oc} at 28°C for 4 devices before stress. The A and J_o values are in Table 29. Note that they are similar to those from the dark log J(V) analysis. But it was not possible to fit the device without Cu using dark log J(V) because of the curvature, while log $J_{sc}(V_{oc})$ gives a linear relation allowing determination of A and J_o.

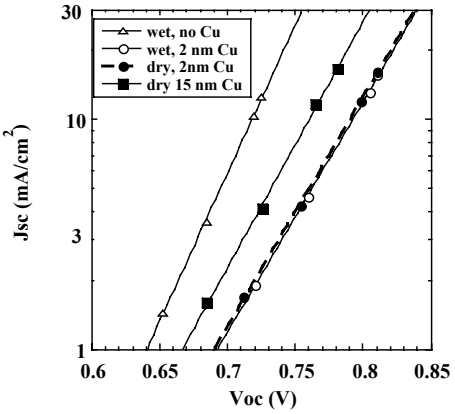


Figure 87. Log (J_{sc}) *vs* V_{oc} at 25°C for devices with different back contact processing.

Table 29. Values before and after stress for V_{oc} (298 K), V_{oc} (0 K), A (298 K) and J_o (298 K) for devices with wet or dry contact, 2 nm Cu each, or wet contact with no Cu. A and J_o obtained in the light from log (J_{sc}) *vs* V_{oc}.

Contact process	Initial or stress	Cu (nm)	V_{oc} (298K) Volts	V_{oc} (0K) Volts	A-factor (298 K)	J_o (298 K)
Wet	Initial	0	0.72	1.23	1.28	$5x10^{-9}$
	Stress		0.68	1.15	1.18	$2x10^{-9}$
Wet	Initial	2	0.79	1.45	1.66	$1x10^{-7}$
	Stress		0.67	1.36	1.86	$2x10^{-5}$
Dry	Initial	2	0.80	1.52	1.66	$1x10^{-7}$
	Stress		0.67	1.44	1.78	$1x10^{-5}$
Dry	Initial	15	0.76	1.47	1.56	$7x10^{-8}$
	Stress		0.72	1.42	2.00	$4x10^{-5}$

4.3.5.4 Post-stress JV Performance and Analysis

The devices were exposed to 1 sun illumination at open circuit for 6 days at 100°C to accelerate any degradation mechanisms. Note that some CdTe devices and modules have been reported to be very stable [95,96] or even to increase in performance with accelerated stressing or extended outdoor exposure, but this behavior cannot be routinely duplicated.

Figure 88 and Figure 89 show light and dark JV curves after stress for devices with 2 and 15 nm Cu, respectively. Results from both wet and dry contact process are shown for each. For comparison, the initial (pre-stress) light JV curve for the device with the dry contact is shown. To first order, all 4 devices behave similarly after stress. V_{oc} decreases by 150-200 mV and J_{sc} decreases slightly due to increased voltage dependence. The FF decreases for a variety of reasons, as will be described in more detail, including weak curvature beyond for $V > V_{oc}$ and an increase in the series resistance. These are similar to results reported by others on other CdTe devices with other contacts.

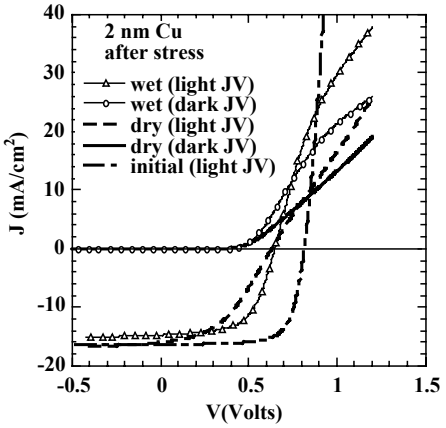


Figure 88. Light and dark JV after stress for devices with 2 nm Cu. Typical initial light curve shown for comparison.

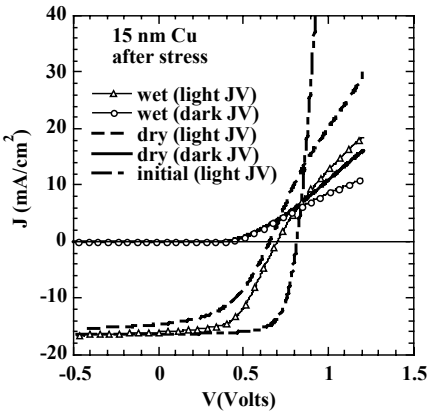


Figure 89. Light and dark JV after stress for devices with 15 nm Cu. Typical initial light curve shown for comparison.

We analyzed the J(V) data as in the previous section to determine more precisely the changes in the device. Figure 90 shows dV/dJ *vs* 1/J for the four dark curves after stress from Figure 88 and Figure 89. The data from one of the devices in the unstressed state from Figure 85 is shown for comparison. This method of examining the J(V) data identifies and quantifies changes not immediately obvious in the standard J(V) plots. For example, the formation of a blocking contact is clearly indicated in Figure 90 for the 2 devices with the wet process by the sharp minimum in dV/dJ for small values of 1/J (corresponding to J > 10 mA/cm^2). The intercept of a line fit to the linear portion of the data at higher values of 1/J gives R_s, as shown by Equation 42. This increases from ~2 Ω-cm^2 for the initial device to 10-15 Ω-cm^2 for the two devices with the wet contact, to ~30 Ω-cm^2 for the two devices with the dry contact. The slopes give the A-factor, in the dark, which decreases from 1.6 before stress to about 1.4 after stress. However, this A-factor behavior is not unique since the A factor can also remain unchanged or increase with stress as we show in other sections of this report.

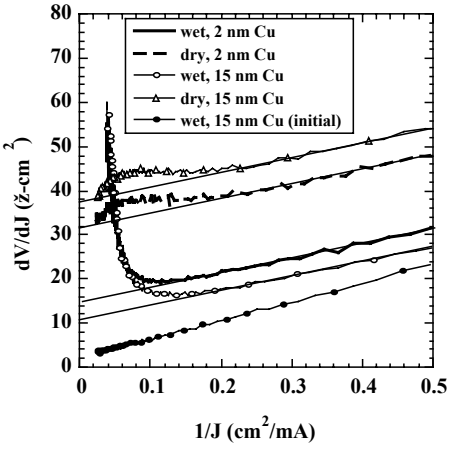


Figure 90. dV/dJ *vs* 1/J for the four dark curves after stress from Figure 88 and Figure 89.

The log $J_{sc}(V_{oc})$ plots after stress were analyzed, and the results are in Table 29. For devices with Cu, the A factor increased slightly, approaching 2, and Jo increased by about 2 orders of magnitude. Note that A factor for the dark J(V) curve decreased after stress (Figure 90). The device without Cu had the lowest Jo and A factor before or after stress, indicating less recombination at deep states and greater resistance to stress.

4.3.5.5 Temperature Dependence of J(V) and V_{oc}

To further characterize the device performance, we have measured the J(V) curves as a function of temperature. Low temperature J(V) measurements can identify contact related problems in CdS/CdTe [97,98]. There are two ways in which low temperature can highlight a poor contact. First, thermal activation over a blocking barrier will be greatly reduced with lower temperature so that a relatively small barrier opposing the main junction barrier can become blocking, i.e., current limiting, at lower temperatures. This will happen even though it is transparent to majority carriers, i.e., Ohmic, at 300K. Second, the lower carrier density in the semiconductor which results at low temperatures may be insufficient to maintain sufficient majority carrier current flow, leading to space charge limited currents.

Figure 91 shows the dark and light J(V) before stress for the device with wet contact process and 15 nm Cu at 25°C and –30°C. At the lower temperature, the LDXO becomes extreme and the light JV curve develops "rollover" beyond V_{oc}. At –50°C the light diode characteristic was horizontal and flat beyond V_{oc}. Similar changes in the JV curve occurred at lower temperature in all of the devices we studied regardless of their contact process or Cu thickness. The light JV characteristic is normal in the power quadrant but the CdTe contact has become current limiting, or blocking, to holes beyond V_{oc}. The simplest explanation is that the back contact forms a Schottky barrier in series with the CdS/CdTe junction [97,98], but other models have been proposed [91,92].

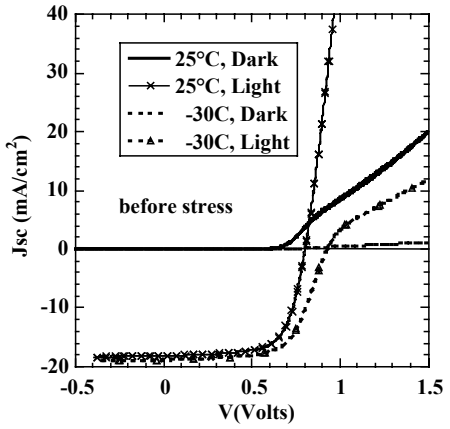


Figure 91. Light and dark JV curves at 25 and –30°C before stress.

It is well known that V_{oc} will vary linearly with temperature in an ideal solar cell as given by Equation 43. Figure 92 shows V_{oc} *vs* T for the same two devices with 2 nm Cu from Figure 84 and Figure 87, along with one having the wet contact with no Cu. All were measured at ~1 sun

intensity. A linear dependence is seen from 220K to 350K for the two devices with Cu. Their common intercept at T = 0K indicates a barrier height ~1.45 eV, which is the CdTe bandgap as predicted by Equation 19, and confirming that recombination is governed by space charge recombination [90]. Figure 93 shows $V_{oc}(T)$ for the device without Cu before stress at 3 intensities. Extrapolation to 0K has an intercept of 1.35 eV for all intensities but there is evidence of carrier freeze-out below 250K. When there are no longer sufficient free carriers, the quasi-Fermi levels no longer respond to changes in light intensity or temperature. V_{oc} reaches its maximum value of V_{bi} which is determined by the absorber bandgap and the contacts. V_{oc} becomes independent of temperature or intensity, violating Equation 43. Thus, even 2 nm of Cu is sufficient to establish idealized junction behavior. Without Cu, the CdTe behaves as though nearly intrinsic. Note that blocking contacts have no effect on V_{oc} at any temperature or intensity because there is no current flow.

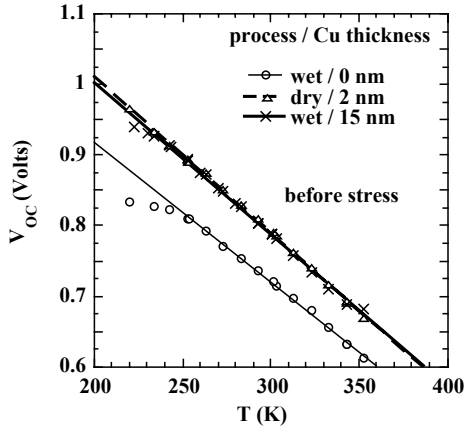


Figure 92. V_{oc} (1 sun) *vs* T before stress for devices with various contact processing.

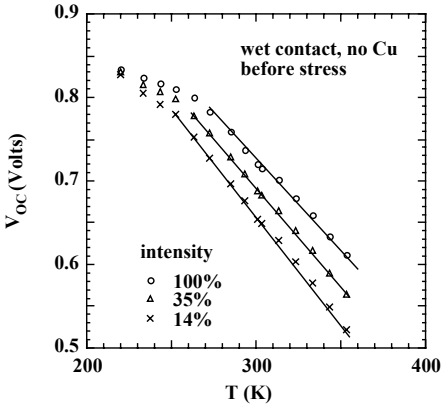


Figure 93. V_{oc} *vs* T for device without any Cu layer at several intensities.

$V_{oc}(T)$ was measured after stress, and results from some devices are given in Table 29. There is little difference between the two different contacts with Cu after stress. The intercept at T = 0 has decreased slightly from ~1.45 before stress to ~1.40 V after stress. This suggests that the

bandgap in the region dominating the recombination has changed. Previous measurements and analysis at IEC [99] and elsewhere have found the bandgap of the CdTe(S) alloy resulting from the S diffusion is approximately 0.1 eV less than bulk CdTe, consistent with the magnitude of the decrease in V_{oc} extrapolated to 0 K. The device without Cu shows little change in any parameters compared to devices with Cu, where the A-factors increase slightly (approaching 2), J_o increases by about 2 orders of magnitude, and the V_{oc} (0 K) decreases ~ 0.1 V. Together, these results suggest that after stressing, the recombination mechanism does not change but the amount of recombination increases significantly. Figure 94 shows how V_{oc}(T = 0K) and V_{oc}(T = 0K)/A vary with the standard parameter V_{oc}(25°C) before and after stress for many of the devices in this study. The intercept at T = 0K is essentially equal to the CdTe bandgap before stress, within the noise of the data, and decreases ~0.05-0.1 V after stress. The intercept divided by A is the effective activation energy for recombination (Equation 41). The A factor used here was determined from V_{oc} *vs* ln(J_{sc}) and was typically 1.5-1.7 before stress and 1.8-2.0 after stress, as in Table 29. This activation energy decreases from about 0.9-1.0 eV before stress to 0.7-0.8 eV after stress, suggesting that the CdTe Fermi level has moved deeper towards midgap after stress for all the devices with Cu. However, note that V_{oc}(T = 0K) and V_{oc}(T = 0K)/A for the device without Cu have a different dependence on V_{oc}(25°C) and on stress. The effective activation energy is much shallower before and after stress. The devices without Cu do not have the same V_{oc} temperature dependence as devices with Cu before and after stress, indicating that they have different limiting recombination mechanisms.

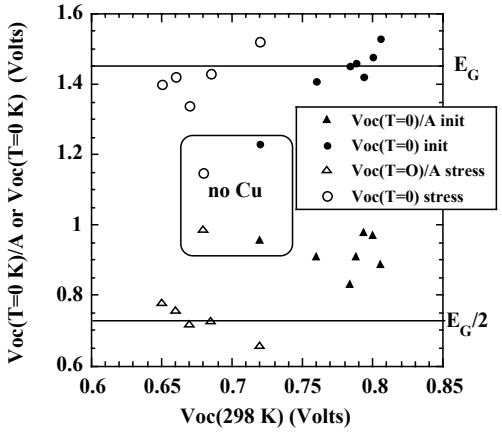


Figure 94. V_{oc}(0K) and V_{oc}(0K)/A *vs* V_{oc} (25°C) for many devices in this study before and after stress. Note the data within the box for the one device without Cu.

4.3.5.6 Capacitance and Space Charge Density

The capacitance voltage C(V) characteristics have been measured at 28°C in light and dark at 10 kHz. Under these conditions, holes trapped within about 0.4 eV from the valence band edge can contribute to the signal, in addition to free carriers (assuming the CdTe is p-type). C(V) in the light was ~10-20% greater than in the dark, indicating that the CdTe devices in their initial state do not have a large number of shallow traps. As is well known, plotting C^{-2} *vs* V for an ideal p-n junction with a uniform space charge yields a straight line whose slope is the space charge density N and whose intercept is the built-in voltage. Figure 95 shows C^{-2} *vs* V for a device with

15 nm Cu and device with no Cu. Many, but not all, devices with Cu contacts had a linear region in reverse bias while devices without Cu had no such a linear region. The slope of Figure 95 for the device with Cu indicates a space charge density of about $3x10^{14}$ and $5x10^{14}$ cm^{-3} and intercepts of 1.6 and 1.3 V, in the dark and light, respectively. These space charge densities obtained from C^{-2} *vs* V at reverse bias are typical of what has been reported by others for CdTe devices deposited by different methods [100,101]. The near saturation at reverse for the device without Cu is typical of a p-i-n structure where the bulk of the CdTe is almost totally depleted at –2V. Assuming a barrier of 1 eV and the measured CdTe thickness of 4 μm suggests a space charge density of 1-$2x10^{14}$ cm-3 can be inferred for the device without any Cu layer. Note that devices with or without Cu have about the same photocapacitance effect, suggesting that Cu-related defects are not responsible for the trapping of photogenerated carriers.

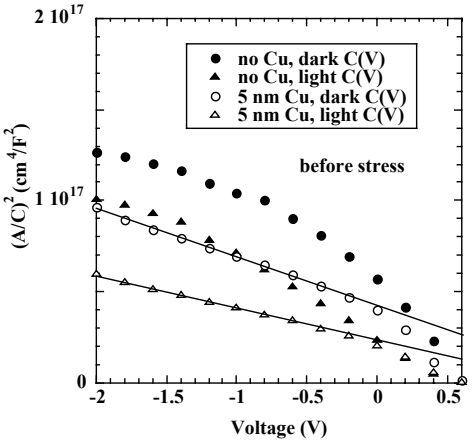


Figure 95. C^{-2} *vs* V for devices with 0 or 5 nm Cu measured in dark and with light bias (before stress).

Figure 96 shows C^{-2} *vs* V in the dark after stress for devices with the 0, 2, and 15 nm Cu. Note that the devices with Cu are no longer linear in reverse bias. Their space charge density has decreased after stress to ~ 1-$2x10^{14}$ cm^{-3} or below.

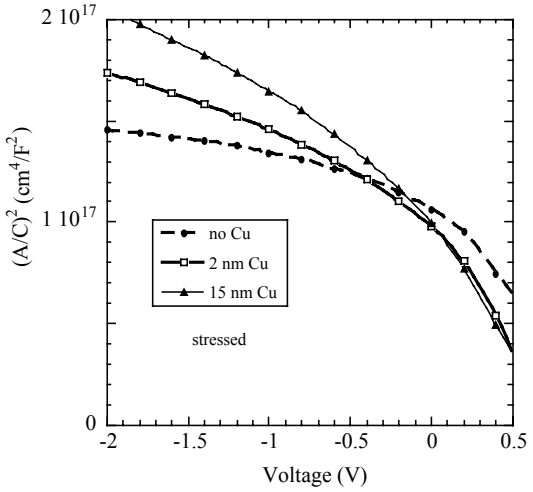


Figure 96. C^{-2} *vs* V in the dark after stress for devices with the 0, 2, and 15 nm Cu.

It is instructive to replot C(V) data in terms of the depletion width W(V) as

$$W(V) = A / (C(V). \quad (45)$$

This form of viewing the C(V) data is especially useful to determine what fraction of the CdTe thickness contains the high field space charge region. Figure 97 shows W(V) for the devices from Figure 95 and Figure 96 calculated from the dark C(V). The depletion width at -2V for the device with the Cu layer increases from 2.6 to 3.9 μm after stressing, while it only increases from 3.3 to 3.5 µm after stressing for the device without the Cu layer. After stress, the space charge profile of the device with Cu is much more similar to the device without Cu, confirming that the devices with Cu become more intrinsic and have lower carrier density after stress. This is an important point since some models of the J(V) characteristics indicate that back contact barriers will impede current flow and become blocking contacts when the carrier density is this low [91].

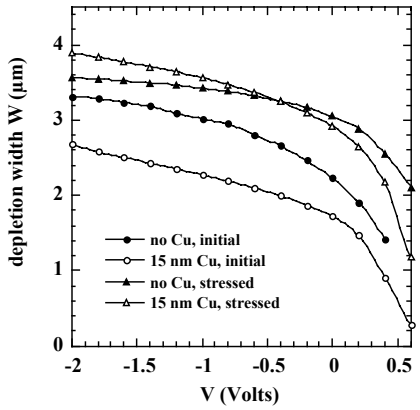


Figure 97. Depletion width W(V) *vs* V for devices with 0 or 15 nm Cu before and after stress, from dark C(V).

4.3.5.7 Effect of Back Contact Process Without Cu Layer

Since devices without Cu seem to degrade differently, and less, than those with Cu, further studies were performed to characterize the degradation of devices without any Cu layer in the back contact. We hesitate to call them "Cu-free" devices since Cu has been reported in the CdS of uncontacted devices or those with no Cu in the contact at roughly 10 times the level in the CdTe, which was essentially the detectability limit [102]. Devices were fabricated from the same CdS/CdTe plate as those previously described and were processed without any intentional Cu layer. Some had the wet contact with and without the BDH etch, and some had the dry contact without the BDH etch. As described in Section 4.3.2, the BDH etch leaves a Te layer > 30 nm while the evaporated Te layer is ~10 nm. Following the surface treatment, the devices received the C ink contact without a Cu layer. Initial J(V) performance, shown in Figure 98, of the devices without Cu with different CdTe surface preparation were comparable with V_{oc} ~ 0.74 V and FF ~ 58%. After stressing (Figure 99) they had comparable V_{oc} ~ 0.68 V but very different FF (47% with BDH etch and <28% without BDH etch). The FF is correlated to the curvature around V_{oc}. After stressing, the slope at open circuit, R_{oc}, was ~20 Ω-cm^2 for the device with BDH etch but >200 Ω-cm^2 for the devices without BDH etch, independent of whether they had wet or dry contact processing. Clearly, for devices without a Cu layer, the surface preparation method has a much greater effect on the stressed J(V) than the initial J(V). After stressing, the sample with BDH processing was less susceptible to blocking contact formation.

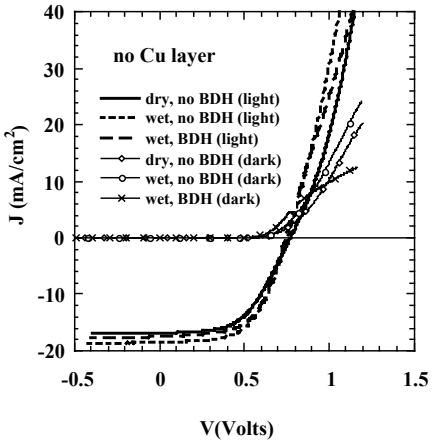


Figure 98. Initial light J(V) curves for devices with no Cu layer in the contact having different CdTe surface treatments prior to C secondary contact.

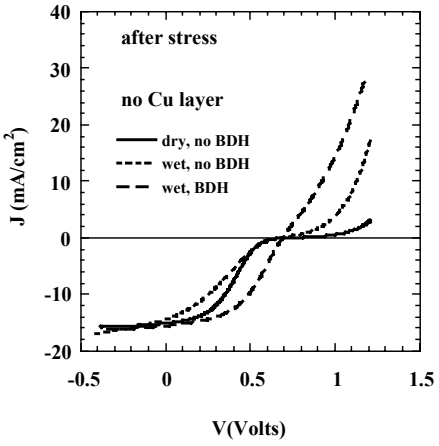


Figure 99. Light J(V) curves after stress for same devices as in Figure 98.

4.3.6 Effect of temperature, bias and ambient during stress

All previous stress-related results in this report are for cells stressed at open circuit, in air, at 100°C. In fact, open circuit bias and air are the two most common conditions used for stress because they are most easily obtained. However, in order to understand the degradation mechanism in more detail, the stress conditions must be varied. In particular, the ambient could influence the chemical reactions at the contact (oxidation vs reduction), hence the oxidation state of the Cu, and the bias will change the electric field which determines the electromigration of ions. Bias also changes the spatial distribution of recombination throughout the device when it is under stress, especially in the presence of a second junction. Reverse bias increases the CdS/CdTe depletion width but shrinks the blocking back contact barrier. Finally, since modules operate at maximum power, around 40-60°C, in inert (encapsulated) environment, we must compare those stress conditions to those more commonly used in the research labs.

Figure 76 already showed the effect of bias for cells stressed at open circuit and 100°C. Figure 100 shows the same relationship, the efficiency ratio *vs* bias during stress, for cells which were stressed in dry air, H_2/Ar or Ar for 10 days. The same general trends are exhibited in each ambient, namely short circuit seems most stable while forward or reverse bias degrades performance more than short circuit. Thus, degradation occurs even in inert or reducing atmospheres. Within the experimental variation, we consider that Figure 100 shows no significant difference due to the ambient during stress. Therefore, we have used dry air from a cylinder for all stressing. Figure 101 shows the effect of temperature during stress in air for 10 days. There is less degradation at the lower temperature, as expected for a thermally activated process. But at V_{oc} or beyond, there is little difference in degradation between 75 or 100°C. This is consistent with our observations reported elsewhere [103] that significant degradation occurs at far forward bias >1.5V even at 60°C.

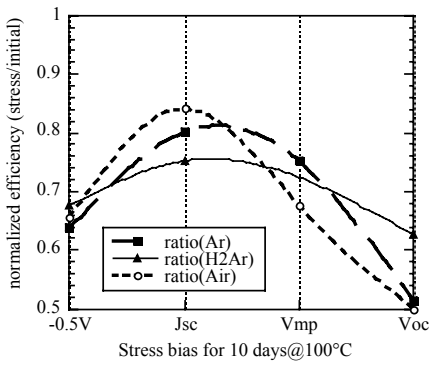


Figure 100. Normalized efficiency *vs* bias during stress at 100ºC for 10 days for three different ambients.

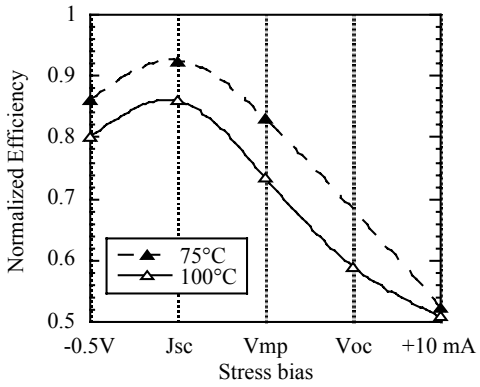


Figure 101. Normalized efficiency *vs* bias during stress at 75 or 100ºC for 10 days in dry air.

We have also repeated these same studies to compare the effect of temperature and ambient using CdS/CdTe devices from BP Solar, and found essentially the same behavior. Thus, it appears that the trends observed here are a function of today's CdS/CdTe devices in general and not unique to one manufacturing process or contact procedure.

4.3.7 Separating the Effect of Primary and Secondary Contacts

4.3.7.1 Background and Motivation

Our understanding of the contact processing and its influence on the device performance has lead to the concept of defining a primary and secondary contact. The primary contact often contains Cu and makes intimate contact with CdTe, and the secondary contact is the current-carrying robust contact layer which is also used in interconnections. IEC has developed processing allowing us to separately manipulate these two regions of the back contact.

4.3.7.2 Contacts, Processing and Stress Conditions

We designed a matrix of back contact structures shown in Table 30 to study the effect of three variables: Cu and Te thickness (these form the primary contact) and secondary contact material. Cu thickness ranged from 0 to 200 nm and the Te thickness was either 10 or 110 nm. This group of samples allowed investigation of the alloy composition of primary contacts including Cu-free, Cu-deficient and Cu-excessive Cu_2-xTe and Cu_2Te, as well as secondary contacts with different work functions. The CdTe/CdS layers were all obtained from the same module plate (20839) provided by First Solar without contacts. All contacting was done at IEC.

Table 30. Matrix of primary (Te and Cu) and secondary (C, Mo, Ni) contacts for CdTe/CdS samples for stress study. Sample number indicates specific piece from glass/SnO_2/CdS/CdTe plate 20839 from First Solar.

d_{Te} (nm)	d_{Cu} (nm)	Phase Field if Homogenized	C Φ = 4.6 eV	Mo Φ = 4.2 eV	Ni Φ = 5.0 eV
10	0	Te	20839G3.1		20839G3.7
10	2	Te + CuTe	20839F4.3	20839I3.3	20839I3.1
10	8	$Cu_{2-x}Te$	20839F4.4	20839F4.7	20839F4.8
10	40	Cu_2Te + Cu	20839F4.5		
110	0	Te	20839G3.2		20839G3.8
110	2	Te + CuTe	20839F4.6		
110	8	Te + CuTe	20839G3.4	20839I3.2	20839I3.4
110	90	$Cu_{2-x}Te$	20839G3.5	20839G3.3	20839I3.5
110	200	Cu_2Te + Cu	20839G3.6		

Immediately prior to contact fabrication, the samples were given a 5 second etch in 0.001 wt% Br_2-CH_3OH to clean the surface. Then the samples were reacted for 1.5 minutes in H_2 + Te vapor to reduce surface oxides and produce a 10 nm thick Te coating. For thicker Te coatings, additional Te was deposited by electron beam evaporation at room temperature. Cu was also deposited by electron beam evaporation. Then the secondary contact was applied, either by painting in the case of C-ink, or by electron beam evaporation in the case of Mo and Ni. Devices were then given a J(V) test, a 30 minute anneal at 200°C in H_2/Ar to activate the contact and interdiffuse Cu and Te, and re-tested.

Based on results in previous sections, we selected stress conditions of 10 days at 60°C, dark, dry air, and three electrical biases (–1V, 0V, and +2V) to focus on the effect of strong forward or reverse bias or strictly thermal effects (0V). Stressing at a lower temperature (60°C rather than 100°C) allows the effect of bias to be more clearly identified. Stress was applied for 1 day at 25°C, then 1 day at 60°C, and then 9 more days at 60°C. After each interval they were removed from stress and tested. We have used this protocol previously [104] to identify processes which occur rapidly (<1 day) and to separate the effects of bias and temperature.

4.3.7.3 Effect of Primary and Secondary Contacts on Initial Performance

Initial results for some of the devices are shown in Table 31.

Table 31. Initial JV performance of best cell on each piece from plate 20839 after HT of 30 min @ 200°C in H_2/Ar.

Piece	Te/Cu (nm)	Secondary contact	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Eff. (%)	R_{oc} (Ω-cm^2)
I3.1	10/2	Ni	0.47	15	49	3.5	14
F4.8	10/ 8	Ni	0.50	14	58	4.0	9
F4.7	10/ 8	Mo	0.50	14	44	4.5	18
F4.4	10/8	C	0.78	20	64	10.3	6
I3.4*	110/ 8	Ni	0.75	18	69	9.5	5
I3.2**	110/ 8	Mo	0.76	18	48	6.8	16
G3.4	110/8	C	0.79	20	67	10.9	5
I3.5	110/ 90	Ni	0.75	17	62	7.7	6
G3.3	110 90	Mo	0.75	16	67	8.2	6
G3.1	10/0	C	0.74	14	40	4	150
G3.8	110/ 0	Ni	0.74	16	65	7.5	9
G3.2	110/0	C	0.74	20	50	7.4	23

* these were the only cells in this series with no curvature in forward bias in either light or dark JV
** before HT, FF > 60% and R_{oc} < 9 Ω-cm^2.

With the thicker Te (110 nm), V_{oc} was typically 0.75-0.76 V with Ni or Mo, while devices with C contacts with the same Cu/Te thicknesses had V_{oc} = 0.77-0.79V. The thicker Te was clearly better regardless of Cu thickness or secondary metal contact. Devices with thinner Te had much lower V_{oc} and no dark diode (J was flat and ~0 in forward bias). Figure 102 shows the light JV curves for 3 devices with Ni contact. Table 31 shows that the devices with 0 or 90 nm of Cu had the same V_{oc} and nearly same FF, yet Figure 102 shows that they had very different behavior in forward bias. The devices with Te/Cu = 10/8 nm and metal contacts (pieces F4.7 and F4.8) had much poorer V_{oc} and larger curvature in forward bias. This ratio of Te/Cu is our standard with C secondary contact, giving much higher V_{oc} and FF (piece F4.4). Figure 103 compares these devices with Te/Cu = 10/8 having C, Ni and Mo secondary contacts. It is clear from the figures and table that the Te/Cu layer thicknesses must be optimized for each secondary contact material.

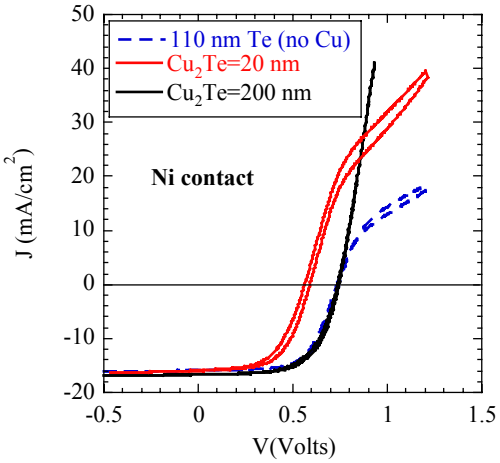


Figure 102. Light JV curves for devices with Ni secondary contact and various Te/Cu thicknesses for primary contact (G3.8 was 110 nm / 0 nm, I3.5 was 110 nm / 90 nm, and F4.8 was 10 nm / 8 nm).

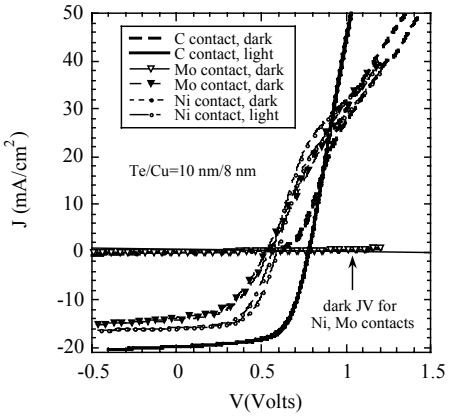


Figure 103. Light and dark JV curves for devices with C, Ni, or Mo secondary contact and Te/Cu = 10 nm / 8 nm for primary contact (F4.4 was C, F4.7 was Mo, and F4.8 was Ni).

The devices with Ni and Mo tended to have $J_{sc} < 17$ mA/cm^2 while those with C tend to have $J_{sc} > 19$ mA/cm^2. Also, as indicated in Table 31, the only devices which had no curvature in forward bias were those with 110 nm Te/ 8 nm Cu/ Ni (piece I3.4) which had the highest FF as well. It is surprising that devices with 90 nm of Cu, which is the thickest Cu layers we have used, still had curvature in forward bias. This indicates a good Ohmic contact is not necessarily achieved with more Cu.

4.3.7.4 C-paste as Secondary Contact: Effect of Cu and Te After Stress

Devices from this matrix with C-contacts having 0 and 8 nm of Cu and 10 and 110 nm of Te have been stressed (G3.1, G3.2, F4.4, G3.4). The normalized efficiency after stress (ratio of stressed efficiency to initial efficiency) *vs* electrical bias during stress is shown for the 4 pieces

after 1 day at 25°C in Figure 104 and after 10 days at 60°C in Figure 105. After 1 day at 25°C with bias Figure 104 shows that all devices lost ~5-10% at –1V but those with Cu lost much more at forward bias than those without Cu. This is consistent with more limited data presented elsewhere [104]. After 10 days at 60°C with bias, the device with thin Te and no Cu shows the largest changes with forward or reverse bias. The changes in devices with Cu are independent of Te thickness, suggesting that the deleterious role of Cu is not influenced by whether the primary contact is stoichiometric Cu_2Te or Cu rich. Both figures confirm past results that degradation is larger at forward bias compared to reverse bias and that zero bias (short circuit) is the most stable bias point. After thermal and bias stressing, the Te thickness has a much greater effect for devices without Cu, indicating it has a more critical role as primary contact without Cu.

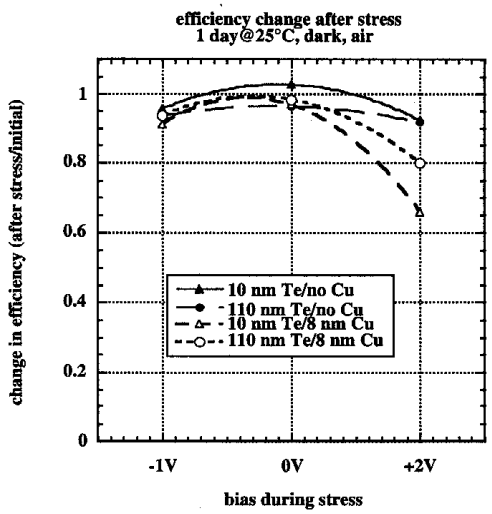


Figure 104. Changes in efficiency after 1 day stressing at 25°C for devices with different Te and Cu thicknesses.

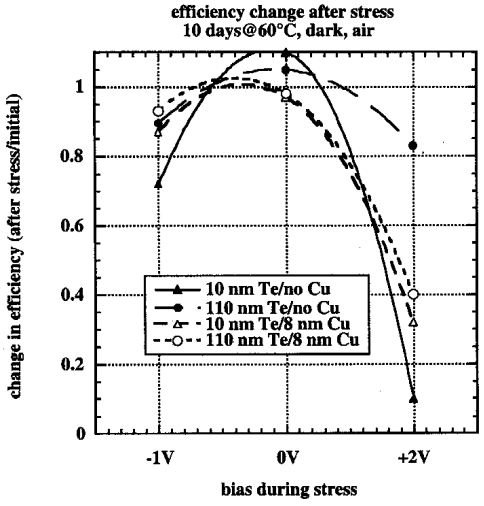


Figure 105. Changes in efficiency after 10 days stressing at 60°C for devices with different Te and Cu thicknesses.

4.3.7.5 Effect of Stability: Te/Cu Thicknesses, Secondary Contact of Ni or Mo

We had planned to repeat exactly the same stress and test protocol on devices with Ni or Mo as used for the devices with C contacts, described above, but an immediate problem arose. Devices with Ni and Mo contacts could not withstand +2V stress bias for more than a few hours before shorting, even at 25°C. (The exception was the device without Cu!) In contrast, devices with C contacts could withstand +2V for 10 days at 60°C, as we have reported above. Therefore, we reduced the forward bias for stressing for Ni or Mo to +1V. Even at this lower bias level, much higher levels of shunting, hysteresis and greater degradation occurred compared to using the C contacts. The rapidity with which severe degradation occurred, even at 25°C, strongly implicates field-driven Cu ion motion down grain boundaries. It is possible that either the metals absorb much less Cu than C, leaving a thicker Cu layer as a diffusion source, or their higher conductivity allows the electric field to penetrate deeper into the contact and into the CdTe, leading to an increased driving force.

Very little change occurred with stress for 1 day at 25°C while significant changes (positive or negative, see below) occurred with stress for 1 day at 60°C. This confirms that temperature and bias are required simultaneously to modify the device performance. Figure 106 shows the relative change in efficiency after the final 10 day stress at 60°C in air for devices with 110 nm Te but different Cu thicknesses and secondary metal contacts. Figure 107 shows the relative change in efficiency for devices with 8 nm Cu layers but different Te thickness and secondary contacts. In both figures, values for +1V stress have larger uncertainty due to hysteresis and shunting effects which were more prevalent in compared to using C as a secondary contact. However, in agreement with those previous studies with C contacts, stress at reverse or forward bias always causes greater losses than at 0V. Note that the efficiency actually increases for the 0V bias stress on 5 of the 8 devices. Typically, FF increased, R_s decreased, and the curvature in forward bias decreased in these cases. This improvement, or recovery, with the low temperature "stress treatment" indicates that the devices with metal secondary contacts were not yet in their optimal state following the pre-stress anneal at 200°C for 30 minutes.

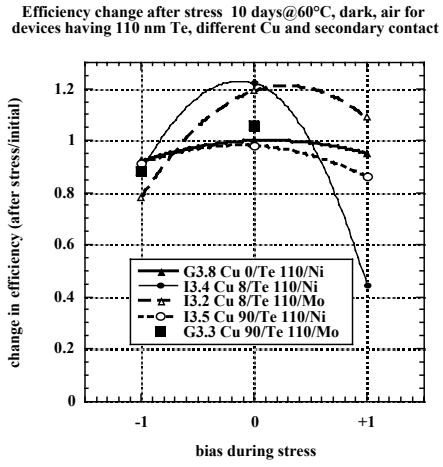


Figure 106. Relative change in efficiency after stressing at –1, 0, or +1V bias. Devices all had 110 nm Te layer but different Cu thickness and secondary contacts.

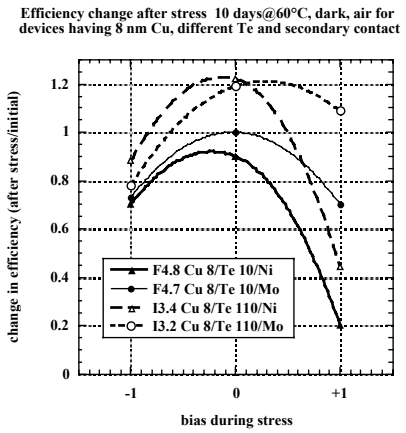


Figure 107. Relative change in efficiency after stressing at –1, 0, or +1V bias. Devices all had 8 nm CuTe layer but different Te thickness and secondary contacts. Values for +1V stress have larger uncertainty due to hysteresis and shunting effects. Note the significant improvements at 0V for devices with thicker Te layers.

From this data, and the initial JV data of Table 31, we conclude the following: thicker Te (~100 nm) is better than thinner Te (~10 nm) layers for both initial and stability considerations; devices with very thick Cu layers can still have non-Ohmic contacts, yet be nearly stable; Te and Cu thickness and their post-contact anneal must optimized for each secondary contact; C contacts tend to give higher V_{oc} and J_{sc}; highly conductive metal contacts like Ni and Mo, in the presence of the Cu layer, cannot withstand nearly as much forward bias stress as C contacts; degradation is not unique to the C ink contact, which we have used in most of our past 2 years of stress evaluations; Cu seems to be required to attain $V_{oc} > 0.75$V and FF > 65%; and, finally, any secondary contact is relatively stable without a Cu layer.

4.3.8 Effect of Temperature and Ambient

There are reports of some CdTe modules being very stable for several years in the field [95,96]. Since modules are encapsulated and some can be stable, and small area cells undergoing accelerated stress in the laboratory are not encapsulated and typically not very stable, it is reasonable to speculate that exposure to oxygen or moisture could be correlated with degradation. This is part of the motivation for building the controlled ambient accelerated stress system at IEC. However, we also investigated the effect of ambient directly. We did this using hybrid devices, consisting of First Solar CdTe with IEC contacts, and also on devices completely made by BP Solar using electrodeposited CdS and CdTe and their proprietary contact. Figure 108 shows the normalized efficiency after stressing in dry air and in H_2/Ar for the two types of devices. They both degrade similarly in dry air or H_2/Ar. We have performed other stress studies in Ar and found similar results. This indicates that to first order, the presence of O_2 is not required for degradation.

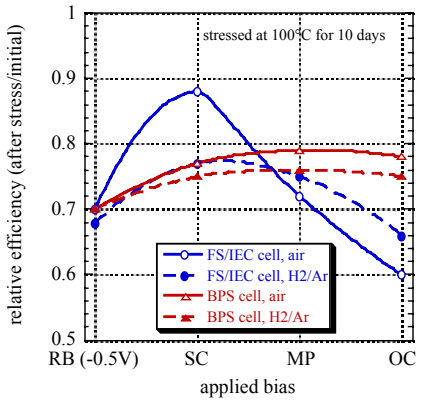


Figure 108. Normalized efficiency of hybrid FS/IEC devices and BP devices stressed in dry air or H_2/Ar at different bias at 100°C.

It is also reasonable to speculate that since modules in the field rarely see temperatures over 60°C, perhaps stressing at 100°C is excessively damaging. Results in Section 0 show stress at 60°C certainly can cause degradation. To further characterize the temperature dependence, we stressed hybrid First Solar and completed BP devices at 80°C and 100°C. Figure 109 compares normalized efficiency for stress at 80 and 100°C for the two types of devices. They degrade similarly, each showing greater degradation at higher temperature, suggesting a thermally activated process.

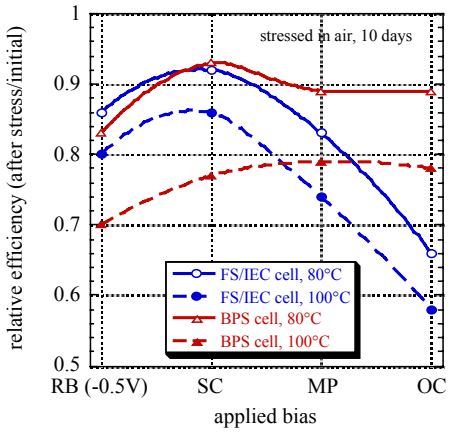


Figure 109. Normalized efficiency of hybrid FS/IEC devices and BP devices stressed in dry air at different bias at 80 or 100°C.

4.3.9 Recovery After Accelerated Degradation

The J(V) performance on a few devices has been measured at intervals for ~6-12 months following stress. The devices have been stored in the dark in air. Results are shown in Figure 110 for a device that was stressed for 10 days at 100°C in air at OC. It was tested 1 day, 17 days, and 10 months after stress. It is commonly observed that the V_{oc} may increase by 30–60 mV

while the FF remained the same or degraded another few percent. The curvature in forward bias J(V), created by stressing, straightens out, indicating the Ohmic CdTe contact was restored, similar to recontacting. The recovery in V_{oc} and Ohmic contact occurred in devices with wet or dry contacts. We have attempted to force recovery in periods of days (for cells stressed at V_{oc} at 100°C in air for periods >6 days) by applying reverse bias, at 25 or 60°C, in dark or light, in air or H_2/Ar, but without success. We also stressed devices at V_{oc} for relatively short periods of 20 hours, then switched them to J_{sc} (by shorting the contacts) while keeping them at 100°C in the light. The V_{oc} degraded ~100 mV in the first 20 hours of stress at V_{oc}, then recovered ~50 mV in the next 200 hours of stress at J_{sc}. However, devices that had been stressed at V_{oc} for extended periods (>10 days) could not be recovered by switching to J_{sc}.

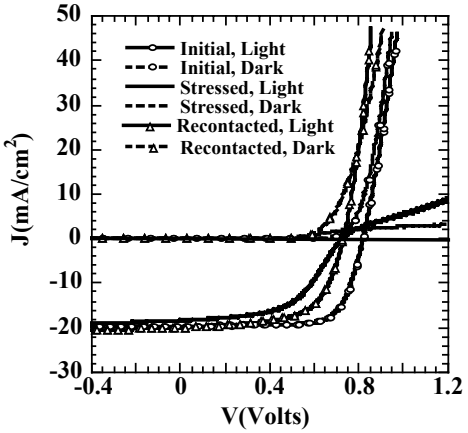


Figure 110. Light J(V) curves for FS/IEC device in initial and post-stress conditions.

Taken together, these results suggest that losses in V_{oc} with stress at V_{oc} are metastable. Perhaps the increase in recombination created with stress relaxes as the midgap centers slowly change their occupancy by capturing or emitting charge and become neutral. Recovery occurs much more slowly than degradation even at 100°C. It is unlikely that the simple movement of Cu ions in the presence of an electric field or diffusion of Cu from back to front can explain these changes.

4.3.10 Summary and Conclusions

Figure 76 summarizes the dependence of relative efficiency on bias stress, and Figure 80 and Figure 81 summarize the dependence of V_{oc} and FF on Cu layer thickness before and after stressing for the wet and dry contact processes. Initial performance is very similar for the two processes independent of Cu thickness. Initial V_{oc} was 0.80 ± 0.02 V and initial FF was 69 ± 2% for all devices except ones without Cu. Note that the device without Cu having the wet contact has the highest V_{oc} after stressing, despite having the lowest initial V_{oc}. But we found no strong dependence of either solar cell performance (V_{oc}, FF, J_{sc}) or device properties (A, J_o, space charge, R_s) on Cu concentration (2-15 nm) or the contact process. These results demonstrate significant degradation occurs independent of the amount of Cu for both of the contact processes. Although we observed that devices with the dry contact process tend to have less "roll over" or curvature in forward bias after stressing, they had no significant difference in FF. This suggests

the wet contact enhanced the formation of the blocking contact despite its having consistently a slightly higher FF after stress (Figure 81). The two key differences between the dry and wet process are that the dry process leaves a thinner Te layer and is less penetrating along grain boundaries. It is not known yet how these differences are responsible for the differences in blocking contact formation.

Analysis of the J(V) characteristics indicates that the junction recombination is a Schockley-Read-Hall (SRH) mechanism. Evidence includes A values between 1.5 and 2.0, $V_{oc}(T)$ values extrapolated to T = 0K equal to the CdTe bandgap, and the temperature dependence of J_o giving an activation energy near midgap of CdTe. This suggests that deep centers in the CdTe, whose concentration increases with stress, are responsible for the recombination limiting V_{oc}.

Losses in V_{oc} and FF occur within the ~1 week stress time used in this study, while stressing for longer times enhances the formation of the blocking contact. Consistent with our recontacting study (Section 4.3.4), we have found that losses in V_{oc} and FF are independent and separable. And finally, since even devices without any Cu layer show degradation (Figure 80, Figure 81, and Figure 99), other non-Cu related degradation mechanisms must be identified and solved. Before stressing, low V_{oc} and FF result without Cu doping layer, consistent with our previous results using both SCI/FS CdTe material. Degradation in V_{oc} for these "Cu free" devices is much less (~0.06V) than typically found for devices with Cu layer (see Figure 80). The relatively smaller loss in V_{oc} after stressing is independent of the contact processing or surface etch. However, severe degradation in FF occurs even without Cu. Devices without the BDH etch show extreme distortion of the JV curve, suggesting formation of a blocking contact is suppressed with sufficient Cu or Te, consistent with maintaining a p+ surface. The changes in J-V behavior due to stress in Section 4.3.5 suggest changes in non-Cu doping sources such as oxygen, chlorine, and excess Te. Devices with insufficient Cu dopant will be more susceptible to presence of other doping species which may be less well controlled.

5. ABSTRACT

This report describes results achieved during a three-year subcontract to develop and understand thin film solar cell technology associated to $CuInSe_2$ and related alloys, a-Si and its alloys and CdTe. Modules based on all these thin films are promising candidates to meet DOE long-range efficiency, reliability and manufacturing cost goals. The critical issues being addressed under this program are intended to provide the science and engineering basis for the development of viable commercial processes and to improve module performance. The generic research issues addressed are: 1) quantitative analysis of processing steps to provide information for efficient commercial scale equipment design and operation; 2) device characterization relating the device performance to materials properties and process conditions; 3) development of alloy materials with different bandgaps to allow improved device structures for stability and compatibility with module design; 4) development of improved window/heterojunction layers and contacts to improve device performance and reliability; and 5) evaluation of cell stability with respect to illumination, temperature and ambient and with respect to device structure and module encapsulation.

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Appendix 1

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30. "Hot-Wire Chemical Vapor Deposition of Silicon from Silane: Effect of Process Conditions," A. Pant, T.W.F. Russell, M. Huff, R. Aparicio and R.W. Birkmire, *Ind. Eng. Chem. Res* **40**, (2001) 1377.

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13. ABSTRACT *(Maximum 200 words)* This report describes results achieved during a three-year subcontract to develop and understand thin-film solar cell technology associated to $CuInSe_2$ and related alloys, a-Si and its alloys, and CdTe. Modules based on all these thin films are promising candidates to meet DOE long-range efficiency, reliability, and manufacturing cost goals. The critical issues being addressed under this program are intended to provide the science and engineering basis for the development of viable commercial processes and to improve module performance. The generic research issues addressed are: 1) quantitative analysis of processing steps to provide information for efficient commercial-scale equipment design and operation; 2) device characterization relating the device performance to materials properties and process conditions; 3) development of alloy materials with different bandgaps to allow improved device structures for stability and compatibility with module design; 4) development of improved window/heterojunction layers and contacts to improve device performance and reliability; and 5) evaluation of cell stability with respect to illumination, temperature, and ambient and with respect to device structure and module encapsulation.

14. SUBJECT TERMS: PV; solar cell performance; solar cell processing; in-line evaporation; grain-boundary diffusion; microcrystalline p-layers; hot-wire CVD; window layer processing; grain enhancement; photoconductive; optimization; modeling; a-Si; CdTe; thin film CIS

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