Revised February 2004 • NREL/SR-520-35348

Subcontractor Report

Research Leading to High Throughput Processing of Thin-Film CdTe PV Module

Phase I Annual Report
October 2003

R.C. Powell and P.V. Meyers
First Solar, LLC
Perrysburg, Ohio

National Renewable Energy Laboratory

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Contract No. DE-AC36-99-GO10337

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Prepared under Subcontract No. RDJ-2-30630-20

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Glossary of Abbreviations

ALF	Alan Farhenbruch consulting
ALT	Accelerated Life Test
CV	Capacitance-Voltage measurement
CSM	Colorado School of Mines
CSU	Colorado State University
DAP	Donor-Acceptor Pair
EH&S	Environmental, Health and Safety
FF	Fill Factor
IEC	Institute of Energy Conversion at the University of Delaware
I-V	Current-Voltage measurement
IVT	Current-Voltage measurements as a function of temperature
J_{sc}	Short circuit current density
NREL	National Renewable Energy Laboratory
OC	Open Circuit
PL	Photoluminescence
PV	Photovoltaics
Roc	Dynamic resistance at open circuit
Rsc	Dynamic resistance at short circuit
SC	Short Circuit
USF	University of South Florida
UT	University of Toledo
V_{Cd}	Cadmium vacancy
V_{oc}	Open circuit voltage
VTD	Vapor Transport Deposition

Abstract

First Solar is committed to commercializing CdTe-based thin film photovoltaics. This commercialization effort includes a major addition of floor space and equipment as well as process improvements to achieve higher efficiency and greater durability. This report presents the results of phase I of the subcontract entitled **"**Research Leading to High Throughput Manufacturing of Thin-Film CdTe PV Modules". The subcontract supports several important aspects needed to begin high volume manufacturing including further development of the semiconductor deposition reactor, advancement of accelerated life testing methods and understanding, and improvements to the environmental, health and safety programs.

Progress in the development of the semiconductor deposition reactor was made in several areas. First, a new style of vapor transport deposition distributor with simpler operational behavior and the potential for improved cross-web uniformity was demonstrated. Second, an improved CdS feed system that will improve down-web uniformity was developed. Third, the core of a numerical model of fluid and heat flow within the distributor was developed including flow in a 3 component gas system at high temperature and low pressure and particle sublimation.

Progress in several measurement systems that support both deposition reactor development and accelerated life testing includes device performance mapping and bandgap determination from optical reflectance. Progress on the core of numeric model for the quantitative assessment of the effects of macro-non-uniformity was also made.

A rapid (3 day) accelerated life test procedure is under development and initial correlation results indicate that the current 56 day test could be replaced. Advancement in understanding stress induced change mechanisms included 1) the elimination of several potential mechanisms, 2) increased sophistication of capacitance-voltage interpretation, 3) identification of several potential degradation markers, and 4) the selection of improved interface control procedures. We did not find a clear mechanism and marker for the stress induced changes investigated however.

Several significant improvements in our Environmental, Health and Safety program were achieved including 1) a reduction in solid waste generation, 2) development of methodology for testing hazardous dust filtration apparatus, 3) investigation of a leaching mitigation strategy, and 4) initiation of a third party verification of our industrial hygiene program. Solid waste reduction was significant with the conversion from disposal to recycling of over 14,000 pounds in 4 months.

Work under this subcontract contributes to the overall manufacturing operation. During phase I, average module efficiency on the line was improved from 7.1 to 7.9% due primarily to increased photocurrent resulting from a decrease in CdS thickness. At the same time production volume for commercial sale increased from 1.5 to 2.5 MW/yr.

Acknowledgements

We gratefully acknowledge the contributions of First Solar employees including, Anke Abken, Dave Berger, Eugene Bykov, Ken Cherry, John Christiansen, Todd Coleman, Tony Draper, Andy Gray, Upali Jayamaha, Peter Meyers, Anne Moser, Nick Reiter, Ken Smigielski, Mike Steele, and Syed Zafar, as well as personnel from First Solar production, engineering and management.

We are also grateful for the support that we have received from National Renewable Energy Laboratory staff, including Dave Albin, Sally Asher, Pat Dippo, Tim Gessert, Tom McMahon, Glenn Teeter, Harin Ullal, Suhuai Wei, Xuanzhi Wu, and Ken Zweibel. Contributions from Steve Hegedus and Brian McCandless of Institute of Energy Conversion; Jim Sites and Samuel Demtsu of Colorado State University; Alan Farhenburch of ALF; Alvin Compaan, Victor Karpov, and Diana Shvydka of University of Toledo; Scott Feldman, Scotty Gilmore, Victor Kaydanov and Tim Ohno of Colorado School of Mines; and Chris Ferekides of University of South Florida are gratefully acknowledged.

Two lower-tier subcontracts are directly contributing to this work. The first project, titled "Direct Integration of Solid-Prescursor Powders into Chemical Vapor Deposition Systems", involves modeling of the heat and mass transfer in the deposition reactor. This work is being conducted by J.P. Delplanque, Robert Kee, and Mark Pavol of Colorado School of Mines. The second project, titled "Nonuniformity Loss in Photovoltaics", involves the modeling of performance loss due to spatial variation. This work is being performed by Victor Karpov and Diana Shvydka at University of Toledo.

1. Introduction

First Solar has developed proprietary thin-film PV module manufacturing technology and has employed that technology in a new module manufacturing plant with an expected capacity of 25 MW/yr. First Solar's plan for rapid, large-scale commercialization of thin-film PV requires significant efforts in a number of areas. Support from this contract addresses three major components – 1) research on enhancements to the high-throughput CdS/CdTe deposition reactor, 2) Accelerated Life Test (ALT) development and research of stress-induced changes in devices, and 3) enhanced environmental, health and safety (EH&S) technology.

Motivation for research on the deposition reactor stems from a relatively young deposition technique for the main semiconductor junction, the need for consistent operation during the production of ~10^4 plates between maintenance cycles, and persistent uniformity issues over large areas.

ALT testing is critical to assure the 20+ year performance that underlies the economics of PV systems.

Large scale manufacturing of a product that contains cadmium, a regulated material, requires development of procedures for further reduction in emissions and solid wastes. This includes further identification, characterization, monitoring and reduction of cadmium emissions and improvements in module recycling.

Related work that is supported with other funding sources (primarily internal) includes:

- Improved transparent conducting layers with buffer layers for use with thin CdS to increase module efficiency
- Improved encapsulation processes to eliminate the risk of encapsulation failure
- Next-generation scribing for reduced costs and increased module efficiency
- New recrystallization approaches, possibly providing improved process robustness and product reliability
- Production process development for increased module efficiency, yield and throughput

During this contract year two additional items are worth noting. First as part of an expansion of the production facility, it was decided to build a new semiconductor deposition system based on the success of the semiconductor deposition reactor. This decision was taken primarily to improve the uptime of the semiconductor coating equipment. Second, in partnership with NREL, work on the VTD method has been recognized with a 2003 R&D 100 award.

2. Deposition Reactor Development

2.1 Distributor Development

At the heart of the First Solar manufacturing technology is the semiconductor coater. CdS and CdTe are deposited sequentially in the same piece of equipment using the vapor transport deposition (VTD) method. VTD is a high-throughput, large- area coating technique pioneered and patented by First Solar [1, 2]. The system capitalizes on the ease with which CdS and CdTe can be vaporized and on the rapid rates at which quality films can be formed from re-condensing vapors. Essentially the method utilizes flash-sublimation of injected semiconductor powders in an inert carrier gas stream to create a dense vapor cloud in a modest vacuum (~5 Torr). The inert carrier gas flow directs and controls the dense vapor cloud. The semiconductor films are formed on glass substrates at temperatures between 500 and 600 ºC. As currently employed, CdTe films are deposited with average growth rates > 1 μm/s and peak rates estimated to be ~20 μm/s. The inert carrier gas and some vapors not deposited are then exhausted from the chamber.

Since the VTD deposition rates are rapid, the length of the deposition zones needed to form the relatively thick (2-5μm) absorber layer at production line speeds of ~1.9 m/min is relatively short. These compact high temperature deposition zones are ideal from a manufacturing equipment perspective as short deposition chambers can be used (lower capital equipment costs) and small critical areas are easier to manage. The production vapor generator and vapor distributor system in use today is relatively simple, robust, and durable. In fact, a recent distributor was used to coat ~17500 plates without maintenance.

The film formation process must be integrated with the control of glass properties. The extremely high deposition rates of the VTD method require high substrate temperatures. From the glass perspective, the VTD system heats low-strength, annealed glass to temperatures in excess of the glass softening point. Quenching during venting of the vacuum exit load lock strengthens the glass. The quenching process must be closely coordinated with overall system thermal management in order to achieve glass flatness and strength uniformity. Glass strength is required for field deployment and glass flatness is needed for consistent laser scribing and module lamination.

Once the overall system reaches steady state, very consistent films are produced. The uniformity of film properties is remarkably good given the simplicity of the distributor and the width of the substrate. CdS and CdTe films with adequate thickness uniformity (±10%) can be produced with the current system. However, device performance varies as a function of position across a plate. In addition, differences between nominally identical distributors and distributor aging effects have been observed. Moreover, in the base distributor design thickness uniformity depends on carrier gas flow. Consequently, carrier gas flow is adjusted to produce the best possible film thickness uniformity and cannot be altered to change dilution or improve input powder transport.

Research on enhancements to the high-throughput CdS/CdTe deposition reactor has 3 main components: the design of improved distributors, process development, and thin

film characterization. It is well known that spatial variation in thin film coatings can lead to a number of parasitic losses. Consequently significant effort has been directed towards measuring, improving, and assessing the impact of film uniformity.

2.1.1 Alternative Distributors

At the heart of the VTD method is the vaporizer/distributor system. The design, materials, and methods of operation of the distributor system fundamentally control film formation including uniformity of thickness, microstructure and junction properties. The distributor serves three main functions. First, the input powder must be vaporized. Second, a uniform cross-web[†] distribution of mass flow must be achieved in order to form films of uniform thickness. Third, presentation of the deposition flux to the glass controls film nucleation and growth and thereby microstructure.

The base distributor design is simple both mechanically and thermally. Film thickness uniformity depends on carrier gas flow and feed injection location. Moreover the dependence is not intuitive and experience is required for uniformity adjustment. A number of possible alternative designs have been investigated, but lack of understanding of distributor operation was one major obstacle limiting progress. In other words, the rudimentary modeling that had been employed to aid the distributor design process was incapable of describing the central features of base distributor operation.

Therefore we began an effort to provide a solid theoretical base for distributor operation as will be described below. The first major result of this modeling highlighted some of the subtleties of vapor flow in a low-pressure, three component gas system. This insight helped guide the selection of alternative distributor designs.

During this contract period, three general types of alternative distributors were tested. The first type involves variation of the base distributor, primarily in the manner in which powder and carrier gas is injected into the vaporizer. The distributor modeling strongly suggested that if two different configurations could be experimentally implemented, that significant improvements were possible. The theoretically most desirable configuration was built and tested. The result was a minor change to base distributor behavior. Apparently the needed conditions were not achieved with the particular experimental implementation. Since no other straightforward arrangement was obvious, the design path was abandoned. The second variation on the base distributor theme is still under investigation. Early tests indicate some significant change to distributor behavior but a clear advantage given the added complexity has not yet been demonstrated.

The second general type of alternative distributor will be designated as VTD-2. In this concept, the problems that arise in a low-pressure, three component gas system are practically eliminated in a robust manner. The VTD-2 idea essentially separates the vaporization and distribution functions of the system. It is intuitively appealing and has

[†] Cross-web denotes transverse to the direction of motion in the deposition system and down-web refers to in the direction of motion in the deposition system.

been a candidate for some time. Input from the theoretical modeling effort has bolstered confidence for this concept. Several different configurations of the VTD-2 idea have been tested. The basic operation of a VTD-2 style distributor is fundamentally different from the base distributor behavior. Here the film thickness uniformity is controlled by distributor geometry and is nearly independent of carrier gas flow (see Figure 1 and Figure 2). The VTD-2 concept necessitates distributors with a greater degree of mechanical and thermal complexity however. As will be described below, the thermal configuration now becomes the central challenge for a practical distributor.

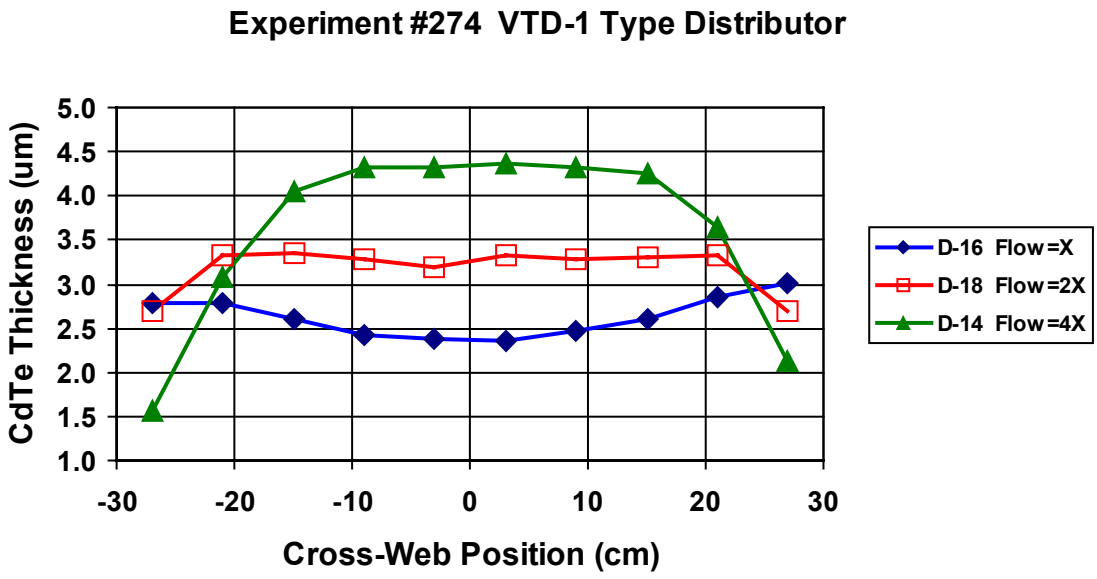


Figure 1. Cross-web thickness uniformity for VTD-1 type distributor.

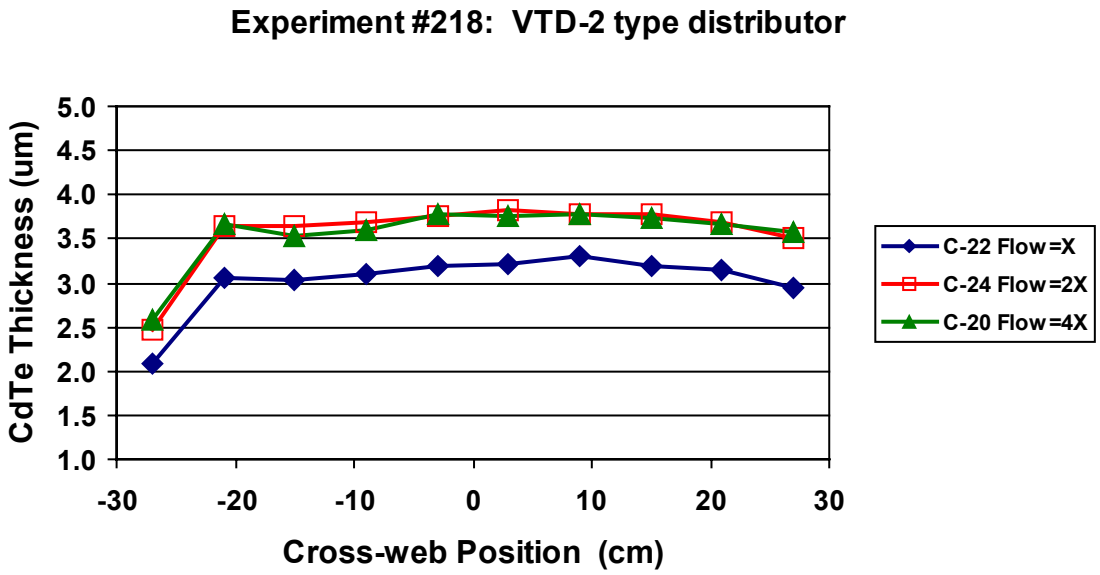


Figure 2. Cross-web thickness uniformity for VTD-2 type distributor.

The third type of alternative distributor is a combination of VTD with a batch load source crucible. This type of distributor is under consideration for CdS only since the material usage rates are low. For very thin films of CdS, input powder metering becomes a significant issue for VTD systems (see below). In this case a batch load system may be a practical alternative, however very tight thermal control is required to control film thickness. For CdTe the greater material usage rate favors continuous material input systems. A batch load VTD distributor system for CdS was built and tested. Good quality films were easily obtained although film thickness uniformity was not adequate. The experiment pointed the path to improved uniformity, however further work will be delayed indefinitely. The direct control of film thickness via powder input rate provided by the standard VTD system is very convenient and even for thin CdS films powder metering has not been shown to be too cumbersome.

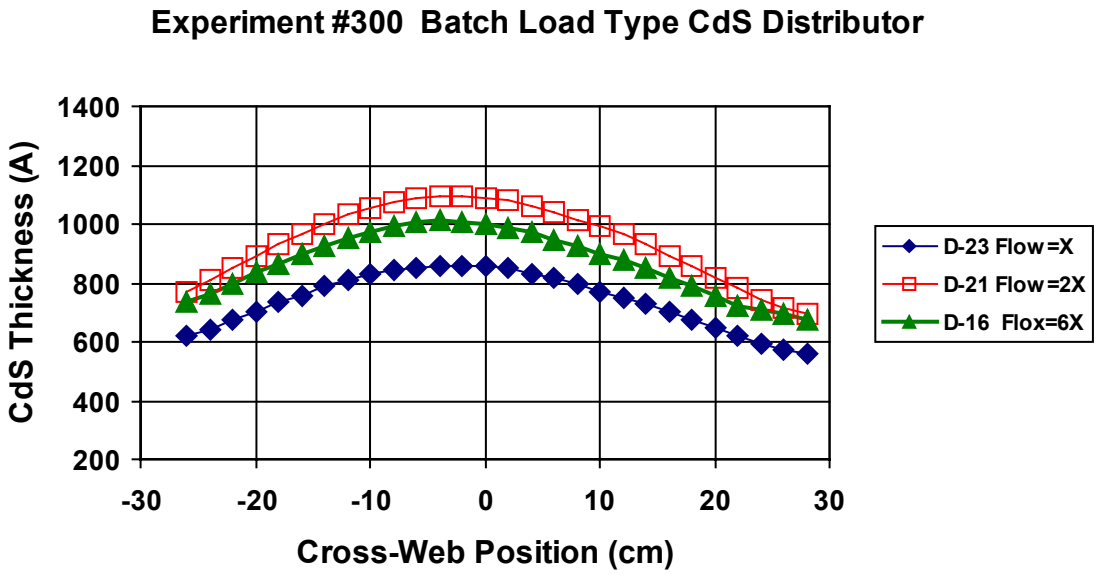


Figure 3. Cross-web thickness uniformity for Batch Load Type CdS distributor.

Several versions of the VTD-2 concept were built and tested. The greater mechanical and thermal complexity of the VTD-2 concept raises additional issues. For example, mechanical tolerances between distributor components at temperature must be considered. The most significant issue however is a thermochemical one. Te_2 and S_2 vapors at high temperature are very aggressive and can attack high temperature components. The corrosion per se is not troublesome, but volatile impurities can form and contaminate the semiconductor layers or disrupt deposition. While this impurity pathway can occur in a base distributor, significant effects do not occur until operation at ~200ºC above normal operating conditions.

Several of the VTD-2 designs tested had regions where the temperature limit was exceeded and thus film contamination was observed. Newer designs are careful to obey the temperature limit.

2.1.2 Distributor Modeling

Despite the simplicity of the basic VTD system, the heat and mass transport processes that occur within it are complex. A program to provide a solid theoretical understanding of the distributor operation was begun in collaboration with a group from Colorado School of Mines. The goal of this effort is to guide the experimental work of distributor design and operation. The distributor function separates into 4 major components: vaporization, fluid flow, heat transfer and deposition. The approach is to first model each functional component separately and then integrate the components.

The first function addressed was fluid flow. Two complementary models have been employed: plug flow and the "Dusty Gas Model". Plug flow is a quasi-one-dimensional approximation within each layer of the distributor and accounts for the flow from one layer to the next using source and sink terms. With the appropriate form of the source and sink terms, both sublimation and geometrical aspects of the distributor can be handled. The Dusty Gas Model is used where appropriate for source and sink terms. The overall fluid flow model has been used without sublimation to study the flow distribution in several distributor designs and to explore the effects of dimensions, geometries, and flow rates. The fluid flow model has also helped in understanding fluid flow in a 3 component gas at high temperatures and low pressure. Elements of the fluid flow model will also be used to treat the mass transport in the gas above the deposition surface.

Heat transfer within the distributor has been modeled using commercially available finite element software. Two aspects of the heat flow have been investigated with 2-dimensional approximations. The first was investigation of axial heat flow at the distributor ends. This was done to simulate thermal edge effects and to investigate the possibility of sourcing impurities from components at the edge of the hot zone. We also used thermal modeling to evaluate excessive temperature conditions for various heating options in a VTD-2 distributor.

Using the fluid flow model, we have found that the vapor source location can have a strong influence on the axial vapor density uniformity for some distributor types. We also know that the thermal budget in the distributor has a variety of effects. Therefore a sublimation model of the powder injection is being developed. When complete, this model will track the path the powder particles take through the distributor as they sublime. This model will be capable of using a non-uniform size distribution of particles and allow for multiple injection points of particles and carrier gas. The flow field calculations in the model will be coupled to the particles by way of mass, momentum, and energy. Currently, the model has the ability to track a single particle through a specified three-dimensional flow field using an approximation for the sublimation rate. We are currently looking at ways to determine the sublimation rate based on the reaction rates, particle size, temperature, velocity, and the conditions in the surrounding gas.

2.2 Process Control and Development

Testing of alternative distributors involves both process development and new process control protocols. In addition, there are a number of process tasks that are common to all VTD deposition systems. This section addresses the optimization and control of film thickness.

The use of thinner CdS films is a well-known path to improve device efficiency. During this contract year the production target for CdS thickness has been reduced from 3800 to 1200 Å. This has resulted in a significant gain in efficiency through improved photocurrent. Further reductions in CdS thickness are expected to yield more efficiency gains.

The on-line measurement system for CdS thickness via optical absorption, first developed under the previous Thin Film Partnership contract, was improved. The primary source of noise was found to be absorption from stray particulates in the input optical beam path. Shields and condensation traps were added to eliminate this noise source. In addition, the input laser stability was improved by the addition of temperature control modules and optical feedback. Despite the improvements in the on-line system, output is not reliable enough to incorporate into a simple closed loop control scheme. Thus the system currently monitored by operators.

The cross-web uniformity of VTD films is primarily controlled by the distributor while the consistency of thickness over time (i.e. down-web) is determined largely by the control of input powder feed rate. For thick films, regular feed pulses common to many powder feeders are frequent enough compared to the characteristic time to sublimate that no effect is seen in the deposited film. Effectively the feed pulses are smoothed out in the vaporization section of the distributor. However, for low feed rates needed for thin films the time between powder pulses can be longer than the characteristic sublimation time. For example, Figure 4 shows variations in CdS film thickness due to feeder pulses.

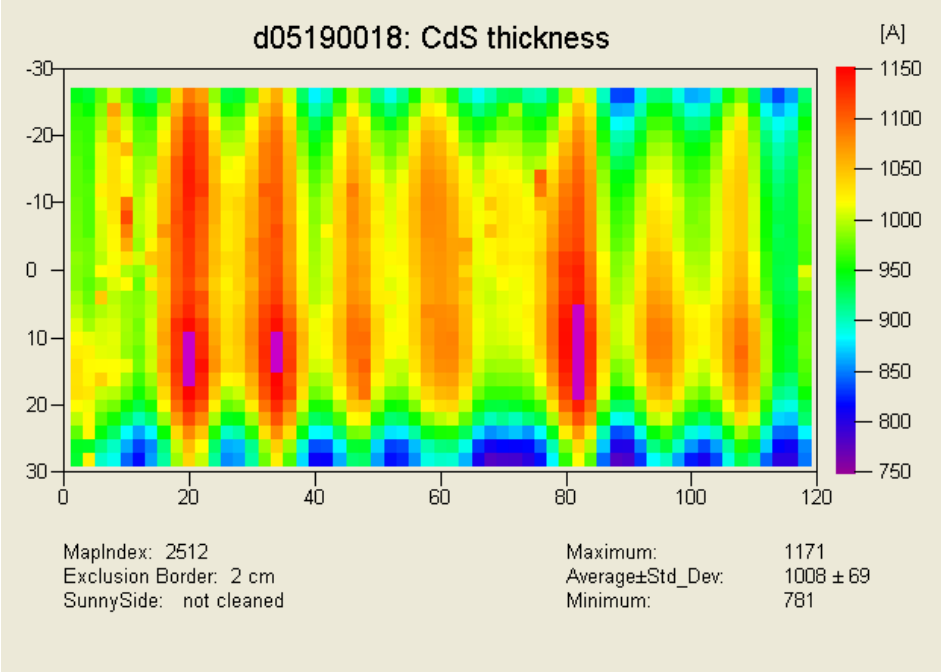


Figure 4. CdS thickness map from a typical film deposited onto a 60 cm x 120 cm substrate using the commercially available powder feeder currently employed in production.

The powder feed rate needed to form CdS films with thickness <1000Å at our production line speed is ~1gm/min. Controlling the powder feed at this level is a formidable task. We have developed a custom powder feeder based on commercial components in order to eliminate feed pulses. Figure 5 illustrates the effectiveness of this equipment. Work continues however to ensure that longer term fluctuations in feed rate can be managed. Several options for in-line monitoring of powder flow are under investigation.

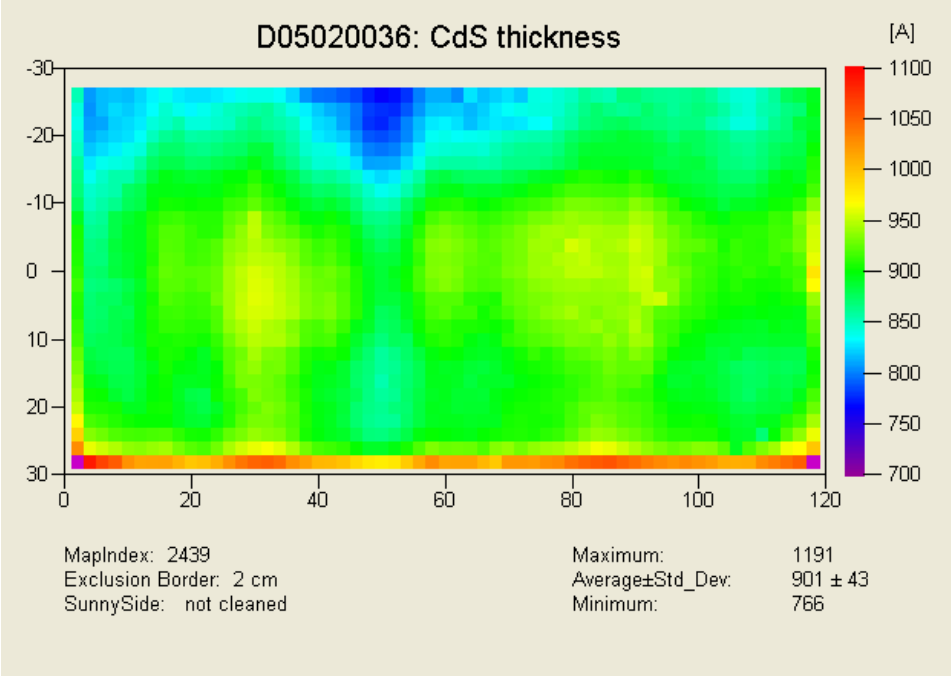


Figure 5. CdS thickness map from a film deposited onto a 60 cm x 120 cm substrate using the alternative powder feeder under development.

Typically we use a target CdTe film thickness ~3.5µm. This value was determined from early experimental optimization. Theoretically no additional optical absorption within CdTe will occur after the first 1 to 1.5µm thickness. Thus we conducted several production scale tests using CdTe films from <2 to 5 µm thick. Some conflicting results were found but essentially based on initial efficiency 2µm thick layers produced similar devices to normal thickness films. More extensive experiments are in progress to determine the behavior of thin absorber devices in accelerated life tests.

2.3 Film Characterization

Film characterization is the essential third component of the development of high-throughput CdS/CdTe deposition reactor. It is also needed to support the work of accelerated life testing described in the next section. Film measurements that have been established previously include automated CdS thickness mapping, automated CdTe roughness mapping, and manual CdTe thickness. Techniques that have been developed or investigated during this contract include time-resolved photoluminescence, bandgap determination via optical reflectance, and automated IV mapping. Many measurement techniques can detect differences in samples but establishing a quantitative correlation to module performance is frequently lacking. As part of the goal to reduce parasitic losses, we have begun working with a group from the University of Toledo on assessing the impact of film non-uniformity.

2.3.1 Optical Reflectance

Optical spectral reflectance of CdTe is a potential parameter to assess large-area film uniformity. The optical reflectance from the front (glass) side of the substrate exhibits a step change as the energy of the probe light is scanned over the CdTe bandgap energy, E_g. An estimate of the CdTe bandgap energy can be found from the inflection point of the step change. We have found consistent differences in bandgap as a function of $CdCl_2$ heat treatment. These are interpreted as shifts due to alloying with CdS. For small samples, a Varian CARY 500 spectrophotometer with an integrating sphere and an enclosed sample chamber is used. In order to map a full size plate, we use a CVI Spectral Products SM-GT2 spectrometer with a spectral range of 1.42 to 1.58 eV. This spectral range includes the fundamental transition of the as-deposited and $CdCl_2$-treated CdTe. The equipment can operate in ordinary room light and spectra are acquired in a few seconds. Figure 6 shows an example of the bandgap energy inferred from optical reflectance data as a function of cross-web position. This data suggests that some alloying (E_g~1.47 eV) has occurred at some locations in as-deposited films.

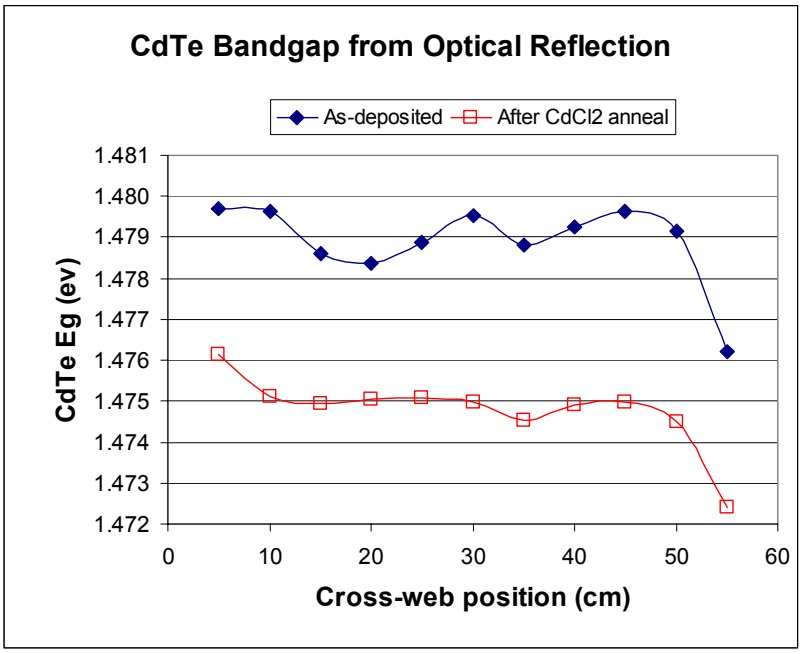


Figure 6. Bandgap energy of CdTe films as a function of cross web position.

2.3.2 Time-Resolved Photoluminescence

Measurements of electronic properties are important in order to analyze CdS and CdTe films deposited and processed under various conditions. Measurement of the excess minority carrier lifetime of CdS and/or CdTe via photoluminescence (PL) decay is an attractive metric as it is non-destructive and does not require a finished device. Recombination dynamics of the excess carriers are influenced by many factors including material quality, purity, band alignment, doping, stress and disorder. For many devices

minority carrier lifetime is expected to directly relate to device performance. The technique is established for Si-based technologies but is not common for thin-film heterostructure PV.

A preliminary evaluation of the excess minority carrier lifetime of CdTe indicated a correlation between device V_{oc} and τ_n of CdTe measured after $CdCl_2$. We thus prepared a set of nominally identical CdS & CdTe samples and varied only the $CdCl_2$ anneal temperature to affect a change in device V_{oc} and PL decay. The lowest anneal temperature resulted in inadequate treatment, and the highest anneal temperature resulted in damaged devices.

For PL decay measurements, the CdTe was excited from the sunny side with a 636 nm light at a repetition rate of 20 MHz and an average excitation power of 0.1 mW. A band pass filter at 850±25 nm was used to suppress background and scattered excitation light. The time-resolved luminescence decay data was fit with a 3-exponential decay model to obtain fast and bulk decay lifetime. Since the excitation was from the CdS/CdTe interface, we expected that the fast decay would be a representative of the quality of the material within the depletion width of CdTe.

Figure 7 shows average dot-cell V_{oc} versus minority carrier lifetime obtained from the PL decay measurements. The device V_{oc} increased monotonically with increasing lifetime for the lower temperature $CdCl_2$ anneals. However, there seems to be an optimum lifetime above which the V_{oc} drops. This set of data suggests that the device V_{oc} is not dominated by minority carrier lifetime limitations. The unexpected behavior was confirmed by measurements from the sister samples at NREL.

In general PL lifetime is useful to investigate factors that relate to recombination dynamics such as impurity density, recombination center density, grain boundary passivation, and electric field strength. The interaction between these factors and the PL decay measurement factors (excitation energy, emission energy, excitation intensity, excitation history and substrate temperature) is complex and is not uniquely correlated with device properties. In other words, the PL decay lifetime did not qualify as a useful metric and we plan no further activity at this time.

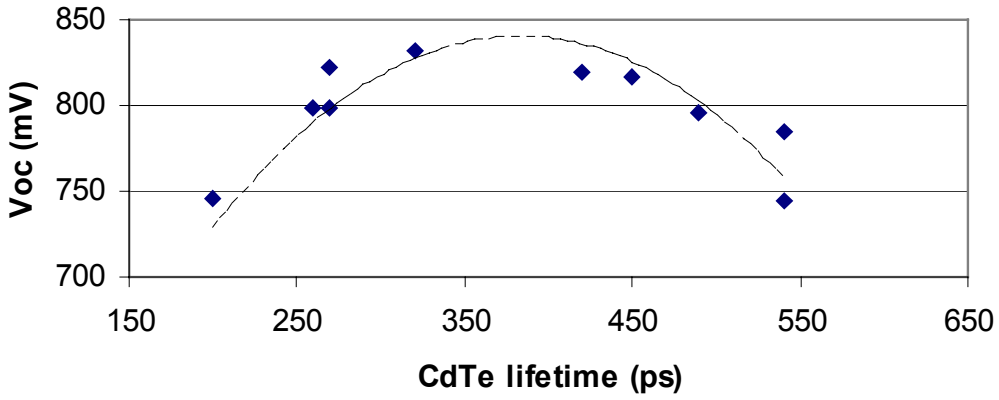


Figure 7. Dot-cell V_{oc} versus excess minority carrier lifetime of CdTe

2.3.3 Expanded Device Measurements

Standard device performance measurements (light IV) constitute the vast majority of all measurements taken. We have occasionally used other techniques including IV as a function of temperature (IVT), quantum efficiency (QE), QE as a function of voltage (QEV), and capacitance voltage (CV). After consultation with CdTe team partners at IEC, CSU, USF, and ALF, we settled on an essential set of measurements that are expected to yield a relatively complete assessment of device operation. The goal of the assessment is to quantify sources of efficiency loss and to relate these to specific process steps. One example would be to quantify macroscopic spatial non-uniformity differences. The essential set includes IVT and QEV. Additional IV measurements as a function of intensity may be included.

From these measurements, we extract parameters that characterize the main junction, the back contact barrier, and voltage dependent current collection. Many devices that have been exposed to extreme stress, made with processing extremes, or failed for various reasons, exhibit very non-ideal device performance. The analysis algorithms for meaningful parameter extraction must be robust, and work continues in this area. For example, Figure 8 shows a device with a significant back contact barrier which was determined to be 0.36 eV in magnitude. Figure 9 shows the QEV characteristics of the same device. This data suggests that red response of the device could be improved. We are beginning to systematically make these measurements and they are expected to provide significant insight for the characterization the deposition and post deposition processes.

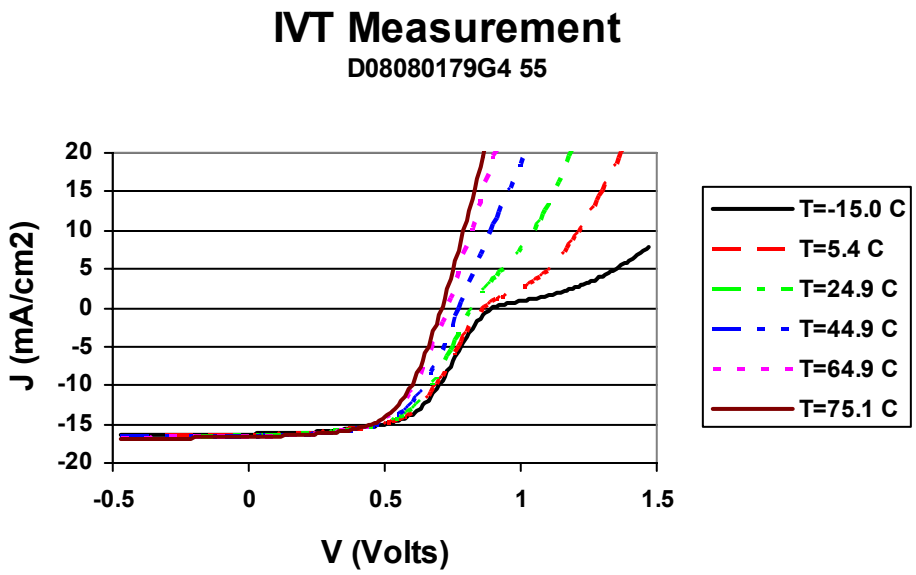


Figure 8. IVT measurement of sample with apparent contact barrier.

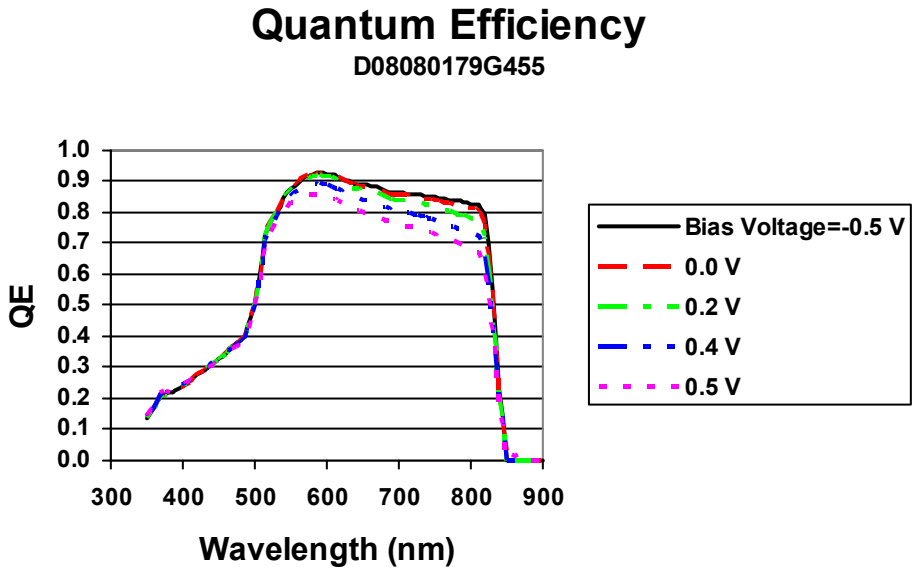


Figure 9. Example of quantum efficiency as a function of bias voltage.

2.3.4 IV Mapping

IV mapping is a powerful technique that can be used to detect variation patterns in processing and locate problem areas during failure analysis. During this contract period, we completed a system to automatically measure small area cells formed from standard

unencapsulated modules. Essentially any unencapsulated module can be divided into small areas by adding additional laser scribes perpendicular to the standard interconnect structure. These so-called interconnect cells ("i-cells") make use of the standard interconnect via that connects the back contact of a cell to the front contact of a neighboring cell. Consequently pogo pin contactors can be used to probe any cell on the plate. Figure 10 shows an example output from this system. Since full IV curves are taken at each point, summary maps of any of the standard IV parameters can be obtained.

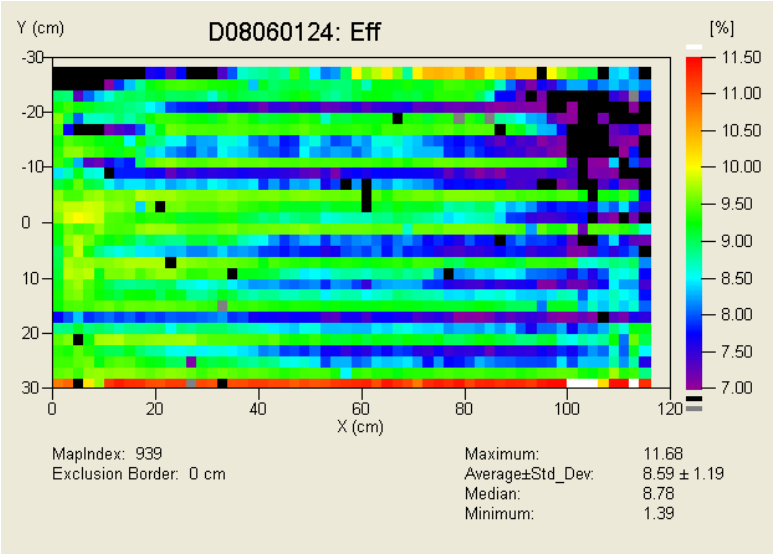


Figure 10. Example IV map from a module that failed light soak testing. In this case every 4th cell was measured.

2.3.5 Non-uniformity loss estimates

In principle, one should be able to reconstruct the full module performance characteristics given the IV mapping data. Once the numerical reconstruction methodology has been verified, it can be used to quantitatively assess the impact of various types of non-uniformity. Moreover, working together the mapping and reconstruction techniques should also be able to assess the impact on non-uniformity on stability. Thus we have begun a project working with a group at the University of Toledo to develop the numeric reconstruction tools.

3. Accelerated Life Testing Development

Stable, predictable performance of PV modules is essential for achievement of cost-effective solar electric fields. This requires the development of predictive accelerated life testing (ALT) protocols and increased understanding of mechanisms of stress-induced changes in devices.

3.1 Development of predictive ALT Protocols

First Solar has done considerable research on accelerated life and field testing of CdTe thin-film PV both independently and in cooperation with other CdTe National Team members. Potential failure modes for thin-film PV are generally thought to be associated with loss of encapsulation integrity or exposure to some combination of light, heat, bias, and time. In the present ALT protocol we focus on the changes due to exposure to combinations of light, heat, bias, and time.

Previous work has primarily been directed toward the validation of reasonable field performance and the correlation between existing light soak procedure (continuous exposure, ~0.7 sun intensity, open circuit bias, ~65ºC for 56 days) and field performance. This approach has a number of deficiencies including the time, space and power needed to conduct the light soak tests, the relatively few measurements obtained during the test, and the lack of predictive capability. The length of the light soak protocol necessarily limits the number of samples that can be tested and thus many conclusions are drawn from an insufficient population sampling. Moreover in the duration of the test the performance of many samples does not approach an asymptote which further complicates analysis. In addition the current light soak system has poor temperature control over the long duration.

Previously we presented data which showed some correlation (with an acceleration factor of ~60) between performance of cells in elevated-temperature, open-circuit light soak and performance of modules in the field [3]. While this correlation was taken as an indication that light soak is a legitimate ALT, large scatter in the data and known problems about the data prevented the result from being quantitative or definitive. Known problems include poorly paired field and laboratory samples and field data that was not corrected for time and temperature in the field.

Consequently we have split ALT development into two stages. The first step is to establish a test that would reliably give the same prediction the existing 56 day protocol, except faster and more consistent. The second step is to select a rapid test protocol that has good correlation to field performance. Presumably the rapid, field-correlated protocol will be similar to the first rapid test, but may have different applied stresses. To perform this work, we have set aside laboratory samples that are paired with modules that have been field deployed.

The ALT apparatus includes a Xe light source and electronics for measuring 16 isolated by laser scribe devices (i-cells) simultaneously in the temperature range between 40º and 135ºC with applied bias in the range from -2 to +2 Volts. I-V data sets are recorded continuously during the stressing at temperature. The key to accelerate degradation processes is testing at elevated temperature with continuous monitoring of the data.

In order to correlate the existing light soak procedure with a new ALT protocol, several modules from different batches were cut in half and the first half was light soaked using current procedure while the second half was used to make set of coupons. Each of the coupons has at least 16 small area devices (~1 cm^2) for ALT. To resolve issue of the spatial difference in degradation and performance, coupons were taken from several locations across the half-module.

Characteristic decay of the efficiency during ALT and corresponding exponential decay fits are presented on the Figure 11 for cells stressed at 125ºC and open circuit (OC) for 3 days. The frequently sampled data allows one to reliably fit an analytic form to the data. Typically the fit used is an exponential decay to an asymptotic (saturation) value. The value of the asymptote is used to summarize the data. The distribution of saturation values from small area cells tested at high temperature is used to compare to data from interconnected modules.

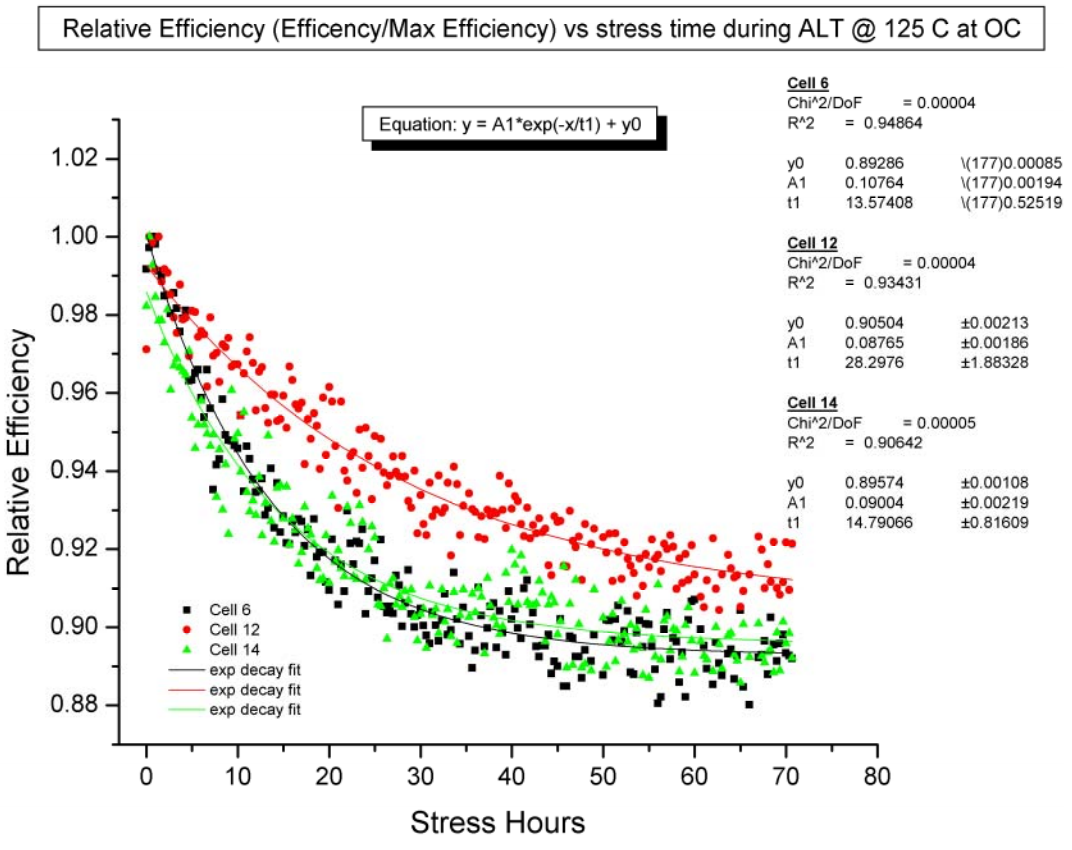


Figure 11. Characteristic decay of the relative efficiency during ALT and exponential fits.

Light soak testing of modules consists of exposure to continuous illumination at ~65ºC under OC conditions for 56 days. Modules are removed from the stress and their performance tested every 7 days. Again the data is fit to an exponential decay with an asymptotic value form. The saturation value of the module data from standard light soak is then compared to the distribution of saturation values found in the high temperature ALT test for small cells. Figure 12 shows an example of this comparison. In this case, the saturated module efficiency extracted was 0.957 of the maximum value during the test while the distribution median for the high temperature small area cells was 0.94.

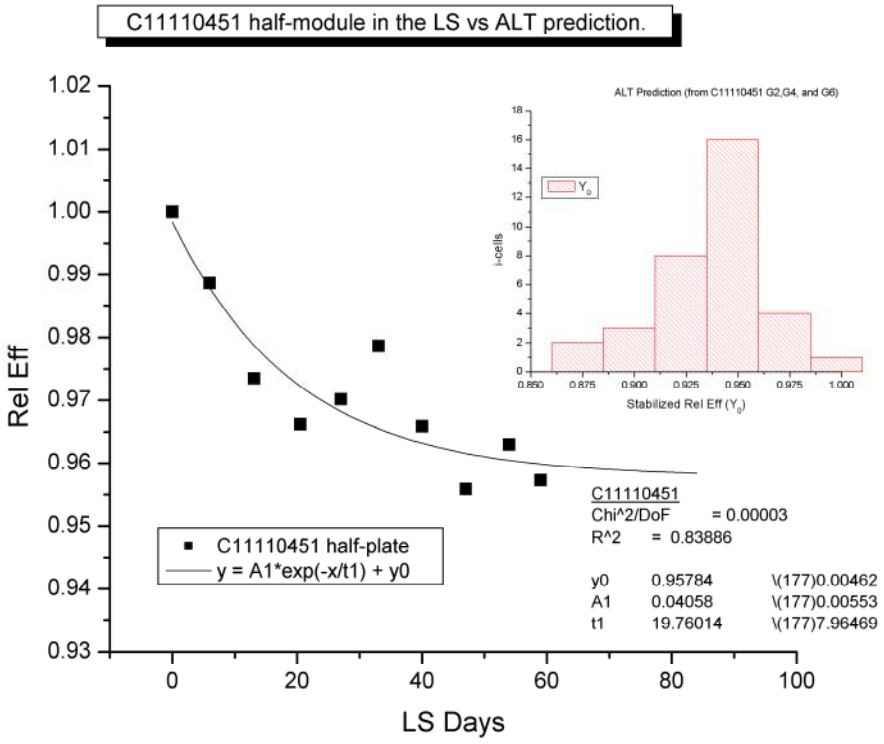


Figure 12. Current light soak vs. ALT prediction comparison for the same module

The correlation between the existing light soak procedure and the new ALT protocol is presented in the Figure 13. While more data is clearly needed, the new ALT protocol appears promising and suggests that a high temperature 3 day test could replace the current 56 day test.

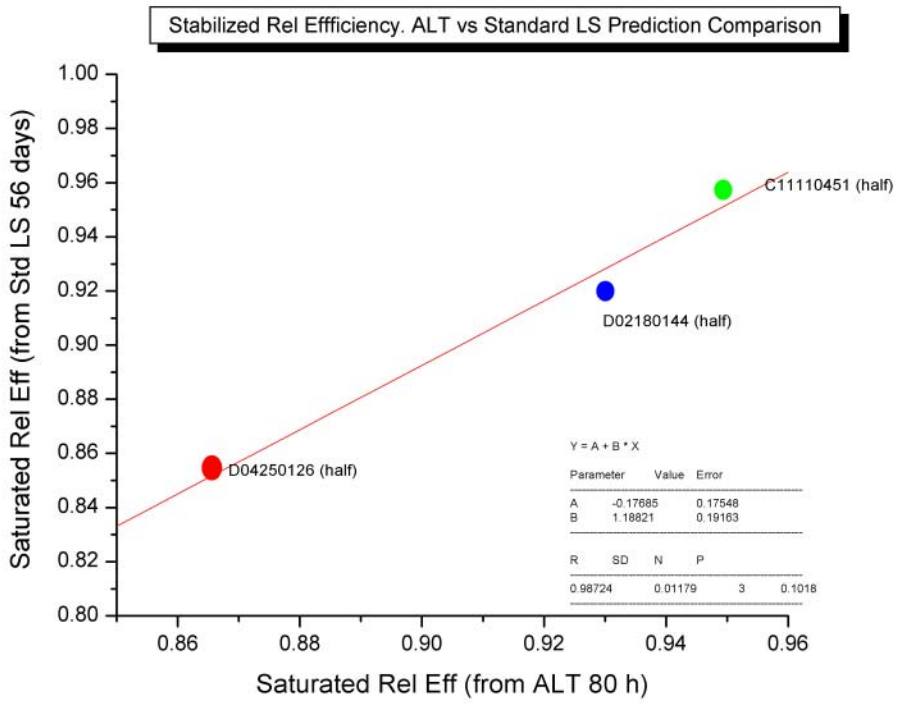


Figure 13. Current light soak procedure prediction vs. ALT prediction for the saturated efficiency value.

In addition to the current ALT analysis procedure as described above, we estimated an activation energy for the degradation process for different devices, which can be used to relate to different failure mechanisms [4]. As an example, Figure 14 shows activation energy obtained for three devices from the same module. In this case voltage bias was applied in cyclic manner with different frequencies as denoted on the graph. An arbitrary power loss point of 10% was chosen and the time for each sample to reach this loss point was calculated from the fit equation.

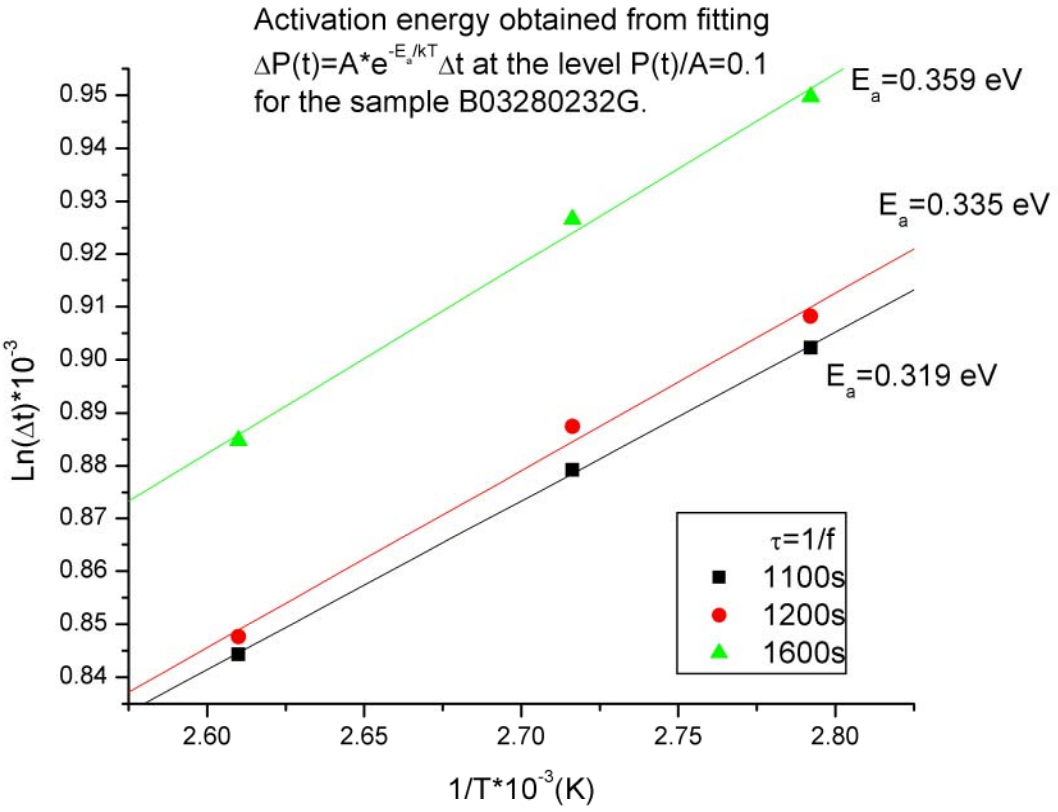


Figure 14. Activation energy estimates from temperature dependence of cyclic bias stress samples.

3.2 Stress-Induced Change Mechanisms

Ideally the identification and understanding of the mechanisms leading to device degradation would allow the development of a mitigation program and thus would be an important step for improving the long-term performance of CdTe thin film modules. Understanding the change mechanisms should provide concepts for tailoring materials properties in order to influence the stress-induced response in the electrical device performance. Many mechanisms are possible in polycrystalline compound semiconductor thin films and techniques for measuring many important properties are lacking. Consequently the process of understanding is quite complex. Our working hypothesis is that, apart from encapsulation failure, module performance is largely determined by cell performance. Cell performance in turn depends on the defect distribution within the device. Defects concentrations are affected by the local quasi-Fermi level (i.e. the chemical potential). Changes in quasi-Fermi due to bias or illumination result in a redistribution of defects. The redistribution can include defect mutation, defect migration, and defect occupancy. The defect redistribution in turn changes the quasi-Fermi level. This framework provides a conceptual understanding of

how current device performance depends on the totality of the device history. Our approach to unravel the observed behavior has been divided into several steps:

- monitoring the electrical response of devices during stressing and identification of the most obvious changes in device performances
- analyzing changes in the defect chemistry of CdS and CdTe due to stress induced material changes
- modeling of the defect chemistry in CdTe and device modeling considering different stress induced defect levels
- modifying the material properties of CdTe and identifying the defect chemistry
- improving the back-contact chemistry
- demonstrating improved long-term stability of modified devices

3.2.1 Monitoring of the electrical response of stressed devices

While we have stressed and monitored devices repeatedly in the past, a complete data set for current vintage devices was needed. For this purpose we made a set of dot cells and exposed them to bias and elevated temperature. Two different illumination levels (dark, 0.7 sun) and three temperature levels (65ºC, 90ºC, 115ºC) were chosen for the stress experiment. For each of those six combinations, twelve different bias conditions including open and short circuit conditions as well as forward and reverse bias were considered. For consistency three individual dot cells were stressed under each of the specific conditions. After 28 days of stressing, the recovery behavior under OC conditions (light/dark) was also investigated.

The most obvious losses in efficiency η, open circuit voltage V_{OC}, short circuit current J_{SC} and Fill Factor FF were observed for devices stressed under reverse bias. These devices recover partially under OC conditions, but show significant permanent changes in PV-performance. In some case the development of a "roll over" in the IV-curves is observed. Slight changes in all parameters could be identified for devices stressed under OC conditions.

3.2.2 Analysis of degraded devices

For specific analysis of material changes concurrent with changes in PV-performance, we focused on two stress conditions: -2V and OC under illumination at 90ºC. In order to identify the pathway of changes within the semiconductor material itself, we examined and compared samples taken from different stages of device degradation using various analytical methods. Standard characterization of stressed devices included IV, quantum efficiency (QE) and capacitance-voltage (CV) measurements.

Further investigations on stressed dot cell devices were performed on a series of devices showing "low efficiency" accompanied by "slow degradation" and on a series showing "high efficiency" accompanied by "fast degradation".

cell	stress light, 90°C	recovery dark, 25°C	η %	V_{OC} mV	J_{SC} mA/cm^2	FF	R_{OC} Ω–cm^2	R_{SC} Ω–cm^2	J_{maxp} mA/cm^2	V_{maxp} mV
1	OC, 12 h	no	9.56	716	19.81	67.39	5.98	1154	17.76	538
1	OC, 7 days	no	9.21	727	19.79	63.98	7.44	1461	17.39	529
2	OC, 12 h	no	9.86	706	20.67	67.61	5.59	1836	18.74	526
2	-2V, 7 days	no	3.25	656	19.67	25.17	28.22	74	9.77	332
2	-2V, 7 days	1 day	3.48	650	19.40	27.59	24.42	70	10.03	347
2	-2V, 7 days	7 days	4.03	653	19.48	31.70	18.91	112	10.81	373
2	-2V, 7 days	20 days	4.50	671	19.58	34.23	17.49	278	10.92	412
2	-2V, 7 days	36 days	4.73	673	19.87	35.36	16.63	166	12.00	394

Table 1. Representative device performance of dot-cells under stress and recovery

Stressing at OC conditions indicates a slow, but obvious tendency for deterioration of significant PV-parameters. Devices stressed under reverse bias exhibit a tremendous drop in performance that seems to saturate with time and temperature (see Table 1). These devices partially recover with storage under OC conditions in the dark at 25ºC after removal from the external bias stress. This stress/recovery behavior suggests that some of the degradation mechanisms that work in parallel may initiate irreversible changes in materials properties.

Photoluminescence (PL) measurements (supported by University of Toledo) were used to detect native defects and impurity related states within the band gap of the CdTe absorber material. This method is particularly suited for the identification of shallow trap levels but can be applied to certain deep traps, provided that the recombination is radiative. A rough comparison of the photoluminescence spectra obtained for an unstressed and a sample of the "low efficiency series" stressed for 6 days under –2V reverse bias shows the development of a feature around 1.5 eV (see Figure 15). This PL-feature disappears during device recovery under OC conditions in the dark and is believed to be a donor-acceptor pair (DAP) presumably related to an impurity introduced during device processing. The DAP PL feature is not observed for devices stressed under OC conditions and illumination. Radiative recombination at this DAP presumably is correlated to a defect equilibrium which is shifted while exposed to biasing. The defect equilibrium returns to a state similar to the original when the bias stress is removed. However the device performance does not fully recover. Thus the 1.5 eV DAP PL signature is not a complete degradation marker. While the DAP may be involved in the significant deterioration of the PV-performance, other degradation mechanisms must be operating in parallel.

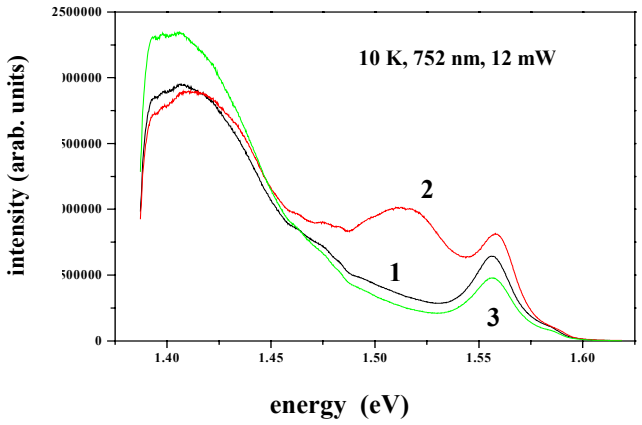


Figure 15. PL spectra of a "low-efficiency" device. 1) unstressed device, 2) device stressed at –2V, 90ºC, light for 6d, and 3) device stressed at –2V, 90ºC, light for 6d; recovery: OC, 25ºC, dark for 6d.

PL measurements were also performed on samples of the "high efficiency series" (at University of Toledo). A preliminary interpretation suggests that the luminescent centers that radiate at around 1.55 eV are associated with donor-acceptor pairs involving Cd-vacancies as acceptors. These defects (V_{Cd}) interact with extrinsic impurities to form defect-complexes whose occupancy and concentration may change due to stressing that shifts the local defect equilibria. Recovery is understood as a relaxation to the original defect species that occurs when the local equilibria return to their non-stressed values. In addition, defect migration may contribute to irreversible degradation phenomena. Compared to the PL-spectra taken from "low efficiency" devices, "high efficiency" devices do not exhibit major PL peaks within the "DAP-region". Differences between the two cases may be associated with the effect on the defect spectra attributable to differences in the $CdTe_xS_{1-x}$ intermixing region of the two sets of devices. In any case, PL-spectra seem to be very sensitive indicators of material changes that correlate with degradation phenomena.

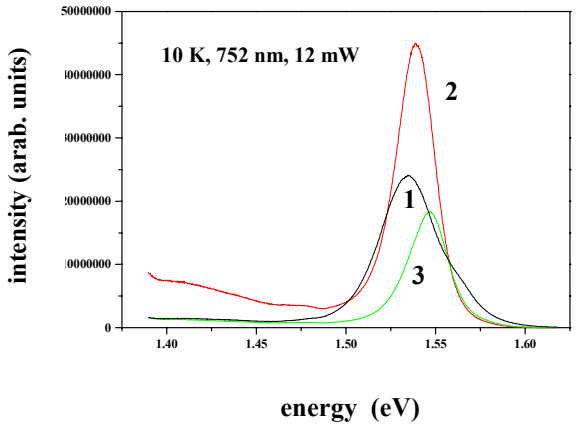


Figure 16. PL spectra of a "high-efficiency" device. 1) unstressed device, 2) device stressed at –2V, 90ºC, light for 7d, and 3) device stressed at –2V, 90ºC, light for 7d; recovery: OC, 25ºC, dark for 5d.

Deep level capacitance profiling (DLCP) (supported by CSM) allows probing the energy and concentration of traps at the point where the Fermi-level crosses the trap energy. First measurements on the "low efficiency series" suggest that a defect level at ~E_V+0.6 eV and a level at ~E_V+0.4 eV are dominating the overall defect chemistry of CdTe during stressing. In general, a decrease in the defect state density is observed for devices stressed under –2 V reverse bias while devices stressed under OC conditions seem to achieve an increase of the defect state density. This counter-intuitive result indicates that DLCP measurements do not provide a simple device degradation marker.

3.2.3 Device modeling

We provided IV, QE, and CV from the "low" and the "high" efficiency sample sets to a sub-group of the National CdTe Team for modeling and interpretation. Device modeling of selected devices was performed by Alan Fahrenbruch. SCAPS was first used to attempt to simulate the CV-data observed for stressed low efficiency devices [5]. The experimental data converted to apparent net hole density vs. depletion width using a simple abrupt junction model is shown in Figure 17. A simulation sequence is presented in Figure 18. The simulations produce CV data which is then converted to apparent net hole density vs. depletion width using the same simple abrupt junction model. The sequence includes the case of a constant shallow hole density, the addition of neutral or donor-like recombination centers, and the addition of a back-contact barrier of 0.5eV. The addition of the back barrier leads to a minimum in the apparent carrier concentration vs. depletion width in both the dark and the illuminated curves. This is in qualitative agreement with the experimental data (Figure 17) and clearly questions the simple conversion of CV data to apparent hole concentration.

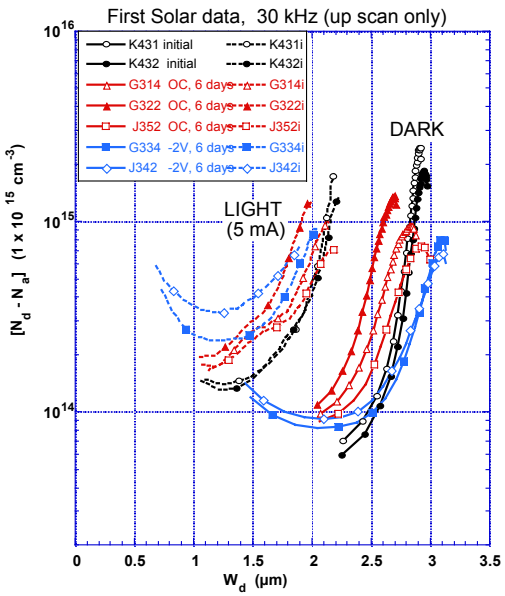


Figure 17. Apparent net hole density vs. depletion layer width in First Solar cells stressed as indicated in legend.

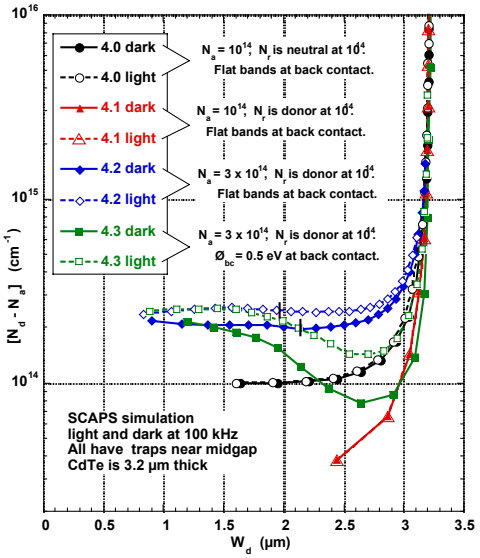
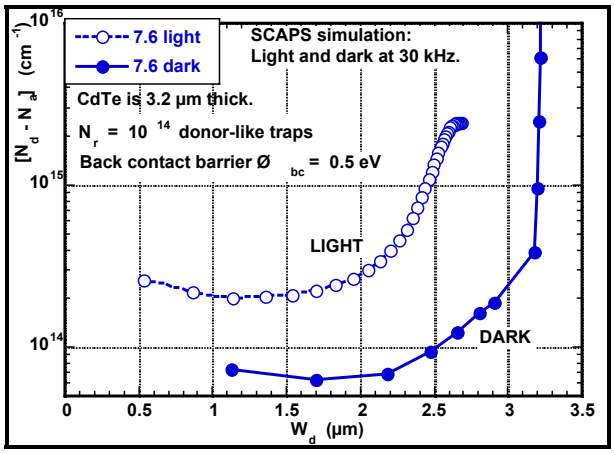


Figure 18. SCAPS simulation of simple CdS/CdTe device with constant doping. (from Alan Fahrenbruch)

For a refined model, a higher doped CdTe sub-layer (1 μm) adjacent to the back-contact was introduced (Figure 19). In the dark the quasi-Fermi level of the electrons is below the donor levels and the donor states are positively charged, thus compensating the net hole density. In the light, the net hole density is raised, but also the electron Fermi level is above the donor levels and many donors have a neutral charge. Thus, the apparent

(electrical) end of the cell shifts from nominal 3.2 µm towards 2 µm. This shift is in qualitative agreement with the experimental results.



	CdTe Layer 1	CdTe Layer 2 (next to back contact)	
Thickness	2.6	1	µm
N_a (shallow)	2 x 10 ^{14}	4 x 10 ^{15}	cm^{-3}
N_r	1 x 10 ^{14}	1.9 x 10 ^{15}	cm^{-3}
E_r	0.75	0.75	eV
σ_n	1 x 10 $^{-12}$	1 x 10 $^{-12}$	cm^2
σ_p	1 x 10 $^{-18}$	1 x 10 $^{-18}$	cm^2

Figure 19. Simulation of model with two CdTe layers. Light intensity gives J_{sc} of ~5mA/cm^2. (from Alan Fahrenbruch)

3.2.4 Investigation of material changes due to impurity ingress

QE measurements performed on devices stressed under reverse bias suggest changes in CdS photoconductivity. It is known from the literature that CdS generally acts as a "sink" for impurities and thus impurity accumulation in CdS under reverse bias stress is possible. Therefore, we treated polycrystalline CdS layers with different impurities present during device processing and analyzed the films with PL and XPS (both supported by NREL). CdS films were annealed both with and without $CdCl_2$ flux.

For annealed samples without intentional impurities, we observed a PL emission at ~2.39 eV, which is believed to be caused by a transition from Cd_i or V_S to the valence band. This feature increases in intensity in $CdCl_2$ annealed samples. The addition of impurities from other device layers, which are known to in-diffuse, did not lead to additional PL emission features. The formation of impurity sulfides at dangling S-bonds on the CdS grain surfaces is plausible. However, XPS measurements did not give any indication for the precipitation of impurity sulfides.

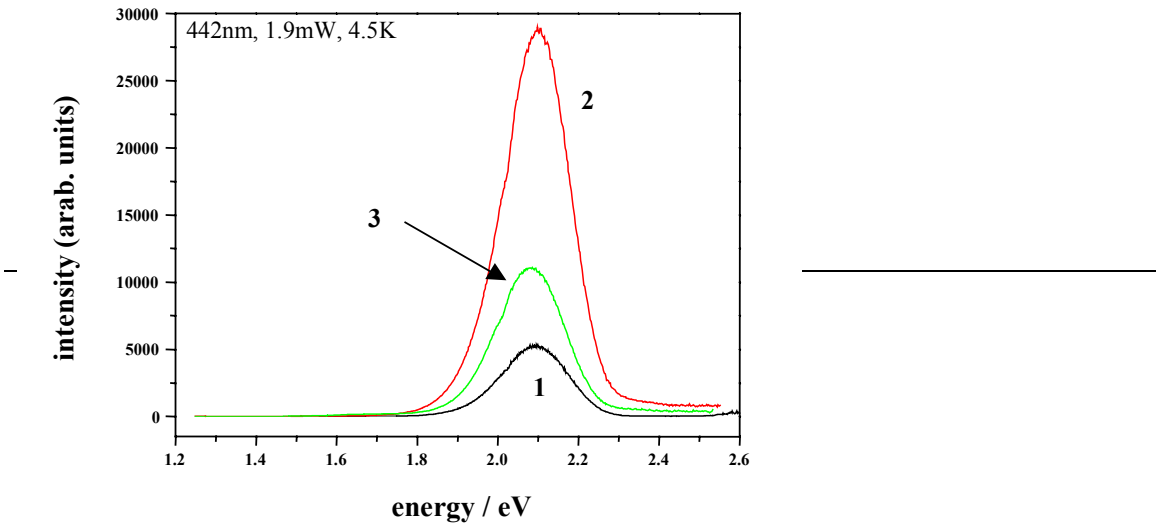


Figure 20. PL spectra of CdS 1) as grown, 2) air annealing 400°C, 45 min, 3) $CdCl_2$ treatment 395°C, 20 min

3.2.5 Identification and modification of back-contact chemistry

As the back-contact area is assumed to be a major source for "degradation", controlling back-contact chemistry during device processing is one of the key factors in achieving long-term stability of high efficiency devices. XRD-measurements (supported by NREL) along the multi-layer back-contact stack were performed. The samples were annealed at temperatures up to 100ºC greater than our normal post-metal heat treatment (PMHT) temperature and for longer times. From the phase diagram of metals involved, the formation and precipitation of stable alloys was expected. However no alloying was detected with XRD. Either an inter-diffusion zone providing the necessary stoichiometry for alloy formation was not created or the kinetic barrier for any solid state reaction has not been surmounted. Thus we consider the back-contact electrode as an impurity source but unwanted phase formation that could be a source of degradation is unlikely.

Surface preparation prior to back-contact application can impact initial and long-term performance of devices. The chemical properties are determined by the thermo-chemical history of CdTe especially the $CdCl_2$ activation step. XRD-measurements performed at different stages of the CdTe post-deposition processing indicate the presence of CdO and $CdTeO_3$ as main surface reaction products during the $CdCl_2$-activation step, where the relative quantities depend on the relative concentrations of $CdCl_2$ and O_2 during annealing. Presumably these residues exist as surface layers. Contact wetting angle measurements (supported by IEC) indicate that $CdCl_2$-activation raises the surface energy compared to as-deposited CdTe.

Major emphasis has been focused on understanding the formation and removal of surface species such as oxides and oxy-chlorides stemming from $CdCl_2$ processing (supported by IEC). In addition, the humidity level of the ambient can change the oxide formation. CdTe annealed at 550°C and 600°C in dry or humid air without $CdCl_2$ exhibits $CdTeO_3$ as a dominating surface oxide. In this case a weak time and moisture dependence was found. Vapor $CdCl_2$ treatment in dry air leads to CdO between $CdTeO_3$. Increasing the humidity, the appearance of $CdTe_2O_5$ between $CdTeO_3$ was observed; no indication for CdO was found. Samples pulled from different $CdCl_2$ manufacturing runs processed under seasonal different humidity levels suggest a slightly altered surface chemistry. Further studies will be carried out if these differences can be attributed to variations in the plant humidity or may have its roots in variations of other processing parameters. However, dot-cell devices, which were exposed to different humidity levels during $CdCl_2$ activation show overall similar values of the PV parameters. The difference in efficiency is not significant for both humidity levels, but marginally lower for a humid $CdCl_2$ treatment compared to the standard $CdCl_2$ process. A slight increase in R_{OC} and a decrease in FF for devices activated under humid conditions are observed.

Ideally the various oxides that form during the $CdCl_2$ activation step should be removed to ensure consistent back-contact formation. Acidic-oxidizing etches are not compatible with our back-contact process, so various alkaline etches were investigated. Different etch times and concentrations were employed to remove surface oxides and oxy-chlorides. For the treatments investigated, neither initial nor long term PV performance was significantly altered compared to non-treated devices. Grazing incidence XRD (GI-XRD) (supported by IEC) measurements indicate that, for the etch investigated, some oxide species are removed but other species remain. Thus this improvement pathway still holds some promise and further studies of surface treatment before back-contact application are underway.

4. Environmental, Health and Safety Improvements

First Solar is committed to producing a safe product and operating a safe factory. Thus Environmental, Health, and Safety (EH&S) programs are a top priority. Large scale manufacturing of CdTe-based photovoltaic modules involves handling a significant amount of material that contains cadmium. Two pathways must be managed: airborne dust and solid waste.

Airborne dust can be generated from the CdTe film coating and film annealing operations as well as processing steps where material is removed, for example, laser scribing for interconnects and module perimeter creation prior to encapsulation. Current emission levels are significantly below OSHA Permissible Exposure Limits, but as production volume increases, improved methods for identifying and capturing dusts are needed.

Solid waste is generated from the coating operation, from module handling during manufacture, from the disposal of broken or scrapped modules, and from waste water treatment. Previously most waste was disposed as a hazardous waste.

In addition maintaining a safe operation environment requires proactive employee training program as well as ongoing verification of the current Industrial Hygiene methodology.

4.1 Dust Emissions

Dust emissions within the factory are primarily controlled using high-efficiency particle air (HEPA) filters. The quality of the filters and the installation method determine the actual effectiveness of operating filters. Several programs are underway to verify the operation of HEPA filters.

First, a HEPA filter testing apparatus has been designed and built to evaluate the effectiveness of HEPA filtration and to evaluate the quality of different vendor's filters (see Figure 21). Intentional injection of known particulates to "challenge" the filter is used. An ARTI airborne particle counter is the primary sensor used. Testing is underway to determine the proper aerosol challenge including particulate size, particulate material, and concentration for accurate HEPA filter testing. As a baseline, documented standards for the HEPA testing in the nuclear industry will be used.

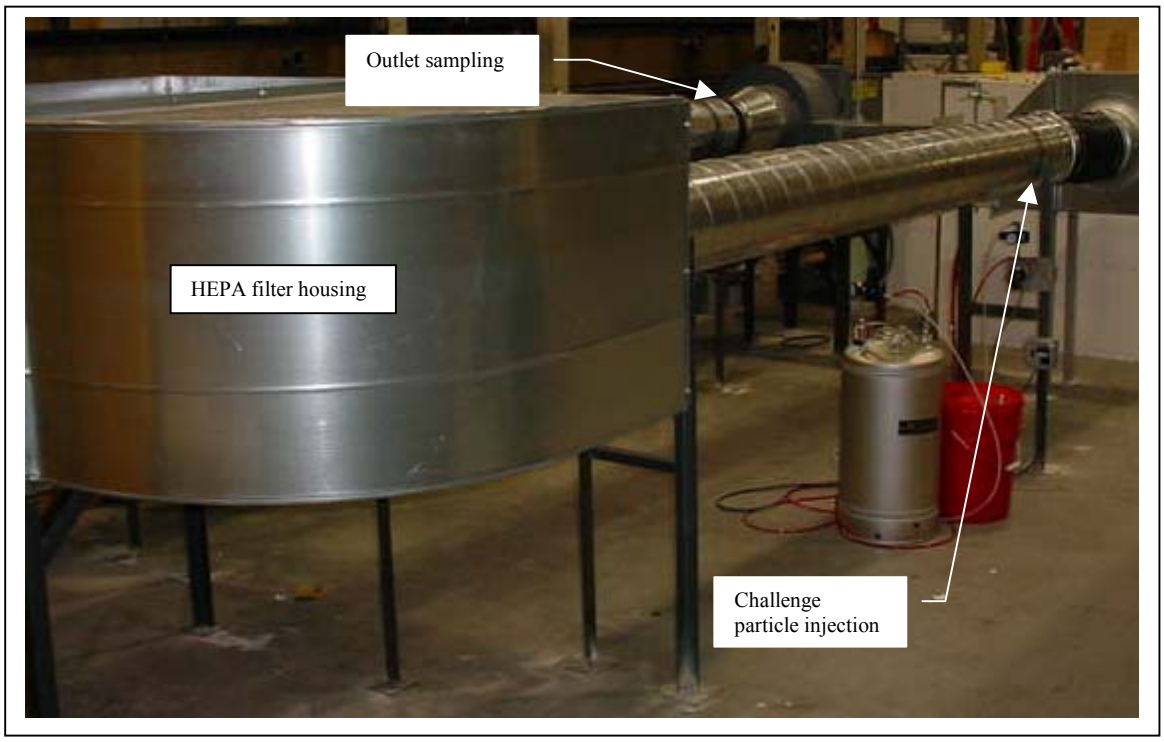


Figure 21. HEPA filter test apparatus.

Development of an operational test for installed filters is also underway. Using UV fluorescent tracer particles introduced via an aerosol generator, detection of HEPA leaks may be possible with black light illumination. Direct visual observation, microscopic observation on capture samples, and specialized vision cameras are planned detection methods. Initial data indicates that the fluorescent particles on capture samples can be viewed under a microscope.

First Solar also attended a HEPA filter Workshop at Harvard's School of Public Health. This program provided educational lectures and hands on experience in testing HEPA filters.

4.2 Recycling

Over the past year, First Solar has made significant progress toward developing methods for recycling solar modules and reducing hazardous waste. Four examples follow.

4.2.1 Module Recycling

For broken and scrap modules, we had previously developed a process in which the modules are first crushed into glass cullet. The semi-conductor, back electrode, and bus bars are dissolved into solution and reformed into a solid, filter cake material. The clean glass cullet is shipped off site to a facility where the glass is reprocessed. Previously the filter cake was disposed as hazardous waste. We have investigated a number of recycling options for both whole modules and filter cake.

We have now begun to work with company that can recycle our filter cake. This company blends our filter cake with waste from other sources and returns it to an input stream of a smelting operation. Since May 2003, over 14,000 pounds of filter cake waste has been recycled in this manner rather than disposed. Thus we have now established a true recycling process for all of the metal components and glass cullet generated from scrap module within the manufacturing operation.

Currently the filter cake contains both Cd and Te. Recycling the filter cake would be more economic if these major constituents could be separated into two enriched filter cakes. A 2-step selective precipitation process has been demonstrated in the laboratory previously. Further development of this process is underway for use in our recycling operation.

Two additional companies for recycling whole modules have been identified and pilot scale tests are in progress. If the pilot tests are successful, processing scrap modules into filter cake could be eliminated at our facility.

4.2.2 Recycling of bulk CdS/CdTe

Another waste stream, bulk cadmium sulfide and cadmium telluride material that is deposited onto chamber walls and transport rollers during the deposition process has been evaluated by a CdTe manufacturer. Testing has been confirmed that this material can be recycled and negotiations are currently underway to complete this process.

4.2.3 Personal protective equipment disposal

First Solar employees wear personal protection equipment, PPE, including Kevlar gloves, arm guards, and aprons when handling glass substrates (modules). This protective equipment becomes soiled with material that potentially contains Cd. Previously the

soiled protective fabrics were disposed as hazardous waste. We have now contracted with a supplier of uniforms, CINTAS, to laundering the fabrics. CINTAS treats the wash water and thus does not discharge Cd. The laundering process saves significant purchase expense of protective equipment and reduces hazardous waste disposal. In the first 4 months of operation, as savings of $6000 has been realized.

4.2.4 Reduction of Cd leaching risk

The designation of a hazardous solid waste depends in part on what might leach into the ground water from a product disposed in an unregulated landfill. The risk of ground water contamination is estimated using various leaching protocols. Some Cd leaching from CdTe based modules can occur depending on sample preparation and leaching conditions. The exact designation of CdTe based modules as a hazardous waste has not been determined and depends on prevailing regulations. However, we have begun to explore a concept of chemical stabilization of the Cd within the module to reduce leaching risk.

The addition of agent to bind Cd into an insoluble form has been developed for Ni-Cd batteries [6]. Such an agent could be incorporated into a module as a layer within the encapsulated structure or in an external package that would release whenever the module itself was broken.

For the initial concept test, three agents known to reduce the solubility of Cd, iron sulfide, (FeS), sodium borohydride ($NaBH_4$), and starch xanthate (ISX) were tried. A common precipitating agent $FeCl_3$ was also tested. These agents were added directly to the extracting solution. The extracting solution used was that designated in the Environmental Protection Agency's Toxic Leachate Protocol (TCLP) test. This extracting solution contains acetic acid and NaOH. The exploratory tests conducted differ from the TCLP protocol in that samples were crushed to a much smaller size (x mm compared to the <9.5mm specified in the TCLP test) and a different mechanical agitation was used. The tests conducted were significantly more aggressive than the actual TCLP test due primarily to the small crushed particles included and the fact that the crushing method causes complete delamination of encapsulated package. The leaching test was conducted for 24 hours.

ISX was found to be difficult to handle and did not produce significant consistent reductions in the cadmium levels found in the tests.

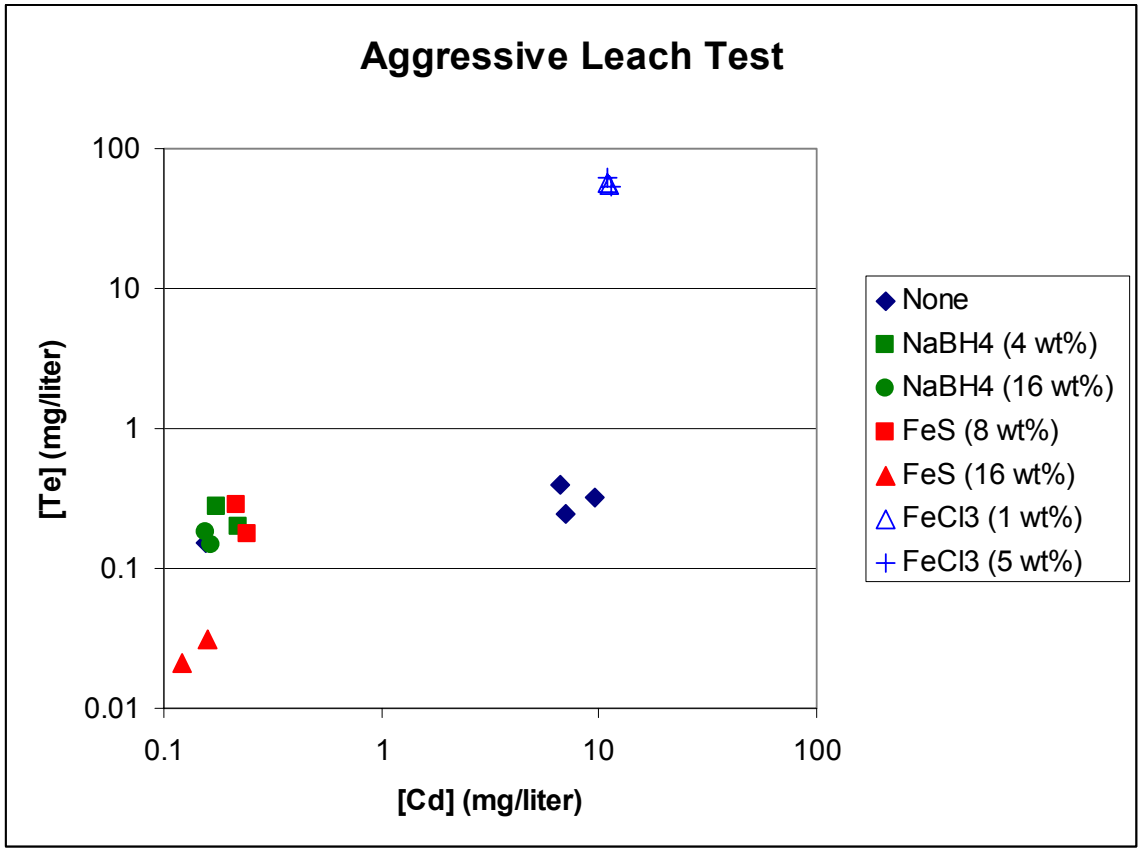


Figure 22. Aggressive Leach Test

Figure 22 shows that the addition of FeS or $NaBH_4$ to the extraction solution reduces the soluble Cd concentration to less than 10% of the values obtained when no stabilization agent is used. Although this test was aggressive, Cd concentrations well below the current regulatory level of 1 mg/l were found with the use of binding agents. Thus this pathway to mitigate Cd leaching appears promising.

4.3 Training

Training is a key element of operating a safe workplace. We have converted our new employee training materials into an electronic format that is easier to manage. These training materials including *Hazard Communication, Cadmium Compliance, Lockout Tagout*, and *Forklift Operation*, are used in a full day session. We have also added three new safety training programs: *Radiation Quality Assurance Plan* (required for Scanning Electronic Microscope operation), *Department of Transportation Awareness Training* (for personnel who ship and receive or handle hazardous materials), and *Department of Transportation Function Specific Training* (for the employees responsible for labeling and signing manifest for hazardous waste disposals).

We are also working to create a training film for new employee and for the required annual training sessions for all employees. This will allow for a more visual retention of the material. Currently a video using florescent particles and a black light to show how particulate matter travels through the air is being developed. Particulate matter is a significant part of First Solar training program due to the use of cadmium compounds. This training film will be complete by January 2004.

4.4 Industrial Hygiene Program Validation

We are currently working with Occupational Health and Industrial Hygiene personnel from the Medical College of Ohio (MCO) for cadmium air and medical sampling verification. At our request, MCO is statistically analyzing all of the industrial hygiene air sampling data generated at the First Solar Cedar Park facility between 2000 and 2003. The purpose of this study is to have a third party verify the sampling data and to make recommendations for future sampling plans.

5. Future Plans

First Solar is committed to commercializing CdTe-based thin film photovoltaics. This commercialization effort includes a major addition of floor space and equipment as well as process improvements to achieve higher efficiency and greater durability. The following activities are planned for phase II of this subcontract.

Work on the deposition reactor will include 1) start-up of a new production coating line, 2) continued work on VTD-2 type distributors, 3) investigation of film nucleation and microstructure control, 4) exploration of CdS powder flow detectors, 5) implementation of more reliable CdS powder feeder, and 6) integration of flow modeling components to include powder sublimation

Work on measurement systems will include 1) improvements to the IVT and QEV hardware and increased sophistication of analysis algorithms, 2) verification of the use and implementation of bandgap mapping system, 3) completion of software and methodology to quantify of non-uniformity losses

For ALT development work we plan to correlate a rapid, continuously-monitored, high temperature ALT test with the current 56 day protocol. We will also begin to correlate this test with field data. While we firmly believe that fundamental understanding of material changes is very important, we plan to revert to a more of an empirical approach to understanding stress induced changes. This is primarily due to a lack of a clear link between the investigated material measurements and device performance.

EH&S work will consist of 1) development of HEPA filtration testing protocols, 2) continued improvements to hazardous waste recycling and reduction procedures, and 3) third party validation of our Industrial Hygiene program.

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REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	February 2004	Phase I Annual Report October 2003

4. TITLE AND SUBTITLE
Research Leading to High Throughput Processing of Thin-Film CdTe PV Module, Phase I Annual Report, October 2003

5. FUNDING NUMBERS
PVP45001
RDJ-2-30630-20

6. AUTHOR(S)
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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
NREL/SR-520-35348

11. SUPPLEMENTARY NOTES
NREL Technical Monitor: Harin Ullal

12a. DISTRIBUTION/AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words):* Work under this subcontract contributes to the overall manufacturing operation. During Phase I, average module efficiency on the line was improved from 7.1% to 7.9%, due primarily to increased photocurrent resulting from a decrease in CdS thickness. At the same time, production volume for commercial sale increased from 1.5 to 2.5 MW/yr. First Solar is committed to commercializing CdTe-based thin-film photovoltaics. This commercialization effort includes a major addition of floor space and equipment, as well as process improvements to achieve higher efficiency and greater durability. This report presents the results of Phase I of the subcontract entitled "Research Leading to High Throughput Processing of Thin-Film CdTe PV Modules." The subcontract supports several important aspects needed to begin high-volume manufacturing, including further development of the semiconductor deposition reactor, advancement of accelerated life testing methods and understanding, and improvements to the environmental, health, and safety programs. Progress in the development of the semiconductor deposition reactor was made in several areas. First, a new style of vapor transport deposition distributor with simpler operational behavior and the potential for improved cross-web uniformity was demonstrated. Second, an improved CdS feed system that will improve down-web uniformity was developed. Third, the core of a numerical model of fluid and heat flow within the distributor was developed, including flow in a 3-component gas system at high temperature and low pressure and particle sublimation.

14. SUBJECT TERMS: PV; manufacturer; module efficiency; photocurrent; CdS thickness; semiconductor deposition reactor; vapor transport deposition; down-web uniformity; 3-component gas system.

15. NUMBER OF PAGES

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL