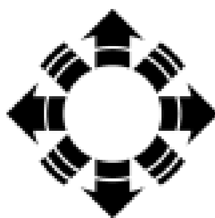
May 2004 • NREL/SR-520-35922

Subcontractor Report

Advanced CIGS Photovoltaic Technology

Annual Technical Report–Phase II
15 November 2002–14 November 2003

A.E. Delahoy and L. Chen
Energy Photovoltaics, Inc.
Princeton, New Jersey



NREL

National Renewable Energy Laboratory
1617 Cole Boulevard, Golden, Colorado 80401-3393
303-275-3000 • www.nrel.gov

Operated for the U.S. Department of Energy
Office of Energy Efficiency and Renewable Energy
by Midwest Research Institute • Battelle

Contract No. DE-AC36-99-GO10337

May 2004 • NREL/SR-520-35922

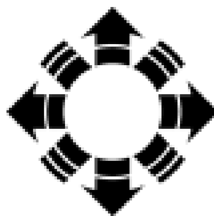
Advanced CIGS Photovoltaic Technology

Annual Technical Report–Phase II
15 November 2002–14 November 2003

A.E. Delahoy and L. Chen
Energy Photovoltaics, Inc.
Princeton, New Jersey

NREL Technical Monitor: H.S. Ullal

Prepared under Subcontract No. ZDJ-2-30630-21



National Renewable Energy Laboratory
1617 Cole Boulevard, Golden, Colorado 80401-3393
303-275-3000 • www.nrel.gov

Operated for the U.S. Department of Energy
Office of Energy Efficiency and Renewable Energy
by Midwest Research Institute • Battelle

Contract No. DE-AC36-99-GO10337

This publication was reproduced from the best available copy
Submitted by the subcontractor and received no editorial review at NREL

NOTICE

This report was prepared as an account of work sponsored by an agency of the United States government. Neither the United States government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States government or any agency thereof.

Available electronically at http://www.osti.gov/bridge

Available for a processing fee to U.S. Department of Energy
and its contractors, in paper, from:
U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831-0062
phone: 865.576.8401
fax: 865.576.5728
email: mailto:reports@adonis.osti.gov

Available for sale to the public, in paper, from:
U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Road
Springfield, VA 22161
phone: 800.553.6847
fax: 703.605.6900
email: orders@ntis.fedworld.gov
online ordering: http://www.ntis.gov/ordering.htm

Printed on paper containing at least 50% wastepaper, including 20% postconsumer waste

Preface

Technically, thin film PV technologies have advanced considerably in the last few years. However, for technologies to survive, they must also perform well commercially [1]. At the time of writing, the leading commercially-available thin film technologies have demonstrated the following record aperture area efficiencies and powers for large area modules:

CIGS	12.5%	74.0W	Wurth Solar
CIGSS	12.1%	44.3W	Shell Solar
CdTe	10.1%	67.1W	First Solar
a-Si/μc-Si (w. back reflector)	10.0%	38.0W	Kaneka
a-Si triple (w. back reflector)	7.9%	35.7W	United Solar
a-Si single	6.7%*	100W	Mitsubishi Heavy Industries
a-Si dual (w. back reflector)	6.1%	33.3W	RWE
a-Si dual (wo. back reflector)	5.7%	42.3W	Energy Photovoltaics

*based on sales literature

Even higher module efficiencies have been demonstrated by some companies that currently do not use the technology commercially, e.g. 13.4% for CIGS by Showa Shell, and 11% for CdTe by BP Solar and Matsushita. It may be noted that CIGSS continues to hold the efficiency record.

For PV to continue growing at 30% per year for the next 30 years so that it can take its place as a significant energy source on the world stage, modules will have to be made in a more energy-efficient manner. At this growth rate, for a new PV factory to generate a positive energy return in less than 10 years, the specific energy for module production must be less than 18MJ/W_p [1]. If a PV technology cannot meet this condition, it may be questioned whether large quantities of energy will in practice be expended to manufacture PV modules. The published range of total energy requirements to produce wafer-based modules is 20-100 MJ/W_p. For CIGS, the figure is 11MJ/W_p (Shell Solar), and for a-Si the figure is 12-15MJ/W_p (EPV).

The driving forces for CIGS are compelling: potentially high efficiency and low specific energy for production. To these we may add the broad advantageous properties of thin-film PV relative to wafer-based PV: monolithic design leading to reduced parts handling, low consumption of both direct and indirect materials, and fewer process steps.

To facilitate the development of CIGS, CdTe, and Si-based thin-film technologies, NREL operates the **Thin-Film Photovoltaics Partnership Program (TFPPP).** The long-term objective of the TFPPP is to demonstrate low-cost, reproducible modules of 15% aperture area efficiency. As a Technology Partner within this program, EPV is performing research under a three-phase, cost-shared subcontract entitled "Advanced CIGS Photovoltaic Technology" and participates in both the Absorber and Alternative Junctions sections of the National CIS Team Meetings. The objective of this subcontract is to develop and integrate the various pieces of new technology that EPV considers enabling for cost-effective production of CIGS modules.

CONTENTS

Preface…… iii
Table of Contents…… iv
List of Tables…… vi
List of Figures…… vi

1.0 **Introduction**…… 1
1.1 Overview of accomplishments during previous subcontract…… 1
1.2 Project objectives…… 1
1.3 Approach…… 2
1.4 Overview of accomplishments during Phase I…… 2

2.0 **Status of Hybrid CIGS** …… 3
2.1 Normal hybrid process …… 3
2.2 All-Zeus process …… 4
2.3 Hybrid CIGS with IGS compound evaporation …… 4

3.0 **Process and Layout for Interim Modules**…… 5

4.0 **Improvement and Readiness of Module Subcomponents**…… 7
4.1 Mo sputtering and adhesion, and Mo laser scribe improvement…… 7
4.2 CIGS deposition …… 8
4.3 CBD CdS…… 9
4.4 CIGS patterning…… 11
4.5 ZnO improvement at elevated substrate temperature…… 12
4.6 Interconnection…… 14
4.6.1 Evaluation of i-ZnO/Mo…… 14
4.6.2 New ZnO configuration for interconnection…… 14
4.6.3 Status of large area ZnO process for modules…… 16

5.0 **Module Performance** …… 16

6.0 **Quality control, module analysis, and modeling** …… 18
6.1 Quality control steps…… 18
6.2 Module analysis …… 19
6.3 Modeling…… 21

7.0 **Progress overview for hybrid CIGS** …… 21

8.0 **Cell studies** …… 22
8.1 Assessment of cell processing …… 22
8.2 New processing for window layer/TCOs…… 23
8.3 Experiments concerning the temperature resistance of junctions …… 24

9.0 **Module reliability** …… 25

10.0 **Safety**…… 26

11.0 **Some plans for the initial quarters of Phase III**………………………………… 27

12.0 **Phase II Summary** ……………………………………………………………… 28

Acknowledgments ………………………………………………………………….. 29
References ………………………………………………………………………….... 29

TABLES

Table I. Device performance from all-Zeus hybrid process……………… ……… … 4
Table II. Device performance from hybrid process with IGS compound evaporation.. 5
Table III. Equipment used for Zeus CIGS processing for standard modules ($0.43m^2$), interim modules ($1ft^2$), and mini-modules ($40cm^2$) ………………………………… … 6
Table IV. Relative laser power for Mo scribing and cutting depth in glass………….. 7
Table V. CIGS films: composition and I-V parameters of their devices…………….. 8
Table VI. Device performance (after light soaking) with and without annealing after CdS. 11
Table VII. Device performance as a function of ZnO preheating temperature …… 13
Table VIII. Mini-module performance with i-ZnO or n-ZnO as interconnection to Mo 14
Table IX(A). Performance comparison of Z1559-51…………………………………. 15
Table IX(B). Performance comparison of Z1559-32…………………………………. 15
Table X. Interconnect resistance for seven mini-modules …………………………… 16
Table XI. 1 ft^2 module performance ………………………………………………….. 17
Table XII. Quality control steps on process line …………………………………….. 18
Table XIII. Module Z1625 analysis sheet …………………………………………… 19
Table XIV. Process comparison for devices and modules …………………………… 19
Table XV. Selected device results using HC-sputtered TCO………………………… 23

FIGURES

Fig. 1. J-V curve of device with V_{oc} of 636mV (Zeus CIGS; normal hybrid process).. 3
Fig. 2. Interim processing of full size plate, showing1 ft^2 module layout and other cut sections. …………………………………………………………………………… 6
Fig. 3. Ga distribution (Z1619)………………………………………………..………… 9
Fig. 4. CdS transmission mapping over $1ft^2$ plate …………………………………….. 10
Fig. 5. Interconnect test structure ……………………………………………………… 12
Fig. 6. Improved ZnO properties at elevated substrate temperature…………… …….. 13
Fig. 7. Light and dark IV curve for $1ft^2$ module Z1625B (5.4% aperture area efficiency) 17
Fig. 8. Resistance distribution for ZnO and interconnection………………………….. 20
Fig. 9. V_{oc} and leakage resistance distribution ………………………………………… 21
Fig. 10. Graphical illustration of progress during subcontract, showing successive development and efficiency of hybrid CIGS cell, mini-module, square foot module, and full size module. ……………………………………………………………………… 22
Fig. 11. J-V curve of cells fabricated by EPV on NREL CIGS: 15.5% with CdS buffer and RF ZnO; 13.3% with no buffer and HC deposition of ZnO.. ……………………… 23
Fig. 12. J-V curve for CIGS cell with IMO TCO …………………………………… 24
Fig. 13. V_{oc} x FF product for junctions annealed at various temperatures before ZnO deposition. ………………………………………………………………………….. 25
Fig. 14. Sheet resistance of various TCO samples versus water immersion time………. 26

1.0 Introduction

This is the Annual Technical Status Report for Phase II of EPV's cost-shared subcontract ZDJ-2-30630-21 **Advanced CIGS Photovoltaic Technology** awarded under the Thin Film Photovoltaics Partnership Program. The nominal period covered by the report is November 15, 2002 - November 14, 2003.

As part of the Thin Film Photovoltaics Partnership Program, EPV has conducted research to help generate a technology base for production of CIGS PV modules using vacuum deposition of CIGS onto glass. This strategy is consistent with the observation that, despite there being several approaches to forming device quality CIGS, vacuum deposition has maintained the world record for the highest efficiency CIGS device. A record thin-film solar cell efficiency of 19.2% (with Ni-Al grid and MgF_2 ARC) for a 0.41 cm^2 device was achieved by NREL in 2003 using vacuum-deposited CIGS [2]. The deposition employed four point sources and detection of the Cu-poor to Cu-rich transition for process control.

In order to extend this type of processing to the realm of large area substrates, EPV developed vacuum equipment designed for heating and coating $0.43m^2$ moving substrates, with a projected further scale up to $0.79m^2$. The substrates are typically low cost, soda-lime glass, and the materials are supplied to the moving substrates using novel linear source technology developed by EPV [3,4]. The use of elemental selenium rather than toxic H_2Se gas helps make for a safe manufacturing environment. These choices concerning film deposition, substrates and source materials help to minimize the processing costs of CIGS.

1.1 Overview of accomplishments during previous subcontract

During its previous 3-year, cost-shared research subcontract with NREL that ended in November 2001, EPV successfully produced high quality $0.43m^2$ Mo-coated glass substrates that, when cut up, enabled NREL to produce 17.1% CIGS cells on such substrates [5]. EPV further successfully utilized its novel linear evaporative sources for supply of Cu, In, Ga and Se to form CIGS on $0.43m^2$ substrates, producing modules with V_{oc}'s up to 37V, although with disappointing fill factor and, especially, reproducibility. It was concluded that the linear source developed by EPV for Cu had drawbacks that precluded its use in manufacturing. A new approach to buffer layer deposition was pioneered through synthesis of the compound $ZnIn_2Se_4$ and its use as a source material [5,6]. In addition, the CIGS current generated in exploratory a-Si/a-Si/CIGS stacked devices was increased from 6 to13 mA/cm^2. Supporting these programs, EPV's upgraded analytical and measurement laboratories provided rapid in-house feedback concerning material and device properties.

1.2 Project Objectives

The principal objective is the fabrication, analysis, and optimization of large area CIGS modules with efficiencies in the range 6 - 10%. To support this activity, we are striving to develop CIGS and junction formation recipes capable of producing small area devices with efficiencies in excess of 14% (without AR coating or special grids). However, only CIGS methods capable of implementation on EPV's large scale processing equipment are being considered. Objectives related to the large-scale equipment include improvement of the quality of the layers and their

uniformity of thickness and composition. Processing repeatability is also a major focus. Advances are also sought in high rate deposition of high quality doped ZnO, and patterning operations that exhibit low area and electrical interconnect losses. The conduct of module reliability testing at the earliest opportunities is of particular importance.

Work around the world during the past decade has revealed CIGS science and technology to be full of complexity. For example, in contrast to previous semiconductor experience, Na in the CIGS was found to be beneficial to device performance, with the Na source being the soda lime glass and the Na concentration in the CIGS depending on transmission through the Mo grain boundaries and the substrate temperature. Perhaps the most remarkable feature of device-quality polycrystalline CIGS is the apparent immunity of this small-grained semiconductor to grain boundary recombination. Only recently has a theory been advanced to account for this [7]. It is also acknowledged that individual processing steps or layers often cannot be regarded as independent but are rather interdependent. This is especially true for CdS/CIGS and CdS/ZnO interfaces. Thus, another of our objectives is to arrive at robust methods of deposition and module fabrication that translates all of the important and complex features of the technology into a straightforward set of rules for reliable, repeatable module fabrication. We believe this will provide a sound foundation for manufacturing of CIGS modules.

1.3 Approach

R&D and process development for CIGS is conducted in the Hercules 4-source system (six 5cm x 10cm stationary substrates per run) and in the Zeus 4-source system (one 4300 cm^2 moving substrate per run). In the latter system, which is load locked, source materials (such as In, Ga, Se) are delivered downwards to the moving glass using custom-built source heads housing three independent linear evaporative sources, the source axes being perpendicular to the direction of glass travel. Copper is supplied by planar-magnetron sputtering.

It is recognized that the traditional method of junction formation involving chemical bath deposition (CBD) of CdS is unavoidable at the current stage. EPV therefore relies on CBD CdS on a day-to-day basis, and continues to improve its processing and equipment for CBD, while exploring alternative methods in parallel. Other methods include buffer layers applied by evaporation (e.g. $ZnIn_2Se_4$ or other materials [6,8]), by spray deposition [9], or by hollow cathode sputtering. For ZnO deposition, two planar-magnetron sputtering systems are available and are fitted with ceramic ZnO targets. In the small area system, RF sputtering is used, while in the in-line system, mid-frequency bipolar sputtering is used. Module encapsulation is accomplished using glass-glass vacuum lamination with EVA, with processing similar to that of the EPV-40 a-Si/a-Si module. For long-term outdoor testing, a Campbell Scientific datalogger is available.

1.4 Overview of accomplishments during Phase I

At the conclusion of the previous subcontract it was resolved that a switch to magnetron sputtering would be undertaken to supply the Cu for CIGS growth. During Phase I of the current subcontract EPV was successful in developing a hybrid approach to CIGS deposition involving supply of In, Ga, and Se by evaporation and Cu by sputtering. Using the hybrid process, a cell efficiency of 13.5% was achieved (569mV, 32.3mA/cm^2, FF 73.5%) [9,10]. Towards the end of Phase I, a 13-segment mini-module was produced using CIGS produced in the Hercules R&D

system having an efficiency of 9.0% [9,10]. It further appeared that both the quality and repeatability of CIGS produced by the hybrid process made the process suitable for implementing in the large area pilot line (Zeus).

It was also recognized that adoption of a different method of forming CIGS would require a thorough re-optimization of the junction formation steps. This was undertaken and accomplished, resulting in some significant changes to the overall process and recipe [9,10]. Firstly, a post-deposition treatment of the CIGS was developed that improved the performance of devices. This is now part of EPV's standard processing. Secondly, for chemical bath deposition of CdS, a change was made from Cd acetate to Cd sulfate, and an increased S/Cd ratio was adopted. Work was continued in the area of alternative junctions, and a 10.1% cell was made using evaporated $ZnIn_2Se_4$ [8-10], and an 8.6% cell using evaporated In_2S_3 [8,9].

2.0 Status of Hybrid CIGS

2.1 Normal hybrid process

The hybrid CIGS deposition process has been operated at EPV for more than a year. It includes evaporation of In and Ga, and sputtering of Cu to take advantage of better uniformity and reproducibility. It was developed in Hercules, an R&D bell jar system, and during Phase I the hybrid process was successfully implemented in the pilot line (Zeus system) for large area CIGS deposition. The basic process concept is related to the NREL three-stage process. The first In and Ga layers are evaporated in the presence of Se in the Hercules or Zeus system to form $(In,Ga)_2Se_3$, and the substrate is then transferred to an in-line sputtering system for Cu deposition. Finally, the substrate is moved back to Hercules or Zeus for selenization and In and Ga finishing evaporations.

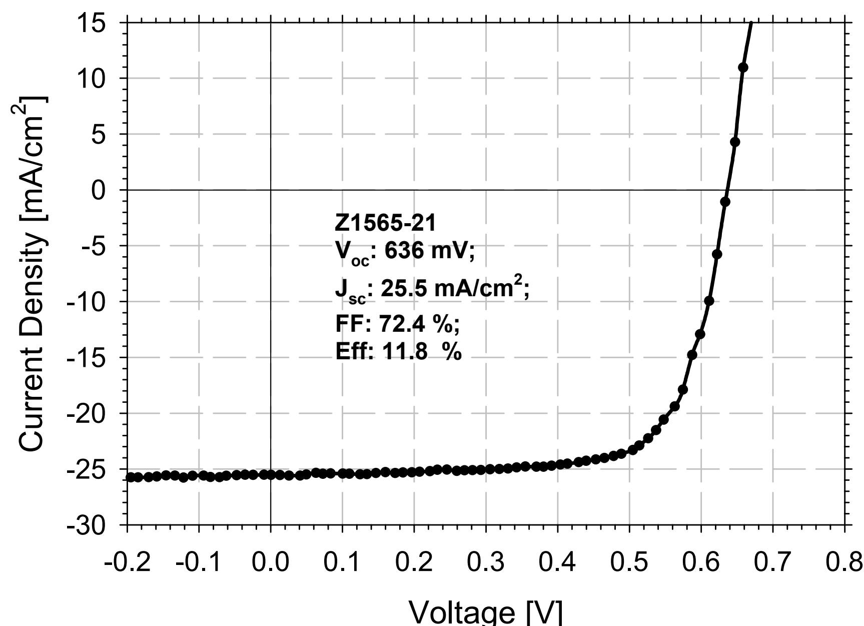


Fig. 1. J-V curve of device with V_{oc} of 636mV (Zeus CIGS; normal hybrid process).

During Phase II, the normal hybrid process run in the Zeus system yielded some exciting results. Never seen before, some devices exhibited a very high V_{oc} of 636 mV as well as an excellent FF of 72.4%. Plotted in Fig. 1 above is the J-V curve of one such device.

2.2 All-Zeus process

In our original (normal) three-stage hybrid process, vacuum has to be broken twice, i.e. before and after sputtering Cu in the in-line system. There is, naturally, the concern that oxidation of the IGS film before sputtering Cu and/or oxidation of the Cu film after sputtering Cu might occur (while the substrate is in air), and that such oxidation might have a negative impact on CIGS device performance. If, on the other hand, we could eliminate the vacuum breaks by depositing all of the layers in the Zeus, then oxidation would be avoided. In addition, we would expect that the process throughput could be increased.

During Phase II, to eliminate such vacuum breaks, we designed and installed a magnetron sputtering cathode fitted with a Cu target in the ante-chamber of the Zeus system so that all three stages could be processed in Zeus. Initially, arcing led to the extinguishing of the Ar plasma. Various steps were taken to solve these teething problems, and sputtering of Cu can now be conducted in the Zeus. Mid-frequency sputtering is used, and operating conditions are different from those used in the in-line sputtering system. The conductivity of sputtered Cu films produced in Zeus is almost as good as that of films produced in the in-line sputtering system. It is also encouraging that Zeus-sputtered Cu films made on large-area glass plates show excellent uniformity.

Listed in Table I is the performance of some devices cut from large plates fully processed in the Zeus system (including sputtering of Cu). Plates 1575 and 1580 were coated in some of the first runs using this technique.

Table I. Device performance from all-Zeus hybrid process

ID	**Process**	**V_{oc} (mV)**	**FF (%)**	**J_{sc}(QE) (mA/cm^2)**	η (%)
Z1575-1 A1	All-Zeus	558	67.8	24.2	**9.2**
Z1575-1 C1	All-Zeus	538	67.1	24.9	**9.0**
Z1580-7 B5	All-Zeus	613	63.0	25.8	**10.0**
Z1580-7 A1	All-Zeus	659	63.9	23.9	**10.0**
Z1604-6	All-Zeus	580	65.1	29.6	**11.2**
Z1604-8	**All-Zeus**	**631**	**59.7**	**25.4**	**9.6**

The results demonstrate great potential for our hybrid process with all-Zeus processing. We are confident that these parameters can be further improved.

2.3 Hybrid CIGS with IGS compound evaporation

Through adoption of the hybrid process, we have reduced the number of evaporation sources from four (Cu, In, Ga, and Se) to three (In, Ga, and Se). A further simplification of the hybrid process is to use the compound source material $(In,Ga)_2Se_3$ (here denoted by In/Ga/Se or IGS),

synthesized at EPV, as a single evaporation source material to replace the individual evaporation elements In and Ga. The merits for such a process include:

- Fixed Ga ratio in starting material
- Lower process temperature due to higher vapor pressure for IGS compound
- Reduced number of control parameters
- Elimination of interaction between multiple evaporation sources at different temperatures

We started by measuring the ratios of Ga/III and Se/III in the IGS compound by ICP AES. As hoped for, the Ga/III ratio is 0.31-0.33 while the Se/III ratio is 1.48-1.51. This indicates that our home-made In/Ga/Se compound is stochiometric $(In_{0.68},Ga_{0.32})_2Se_3$. Evaporations involving the IGS material were conducted in the Hercules system. An In/Ga/Se film evaporated from the compound at a substrate temperature 350°C without Se presence exhibits a similar Ga/III ratio. However, the Se/III ratio of the film drops to 1.2-1.3, which indicates some Se loss due to compound decomposition (either of the source material or of the material on the heated substrate). It is very interesting to find that the Se/III ratio for the film on the heated substrate becomes close to 1.5 once again when the IGS compound is evaporated with co-evaporation of additional Se.

The performance of some of the devices made from CIGS prepared using this hybrid process (IGS compound evaporation and sputtered Cu) is rather encouraging. The performance parameters are listed in Table II.

Table II. Device performance from hybrid process with IGS compound evaporation

ID	Process	V_{oc}	FF	J_{sc}	η
H193-2 A	IGS compound	527	59.5	32.3	**10.1**
H193-2 B	**IGS compound**	**560**	**58.0**	**31.3**	**10.1**

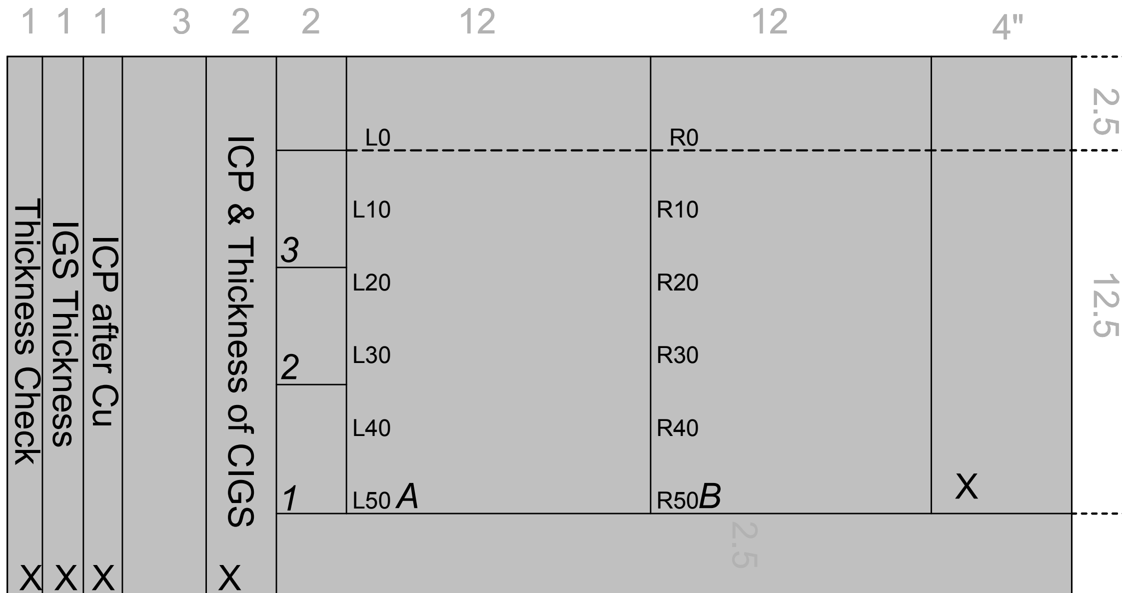
An excellent current density was achieved. The modest values of Voc and FF leave plenty of room for further process optimization. It is not yet clear whether the compound source can be reliably utilized in the Zeus system.

3.0 Process and layout for interim module

After careful preparation and quality control for each process component (see Section 4 for details), we were able to restore module processing in the last quarter of Phase II. Our standard module size is 0.43 m^2 with dimensions of 96.5 cm x 44.5 cm (38” x 17.5”). However, the newly-designed full size dipping tanks for CBD CdS were not completed until the end of the year. Therefore, we decided to process 1 square foot modules (size: 12” x 12.5”) as an interim step based on the availability of new 1 ft^2 dipping tanks for the CdS process. Except for the CdS dipping, all of the 1 ft^2 module processes are exactly the same as those used for the full size module process.

We start with Mo deposition by sputtering and laser separation of the Mo on a full size piece of soda-lime glass, followed by hybrid CIGS deposition on the full size plate. Then, two substrate

pieces (12” x 15”) are cut from the full size CIGS plate for fabrication of 1 ft^2 modules (see module layout in Fig. 2), and the rest of the plate is retained for process control and module analysis (see Sec. 4). The cutting size of 12” x 15” is larger than that of the finished 1 ft^2 module (12” x 12.5”) to allow one side of the cut pieces to serve as a reference for the patterning alignment. After the two 1 ft^2 plates are coated with CdS in the 1 ft^2 tank, we pattern them on a full size X-Y table and sputter ZnO on a full size carrier. Table III lists the equipment used for standard 0.43 m^2 modules, interim 1 ft^2 modules, and diagnostic mini-modules.



1,3: Dot device with Beaker CdS/Airco ZnO
2: Mini-module and test device with Beaker CdS/ILS ZnO
A,B: Module with Tank CdS/ILS ZnO
All units in the Graph are inches

Fig. 2. Interim processing of full size plate, showing1 ft^2 module layout and other cut sections.

Table III. Equipment used for Zeus CIGS processing for standard modules (0.43m^2), interim modules (1ft^2), and mini-modules (40cm^2)

Process steps	Standard module	Interim module	Mini-module
Mo deposition	ILS	ILS	ILS
Mo separation (laser)	60” x 30”X-Y table	60” x 30”X-Y table	60” x 30”X-Y
1st IGS evaporation	Zeus	Zeus	Zeus
Cu sputtering	ILS or Zeus	ILS or Zeus	ILS or Zeus
2nd IGS evaporation	Zeus	Zeus	Zeus
CBD CdS	4 ft^2 dipping tanks	1 ft^2 dipping tanks	Beaker process
i-ZnO	ILS	ILS	Airco (RF) or ILS
CIGS scratch	60” x 30”X-Y table	60” x 30”X-Y table	Hand
n-ZnO	ILS	ILS	Airco (RF) or ILS
ZnO scratch	60” x 30”X-Y table	60” x 30”X-Y table	Hand
IV measurement	Bench table	Bench table	Bench table

Note. ILS denotes in-line sputtering system

4.0 Improvement and Readiness of Module Subcomponents

Great components with excellent and stable performance are the foundation for module production. We have spent a few months to make sure all components in module process with stable and controllable performance, which has to be checkable individually. Included in this Section are some major processes among others:

4.1 Mo sputtering and adhesion, and Mo laser scribe improvement

We recently found that Mo films sputtered in the in-line system tended to peel off during the laser scribe process. This was quite abnormal. It was realized that the peeling materialized after the Cr target had been moved to a new position to make room for the installation of a large area heater. Having checked many process parameters such as glass side, cleaning procedure, laser condition, Mo power etc., we eventually found the plasma voltage in the Cr sputtering step to be about 40-50 V higher than normal, which we took to imply that the Cr target was somehow contaminated. After thoroughly pre-sputtering the Cr target at a higher power and for a substantially longer time than that normally used in our operations, we were able to restore the plasma voltage to its original value around 270V. The exercise confirmed our previous experience that a thin underlayer is essential to maintain good adhesion of the Mo.

Barring such anomalies, the large area sputtering of bi-layer Mo in the in-line system is one of the most stable processes in our module production. The Mo sheet resistance is very stable and close to 0.3 ohm per square with a thickness around 8000 A.

As a by-product of these investigations, we found that the laser used for Mo scribing was cutting about 3000 A deep into the glass when 'normal' Mo scribing conditions were used. It was feared that this could cause module breakage during lamination. After carefully optimizing the laser power, we found that 80% of the original power is sufficient to separate the Mo quite well, while the depth of cutting into the glass is much shallower. Listed in Table IV are some experiments regarding laser power optimization.

Table IV. Relative laser power for Mo scribing and cutting depth in glass

Laser power	100 %	90 %	80 %	**70 %**
Cutting depth into glass	**3 kA**	**2 kA**	**500 A**	**None**

Recently, we carefully investigated laser separation of Mo. One study showed that some incomplete scribes exhibit a pattern in which they appear only in every other line. In view of our laser scribe program cutting one line in the forward direction and the next in the reverse direction, it is evident that the IR laser cutting effect is moving direction-dependent. Having identified the better direction, we were able to change our program to make the cutting always in this better direction, and separation quality improved immediately. Furthermore, to ablate the remains of debris in the Mo line more thoroughly, we adopted a double scribe procedure. Now, complete and clear Mo separation is routinely achieved in our module production. In addition, an electrical burn process proved to be useful to eliminate shorting debris in the Mo line.

4.2 CIGS deposition

Investigation of the Cu selenization conditions was our main focus in this period. A 38″ x 17.5″ plate (Z1559) was cut into several 3″ x 12.5″ strips, which were then employed to investigate the effects of selenization conditions on device performance. The main purpose of this experiment is to find an optimal selenization temperature. Two kinds of Cu/$(In,Ga)_2Se_3$ precursor, Cu-poor (Cu/(In+Ga) = 0.87 in Z1559-1,2,3) and Cu-rich (Cu/(In+Ga) = 1.27 in Z1559-5,6,7) as measured after first IGS layer and sputtered Cu deposition, were used. The third stage IGS deposition followed Cu selenization for all strips except Z1559-2, on which no third layer was deposited.

Listed in Table V is a summary of CIGS film composition before and after the third IGS layer, as measured by ICP, and the I-V parameters of small cells having an area of ~ 0.2 cm^2. The results in Table I clearly show that:

1) CIGS film (Z1559-2), with Cu selenization but without a third-stage IGS layer, does not yield good devices. Most of the small devices in this sample show shunted dark and light I-V behavior which implies that a conductive Cu-Se phase might emerge on the surface of the CIGS and grain boundaries, constituting shunting paths even though the total Cu/(In+Ga) ratio is only 0.86;

2) Devices on CIGS films made from precursors that passed through a Cu-rich period ("Cu-rich precursors") (Z1559-5,6,7) demonstrate noticeably higher V_{oc} even though their Ga ratio is lower;

3) Devices with Cu-rich precursors (Z1559-5,6,7) selenized at 550ºC show higher efficiencies than those selenized at 525ºC and 500ºC, while there was no obvious performance difference for different selenization temperatures for Cu-poor precursors (Z1559-1,3).

Table V. CIGS films: composition and I-V parameters of their devices

Z1559	Cu/ (In+Ga) (**before** 3rd IGS)	Selenization conditions (temp/time)	Cu/ (In+Ga) (**after** 3rd IGS)	Ga/ (In+Ga)	Thick-ness (μm)	V_{oc} [mV]	FF [%]	J_{sc}(QE) [mA/ cm^2]	Eff [%]
Z1559-2	0.87	550°C/30min*	0.86	0.31	1.55	351	52.4	27.2	5.0
Z1559-1	0.87	550°C/30min	0.63	0.31	2.11	483	64.4	26.5	8.2
Z1559-3	0.87	525°C/30min	0.65	0.30	2.11	499	62.2	26.9	8.4
Z1559-5	1.27	550°C/30min	0.72	0.28	2.55	558	72.7	26.9	10.9
Z1559-6	1.27	525°C/30min	0.68	0.26	2.56	529	64.7	23.1	7.9
Z1559-7	1.27	500°C/30min	0.72	0.28	2.70	525	68.9	22.9	8.3

* *without 3rd IGS layer*

In a 3-stage process, achievement of a Cu-rich film at the end of the second stage Cu-Se delivery onto a $(In,Ga)_2Se_3$ precursor is thought to result in a Cu_xSe liquid-phase that aids grain growth and yields large and columnar morphologies and better devices [11]. This requires a Cu-rich stage before the third IGS deposition as well as a high substrate temperature (>523ºC for a Cu_xSe liquid phase). Our results agree well with the ideas and reported results of CIGS growth by a 3-stage process. This investigation clearly suggests that a Cu-rich precursor having a Cu ratio 1.2-1.3 after the sputtered Cu step is needed in order to fabricate good devices. Further increase of

substrate temperature during selenization is planned. An investigation of the selenization time is also under way. Right now, the best efficiency for small cells made on Zeus material is 11.8% (Fig. 1).

In order to make $0.43m^2$ modules, CIGS uniformity is a critical factor. Lately, we found that the Ga linear source shows a severely non-uniform distribution. The ratio of Ga/(In+Ga) at the two ends of the linear source is as high as 1.5. We were able to obtain much better uniformity by switching the Ga source to another existing delivery line. However, we are unable to use this line to deliver Ga in module production because it is adjacent to the Se source and causes the Se source temperature to become uncontrollable.

The temporary solution in our module process is that we rotate the plate 180 degrees in the 3rd stage IGS evaporation so that at the higher Ga region from the 1st stage IGS receives less Ga in the 3rd stage. The global bulk Ga ratio after the plate rotation is improving substantially (see Fig. 3 below). However, the composition depth profile in CIGS film from location to location along the delivery line is now different.

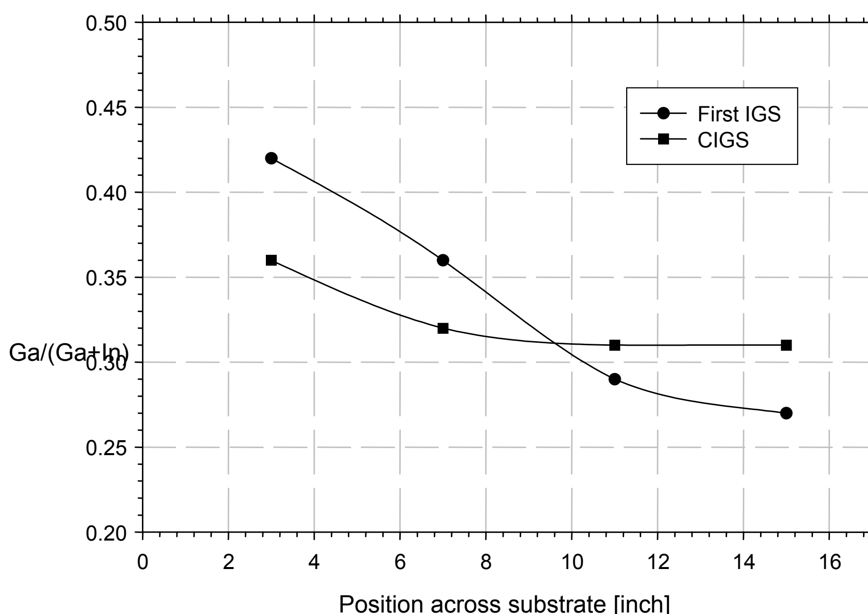


Fig. 3. Ga distribution (Z1619)

Changing the delivery line without spare parts in hand involves a substantial risk and is also time-consuming. In order to not interfere with our main effort to restore module production, replacement of the Ga line was not attempted during Phase II. However, adjustment of the Ga distribution will be a must during Phase III.

4.3 CBD CdS

The chemical bath deposition process for CdS was optimized once again, this time for module production. We believe that a slow chemical reaction is essential to deposit uniform CdS films over large areas, which is a necessity for the module process. By reducing both reaction temperature and the ratio of thiourea to cadmium salt, we were able to increase deposition time

from the original 15 minutes to 35 minutes before the on-set of colloidal growth. Furthermore, we found that sufficient stirring in the dipping tank is also crucial to forming a uniform film. Therefore we increased both the number of electrical stirring propellers and their rotation speed. The improvement of performance and uniformity was dramatic after the re-optimization.

To have better quality control for the CdS film thickness, optical transmission at 420 nm and 440 nm on CTO glass was adopted as a process monitor. Plotted in Fig. 4 is an example of transmission contour mapping on a 1 ft^2 CdS/CTO glass. In addition, we also use the QE value at 480 nm of real devices to monitor the CdS thickness since it is not easy to directly measure the thickness of thin Cd films.

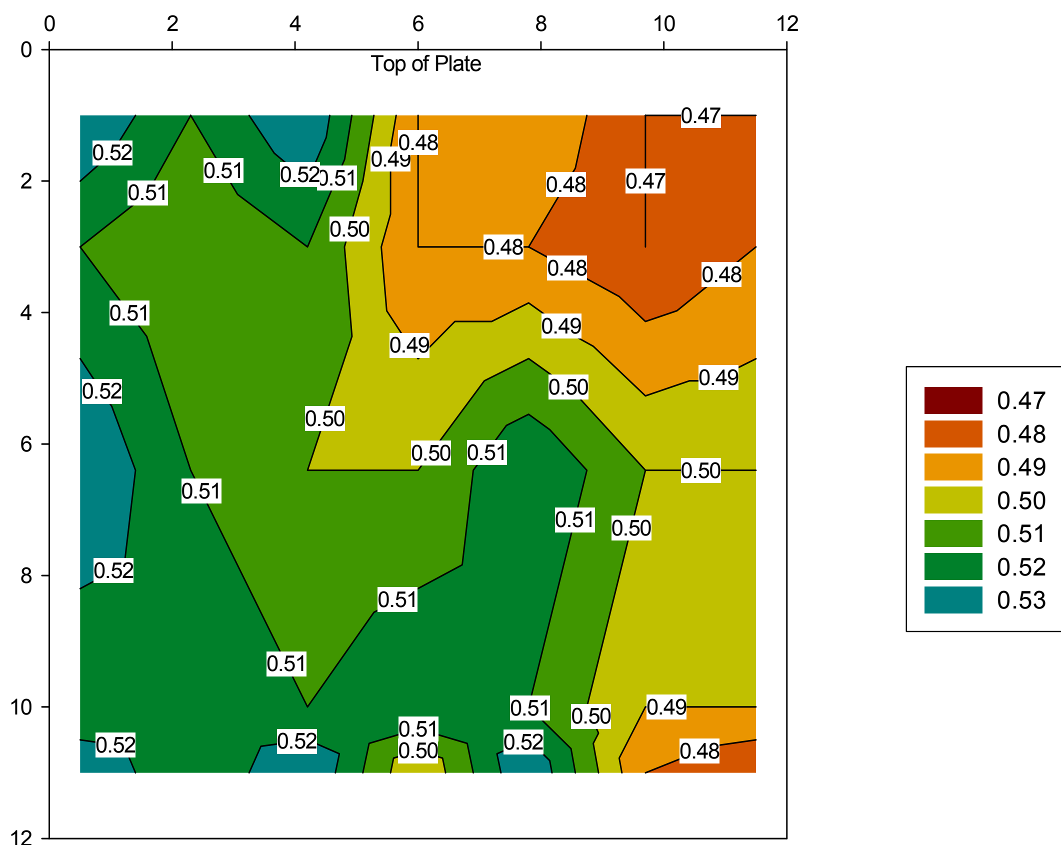


Fig. 4. CdS transmission mapping over 1ft^2 plate

Recently, we tested annealing the CIGS/CdS film before ZnO deposition based on a concern that trapped water from the CdS dipping might degrade the junction or the ZnO. An improvement of device performance after annealing was observed, which is documented in Table VI. It is also interesting to observe that the samples after annealing showed a smaller difference of performance before and after light soaking.

Table VI. Device performance (after light soaking) with and without annealing after CdS

ID	Annealing	V_{oc}	FF	J_{sc}	Efficiency	R_{oc} (norm.)
Z24-3A1	Yes	555	69.3	22.3	8.6	**0.10**
Z24-3A2	Yes	557	70.2	24.8	9.7	**0.08**
Z24-3A3	Yes	562	70.5	24.3	9.6	**0.09**
Z24-3A4	Yes	556	68.3	24.5	9.3	**0.11**
Z24-3A5	Yes	536	65.2	23.8	8.3	**0.12**
Z24-3A6	Yes	552	70.3	24.1	9.4	**0.09**
Z24-3B1	No	529	64.1	23.8	8.1	**0.13**
Z24-3B2	No	537	64.7	24.5	8.5	**0.11**
Z24-3B3	No	546	65.6	23.8	8.5	**0.11**
Z24-3B4	No	522	58.9	24.4	7.5	**0.18**
Z24-3B5	No	534	62.9	24.1	8.1	**0.14**
Z24-3B6	**No**	**540**	**64.5**	**23.4**	**8.2**	**0.14**

The data clearly shows that both V_{oc} and FF were significantly improved in the annealed samples, together with an increase in the slope of the I-V curve at V_{oc}.

4.4 CIGS patterning

A good mechanical scribing process for the CIGS is one prerequisite for forming a low resistance interconnection between Mo and ZnO. It must meet the following requirements:

- Removing CIGS down to the Mo surface, but not cutting through the Mo layer.
- Forming an appropriate CIGS step so that the following n-ZnO can cover the wall conformally (no flakes of CIGS raised above the Mo surface).
- Having sufficient Mo surface area exposed to achieve a low interconnection resistance, but not so much as to waste area.
- Achievement and maintenance of a clean Mo surface for low contact resistance with ZnO.

To meet the first two requirements, the shape and material of the scribing tip, and adjustment of tip pressure and orientation are obviously important variables, while changing X-Y table speed and number of scribes may help in obtaining a continuous Mo line of appropriate width.

To speed the optimization with so many parameters, we need fast feedback from the experimental results. Therefore, we designed a special test structure, which is shown in Fig. 5. By processing a single test structure, a variety of different scribing conditions can be evaluated, such as tip material, pressure, table speed, etc. Following CIGS scribing, an n-ZnO layer is deposited on the test structure, then separated as shown, and the interconnection resistance for each individual condition can be measured. Thus, the best conditions for scribing can be identified.

Fig. 5. Interconnect test structure

Accurate and close alignment of the Mo line and the CIGS line is the key to reducing the dead area current loss. As simple as this sounds, it is however complicated by the Mo film being face down during laser separation of Mo, and face up during mechanical scribing of the CIGS, causing loss of registration. Moreover, in the real world, the lines are not perfectly straight, and do not maintain constant spacing because of the inversion of the plate. A video monitor would be very helpful as a QC check on scribe alignment, and a design is under way.

4.5 ZnO improvement at elevated substrate temperature

For quite some time we have known that one of the best ways to improve our large area ZnO film properties, such ZnO being produced by mid-frequency sputtering of a ceramic target, is to preheat the substrate. However, because of the unusually short inner vertical dimension of the sputtering chambers, this had never been properly implemented. We have now successfully designed, built, and installed a large area heater with temperature control in the in-line sputtering system. This has enabled us to produce a higher quality ZnO on 0.43 m^2 glass substrates, and the hope is that this advance can be successfully applied to our module processing. Much effort was devoted to re-optimizing the process parameters for ZnO, the parameters including sputter power, plate moving speed, gas ratio of Ar to O_2, number of scans, and preheating temperature. Finally, we settled upon a set of parameters except preheating temperature, which we are using as one of the last fine tuning parameters to optimize ZnO properties as well as device performance. Plotted in Fig. 6 are the ZnO film properties as a function of preheating temperature.

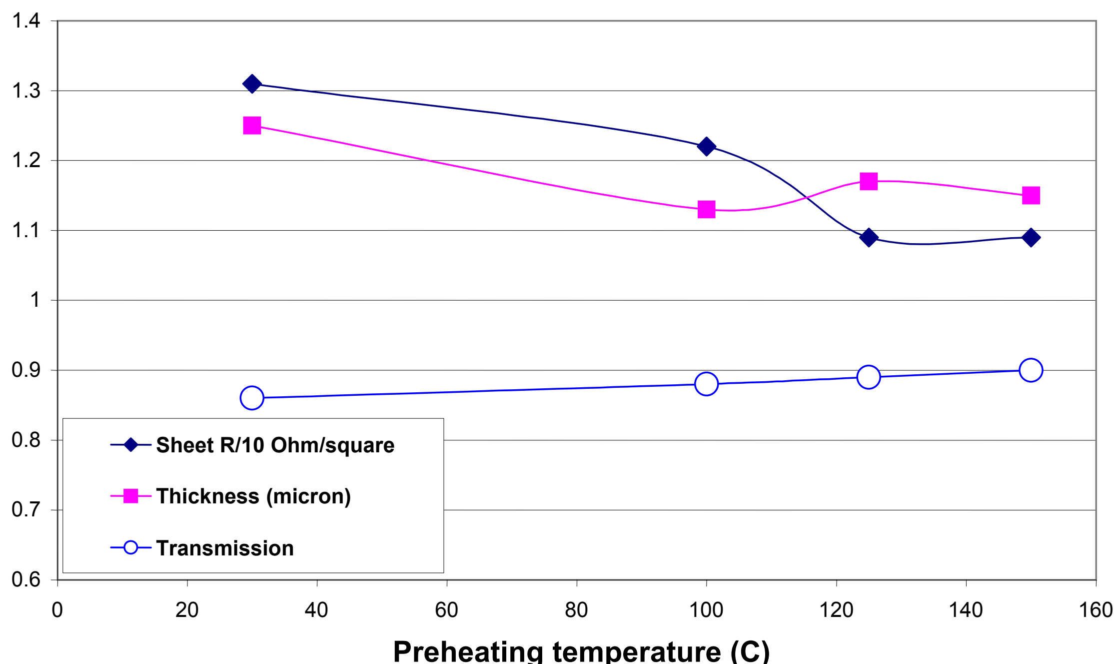


Fig. 6. Improved ZnO properties at elevated substrate temperature

The data in Fig. 6 show that ZnO properties keep improving at elevated temperature, which is consistent with what we have reported earlier. However, to determine final process conditions, optimization should be conducted with respect to the performance of CIGS modules, or at least performance of CIGS devices, rather than just the ZnO film on plain glass. With this in mind, a series of CIGS devices was processed at different elevated temperatures for ZnO deposition. The results are shown in Table VII.

Table VII. Device performance as a function of ZnO preheating temperature

Sample	Preheating T (°C)	Voc (mV)	Jsc (mA/cm^2)	Jsc (-1V) (mA/cm^2)	FF (%)	Eff (%)
Z1575-2	30	568	23.3	25.5	39.2	5.18
Z1575-6	30	527	22.1	25.0	26.6	3.10
Z1575-1A	100	562	20.9	24.7	58.9	6.93
Z1575-5A	100	562	20.7	24.7	58.3	6.80
Z1575-3A	125	532	19.8	25.4	52.71	5.56
Z1575-6A	125	552	19.8	25.6	50.1	5.47
Z1575-3	150	553	16.4	26.5	43.6	3.95
Z1575-5	150	498	17.9	27.2	43.9	3.91

Table VII strongly suggests that device performance deteriorates at a preheating temperature at 150°C. The main indication is that Jsc at zero bias drops severely despite being recoverable at a reverse bias of -1V. This is probably caused by junction damage at high temperature. The best device performance emerges at a preheating temperature of 100°C. It may be noted that the ‘real’ CIGS temperature under the sputtering target is probably higher than the substrate preheating temperature.

4.6 Interconnection

4.6.1 Evaluation of i-ZnO/Mo

In our normal module process, we use n-ZnO as interconnection between Mo back contact and ZnO front contact of the next segment. One disadvantage of this process is that we have to break vacuum for the 2nd (CIGS) scribe after i-ZnO and before n-ZnO. As an alternative, we could perform the 2nd (CIGS) scribe first and simply deposit i-ZnO followed by n-ZnO without breaking vacuum. This would entail trying to use i-ZnO plus n-ZnO as interconnection to the Mo. The higher resistance of i-ZnO is a concern in this case. However, it could conceivably not be a problem since there is no obvious huge resistance jump after coating i-ZnO on CTO due mainly to its thinness (about 500A-1000A). To test this idea, four mini-modules were processed for comparison. On two of them the n-ZnO/Mo interconnection is used as a reference, while on the other two the interconnection n-ZnO/i-ZnO/Mo is tested as an experiment. The performance results are listed in Table VIII.

Table VIII. Mini-module performance with i-ZnO or n-ZnO as interconnection to Mo

ID	Interconnection	V_{oc} (V)	V_{oc}/seg (mV)	FF %	J_{sc}(aper) (mA/cm^2)	Eff.(aper.) %	Eff.(active) %
Z1565-41	n-ZnO	7.52	537	54.8	32.5	9.6	10.9
Z1565-42	i-ZnO+n-ZnO	6.62	509	38.8	31.7	6.3	7.1
Z1565-51	i-ZnO+n-ZnO	8.03	535	43.2	30.3	7.0	8.0
Z1565-52	n-ZnO	6.99	499	53.0	34.3	9.1	10.3

The results clearly show that our normal process using n-ZnO as the interconnection is superior to i-ZnO+n-ZnO. The noticeably different module FF indicates that i-ZnO is indeed too resistive for the first layer of interconnection and leads to unacceptable contact resistance.

4.6.2 New ZnO configuration for interconnection

The disadvantage of using the conventional i-n, two-layer ZnO structure in conjunction with the interconnection between the ZnO front contact and the Mo back contact is that we have to break vacuum for the 2nd (CIGS) scribe after depositing the i-ZnO and before depositing the n-ZnO. This awkward vacuum break is the least time-effective process during the entire module production sequence. Many other groups, such as ZSW/Wuerth Solar [12], are also actively seeking a better process. We have tried scribe #2 followed by i-ZnO+n-ZnO as an alternative. However, the FF of mini-modules with such an interconnection appears much worse than that with a n-ZnO interconnection. This is due to a larger contact resistance at the interconnect, as reflected in the J-V curve. This large interconnection resistance was also confirmed by directly measuring the ZnO/Mo voltage drop over the interconnection line with the module forward biased (see Table X below).

During Phase II, a new type of ZnO configuration was conceived and evaluated at EPV for use in an interconnection process without vacuum break. It not only maintains device performance at the level of the normal two-layer ZnO, but it also yields a small interconnect resistance like n-

ZnO. This configuration allows the processing sequence CBD CdS, followed right away by the CIGS scribe, followed by the new type of ZnO without vacuum break, followed by the ZnO scribe.

Listed in Table IX are two set of J-V test data comparing the new type of ZnO with the normal two-layer ZnO. There are eight pairs of devices in Table IX altogether. The two devices in each pair have the normal and new ZnO for comparison. The devices in each pair are spaced only 1mm apart to eliminate any effect of CIGS non-uniformity.

Table IX(A). Performance comparison of Z1559-51

	Voc		FF		Roc (norm)	
Z1559-51	Normal	New	Normal	New	Normal	New
1	525.8	549.9	58.96	67.86	0.156	0.123
2	555.6	555.7	65.09	66.96	0.127	0.113
3	554.4	561.4	59.97	66.42	0.137	0.118
4	541.4		60.71		0.142	
Average	**544.3**	**555.7**	**61.2**	**67.1**	**0.141**	**0.118**

Table IX(B). Performance comparison of Z1559-32

	Voc		FF		Roc (norm)	
Z1559-32	Normal	New	Normal	New	Normal	New
1	460.5	468.9	60.01	63.76	0.163	0.12
2	454.6	470.8	56.63	62.53	0.208	0.137
3	456.9	460.2	58.71	62.33	0.152	0.142
4	453	458.2	60.75	60.73	0.162	0.139
Average	**456.3**	**464.5**	**59.0**	**62.3**	**0.171**	**0.135**

The data in Table IX clearly show that the device performance obtained with the new type of ZnO is at least as good as that with normal two-layer ZnO. In fact, an improvement of FF is apparent, and V_{oc} is a little higher, too. The improved FF is due mainly to the lower series resistance, as reflected in the value of R_{oc}(normalized) shown in the far right column.

Encouraged by its performance, we used the new type of ZnO to form the interconnects in mini-modules. Listed in Table X are seven mini-modules processed with three different processes for the ZnO interconnection, namely, the normal process (H188-2, H190-4 and H190-5), the new type of ZnO (H188-4, H190-2 and H190-3), as well as the failed process (H188-3) with the i-ZnO+n-ZnO interconnection mentioned earlier in section 4.6.1. Their interconnection resistances were determined by measuring the voltage drop at ZnO/Mo under forward bias.

The interconnect resistance for all three mini-modules in the new process group is in the range of 0.13-0.36 ohm, which is as good or better than that for the normal group (0.4-1.28 ohm) within experimental error. The resistance yielded by the failed process using i-ZnO plus n-ZnO jumps to 10 ohm, more than an order of magnitude higher. Similar experiments, both at the device level and module level, have now been repeated several times at EPV. It remains to be seen whether the new ZnO configuration can ultimately replace the conventional two-layer ZnO (and eliminate the vacuum break) in large area module production.

Table X. Interconnect resistance for seven mini-modules

Sample ID	ZnO type	CIGS scribe after	Interconnection	Resistance (Ω)
H188-2	Normal process	i-ZnO	n-ZnO	0.4
H188-3	Failed Process	CdS	i-ZnO/n-ZnO	10
H188-4	New Process	CdS	New type ZnO	0.13
H190-2	New Process	CdS	New type ZnO	0.36
H190-3	New Process	CdS	New type ZnO	0.36
H190-4	Normal process	i-ZnO	n-ZnO	0.44
H190-5	Normal process	i-ZnO	n-ZnO	1.28

4.6.3 Status of large area ZnO process for modules

We were very excited by the improvement of ZnO properties at elevated substrate temperature reported in section 4.5. Also, we were encouraged by the annealing results for devices, which indicated our junction would survive up to 150 °C in vacuum. So we were rather confident that the process combination, i.e. sputtering ZnO on devices at an elevated substrate temperature, would work well.

To our dismay, devices made recently with ZnO using pulsed DC power in a reactive (conditioning) O_2 environment failed to work at any elevated temperatures, even as low as 60 °C substrate temperature in most cases. It is not yet clear if it is an intrinsic difficulty due to DC pulse/reactive mode or just a simple problem such as a damaged junction resulting from degassing at elevated temperature. Some tests are planned for the next quarter. Another puzzle associated with reactive sputtering operated in DC pulsed mode is that our new type of ZnO for interconnects, which works very well for RF sputtering, also failed to work in the in-line system. Other groups also have expended considerable effort in developing suitable ZnO layers, e.g. Showa Shell Sekiyu reports use of a tri-layer structure [13].

For the time being, then, we have to deposit large area ZnO using our previous standard conditions. The film (on glass) looks somewhat yellowish due to optical absorption in the blue part of the spectrum, and the sheet resistance is higher than desired. Another confounding effect is that the sheet resistance of such ZnO films deposited on CdS increases substantially in some cases compared to films deposited on plain glass. Using this kind of ZnO in the module process, we have to increase its thickness to reduce its resistance, and that results in reduction of module current due to optical absorption loss in the ZnO. The ZnO process thus remains one of the main problems in our module production, and will be attacked again in Phase III.

5.0 Module performance

We made six rounds of pilot-line runs in the last quarter with a maximum throughput of six pieces of 1 ft^2 modules per week. For most of the plates, all process steps were completed and their I-V curve measured, while a few plates terminated at some process stations due to obvious operation problems. Listed in Table XI are some results of the module performance in each round.

Table XI. 1 ft^2 module performance

Round	ID	Mod. V_{oc} (V)	V_{oc}/cell (mV)	Mod. FF(%)	Mod. I_{sc} (A)	J_{sc} (ap.) (mA/cm^2)	Efficiency (%; ap.)	Power (W)	R_{oc} (nor)
0	Z1606B	23.9	478	24.5	0.302	18.9	2.21	1.77	0.99
1	Z1609A	24.6	491	44.5	0.293	18.3	4.01	3.21	0.42
2	Z1616B	22.7	454	44.9	0.328	20.5	4.18	3.34	0.38
3	Z1622A	25.2	503	48.3	0.363	22.7	5.51	4.41	0.34
3	Z1622B	26.2	523	47.1	0.331	20.7	5.09	4.07	0.39
4	Z1623A	22.3	446	47.1	0.307	19.2	4.04	3.23	0.31
5	Z1625A	25.7	514	50.3	0.320	20.0	5.17	4.13	0.36
5	Z1625B	26.3	525	55.2	0.298	18.6	5.38	4.31	0.24

Each module consists of 50 segments with a cell width 5.58 mm and an aperture area around 800 cm^2. The values shown in Table XI are before lamination, and the current density and efficiency are aperture area values. The module test results demonstrate that we have been able to repeatedly produce 1 ft^2 modules with reasonable performance in a very short period. For these modules, we fully realize that our major performance problems stem from mediocre FF due in large part to large series resistance (see normalized R_{oc} in the far right column), while low short-circuit current density J_{sc} deteriorates the performance further. We discuss these problems and their root cause in Sec. 6. Light and dark I-V curves for module Z1625B are plotted in Fig 7.

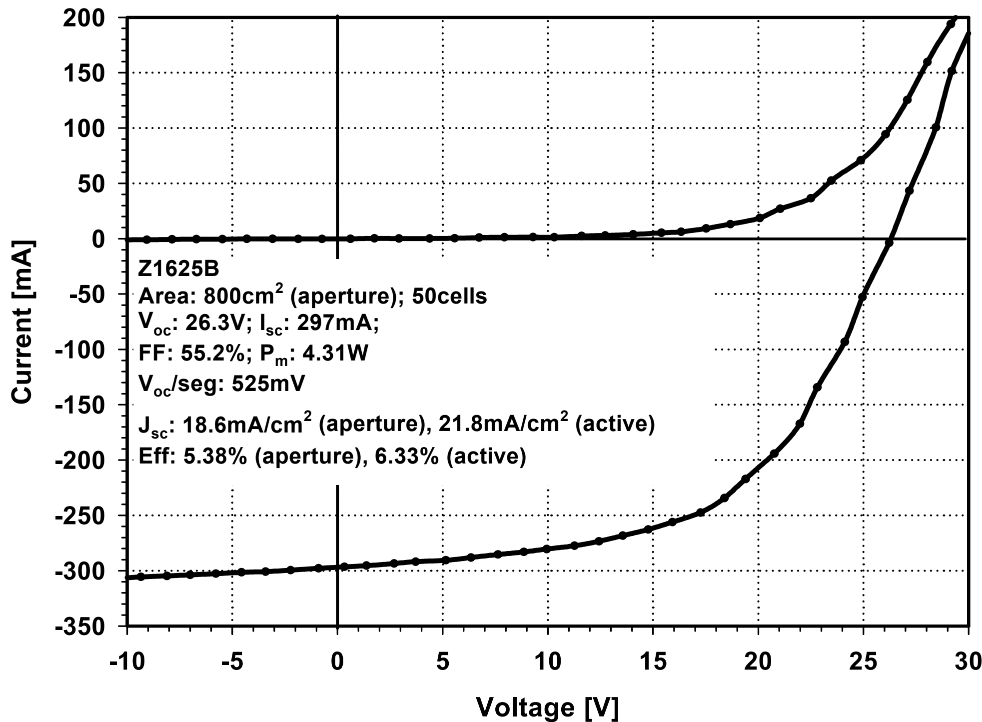


Fig. 7. Light and dark I-V curves for 1ft^2 module Z1625B (5.4% aperture area efficiency)

It is worth noting that we have reached over 5 % efficiency on both pieces (A & B) of 1 ft^2 plate from runs Z1622 and Z1625. As mentioned earlier, these two pieces underwent processing on

full size equipment except for CdS deposition, where we had to cut a larger size plate to obtain two 1 ft^2 pieces to fit the dipping tank. We therefore believe that we are well-positioned to make the larger size modules with over 5 % efficiency in the first quarters of Phase III after our CBD CdS process in the new large tanks is developed and optimized and after patterning registration problems are solved.

6.0 Quality control, module analysis and modeling

6.1 Quality control steps

The key to making reproducible modules with good performance is that *all* components in the process line have to be reproducible. At EPV, we have established rigorous quality controls for each module process step. Listed in Table XII are some main quality control steps in our process line.

Table XII. Quality control steps on process line

Process	Measurement	Purposes
Mo deposition	Measure sheet resistance and thickness	Process reproducibility
Mo Laser scribing	Resistance between Mo	Check separation of Mo
First IGS evaporation	Thickness distribution on a strip (every 4”)	Process reproducibility and uniformity
Sputter Cu	Thickness distribution on a strip (every 4”)	Process reproducibility and uniformity
Cu on the first IGS	Composition by ICP on a strip (every 4”)	Check Cu ratio to make sure Cu rich regime is reached
After second IGS evaporation	Total CIGS thickness on a strip (every 4”)	Process reproducibility and uniformity
	Composition by ICP on a strip (every 4”)	Check Cu and Ga ratio and uniformity
	Vertical resistance on a strip (every 4”)	Quick check of Cu ratio
	Lateral resistance between two ends of separated Mo segments	Check possible shunting path through CIGS between Mo pads
CBD CdS	Optical transmission at 420 nm and 440 nm co-deposited on CTO glass	CdS film thickness
	Lateral resistance between two ends of Mo	Check possible shunting path through CIGS between Mo pads
CIGS patterning	Check cutting under microscope	Line quality
Sputter ZnO	n-ZnO sheet resistance and transmission co-deposited on plain glass	ZnO performance
	Sheet resistance on Cds of modules	ZnO performance on CdS
ZnO patterning	Check cutting under microscope	Line quality

A travel sheet recording all individual process steps and procedures is assigned to each 1 ft^2 module. The travel sheet raises an early warning signal if any process shows abnormal operation, and is very helpful for post I-V analyses. It may be noted that the composition of the CIGS produced in every run is currently measured by ICP AES in order to maintain composition

in the face of possible deposition rate drift. Such drift has been carefully documented by Shell Solar in the case of In sputtering [14].

6.2 Module analysis

We also thoroughly analyzed one 1 ft^2 module after I-V measurement in each round to extract further useful information including:

a) Performance comparison of mini-modules and devices passed through different process lines to crosscheck individual processes.
b) Mapping of device performance on two sides of the module to check module uniformity.
c) Measurement of ZnO sheet resistance on CdS on each cell by voltage drop method to find out if ZnO is responsible for the large series resistance of the module.
d) Measurement of interconnection resistance on each line by voltage drop method to find out if contact resistance or conformal coverage contributes to the series resistance of the module.
e) V_{oc} and dark leakage current under reverse bias on each cell to reveal shunting paths.

An example of the module analysis summary sheet for Z1625 for steps a) and b) above is shown in Table XIII.

Table XIII. Module Z1625 analysis sheet
Performance of modules and devices cut from large plate

Pieces (Dist.)	Device Voc (A)	Device Voc (B)	Voc P1/P2/ P3	Device FF (A)	Device FF (B)	FF P1/P2/ P3	Device J_{sc} (A)	Device J_{sc} (B)	Jsc P1/P2/ P3	Device Eff. (A)	Device Eff. (B)	Eff. P1/P2/ P3
P1 (0)	516	515	392	64.27	62.27	45.61	24.81	23.84	26.17	8.22	7.64	**4.67**
P1 (10)	533	505	507	66.63	66.99	58.18	23.97	24.65	26.63	8.51	8.33	**7.85**
P2 (20)	507	508	544	64.74	62.23	62.4	23.13	22.3	22.13	7.59	7.04	**7.52**
P2 (30)	524	532	528	66.6	66.55	61.0	23.91	22.41	23.8	8.34	7.93	**7.65**
P3 (40)	514	519	533	63.26	67.02	59.54	23.87	22.9	26.89	7.76	7.97	**8.53**
P3 (50)	514	506	496	68.72	66.74	56.73	23.64	24.09	28.31	8.35	8.14	**7.97**
Avg	**518**	**514**	**482**	**65.7**	**65.3**	**55**	**23.9**	**23.4**	**27**	**8.1**	**7.8**	7
Median	**515**	**511**	**501**	**66**	**67**	**57**	**24**	**23**	**27**	**8**	**8**	8
ModuleA	**514**			**50.3**			**20.0**			**5.17**		
ModuleB		**525**			**55.2**			**18.6**			**5.39**	
Mini-Mo. P2			405			23.0			14.2			1.32

As indicated in the module layout figure in Section 3.0, we also cut from the full size plate three pieces (P1, P2, P3) of size 2" x 4" from a strip adjacent to 1 ft^2 module A. All three pieces are dipped in a glass beaker for CdS CBD. Pieces P1 and P3 are then processed in our device line with RF ZnO deposition in Airco, while piece P2 is processed as a mini-module with in-line ZnO deposition. Listed in Table XIV is the process comparison for these pieces as well as the 1 ft^2 modules A & B.

Table XIV. Process comparison for devices and modules

Piece	Process as	CdS	ZnO	CIGS/ZnO scribe	Measure as
P1 and P3	Devices	Beaker	Airco (RF)	No	Device
P2	Mini-module	Beaker	In-line (pulsed DC)	By hand	Module & device
1 ft^2 A & B	Module	Tank	In-line (pulsed DC)	X-Y table	Module & device

After comparing the various module and device performance data, a lot of important information can be extracted such as:

- The effect due to different mechanical scribing (hand and machine) and module uniformity can be seen by comparison of 1 ft^2 module and mini-module performance. For instance, in this run (Z1625) we found our hand scribing had a problem resulting in high R_s and low fill factor on the mini-module and small area, reverse-connected parasitic cells that lower V_{oc}.

- The effect due to different containers (beaker and tank) for CdS deposition can be obtained by comparison of devices' performance defined from 1 ft^2 module and mini-module. For example, we found device performance processed in large tank is as good as that in small beaker.

- The effect due to ZnO film deposited with different power sources (RF power in Airco and pulsed DC power in in-line) can be observed by comparison of devices' performance from pieces P1 and P3 with piece P2. For example, we found a severe drop of J_{sc} with ILS ZnO to 23 mA/cm^2 from the 28 mA/cm^2 obtained with Airco ZnO.

- By comparison of module and device performance, we found: the V_{oc}/cell is basically equal to device V_{oc} indicating that any shunting effects in our module are small; the J_{sc} drop to 19 mA/cm^2 from 23 mA/cm^2 is due to dead area loss; FF has an 18 % drop to 55 % from 67 % and is due to series resistance. Therefore, we have to quantify the contributions from ZnO sheet resistance and interconnection resistance.

Firstly, we directly measured ZnO sheet resistance on CdS and found it was about 11-13 ohm per square, which is very good. To confirm this, the resistance distribution of ZnO on each cell and interconnection resistance on each line in the module Z1625A were measured as in steps c) and d) above and are plotted in Fig. 8.

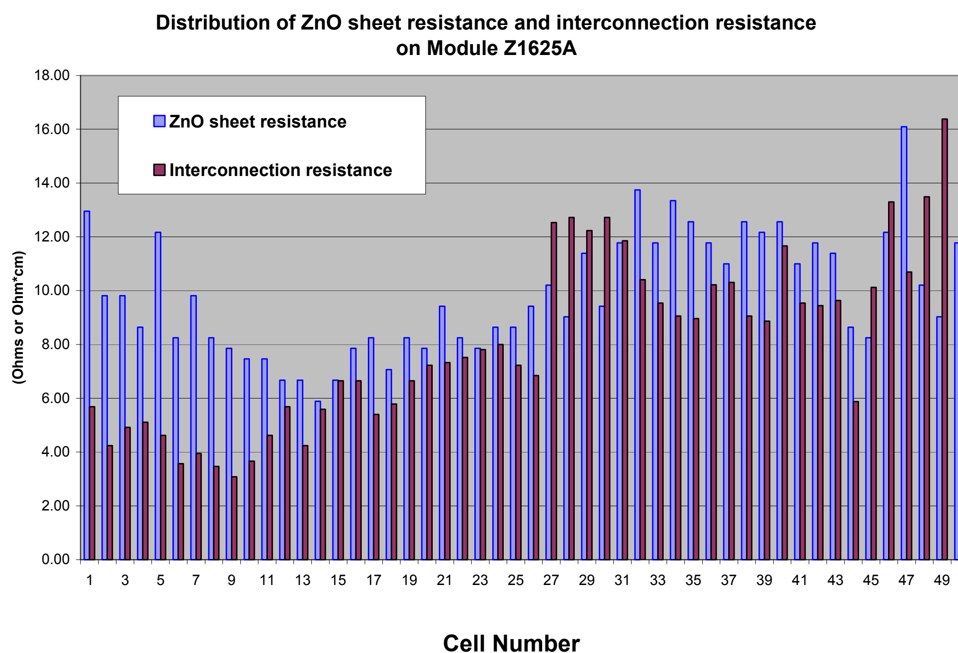


Fig. 8. Resistance distributions for ZnO and interconnects

6.3 **Modeling**

The median value for ZnO sheet resistance from the distribution is about 9-10 ohms per square, close to the value from direct measurement. Having input these values into our modeling program, the calculation predicts a FF drop of 5-6 %. The median value for interconnection resistance is about 7 ohm*cm, which reduces FF about 13-14 % according to the modeling, a value larger than we expected. Upon summing the losses from these two factors, we obtained excellent consistency between modeling and experimental data. After the detailed module analysis, we had a clear picture of our process and could draw the conclusion that the main series resistance problem in this particular module results from the interconnects. Many thoughts and ideas were brought out by the team, and more experiments are planned for the next quarter.

To further verify that module shunting is not a significant problem, we measured V_{oc} and leakage resistance distribution as step e), and these are plotted in Fig. 9. A very uniform V_{oc} distribution in module Z1625A can be seen, while the shunting distribution shows higher resistances in the middle of module. Even inputting the lower leakage resistance value of about 500 ohms found at the module edges into the model, we calculate the power loss from shunting to be less than 1 %, a remarkable result.

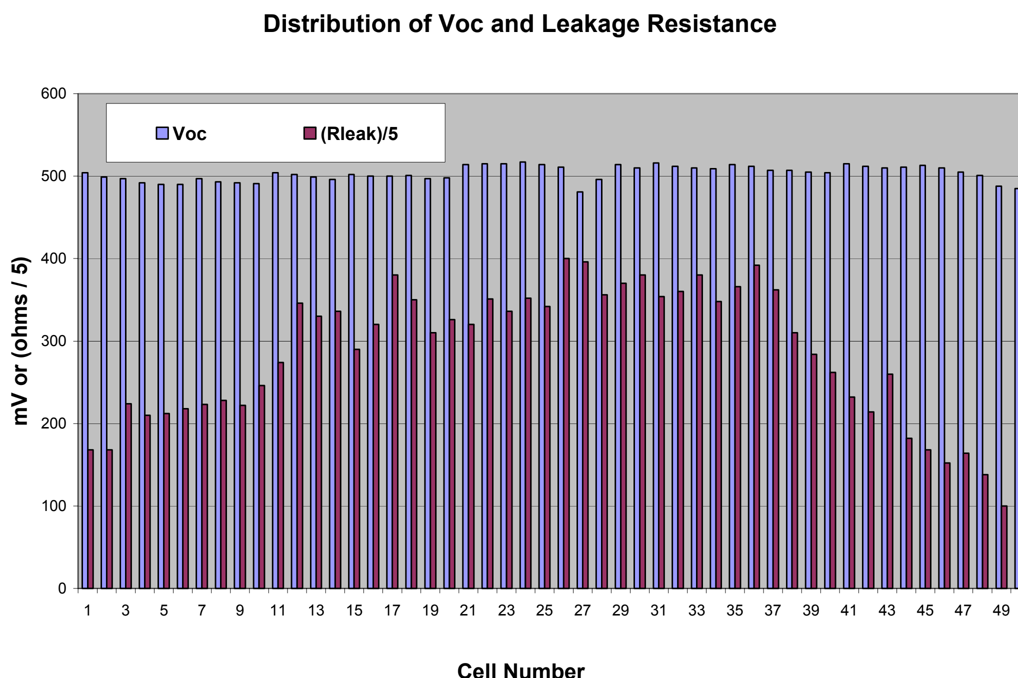


Fig. 9. V_{oc} and leakage resistance distribution

We strongly believe systematic process quality control and module analysis are powerful methods to identify, and then help solve, processing problems.

7.0 Progress Overview for Hybrid CIGS

We embarked upon development of the hybrid process involving sputtered Cu at the beginning of this subcontract. EPV's overall progress to date during this subcontract is shown on the time

line of Fig. 10, which shows the successive development of hybrid CIGS material, and best efficiency for hybrid CIGS cells, mini-modules, and square foot modules. Full size modules will be fabricated starting in Q1 of Phase III.

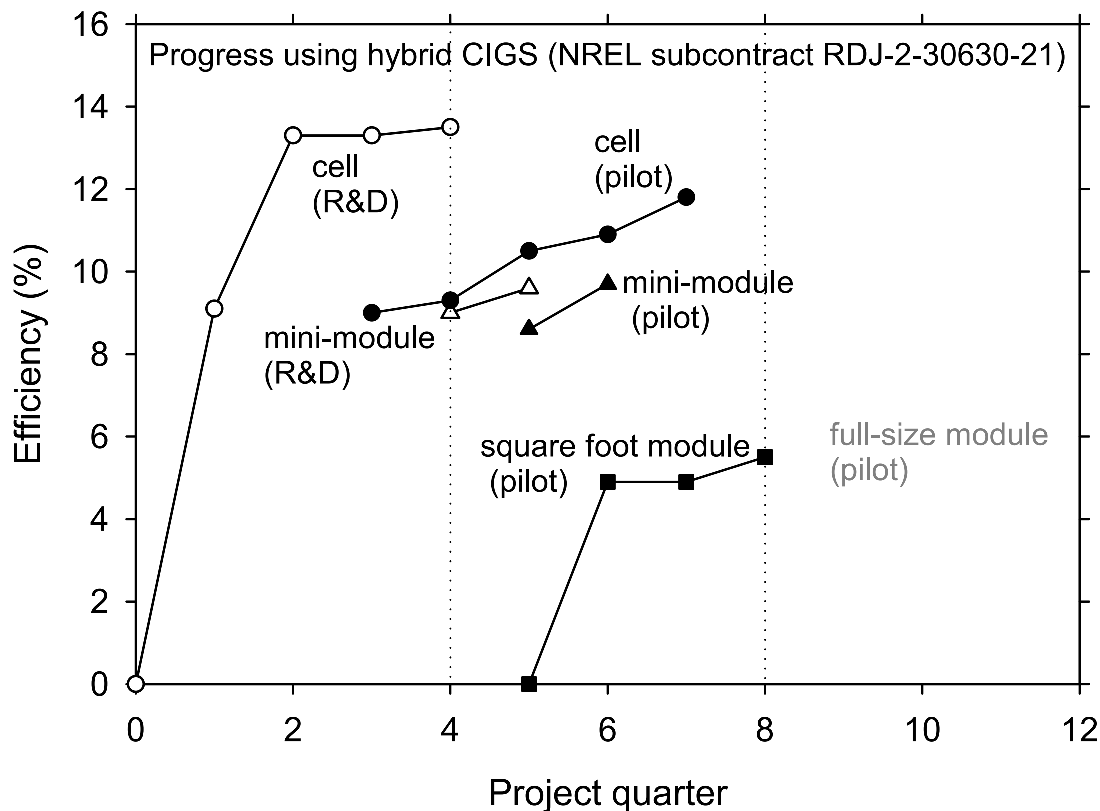


Fig. 10. Graphical illustration of progress during subcontract, showing successive development and efficiency of hybrid CIGS cell, mini-module, square foot module, and full size module.

8.0 Cell Studies

8.1 Assessment of cell processing

Following the introduction of a post-CIGS treatment and adoption of a re-optimized CBD recipe, it became of interest to assess the performance of these junction formation techniques on a sample of high quality, three-stage CIGS prepared by NREL. Sample S2061 was provided by Kannan Ramanathan, and Fig. 11 shows the I-V curve of a device prepared at EPV on this sample of CIGS. A device efficiency of 15.1 - 15.5% (without collection grid or AR coating) was achieved [10]. This was considered sufficiently high to validate the quality of EPV's CdS and ZnO recipes.

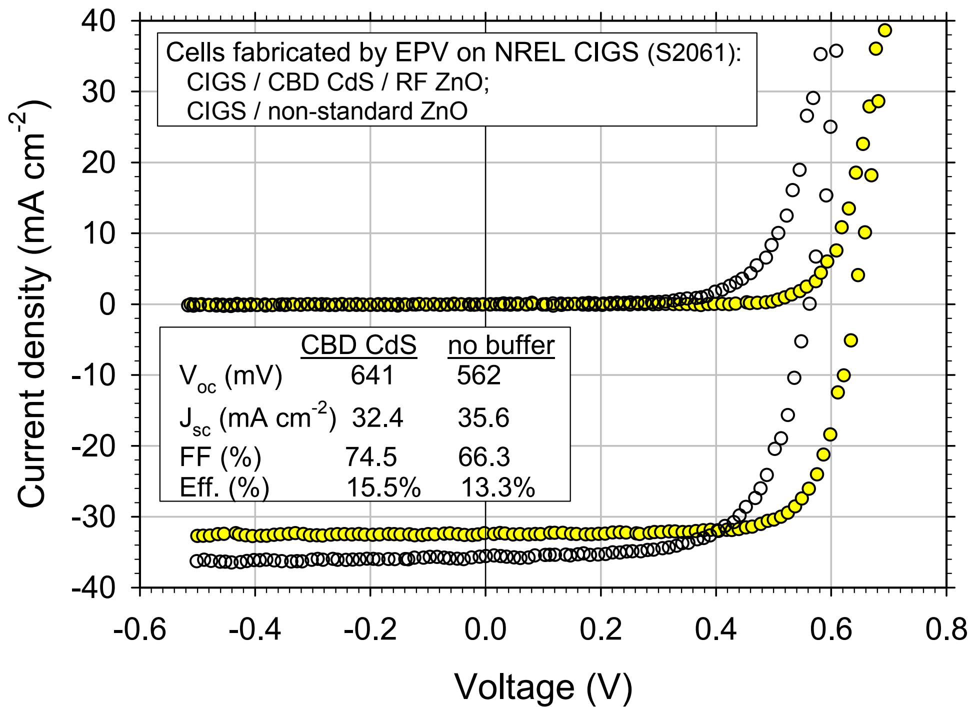


Fig. 11. J-V curve of cells fabricated by EPV on NREL CIGS: 15.5% with CdS buffer and RF ZnO; 13.3% with no buffer and HC deposition of ZnO.

8.2 New processing for window layer/TCOs

The hollow cathode (HC) sputtering system developed under EPV's ATP award with NIST has been used to prepare several types of transparent conducting oxide [15,16]. These TCOs have been applied to CIGS with various buffer layers to fabricate devices. Some of the results are collected in Table XV. In the "Buffer" column, T denotes a CIGS post-deposition treatment.

Table XV. Selected device results using HC-sputtered TCO

HC run	CIGS sample #	TCO	Buffer	i layer	Power (W)	T (°C)	V_{OC}	J_{SC}	FF (%)	η (%)
148	H146	ZnO	No CdS	N	300	100	444	31	56	7.7
539	NREL	ZnO:B	T/No CdS	Y	300	155	564	36	63	12.7
547	Hercules	ZnO:B	CdS	Y	300	120	510	29	65.5	9.6
554	H224	ZnO:B	T/ZIS+	Y	300	120	428	32	48	6.6
786	Z1574-I	In_2O_3:Mo	T/CdS	N	180	150	322	25	45	3.6
	Z1607-5	In_2O_3:Mo	T/CdS	N			476	27	64	8.2

The first two entries in Table XV have been reported previously. The third entry shows a 9.6% cell using HC-sputtered ZnO:B and a CdS buffer, and the fourth entry 6.6% using a $ZnIn_2Se_4$ buffer. Excellent In_2O_3:Mo TCO layers have been produced by HC sputtering [15], but early cell results were disappointing (fifth entry, 3.6%). More recently, devices up to 8.2-8.4% have

been prepared using In_2O_3:Mo TCO layers (see last entry in Table XV and I-V curve in Fig. 12) [17]. Work in this area will be continued.

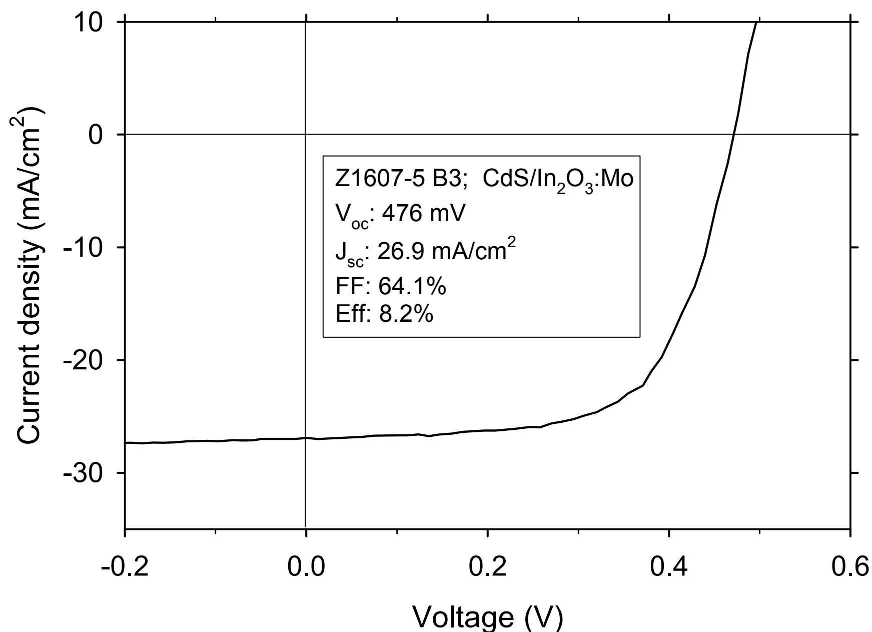


Fig. 12. J-V curve for CIGS cell with IMO TCO

8.3 Experiments concerning the temperature resistance of junctions

What are the maximum temperature/time exposures a CIGS junction can sustain? This kind of information is needed for ZnO deposition optimization at elevated temperature, as mentioned in section 4.5 above. Similar information and testing is required to design a process for top junction deposition in a tandem structure for advanced high performance cells.

In this period, two more annealing experiments were conducted. First, a normal CBD CdS layer was deposited on CIGS samples to form the device junction. Then the samples were annealed for half an hour at elevated temperatures in either a vacuum or N_2 environment. Finally, the devices were finished with normal RF sputtered, two-layer ZnO. In both environments the devices' performance deteriorated at high temperature. However, the observed threshold was quite different. As can be seen in Fig. 13, the performance of devices annealed in N_2 was maintained even at annealing temperatures as high as 200°C, while that of devices annealed in vacuum declined dramatically between 140-170°C. Thus far, it is not clear what causes the difference.

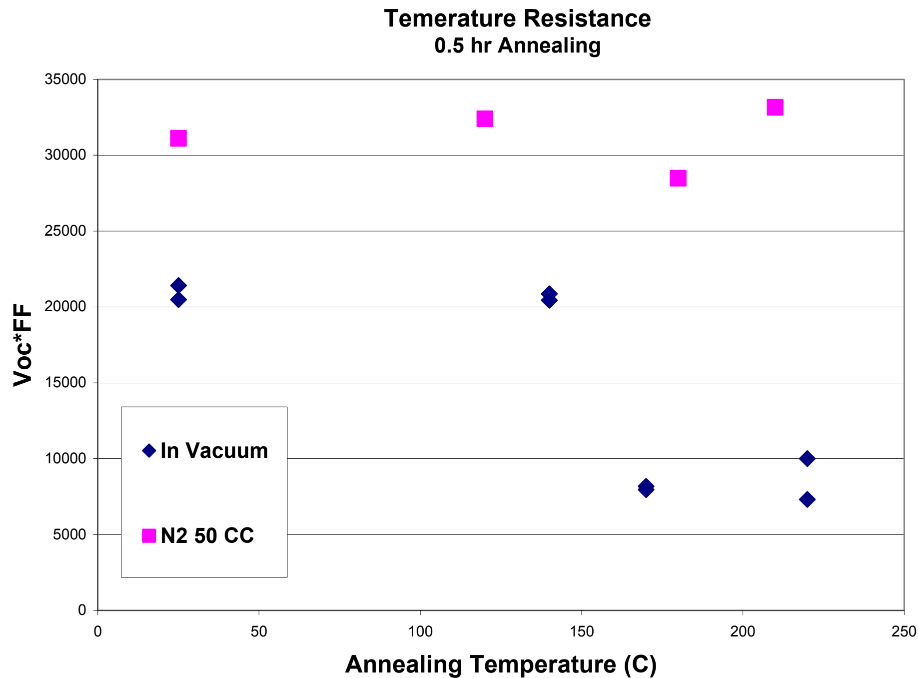


Fig. 13. V_{oc} x FF product for junctions annealed at various temperatures before ZnO deposition

9.0 Module reliability

Module reliability is an important concern of the PV industry, and the various thin films face particularly challenging issues in order to demonstrate reliability. A recently-organized National Team (Thin Film Module Reliability National Team) is focused on these issues, and EPV is one of the active contributors in both the Si thin film and polycrystalline thin film areas. In the former area, EPV has reported longevity data for a-Si:H modules [18] and a laboratory technique for quantifying TCO resistance to delamination [19]. EPV is also active in studying and reporting on glass breakage susceptibility, an effort that is applicable to both thin film areas [20].

In the area of CIGS, work in Germany has revealed damp heat degradation of ZnO (plus interaction with the CdS) and also Mo corrosion [21]. Another study observed the creation of deep states in the surface region of the absorber [22]. The Uppsala group has observed degradation of the ZnO:Al/Mo interconnect [23]. In the CIGS group of EPV, we recently started a damp heat (DH) program for various TCOs (including ZnO, SnO_2 and In_2O_3) with the intention of extending the work to devices and modules. The motivation is to study how DH impacts TCO properties, especially resistivity. As a first step, we investigated the effect of water immersion. All films were deposited on plain glass. The ZnO:Al was prepared by RF sputtering, the In_2O_3:Mo by hollow cathode sputtering, and the SnO_2:F was procured commercially. Most of the samples were un-laminated except for one ZnO sample that was laminated with EVA and a top glass sheet. De-ionized water temperatures of 25°C and 60°C were selected. Plotted in Fig. 14 is the measured CTO sheet resistance as a function of immersion time. As can be seen from the figure, the resistivity of un-laminated ZnO keeps increasing with immersion time, while that of laminated ZnO basically doesn't change even at 60°C. In contrast to un-laminated ZnO, the

resistivity for un-laminated SnO_2:F and for In_2O_3:Mo both appear stable even for immersion at 60°C.

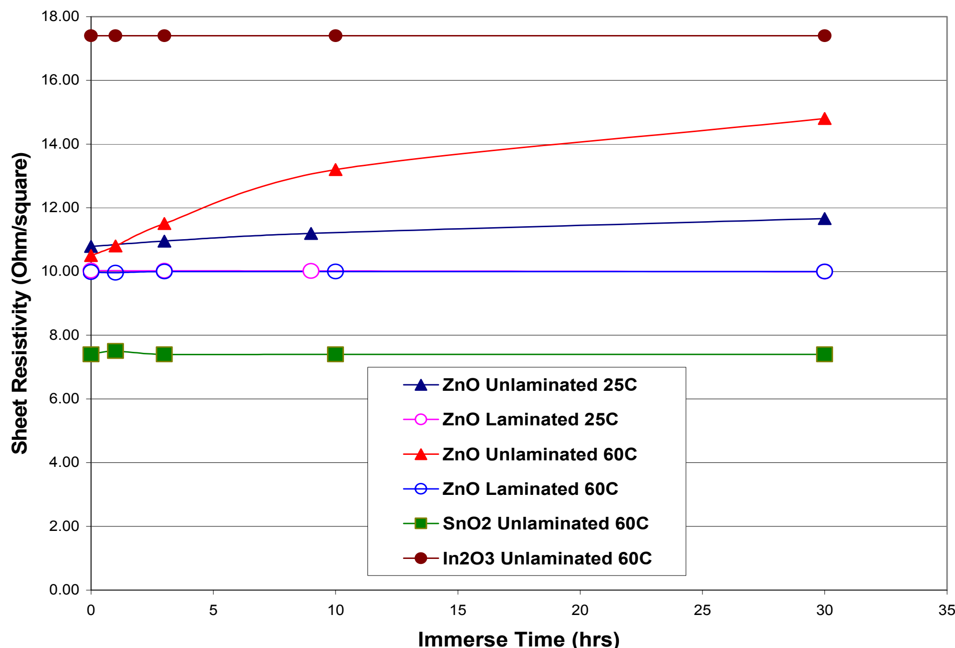


Fig. 14. Sheet resistance of various TCO samples versus water immersion time

10.0 Safety

Several safety-related issues were addressed during this Phase. The issues concerned possible emissions from the Zeus system, the CBD set up for CdS, and glass storage.

Firstly, specialized consulting firms, Air Consulting Services and Princeton Analytical, were hired to conduct an air test for total nuisance particulates, the metals selenium, indium and gallium, their selenides, and hydrogen selenide in the area adjacent to the Zeus deposition chamber. In particular, samples were drawn immediately after venting the main chamber and the antechamber. The test results indicated that the concentration of all of these metals, selenides, gases, and particles were below the OSHA PEL (Permissible Exposure Limit).

Secondly, a set of detector tubes for the Matheson-Kitagawa hydrogen selenide detector system were purchased for use as an in-house routine tester during the venting of the antechamber (load-lock) for loading and unloading large plates. No concentration of concern was detected thus far.

Thirdly, more cautious procedures have been imposed for the venting of the main chamber and antechamber of Zeus. Pre-vent cycles of purging and pumping have been implemented to reduce the level of any possible harmful gases or airborne particles. A new exhaust system for the Zeus with a filter and blower has been designed and should be finished soon.

An improved large area chemical bath deposition station has been set up with a total of four large tanks. The main motivations for discarding the old station and building the new one were to

streamline the handling of the plates and to reduce spillage or dripping of the solutions used, to improve the removal of ambient air, as well as to improve deposition uniformity.

All employees who perform processing in which air quality is of concern have been provided with appropriate masks.

The storage of glass sheets on the R&D racks has been improved by adding safety bars to the racks to eliminate the possibility of glass slipping off.

11.0 Some plans for the initial quarters of Phase III

- Improve large area CIGS composition uniformity by rebuilding the Ga delivery line.
- Optimize Na for the hybrid CIGS process.
- Utilize the full size (0.43 m^2) dipping tanks for CBD CdS and characterize the results.
- Continue to explore the use of hollow cathode sputtering for TCO deposition.
- Investigate whether some non-obvious effects are influencing ZnO:Al resistivity.
- Improve large area ZnO properties while maintaining low interconnect resistance.
- Install a vision system on the X-Y table to help reduce dead area loss in patterning.
- Find the best way to scribe the CIGS line with contact resistance less than 1 ohm*cm.
- Fabricate both 1ft^2 and full size CIGS modules.
- Continue to improve module encapsulation and resume life testing.

Most of these planned activities are direct extensions of work in progress. The immediate focus is to realize module power potential through improvement of the back-end operations of patterning and TCO deposition. It is felt that most of the problems that can plague module production have been identified and are sufficiently well understood to enable good progress to be made in Phase III. In addition, since Na transmission through the Mo into the absorber is known to influence device performance [24], a fresh look at whether our levels of Na remain appropriate for current processing will be undertaken.

Note added in proof: The above photo shows a recently-made, full-size, hybrid CIGS module

12.0 Phase II Summary

EPV, Inc.
Advanced CIGS Photovoltaic Technology
Subcontract No. ZDJ-2-30630-21

- **EPV continued to improve the performance of CIGS prepared by a *hybrid process* that involves evaporation of In and Ga and sputtering of Cu. The process shows good reproducibility, and shows promise for being manufacturable.**

- Both in-situ and ex-situ sputtering of the Cu have been successfully utilized to form high quality CIGS by the hybrid process.

- Diagnostic devices formed on large area ($0.43m^2$) CIGS prepared by the hybrid process have been produced with V_{oc}s as high as 659mV, and efficiencies up to 11.8%.

- Devices processed through a Cu-rich stage demonstrated higher V_{oc}.

- 10.1% devices were prepared by an exploratory process that involves evaporation of IGS compound and Cu sputtering.

- The CBD process for CdS was improved through adoption of a slow reaction. This improved uniformity.

- Annealing the CIGS/CdS before ZnO deposition was shown in some experiments to be beneficial to device efficiency and to reduce the light soaking effect.

- Improved ZnO properties were obtained at elevated substrate temperatures, but so far the process has resulted in inferior device performance in the most cases.

- The type of ZnO best suited to the ZnO/Mo interconnection has been investigated and important rules have been developed.

- Large area module processing was restored, and reasonably reproducible $1ft^2$ modules were produced relatively quickly in the 5.0 -5.5% efficiency range.

- Extensive QC checks and module analysis procedures were implemented. Non-idealities in module fabrication were shown to introduce parasitic circuit elements.

- A 15.5% cell (with CdS) was fabricated by EPV on bare NREL CIGS, and a 13.3% cell was fabricated using no CdS but with hollow cathode sputtering of the ZnO.

- An 8.2% cell (with CdS) was fabricated on EPV CIGS using IMO instead of ZnO.

- Water immersion tests indicated superior stability of IMO relative to ZnO.

ACKNOWLEDGMENTS

This research was carried out by EPV's CIGS group: Dr. M. Akhtar, J. Cambridge, Dr. L. Chen (Group Leader), Dr. A. Delahoy (Principal Investigator), R. Govindarajan, Dr. S. Guo, S. Kleindienst, Dr. B. Sang, R. Saramak, and F. Ziobro. The Company wishes to thank all members for their sterling work. Notable technical support was also provided by A. Foustotchenko, R. Lyndall, and J. Allen (consultant), as well as by manufacturing, equipment development, facilities, and the machine shop.

The following individuals (and institutions) are also acknowledged for their analyses, advice, or interest: S. Asher, K. Ramanathan, R. Noufi, H. Ullal, K. Zweibel (National Renewable Energy Laboratory); J. Sites (Colorado State University); A. Rockett (University of Illinois); W. Shafarman (Institute of Energy Conversion/University of Delaware); T. Anderson, S. Li (University of Florida); Neelkanth Dhere (University of Central Florida).

Thanks are due also to all members of the National CIS Team for their collaborations and discussions.

Finally, EPV thanks the US DOE for support under subcontract ZDJ-2-30630-21 with NREL.

REFERENCES

[1] James Groelinger and Alan Delahoy "The Future of Thin Film PV" SolarAccess.com RE Outlook 2003 (Jan. 17, 2003) http://www.solaraccess.com/news/story?storyid=3448

[2] K. Ramanathan, M. Contreras, C. Perkins, S. Asher, F. Hasoon, J. Keane, D. Young, M. Romero, W. Metzger, R. Noufi, J. Ward and A. Duda, "Properties of 19.2% Efficiency ZnO/CdS/$CuInGaSe_2$ Thin-film Solar Cells", *Prog. Photovolt: Res. Appl.* 2003; **11**:225-230.

[3] A.E. Delahoy, J.S. Britt, A.M. Gabor, and Z.J. Kiss, *AIP Conf. Proc. Vol.* ***353*** (AIP, NY, 1996) pp. 3-11.

[4] A. Delahoy, J. Bruns, L. Chen, M. Akhtar, Z. Kiss "Advances in Large Area CIGS Technology," *Proc. 28th IEEE PV Specialists Conference*, September 15-22, 2000, Anchorage, AK, pp. 1437-1440.

[5] A.E. Delahoy, J. Cambridge, L. Chen, and Z. Kiss "Thin Film CIGS Photovoltaic Technology," Final Technical Report, NREL/SR-520-31739 (2002).

[6] A. Delahoy, M. Akhtar, J. Bruns, A. Ruppert, L. Chen, Z. Kiss. "Ternary Source Materials for CIGS Buffer Layers," *Proc. 16th European PVSEC*, 1-5 May 2000, Glasgow, UK, pp. 767-770.

[7] Clas Persson and Alex Zunger "Anomalous Grain Boundary Physics in Polycrystalline $CuInSe_2$: the Existence of a Hole Barrier" submitted to *Phys. Rev. Lett.*, Nov. 2003.

[8] A.E. Delahoy, M. Akhtar, J. Cambridge, L. Chen, R. Govindarajan, S. Guo, and M.J. Romero "CIGS Devices with ZIS, In_2S_3, and CdS Buffer Layers" *Proc. 29th IEEE PV Specialists Conference*, May 20-24, 2002, New Orleans, LA, pp. 640-643.

[9] A.E. Delahoy and L. Chen "Advanced CIGS Photovoltaic Technology" Annual Technical Report, Phase I, Subcontract No. ZDJ-2-30630-21, Jan. 2003.

[10] A.E. Delahoy, L. Chen, M. Akhtar, J. Cambridge, R. Govindarajan, and F. Ziobro "Advanced CIGS Technology," *Proc. NCPV and Solar Program Review Meeting*, Denver, CO, March 24-26, 2003.
[11] M.A. Contreras, J. Tuttle, A. Gabor, A. Tennant, K. Ramanathan, S. Asher, A. Franz, J. Keane, L. Wang, J. Scofield, and R. Noufi "High efficiency Cu(In,Ga)Se_2-based solar cells: processing of novel absorber structures" *Conf. Proc. 1st WCPEC, Hawaii*, 1994, pp. 68-75.
[12] M. Powalla and B. Dimmler "New Developments in CIGS Thin-film Solar Cell Technology" *presented at the 3rd WCPEC, Osaka*, May 2003.
[13] K. Kushiya, B. Sang, D. Okumura, and O. Yamase "Application of stacked ZnO films as a window layer to Cu(In,Ga)Se_2-based thin-film modules" *Jpn. J. Appl. Phys.* **38** (1999) pp. 3997-4001.
[14] R.D. Wieting, "CIS manufacturing at the MW scale" *Conf. Proc. 29th IEEE PVSC*, (2002) pp. 478-483.
[15] A.E. Delahoy, S.Y. Guo, C. Paduraru and A. Belkind, "Reactive-environment, hollow cathode sputtering: basic characteristics and application to Al_2O_3, doped ZnO, and In_2O_3:Mo", *J. Vac. Sci. Technol. A*, accepted for publication.
[16] J. A. Anna Selvan, A.E. Delahoy, S. Guo, and Y-M. Li, "A New Light Trapping TCO for nc-Si:H Solar Cells, *to be presented at the 14th International PVSEC, Bangkok, Thailand*, Jan. 2004)
[17] A.E. Delahoy and L. Chen, *presented at the National CIS Team Meeting, Florida Solar Energy Center*, Nov. 13-14, 2003.
[18] A.E. Delahoy, Y-M. Li, J.A. Anna Selvan, L. Chen, T. Varvar, H. Volltrauer "Massive Parallel Processing for Low Cost a-Si Production", *Proc."PV in Europe: From PV Technology to Energy Solutions" Conference*, Rome, October 11, 2002, pp. 444-447.
[19**]** K. Jansen and A. Delahoy "A laboratory technique for the evaluation of electrochemical transparent conductive oxide delamination from glass substrates", *Thin Solid Films* **422/3**, pp 153 – 160, 2003.
[20] K.W. Jansen "EPV Reliability Update" *presented at the Thin Film Module Reliability National Team Meeting, Albuquerque*, Sept. 2003.
[21] M. Powalla, B. Dimmler "Process development of high performance CIGS modules for mass production" *Thin Solid Films* **387** (2001) 251-256.
[22] C. Deibel, V. Dyakonov, J. Parisi, J. Palm, and F. Karg "Damp-heat treatment of Cu(In,Ga)$(S,Se)_2$ solar cells" *Proc. 29th IEEE PVSC,* (2002) pp.592-595.
[23] J. Wennerberg, J. Kessler, and L. Stolt, "Degradation mechanisms of Cu(In,Ga)Se_2-based thin film PV modules" *Proc. 16th European PVSEC,* Glasgow, 2000, pp. 309-312.
[24] H.A. Al-Thani, F.S.Hasoon, M. Young, S. Asher, J.L. Alleman, M.M. Al-Jassim, and D.L. Williamson "The effect of Mo back contact on Na out-diffusion and device performance of Mo/Cu(In,Ga)Se_2/CdS/ZnO solar cells" *Conf. Proc. 29th IEEE PVSC*, (2002) pp. 720-723.

REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE May 2004	3. REPORT TYPE AND DATES COVERED Annual Technical Report - Phase II 15 November 2002–14 November 2003

4. TITLE AND SUBTITLE
Advanced CIGS Photovoltaic Technology: Annual Technical Report – Phase II, 15 November 2002–14 November 2003

5. FUNDING NUMBERS
PVP45001
ZDJ-2-30630-21

6. AUTHOR:
A.E. Delahoy and L. Chen

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Energy Photovoltaics, Inc.
P.O. Box 7456
Princeton, New Jersey 08543

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
NREL/SR-520-35922

11. SUPPLEMENTARY NOTES
NREL Technical Monitor: H.S. Ullal

12a. DISTRIBUTION/AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words):* The objective of this subcontract is to develop and integrate the various pieces of new technology that EPV considers enabling for cost-effective production of CIGS modules. EPV has conducted research to help generate a technology base for production of CIGS PV modules using vacuum deposition of CIGS onto glass. This strategy is consistent with the observation that, despite there being several approaches to forming device-quality CIGS, vacuum deposition has maintained the world record for the highest-efficiency CIGS device. A record thin-film solar cell efficiency of 19.2% (with Ni-Al grid and MgF_2 ARC) for a 0.41-cm^2 device was achieved by NREL in 2003 using vacuum-deposited CIGS. The deposition employed four point sources and detection of the Cu-poor to Cu-rich transition for process control.
To extend this type of processing to the realm of large-area substrates, EPV developed vacuum equipment designed for heating and coating 0.43-m^2 moving substrates, with a projected further scale up to 0.79 m^2. The substrates are typically low-cost, soda-lime glass, and the materials are supplied to the moving substrates using novel linear-source technology developed by EPV. The use of elemental selenium rather than toxic H_2Se gas helps make for a safe manufacturing environment. These choices concerning film deposition, substrates, and source materials help to minimize the processing costs of CIGS.

14. SUBJECT TERMS: PV; thin film; solar cell; vacuum deposition; Cu(In,Ga)Se_2; CIGS; manufacturer; process control; large-scale process; module reliability; soda-lime glass; magnetron sputtering; linear-source technology; safety

15. NUMBER OF PAGES

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL