June 2004 • NREL/SR-520-36101

Subcontractor Report

Nanostructure Arrays for Multijunction Solar Cells

Final Subcontract Report
12 May 1999–11 July 2002

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West Virginia University
Morgantown, West Virginia

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SUMMARY

This project developed the process technologies for the fabrication of high efficiency multijunction photovoltaic cells using semiconductor nanostructure arrays. These devices are expected to provide increased energy conversion efficiency as well as increased carrier collection efficiency. In addition, this approach provides the ability to tune the absorption spectrum to match selected windows of the solar spectrum. At the same time, these devices can be fabricated using existing industrial electrochemical processing techniques that can substantially reduce the cost of each device. The fabrication technique is based on electrochemical synthesis of II-VI semiconductor quantum wires using a preformed alumina template. This project focused on and solved the technical challenges that need to be addressed for the implementation of such devices. Specific issues addressed include (a) improved pore ordering on thin film templates, (b) synthesis of II-VI semiconductor nanostructures by both AC and DC deposition, (c) an in-situ barrier layer engineering process that allow the fabrication of superior quality materials and improved template/substrate interface, (d) characterization techniques for templates, (e) process technology for creating stacked layers of nanostructures, (f) process throughput and improved apparatus, (g) modeling tools, (h) use of glass substrates, and (i) a nonlithographic surface texturing technique for silicon PV cells. An important outcome of this project is the demonstration of the fabrication technique on glass substrates. This breakthrough provides the possibility of covering buildings with “transparent” solar cells fabricated on architectural glass. The accomplishments of this project position it well for the next phase of research, namely creation and optimization of the nanostructure based PV cells.

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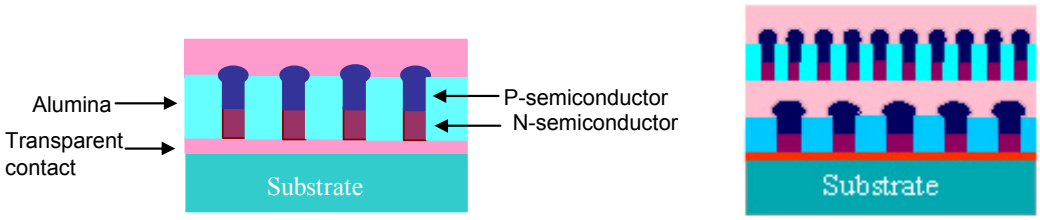
PROJECT OBJECTIVE

The objective of this project is to develop the process technologies for the implementation of multijunction photovoltaic cells using stacked layers of semiconductor nanostructures. The foundation of the fabrication technique is the electrochemical formation of a self-assembled nanoporous alumina template. The active nanostructures forming the PV cell are synthesized inside the template pores by a low cost electrochemical synthesis technique.

INTRODUCTION

While photovoltaic cells based on thin film technologies are among the most promising for commercial applications, many technical challenges still remain such as reduced cell efficiency, poorer material quality, spatial non-uniformity, material stability and manufacturing costs [1-4]. In order to address these limitations, we are developing a new *inexpensive* photovoltaic cell technology based on the electrochemical fabrication of semiconductor *nanostructures*. Nanostructure based PV cells have the potential to provide very high energy conversion efficiencies resulting from the following effects: (a) nanostructure *crystallite sizes* are comparable to the *carrier scattering lengths*, which significantly reduces the carrier scattering rate, thus *increasing the carrier collection efficiency*; and (b) the *strong absorption coefficient* of nanostructures due to the increased density of states. In addition, by varying the size of the nanostructures, the band gap can be tuned to absorb in a particular photon energy range [5]. Nanostructure based PV cells have been previously proposed due to their many advantages. However, a major impediment to the development of a nanostructure based PV technology has been the inability to fabricate large arrays of nanostructures with the required periodicity and size control at low cost. To meet this challenge, we have developed a unique low cost technology for the fabrication of periodic arrays of semiconductor nanostructures with very good size control (± 10%) and periodicity. This technique uses electrochemical synthesis on a preformed template of anodized aluminum to form the nanostructures. This technology is also ideally suited for the formation of multijunction structures, which can further increase photo-conversion efficiency [6].

The photovoltaic cells fabricated using this technique can be formed by stacking layers of nanostructures arrays with (a) the same semiconductor material of varying nano structure size or, (b) different semiconductor materials with or withourt varying dimensions. Fig 1a shows a photovoltaic cell with a single layer of nanostructure PN junctions. Fig.1b shows a PV cell that uses multiple layers of PN junctions of the same material, but of different dimensions.The multi-junction feature in this cell is achieved by using band-gap tuning through nanostructure size control. The diameter of the nano structure PN junctions in each layer is smaller than that in the layer immediately below it. The nanostructures with smaller dimensions have larger energy band-gaps thus allowing them to absorb light with shorter wavelengths. This ability to absorb light over a wide wavelength range will contribute towards its higher cell efficiency. Multijunction feature can also be implemented using stacked layers of nanostructures of same dimensions, but of different materials. In this case, the band-gap of material used in each layer is higher than the layer immediately below it, thus allowing this cell to absorb light of a wide wavelength range resulting in a higher cell efficiency.



(a) (b)

Figure 1. Nanostructure based photovoltaic cells : (a) single junction, (b) multijunction.

The nanostructure based PV cells shown in Fig 1a and 1b are expected to show very high energy conversion efficiencies due to the reasons described above. In addition, the structure of this cells also eliminates the large area spatial non-uniformity that is associated with most thin film technologies. In these devices, spatial uniformity only over the diameter of the nano structure (a few nano meteres) is required. The large area manufacturability problems associated with thin films are thus eliminated in this devices. However, it should be emphasized that since this electrochemical fabrication technology uses the same techniques as the commercial annodization of aluminum for corrosion resistance, this fabrication process can be scaled up to provide arrays of any arbitrary size.

FABRICATION TECHNIQUE

The nanostructure fabrication technique that is at the foundation of this project is based on the electrochemical formation of a self-assembled nanoporous alumina template. When aluminum is anodized in an appropriate acidic electrolyte under controlled conditions, it oxidizes to form a hydrated aluminum oxide (alumina) containing a two dimensional hexagonal arrays of cylindrical pores as schematically shown in Figure 2. The pore diameter and the inter-pore spacing depend on the anodization conditions such as electrolyte pH, type of acid, anodization current/voltage, electrolyte temperature and the substrate parameters. The pore diameter can be varied between 4 nm to 100s of nm and the pores can be several microns deep [7] –[15]. Due to the excellent periodicity of the pores, and the ability to control the pore diameters, such anodized alumina films can be used as templates for the fabrication of periodic arrays of nanostructures. Since alumina (Al_2O_3) is electrically insulating (10^{18} Ω-cm resistivity), optically transparent over a wide spectra, and chemically robust, it is an ideal embedding material for optical and electronic devices [9}. The pores in alumina templates can be used to synthesize a variety of metal and semiconductor nanostructures [16]. In addition, the template can be used as a mask for pattern transfer to create periodic arrays of pores on a substrate. In summary, this technology, allows economic fabrication of large periodic arrays of nanostructures that allow (a) the size and composition of the nanostructures to be varied, (b) encapsulation of nanostructures in a rugged host material, (c) flexibility to use a variety of substrate materials, and (d) compatibility with standard silicon fabrication technique.

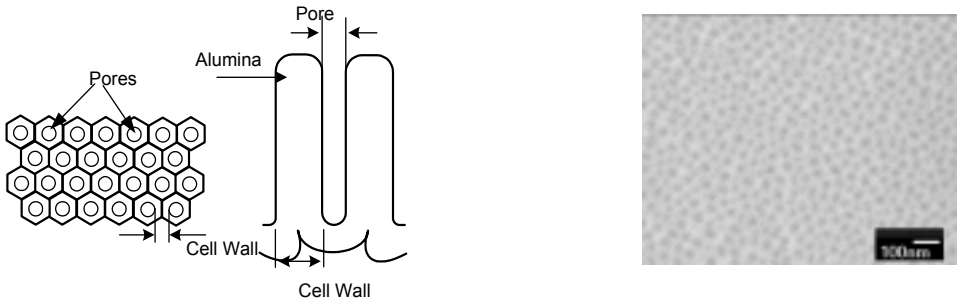


Figure 2. Left : Schematic top and cross-sectional views of hexagonal array of pores formed in porous alumina template. Right: SEM top image of porous alumina template.

PROJECT ACCOMPLISHMENTS

This project has accomplished its objective to develop the process technologies for the implementation of nanostructure based multijunction PV cells in an economical manner. This will enable the ability to implement previosly proposed nanostructure based photovoltaic device concepts that can provide high energy conversion efficiencies. This project also demonstated the feasibility of creating the semiconductor nanostructures on an arbitrary substrate. The breakthrough provides the possibility of covering buildings with "transparent" solar cells fabricated on architectural glass, thus reducing the overall infrastructure cost . Some of the specific project accomplished are summarized below.

1. Process development for thin film templates

While the template based fabrication technique is flexible regarding the substrate material, in this project we used silicon substrates for initial process development. Towards this goal, p-type <100> 0.1-0.3 ohm-cm silicon wafers were first cleaned using a standard technique and etched in a 1% hydrofluoric acid solution to remove any native oxide. Next, a 0.5 μm thick aluminum layer was deposited on the back of the wafers and annealed at 450^0 C for 30 minutes to form a good electrical contact. Following this, an aluminum layer (0.1 μm to 0.5 μm thick) was deposited by either sputtering or electron beam evaporation. In most cases, the samples were then annealed at 400^o C for 30 minutes to ensure good adhesion. The top aluminum layers were then anodized in 20% sulfuric or 20% oxalic acid under constant voltage or constant current conditions. Anodization in sulfuric acid creates templates with smaller pore diameters compared to anodization in oxalic acid under the same conditions. Constant current anodizations were performed at current densities ranging between 10 and 70 mA/cm^2, and constant voltage anodizations were carried out at voltages ranging between 10 and 40 Volts. The acid solution is circulated using a pump and chilled using a Julabo F10 chiller to prevent heat buildup at the aluminum/electrolyte interface. To investigate the effect of electrolyte temperature on template properties, anodizations were performed at different electrolyte temperatures. The anodization process was monitored by observing the voltage-time characteristics for constant current anodizations, and current-time characteristics for constant voltage anodizations.

Figure 3 shows a typical voltage-time characteristic for constant-current anodization in sulfuric acid for an aluminum thin film on a silicon substrate. The voltage-time characteristic provides an insight into the anodization process as explained below. While the pore formation mechanism during anodization is not yet fully understood, it is believed to take place in the following steps. During the first 3-5 seconds of anodization, a thin non-porous film of alumina (Al_2O_3) called the barrier layer is formed on top of the aluminum film. As anodization is continued, an array of pores develops on the barrier layer, whose diameters increase until reaching a final dimension determined by the anodization conditions. Once the final diameter is reached, the pore diameter does not increase any further, the pore depths increase at a rate proportional to the anodization current. For constant-current anodization, the potential across anode and cathode is proportional to the device resistance. Thus, the potential increases during the first 3-5 seconds when the high resistance barrier layer is formed. Next, as the pores start to develop, the potential decreases until the final pore diameter is reached, after which the potential remains constant as the pores propagate. When the pores reach the substrate, the potential-time characteristic shows a sharp rise in the voltage. This sharp rise is believed to be due to oxidation of the silicon surface, and will be discussed in a later section.

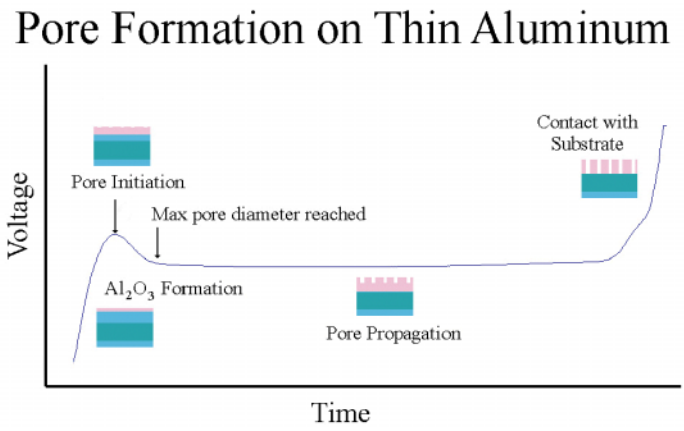


Figure 3. Experimental voltage-time characteristic during constant current anodization of aluminum thin film on silicon showing barrier layer formation, pore initiation, pore propagation and contact with substrate.

The potential-time characteristic, shown in Figure 3, allows precise determination of the pore propagation rate from the known values of aluminum layer thickness and pore propagation time. Figure 4 shows the results of a systematic study carried out in this project of the pore propagation rate calculated from the potential-time curves for a number of samples anodized under different conditions. The data shown in Figure 4 are for two different aluminum film thicknesses anodized at two different electrolyte temperatures, as well as for an un-annealed aluminum thin film. Figure 4 shows that pore propagation rate increases approximately linearly with the anodization current density, which is expected. It is observed that the pore propagation rate is insensitive to the electrolyte temperature. Also, the pore propagation rates for annealed and un-annealed samples do not show any noticeable differences. It may also be noted that the pore propagation rate show very small sample-to-sample spread at lower anodization current densities, however, the spread increases at higher current densities. From voltage-time characteristics of the samples, we also calculated the (a) barrier layer formation time, and the (b) pore formation time, as a function of current density; the results are shown in Figures 5a and 5b respectively. It can be seen that both parameters decrease exponentially with the anodization

current density. This exponential dependence can be explained using a simple ion concentration limited electrochemical reaction model.

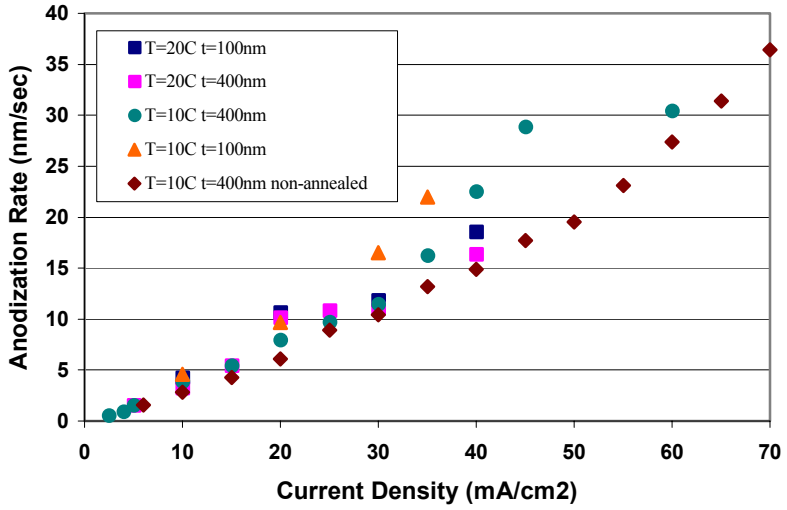


Figure 4. Experimentally determined pore propagation rate (anodization rate) as a function of anodization current density for a variety of thin film and anodization parameters.

In Figure 3, the voltage-time characteristic shows a sharp rise corresponding to the pores reaching the silicon substrate. We demonstrated that the sharp rise in the voltage-time characteristic is due to the following reason. After the aluminum layer is exhausted, if the anodization process is still continued, the electrolyte first etches the barrier layer and then oxidizes the surface of the silicon. To verify this, we removed the alumina template from the silicon substrate by etching in a chromic acid solution, and then inspected the surface under a scanning electron microscope (SEM). Figure 6 shows the Field Emission SEM picture of the surface of the silicon substrate after the alumina template was removed. It may be seen from Figure 6 that the complete surface is covered with oxidized silicon, the circular features are thicker islands of oxide at the locations of the alumina pores. By using angle-dependent imaging, it was confirmed that the circular features were islands and not pits. We believe that the silicon surface under the pores got oxidized first after which the oxidation process spread laterally, which is the reason why the circular islands are larger than the pore dimensions. These results suggest that special care needs to be taken during the anodization of aluminum thin films on silicon substrates; the anodization process should be stopped as soon as the potential starts to increase. Another solution is to incorporate a protective layer of metal, such as platinum or gold, between the aluminum layer and the silicon substrate.

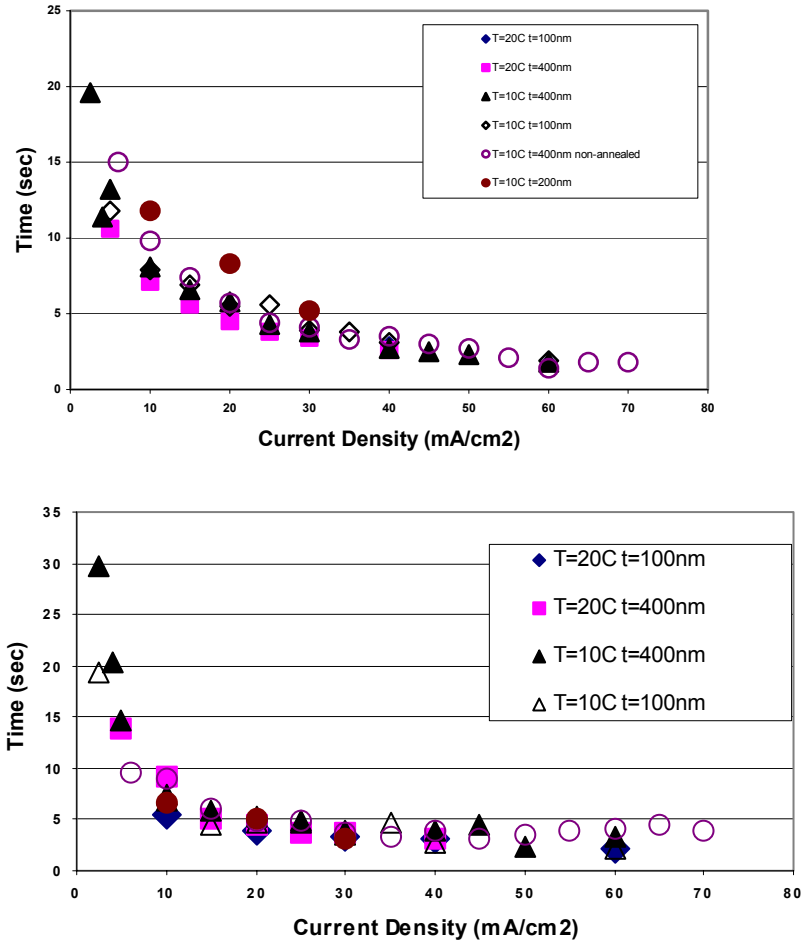


Figure 5. (Top) Barrier layer formation time, and (bottom) pore formation time, as a function of anodization current density for a variety of thin film and anodization parameters.

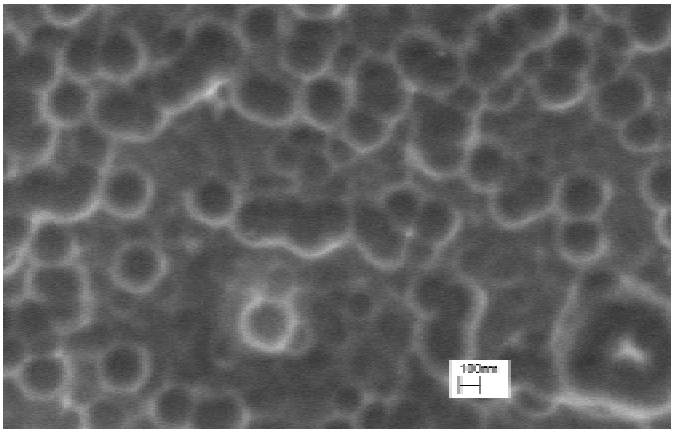


Figure 6. Field emission SEM image of the silicon surface after removal of the alumina template. The circular islands are oxidized silicon formed through the pores.

2. Process development for increased pore ordering on thin film templates

An important challenge in this project was to create a thin film templates with the improved pore size uniformity and ordering that are seen in bulk substracts. Previous research has demonstrated that pre-patterning morphology can enhance self-ordering of nano pores during anodization [11]-[13]. However, the effects of very small grain size typical of thin films and the impact of aluminium /substrate interface where unknown. Additionally, the late stage ordering dynamics was also not well understood. This late stage ordering seems to be independent of the initial morphology, but is sensitive to applied voltage and the electrolyte composition. We investigated different appraches and developed a cyclic annodization/dissolution process for improving pore ordering in thin film alumina templates. The successive annodizzation/dissolution cycles leave behind shallow pits that help in the self ordering process. P-type silicon wafers with <100> orientation were used for these experiments. Silicon wafers, cleaned by standard techniques, were deposited with 0.25 micron of aluminum on the back followed by annealing to form a good ohmic contact. Next, around 0.5 microns of pure aluminum was deposited on the top of the wafer using electron beam evaporation. The top aluminum layer was then anodized in 20% oxalic acid solution using the two-step anodization process. Oxalic acid was used in order to create larger pore diameters for the ease of imaging. In the first step, around 0.25 micron of aluminum was anodized and was then completely removed using a chromic acid solution. The wafer was then anodized again until the potential starts to rise indicating that the pores have reached the silicon surface. The anodization current density was varied between 5 mA/cm2 and 70 mA/cm2. Figure 7 shows a typical sample created at 40 mA/cm2 current density. It may be seen form Figure 7 that the two-step anodization process significantly increases the pore periodicity and pore size distribution.

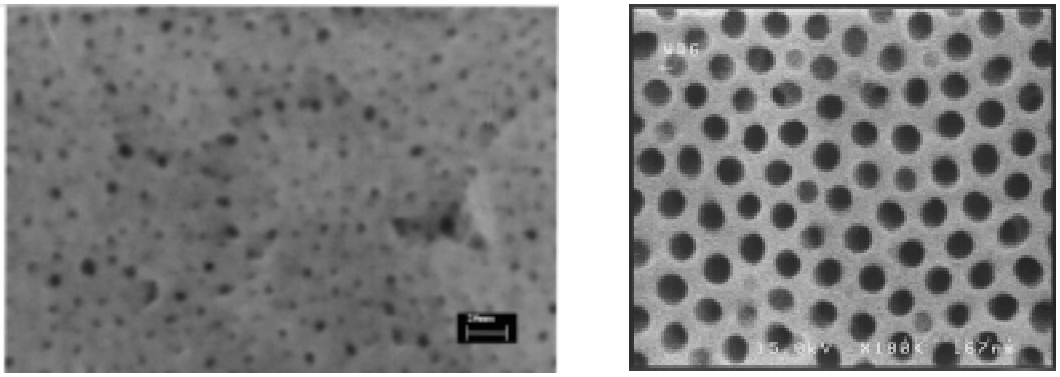


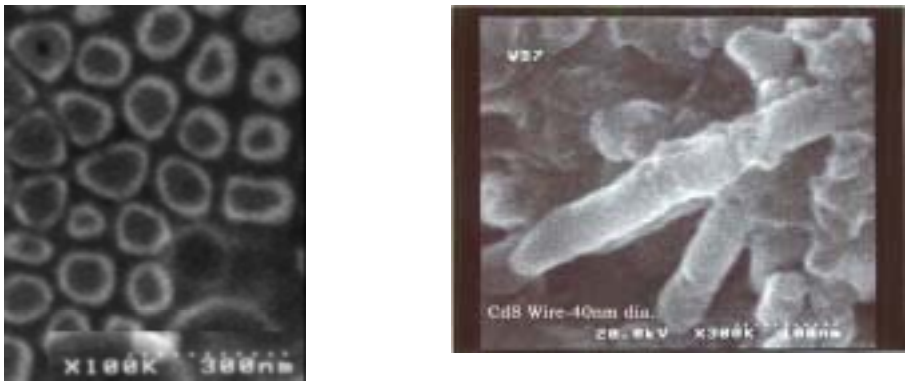
Figure 7. SEM top image of thin film porous alumina templates formed by one-step (left) and two-step (right) anodization steps. The two-step process significantly improves pore regularity.

3. Process development for the synthesis of single crystal II – VI quantum wires by AC deposition

The active semiconductor material for nanostructure was formed by electrochemical synthesis inside the template pores. While it is possible to synthesize almost any II-VI semiconductor material by electrochemical techniques, for this research we focused on CdS due to high degree of optical activity and non-linear optical properties. For the deposition of CdS, first CdCl2 and elemental sulphur are dissolved in DMSO. The material is then deposited at a temperature

ranging from between 100-160 C with an applied AC current. The use of an AC current was required initially due to the presence of an insulating layer at the silicon/alumina interface. From this investigation , we were able to conclude that : (a) uniform CdS quantum wires were formed without the presence of structural voids, and (b) the quantum wires conform to the template dimensions.

Field Emission SEM images of typical CdS quantum wires fabricated by the AC deposition technique are shown in Figures 8a and 8b. The CdS quantum wires were exposed by dissolving the template partially (Fig. 8a) and completely (Fig. 8b) in a 10% NaOH solution.The CdS quantum wires were characterized by photoluminescence (PL) and Ramen measurements. Fig 9 shows the PL data for quantum wires with 15 nm and 40 nm diameteres. The PL results show intense luminescience with a peak energy below the bandgap, and is believed to be dominated by impurity lumniscence. However, the luminescence from 15 nm wires is more intense compared to that from 40 nm wires, suggesting possible quantum confinement.



(a) (b)

Figure 8. FESEM image of CdS nanowire arrays with the alumina template (a) partially and (b) completely dissolved.

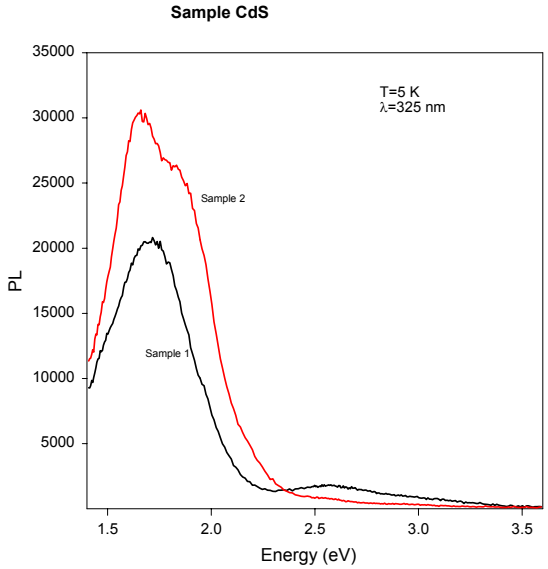


Figure 9. Photoluminescence data from CdS quantum wires formed by AC deposition. Sample1: 40 nm diameter; Sample 2 : 15 nm diameter.

Raman measurement results on the above CdS quantum wires are shown in Figure 10 in two different ranges of Raman shift. As can be seen from Figure 10, there is a significant enhancement in Raman scattering from the sample with 15 nm diameter at the value of the first LO phonon in CdS (300 cm^{-1}). Weal scattering is observed for the 40 nm sample at approximately 313 cm^{-1}. The decrease in the first LO phonon position with decreasing wire size is consistent with that reported in the literature, which shows a shift from 308 cm^{-1} to 300 cm^{-1} for wires wqith dimensions less than 10 nm. The broad peak in the range between 1000 –4000 cm^{-1} is believed to be due to inter-subband transitions. This feature is not observed in the 40 nm sample and therefore tend to indicate the onset of quantum confinement in the 15 nm diameter sample. The series of ahsrp lines around 1300 cm^{-1} is believed to be due luminescence from trace amounts of rare earth impurites.

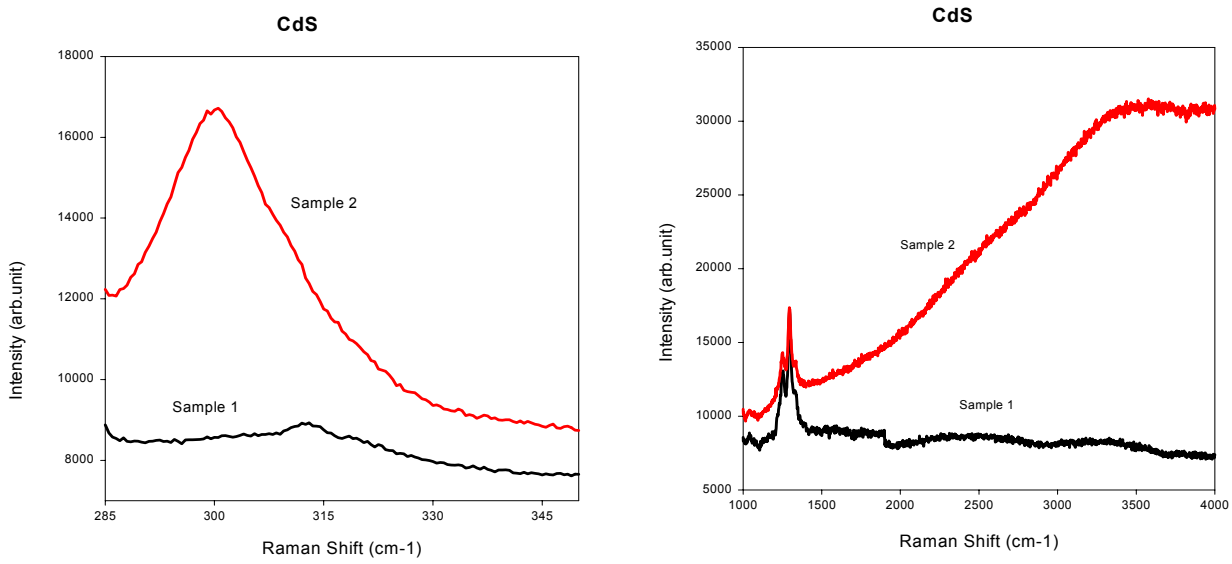


Figure 10. Results of Raman measurements on CdS quantum wires formed by AC deposition.
Sample 1 : 40 nm diameter; Sample 2 : 15 nm diameter.

4. Barrier layer engineering : process development for *in-situ* barrier layer removal

An important concern for devices that rely on charge transport is the state of the nanostructure/substrate interface. During template formation, a barrier layer equal to the thickness of the pore diameter remains after the anodization process is completed. A second concern is that anodic oxidation of the silicon surface can occur, leading to the formation of an insulating silicon dicoxide layer at this interface as shown in Figure 6. To alleviate these concerns, an Al/Pt/Si structure has been developed in collbaoration with University of Notre Dame that provides *in-situ* barrier layer removal and prevents anodic oxidation of the silicon surface. Cross-sectional FESEM images of this inetrface are shown in Figure 11. In this case, a platinum layer is first deposited on the silicon substrate followed by the deposition of an aluminum layer. During anodization of the aluminum layer, the platinum layer acts as a barrier and prevents oxidation of the silicon surface. This allow slight over anodization of the aluminum layer, a step that etches the barrier layer. The in-situ barrier layer removal process is significant

since it enables the use of under potential direct-current electrochemical deposition. The use of these techniques has been demonstarted to substantially improve semicondutor material quality.

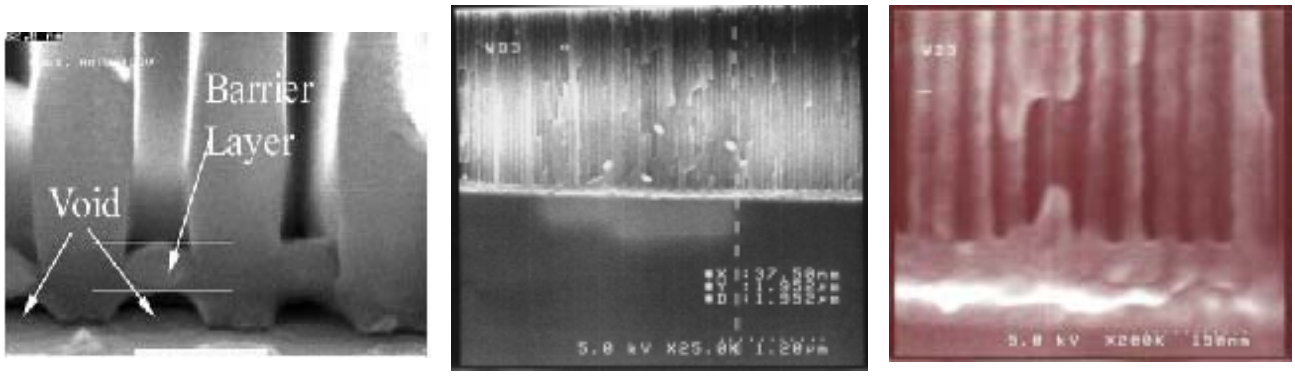


Figure 11. *Left :* SEM image of alumina barrier layer*, Center and Right*: in-situ barrier layer removal in Al/Pt/Si system.

5. Process development for the syntehsis of superior quality II-VI quantum wires DC deposition

The barrier layer engineering process developed in this project provided a significant breakthrough since it allowed direct-current atomic layer electrochemical deposition of semiconductor materials. The use of DC deposition technique has been shown to provide: (a) uniform CdS quantum wires without structural voids, and (b) oriented growth of CdS with the C-axis of the hexagonal wurtzite phase aligned normal to the substrate surface. This approach provides a low cost, non-vacuum method for the fabrication of quantum wires that proivides the ability for enhanced photovoltaic energy conversion efficiency and material reliability. SEM cross-sectional images of CdS quantum wires synthesized by this technique are shown in Figure 12. The results of photoluminescence characetrization of CdS quantum wires with a diameter of 15 nm is shown in Figure 13. The primary luminescent recombination occurs below the band-edge and is belieevd to result from crystal defects in CdS quantum wires. A secondary peak is observed near the band-edge of CdS that shows a small blue shift from the bulk bandgap 2.58 eV. Since the diameter of the quantum wires (15 nm) is greater than the bulk exciton Bohr radius, a significant blue-shift bulk band-edge is not expected from these samples. However, the presence of the blue-shift confirms the feasibility of using this fabrication technique for the implementation of devices that operate on quantum confinement.

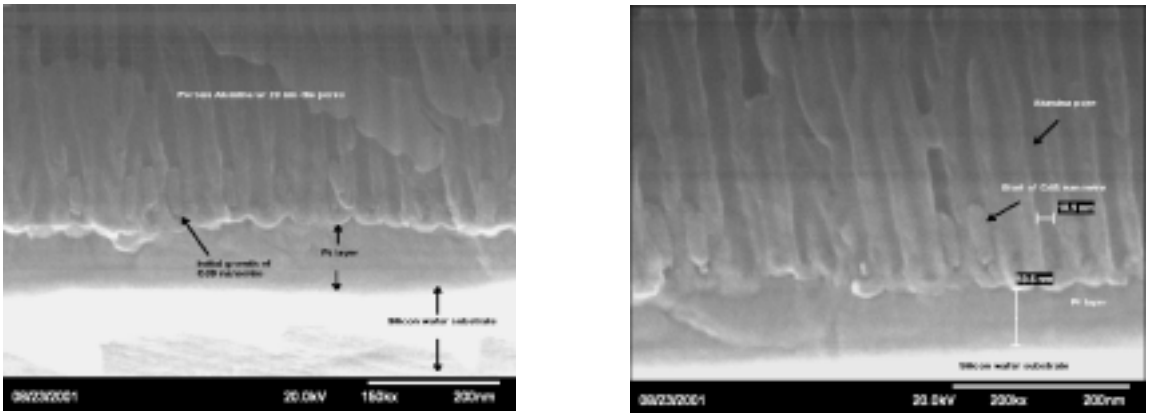


Figure 12. Cross-sectional SEM image of CdS quantum wires inside alumina template pores fabricated by DC Under-potential deposition technique developed in this project.

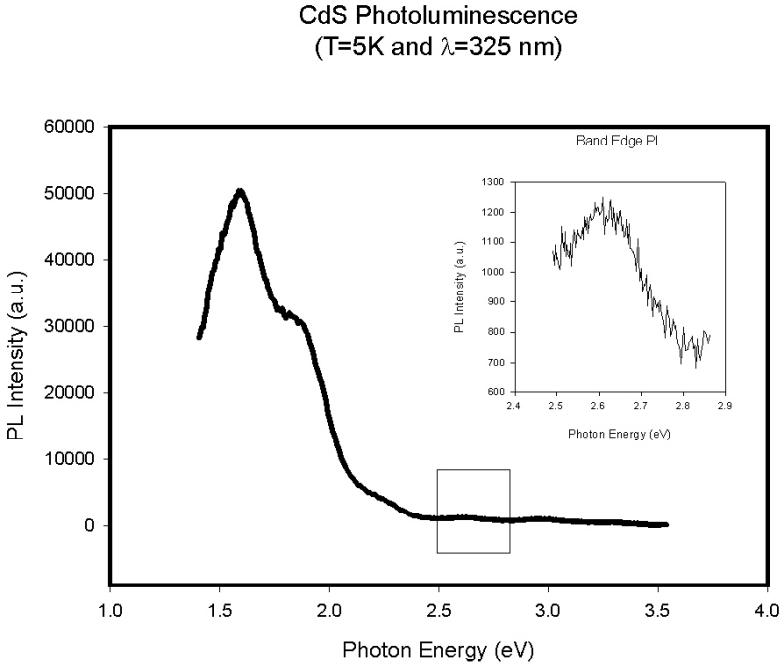


Figure 13. Results of photoluminescence measurements on CdS quantum wires fabricated by the DC under-potential deposition technique. Inset shows the band-edge luminescence showing a small blue shift. The peak around 1.5 eV is believed to be due to mid-gap defects

6. Alumina/Silicon interface characterization usng C-V measurements

The interface between the thin film alumina template and the substrate will play an important role in device performance. A capacitance-voltage characterization technique was developed that allows rapid electrical characterization of the alumina templates. It was observed that the template pore size has a profound effect on the capacitance-voltage characteristics, which can be used for their estimation.

Capacitance-voltage measurement is a widely accepted means of testing metal insulator semiconductor (MIS) capacitor samples and for determining device parameters such as carrier density, Fermi level, flatband voltage and threshold voltage. Since anodized alumina is an insulator, CV characterization could be used to characterize the templates as well as the template/silicon interface. Towards this goal, a number of aluminum/alumina/P-Si MIS capacitors were fabricated using the following technique. P-type silicon substrates were first summa-cleaned, then immersed in a 1% HF bath, rinsed, and dried with N_2. Then, a 100 nm layer of Al was sputter deposited on the back of the wafer, followed by annealing at 450^o C for 30 minutes. Next, a 100 nm layer of Al was deposited on the top of the wafer, which was then annealed at 400^o C for 30 minutes to ensure good adhesion. The wafers were then anodized in 20% sulfuric acid at current densities of 20, 40 and 60 mA/cm^2. The voltage-time characteristics were monitored during the anodization and the process was stopped as soon as the voltage started to increase to avoid the oxidation of the silicon surface. Finally, a number of aluminum contacts, each 1.59 mm in diameter, were sputter deposited through a shadow mask on top of the template to create the capacitors.

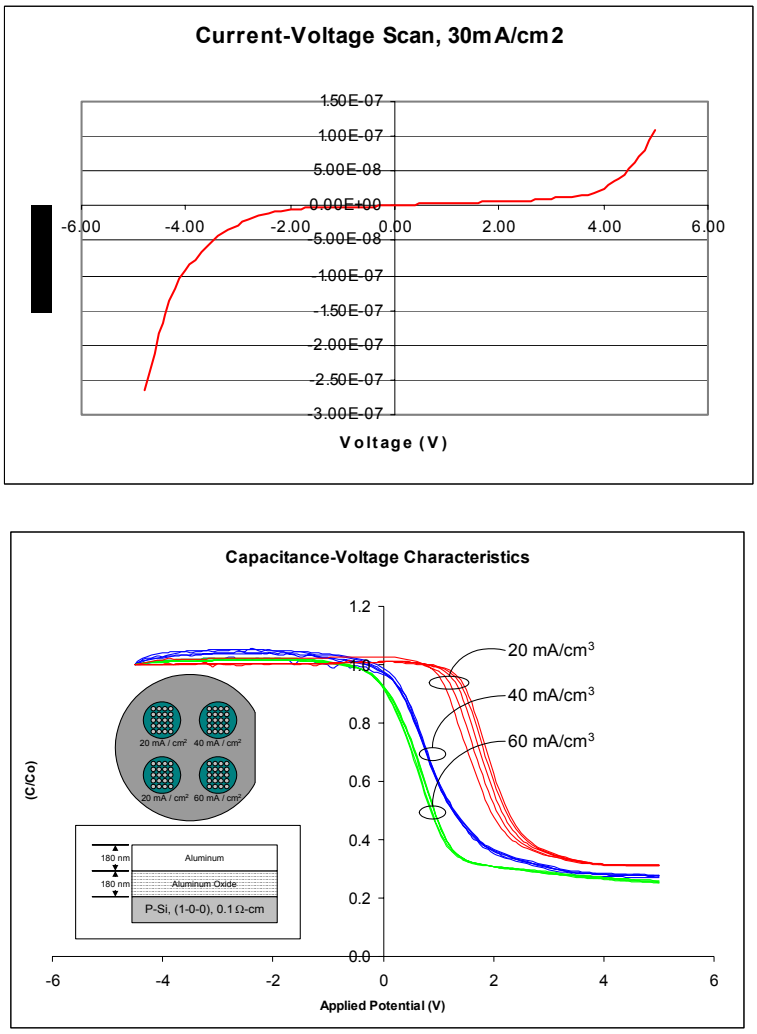


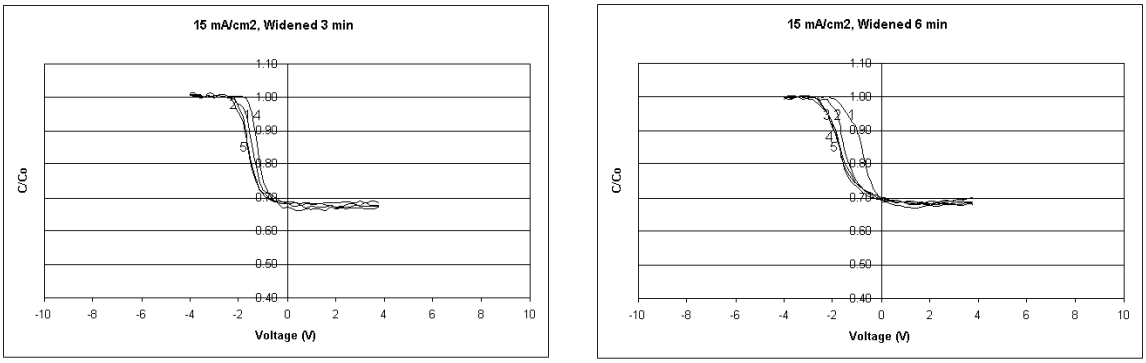
Figure 14. Current-voltage (top) and Capacitance-voltage (bottom) characteristics of alumina templates formed on silicon substrates. The inset shows the devices used in the experiments. The C-V data confirms the excellent quality of the template/substrate interface.

CV measurements were performed at a frequency of 1.0 MHz. The bias voltage was varied from -5 VDC to +5 VDC, using a HP 4140A DC voltage source, controlled by Lab View software. This voltage range was selected to avoid excessive leakage currents (Figure 14). The CV characteristics for the samples are summarized in Figure 14 which also shows the capacitors used in the experiments. From Figure 14, the CV characteristics are very similar to that of metal oxide silicon (MOS) capacitors fabricated on p-type substrates. For negative bias voltages, the capacitance remains constant at C_0 (the accumulation capacitance), then decreases with positive voltage as the depletion layer forms, and then becomes constant again at C_i (the inversion capacitance). The data in Figure 14 were normalized to C_0. The results are very encouraging since they suggest that the template/silicon interface is of good device quality. It may be noted from Figure 14 that the threshold voltage (the bias voltage at which the capacitance starts decreasing) is close to zero for samples that were anodized at 40 and 60 mA/cm^2, and is close to 1.5 V for the samples anodized at 20 mA/cm^2. It is also encouraging to note the very small sample-to-sample variation in the CV data, suggesting good uniformity of the alumina layer on silicon. In summary, the CV measurements confirm that the alumina/silicon interface is of good device quality with the potential for nanostructure integration with silicon electronics.

7. Investigation of template pore-widening

A pore widening step is often performed after the anodization step on anodized alumina by immersing it in a 5% solution of phosphoric acid for 3-5 minutes. The pore widening step removes a thin layer of the alumina thus widening the pores to some degree. The purpose of pore widening is to remove any remaining barrier layer (alumina) at the alumina/silicon interface, as well as to remove impurity ions remaining from the anodization process. In this project, we performed the pore widening process primarily as a 'clean up' step. We investigated the effect of pore widening using photoluminescence and Capacitance-voltage measurements.

A number of aluminum/porous alumina/p-Si MIS capacitors were fabricated using the following technique. P-type silicon substrates were first summa-cleaned, then immersed in a 1% HF bath, rinsed, and dried in N_2. Then, a 100 nm layer of Al was sputter deposited on the back of the wafer, followed by annealing at 450^o C for 30 minutes to form an ohmic back contact. Next, a 100 nm layer of Al was deposited on the top of the wafer, which was then annealed at 400^o C for 30 minutes to ensure good adhesion. The wafers were then anodized in 20% sulfuric acid at current densities of 15, 20 and 30 mA/cm^2. Some of these wafers were then pore widened in 5% phosphoric acid for either 3 or 6 minute durations. Finally, a number of Al contacts, each 1.59 mm in diameter, were sputter deposited through a shadow mask on top of the template to create the capacitors. The CV measurements were carried out in the dark to avoid photocurrent effects. The results of CV measurements on samples anodized at 15 mA/cm^2 are shown in Figures 15a-15b respectively.



(a) (b)

Figure 15. Capacitance-voltage characteristics of thin film alumina templates on silicon pore widened for (a) 3 minutes, (b) 6 minutes.

The threshold voltages for each capacitor were obtained from the CV data using the relationship:

$$V_{TH} = V\ (C_{inv} + (C_0 - C_{inv}).0.05);$$

this is the voltage at which the capacitance drops to 5% of the difference between its maximum and minimum values. The results of the calculations are shown in Fig. 16. For each anodization current density, the threshold voltages are plotted for different capacitor pad of the various samples: those not pore widened, those widened for 3 minutes, and those widened for 6 minutes. It may be noted that pore widening has a significant effect on threshold voltage distribution for samples anodized at 15 mA/cm^2.

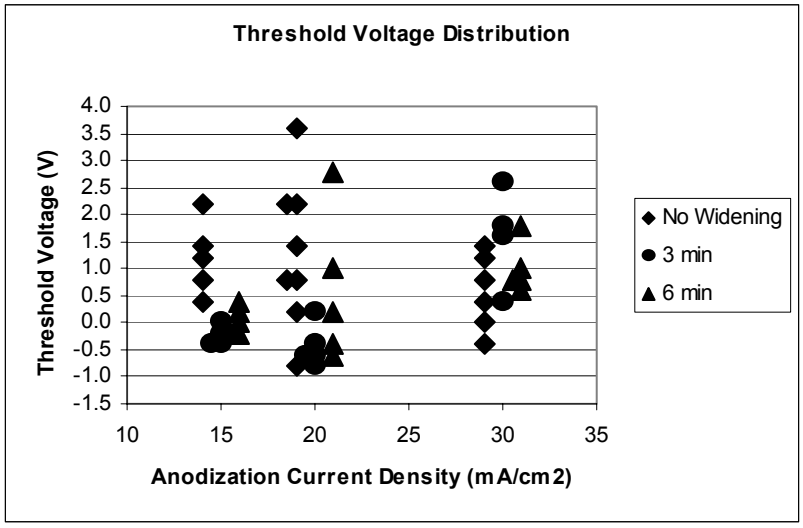


Figure 16. Threshold voltage distribution for the Al/alumina/p-si capacitors formed under different fabrication conditions.

To investigate this further, we carried out photoluminescence (PL) measurements on alumina templates that were pore widened for 3 and 6 minutes, and compared them with an un-widened sample. The results are shown in Figure 17. The PL measurements were performed at 5K with a laser excitation wavelength of 325 nm. It may be noted from Figure 17 that the PL intensity increases as well as undergoes a blue shift with increased pore widening time. We believe that the shift in the PL spectra indicates that the pore widening process removes some of the impurities, however, it also introduces some new impurities on the template.

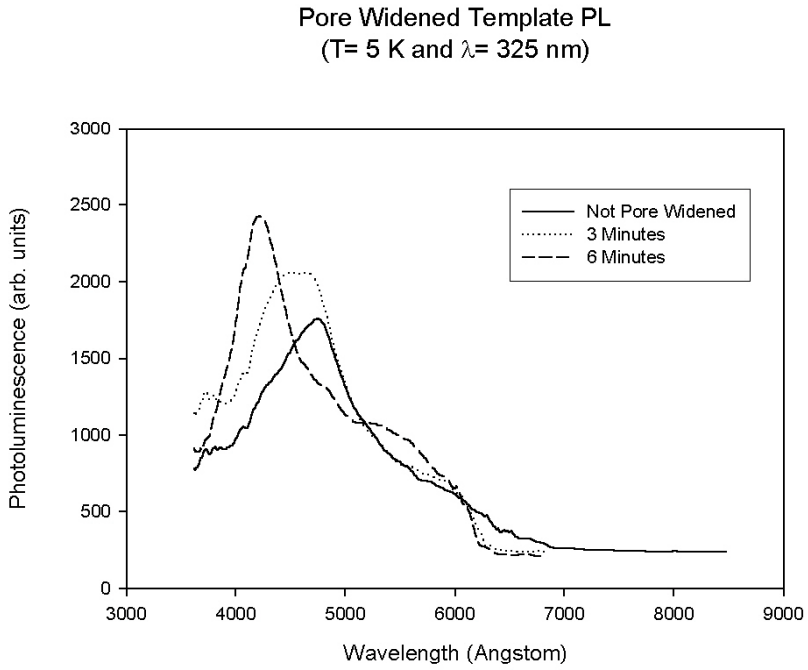


Figure 17. Photoluminescence spectra from alumina templates that were not pore widened, and pore widened for 3 and 6 minutes. Laser excitation wavelength : 325 nm. T=5K.

8. Fabrication of thin film template on non-silicon substrates

Since the objective of this project is to develop low-cost high-efficiency PV cells, various other substrates were also investigated to create thin film alumina templates. One of the advantages of the template based fabrication technique is that it is versatile regarding the choice of substrates. We have formed alumina templates on glass, ITO-coated glass and SiC substrates. One of the challenges of using a non-conducting substrate is the formation of the anode contact. For glass and ITO-coated glass substrates, the anodic contact could not be taken from the back, and the configuration shown in the inset of Figure 18 was used. The potential-time curve for the constant current anodization of aluminum deposited on ITO-coated glass is shown in Figure 18. The voltage-time characteristics in Figure 18 is very similar to that for aluminum deposited on a silicon substrate. We believe that the rise in the voltage-time curve at the end of anodization is due to the electrochemical oxidation of the ITO. A typical alumina template formed on an ITO coated glass substrate is shown in Figure 19. This particular sample was used to synthesize Ni in the template pores, which has covered the template surface to a certain degree. The pore

morphology and configuration were found to be very similar to that for silicon substrates. The glass substrates are of particular interest since they open up the possibility of creating PV cells on architectural glass that can be used to cover buildings.

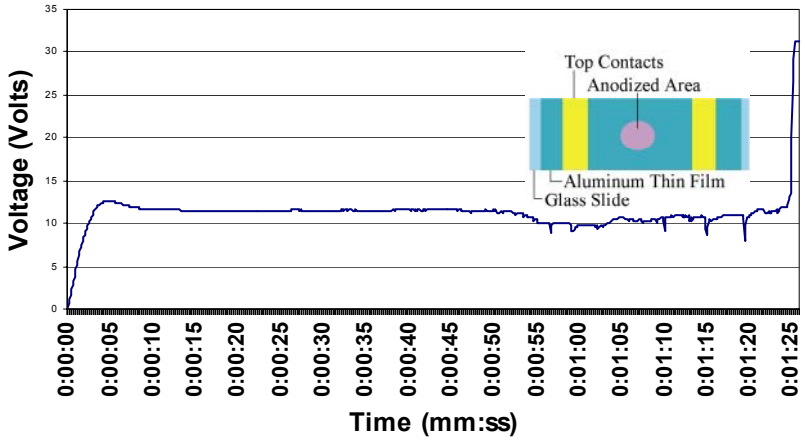


Figure 18. Voltage-time characteristic for constant current anodization of aluminum thin film deposited on ITO-coated glass substrate. The inset shows the electrical contact configuration used in the experiment.

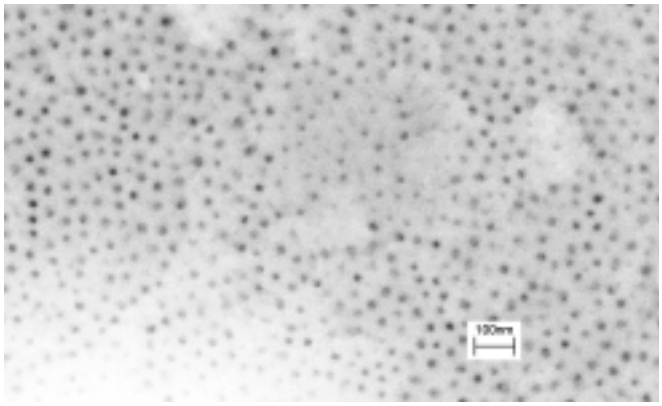


Figure 19. Field emission SEM image of thin film alumina template formed on ITO-coated glass substrate. The surface is partially coated with nickel.

We have also demonstrated the formation of stacked layers of templates on silicon substrates, this will be required in the PV cell configuration shown in Figure 1b. Due to our imaging limitation at the time, we could not obtain images of this stacked structure. However, the voltage-time characteristics demonstrated the formation of the stacked layers of thin film templates. These results will be important for the next phase of this project.

9. Development of an improved anodization apparatus

One of the outcomes of this project is the development of an improved anodization apparatus that is safer, more efficient and more environment-friendly. The previous apparatus, which is

widely used by the electrochemical community is restricted in terms of wafer size and requires a change of sulphuric acid with each process run. In addition, this also substantially increases the time required for each process run (at least 45 minutes). To improve this, we designed and fabricated a compeltely new anodization apparatus. This design permits the use of an arbitrariliy sized substrate, and allows us to perform a large number of process runs before changing sulphuric acid. With this new technique, we have reduced the process time to approximately 3 minutes per sample, and reduced sulphuric acid utlization from 750 ml per sample to approximately 75 ml per sample. In addition, this approach makes fabrication on non-silicon substrates much easier by permitting a front-side substrate connection. This will be particularly useful for the fabrication of PV cells on inexpensive substrates, which is one of the proejct goals. A complete description of this new system is described in the attached journal paper published in the Review of Scientific Instruments. An image of the apparatus developed as a part of this project is shown in Figure 20.

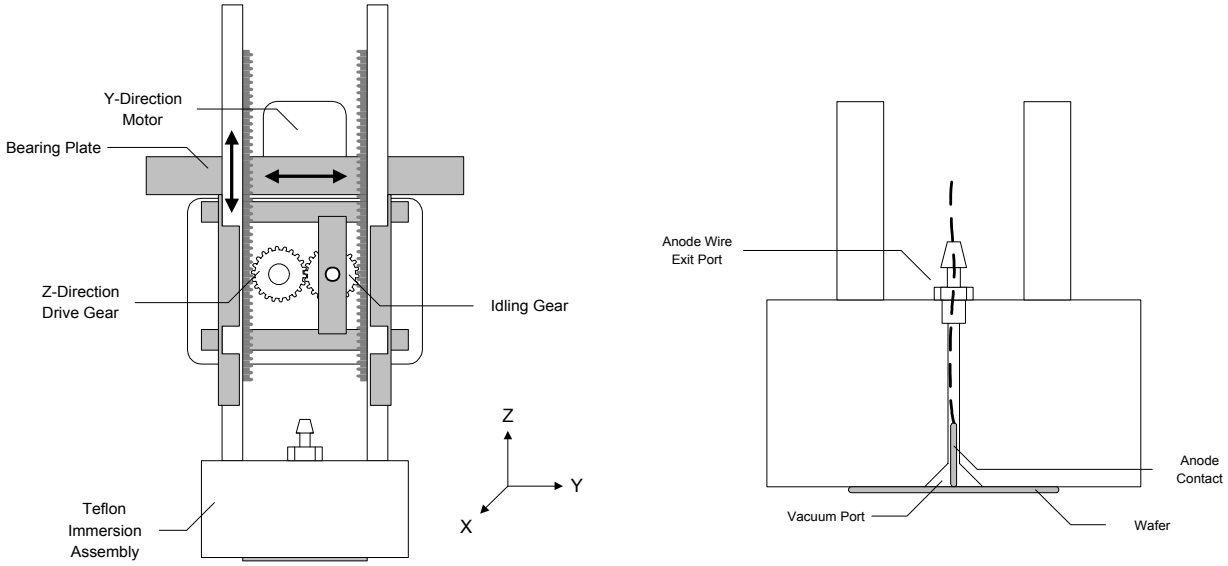
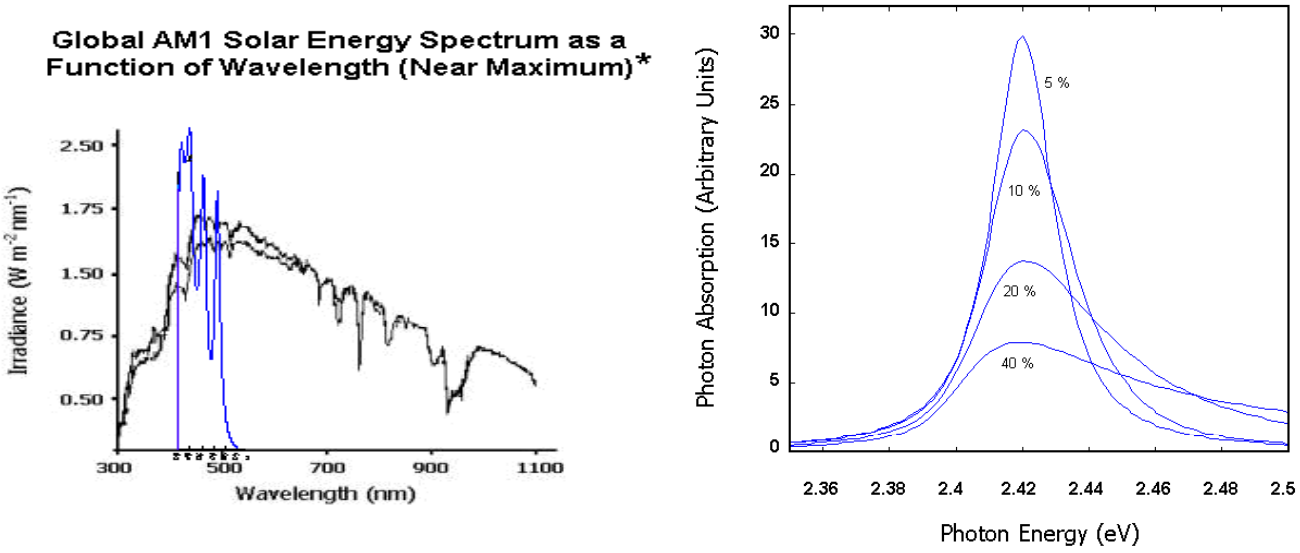


Figure 20. Improved anodization apparatus developed as a part of this project. The wafer is held on the chuck using vacuum suction and the sample is immersed in the electrolyte using x,y,z control of the sample holder. After anodization, the sample is removed from the electrolyte and the vacuum deactivated to release sample. The acid handling is minimum and the anodization time is faster than older apparatus. This apparatus also has the potential to be automated.

10. Development of modeling tools

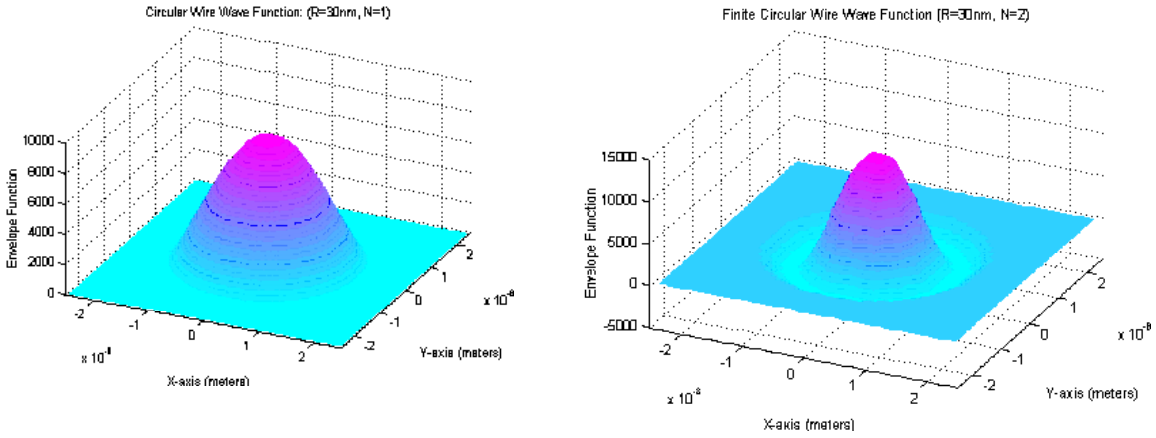
We developed the modeling tools for determining the absorption properties of the nanostructure arrays. This model includes the effects of nanostructure dimensionality, size, shape and composition. In addition, this model provides the ability to relate distributions in nanostructure size to observed optical properties. Specifically, the model took into account the (1) excitonic contribution to spectra, (2) size distribution effects, and (3) Coulomb correlation. This model was used to show the high degree of correlation between the absorption spectra of the quantum wire arrays with the solar spectrum (Figure 21a). This work verifies that nanostructure based photovoltaic cells can be engineered to maximize photovoltaic energy conversion efficiency and provides a guide for designing these devices. Figure 21b shows the effect of size variation



(a) (b)

Figure 21. (a) Matching nanostructure absorption spectra to specific range of the solar spectrum. (b) Effect of size variation on the absorption spectra of semiconductor quantum wires. The results confirm that the template based fabrication technique with ~10% size variation is appropriate for the implementation of high efficiency photovoltaic cells.

on the abosrption spectra of semiconductor quantum wires. In these calculations, the size distribution was assumed to be gaussian over which an ensembled avaerage was taken. Figures 22a and 22b show the lowest two electronic wave functions in the quantum wires that were used in the calculations.



(a) (b)

Figure 22. Wavefunctions corresponding to the lowest two energy levels (a) n=1, and (b) n=2, of CdS quantum wires with a diameter of 30 nm.

List of Publications resulting from this project:

C. Garman, P. Sines, S. McGinnis and B. Das, "An improved automated anodization apparatus for fabricating nanostructure devices and porous silicon", *Rev. Scientific. Instruments*, 72, pp. 1-4, 2001.

B. Das and S. McGinnis, "Novel template based semiconductor nanostructures and their applications", *Applied Physics A*, 71, pp. 1-8, (2000).

B. Das, S.P. McGinnis and P. Sines, "High efficiency solar cells based on Semiconductor nanostructures", *Solar Energy Materials & Solar Cells*, 63, pp. 117-123, (2000).

A.E. Miller, M. Crouse, S.P. McGinnis, and B. Das, "Template Based Semiconductor Nanostructures and their Applications", Electronic Materials Conferences, South Bend, IN, June, 2001.

B. Das, S.P. McGinnis, P. Sines, and D. Gray, "Multijunction Solar Cells Based on Nanostructure Arrays", 2001 Electrochemical Society Meeting, Washington, D.C., March, 2001.

B. Das, S.P. McGinnis, D. Gray, A.E. Miller, C. Arvin, P. Takhistov, and M. Crouse, "Template based semiconductor nanostructures for photonic applications", Fall Meeting of the American Chemical Society, (*Invited Paper),* Chicago, IL, August, 2001.

B. Das, S.P. McGinnis, and P. Sines, "Template baesd semiconductor nanostructure fabrication and applications", Eleventh International Workshop on the Physics of Semiconductor Devices, (*Invited Paper)*, Delhi, India, December, 2001.

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13. ABSTRACT (Maximum 200 words): This project developed the process technologies for the fabrication of high-efficiency multijunction photovoltaic cells using semiconductor nanostructure arrays. These devices are expected to provide increased energy conversion efficiency, as well as increased carrier collection efficiency. In addition, this approach provides the ability to tune the absorption spectrum to match selected windows of the solar spectrum. At the same time, these devices can be fabricated using existing industrial electrochemical processing techniques that can substantially reduce the cost of each device. The fabrication technique is based on electrochemical synthesis of II-VI semiconductor quantum wires using a preformed alumina template. This project focused on and solved the technical challenges that need to be addressed for the implementation of such devices. Specific issues addressed include (a) improved pore ordering on thin-film templates, (b) synthesis of II-VI semiconductor nanostructures by both AC and DC deposition, (c) an in-situ barrier-layer engineering process that allow the fabrication of superior-quality materials and improved template/substrate interface, (d) characterization techniques for templates, (e) process technology for creating stacked layers of nanostructures, (f) process throughput and improved apparatus, (g) modeling tools, (h) use of glass substrates, and (i) a nonlithographic surface texturing technique for silicon PV cells. An important outcome of this project is the demonstration of the fabrication technique on glass substrates. This breakthrough provides the possibility of covering buildings with “transparent” solar cells fabricated on architectural glass. The accomplishments of this project position it well for the next phase of research, namely, creation and optimization of the nanostructure-based PV cells.

14. SUBJECT TERMS: PV; multijunction; solar cells; semiconductor; nanostructure arrays; device; energy conversion; carrier collection; electrochemical synthesis; II-VI; thin film; in-situ barrier; characterization; modeling tools; glass substrate; solar cells

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