January 2005 • NREL/SR-520-37284

Subcontractor Report

Lab to Large Scale Transition for Non-Vacuum Thin Film CIGS Solar Cells

Phase II—Annual Technical Report August 2003–July 2004

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International Solar Electric Technology, Inc. (ISET)
Chatsworth, California

National Renewable Energy Laboratory
1617 Cole Boulevard, Golden, Colorado 80401-3393
303-275-3000 • www.nrel.gov

Operated for the U.S. Department of Energy
Office of Energy Efficiency and Renewable Energy
by Midwest Research Institute • Battelle

Contract No. DE-AC36-99-GO10337

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NREL Technical Monitor: H.S. Ullal

Prepared under Subcontract No. XCQ-230630-30

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2.0 BACKGROUND

The purpose of the Thin-Film Photovoltaics Partnership Program (TFPPP) is to accelerate the progress of thin film solar cell and module development as well as to address mid and long-term research and development issues. The long-term objective of the TFPPP is to demonstrate commercial, low-cost, reproducible, high yield and robust modules of 15% aperture-area efficiency. Furthermore, this research is directed at making progress toward this objective by achieving interim goals in thin film module efficiencies; cell and module processing; cell and module reliability and the necessary fundamental research needed to build the technology base that support these key areas. Participation in the National R&D Teams is paramount to the success of this project. The DOE/NREL/NCPV strategy in undertaking this R&D effort is to maintain good coupling between laboratory results from fundamental materials and processes research to manufacturing R&D, pilot-line operation, and early entry of advanced thin-film PV products to the ever-growing marketplace worldwide.

The purpose of this subcontract, as part of the R&D Partners category is to, (i) identify the challenges that ISET may face in the process of making a 'Lab to Large Scale' transition for its ink based non-vacuum process in production of thin film CIGS solar cells and modules, and (ii) develop workable solutions for these challenges such that they can readily be implemented in a large-scale processing line for CIGS modules.

This report summarizes the activities of Year Two of the 'Lab to Large Scale Transition' effort

2.1 INTRODUCTION & OVERVIEW

The primary objective of this research is to streamline ISET's ink based non-vacuum process for fabricating efficient CIGS modules to lower the cost of module production << $1.0/watt. To achieve this objective, ISET has focused R&D efforts on investigating topics that directly impact the ultimate cost of processing CIGS modules. These topics of concern include (i) module output and therefore the solar cell and the module efficiency, (ii) overall process yield – which requires developing a process that offers a very high degree of repeatability for every manufacturing step, and (iii) a process approach that maximizes the utilization of the materials used.

In accordance with the above, this report will cover activity during Phase II in the investigation of methods for low-cost manufacturing and process development. Specific tasks cover four broad areas: (1) solar cell efficiency (2) process control (3) module integration and (4) enhanced material utilization by reduction of waste stream.

Table I. Overview of Phase II Tasks

1	Solar Cell Efficiency Improvement	This is a primary task of the contract. In this task we continue to improve the efficiency of CIGS solar cells by grading the composition of the absorber layer by surface modification to achieve gallium rich wider bandgap layers near the photoactive junction. This approach will increase the cell efficiency by increasing the open circuit voltage.
2	Process Improvement and Control	This task will aim to develop an insight into the kinetics of reduction and selenization steps of ISET's ink based process. Data will be collected with the goal of improving the process conditions and designing reduction and selenization furnaces capable of processing larger area substrates.
3	Module Integration	This task will evaluate issues unique to module formation. Monolithic integration schemes will be developed and optimized. Different inks and printing techniques will be evaluated for front contact deposition. Moly patterning schemes will be developed.
4	Waste Minimization	This task will aim to increase material's usage and to minimize waste. This task will have significant environmental impact and will enable significant cost reduction.

2.2 CELL EFFICIENCY IMPROVEMENT BY SURFACE MODIFICATION

Photovoltaic module output is determined by the cell efficiency. We are focusing on increasing the open-circuit voltage and the overall conversion efficiency by modifying CIGS solar cells using an overall non-vacuum approach.

Building on our current ink based fabrication methods, we have turned our attention to producing graded layers of the $Cu(In,Ga)Se_2$ solar cell absorber by surface modification at the junction interface. The objective is to grade the solar cell absorber layer via gallium surface treatments. Briefly, gallium alloying makes it easier to produce higher open-circuit voltages and when spiked in atomic ratios of Ga/(In+Ga) of 25% to 30%, groups worldwide using vacuum techniques have been able to produce CIGS device efficiencies above 18-19% with an effective bandgap 1.1 – 1.2 eV.[1-2]

2.2.1 Surface Modification of Cell Absorber with Thin Surface Layers

We have made strides towards understanding how to increase solar cell output by modifying the surface of the CIGS absorber layer. We have used this understanding to extend our champion cell efficiency. In keeping with

ISET's technology, the surface treatment is done via non-vacuum methods with a convenient ***solution-spray technique*** that has given us improved cell performance. Our strategy of surface band gap engineering requires wider band gap material near the junction to increase Voc, yet thin enough to allow lower band gap material deeper within the absorber to absorb lower energy photons and maintain the short-ciccuit currents. This method of surface band gap engineering allowed us to extend ***champion efficiency to 13.7% with low cost ink and solution-based methods***. As predicted, gains in efficiency were primarily by increase in open-circuit voltages. We will highlight important features of our process, outline new understanding on when cell efficiency can be improved, and explore definitive steps that will lead us to our goal of routinely produced 15-16% cells.

2.2.2 Current Problems in Gallium Distribution

It is well known that the addition of gallium to the CIS structure opens up the bandgap and increases the Voc of the resulting cell. At ISET, past efficiency and spectral response results indicated that in spite of adding Ga to the absorber layer, we were not getting the full benefit of increased open circuit voltage. SIMS measurements on our samples revealed that during the conversion process in which the Cu-In-Ga alloy was converted to CIGS, gallium accumulates at the rear of the absorber layer nearing the Mo interface (Figure 1) due to the kinetics of the selenization step.

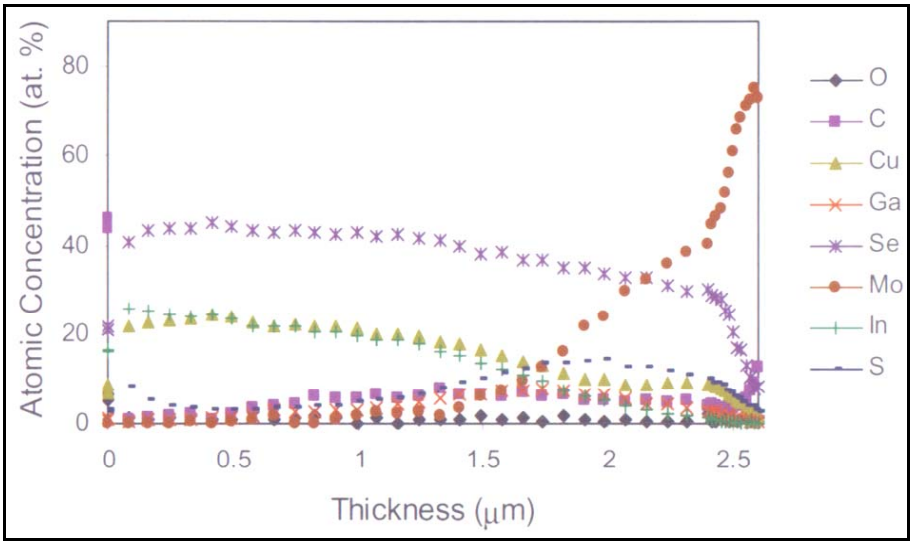


Figure 1. SIMS Depth Profile of a CIGS Absorber Layer Involving Selenization of Nanoparticle Precursors.

The lack of any gallium at the junction interface limited our ability to increase the band gap from otherwise CIS-type material, placing a ceiling on cell voltages. Consequently, as we introduced gallium in our standard nanoparticle ink process, kinetic limitations of selenization led us to focus

on externally introducing gallium at the surface to increase limited cell voltages. We investigated various surface treatments with gallium precursors and developed an understanding on the feasibility of incorporating thin layers into front-graded chalcopyrite.

2.2.3 Modifying the Surface: Method Development

In our *Lab to Large Scale Transition* effort, we experimented with both ink suspensions and solution-based deposition schemes for bringing in gallium at the surface. The general strategy was to deposit Ga-containing interlayer over the base absorber film. Through film annealing and gas-solid exchange, the interlayer diffuses and is converted *in-situ* into modified CIGS chalcopyrite (see Figure 2). Our method aims to lock gallium into the CIS structure in the active near surface region. We follow through with a post-modification etching procedure to remove defective phases from the surface.

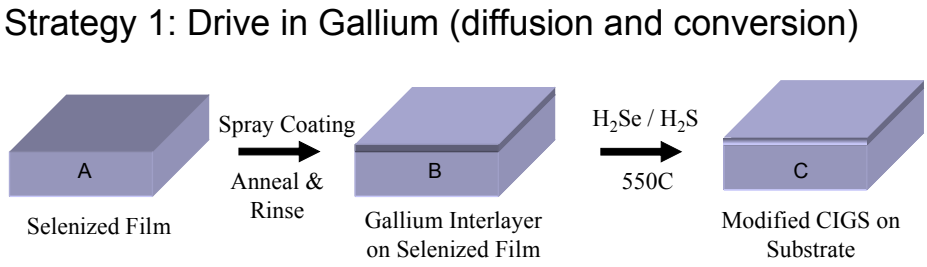


Figure 2. Method Development for Surface Modification.

2.2.4 Surface Modification and V_{OC} Enhancement

Our early attempts at modifying CIGS with gallium surface treatments were quite modest. We sprayed on thin chalcogenide films of various interlayer thicknesses, to define a window that would avoid degrading the performance of the cells. We discovered, using a single-step high temperature 'drive-in' profile that devices shorted as the thickness of the gallium containing interlayer was increased. Our main control over the thickness of the adlayer was in the time of deposition.

Time of deposition (sec) $\propto$ Interlayer Film Thickness (nm)

We could therefore directly translate the amount of gallium at the surface with spray deposition time. Using this approach, we identified three main thickness regions of interest. First, relatively thick gallium adlayers (up to ~half micron) degraded the solar cells. As we gradually went thinner, we began to see some evidence for marginal gains in open-circuit voltages until eventually our films became too thin to report statistically significant results from reference controls. These findings helped us define a more elaborate process for surface modification.

We observed during a high temperature post-annealing treatment (in an inert atmosphere) that between 400°C - 500°C we lost a substantial amount of selenium from the modified chalcopyrite. These findings are consistent with other published results showing selenium loss as an effect of high temperature annealing [3]. We understood that we would need to supplant Se-vacancies in modified films by arranging a group VI ambient during the important drive-in step. After introducing small quantities of both hydrogen selenide (H_2Se) and hydrogen sulfide (H_2S) gases independently, **we obtained respectable cell voltage increases ranging from 70-130mV from our controls**. This was our first direct evidence for gallium incorporation from the surface.

2.2.5 Tradeoff in V_{oc} Enhancement and Current Collection

Despite statistically significant voltage increases, we observed a drop in Jsc and fill factor resulting in an overall drop in the cell efficiency. We suspected that any remaining defective material (binary phases or partially reacted ternary phases) needed to be removed by etching. Our objective here was to see whether we could identify certain etching conditions that would clean up the surface and maintain device currents along with new gains in cell voltages.

Table II lists key results of various etchants in search for a selective dissolution procedure. The nature of the etchant had a direct impact on the current-voltage characteristics of processed devices after the surface modification. As a general trend, we found increased open-circuit voltages (Voc) with longer etching times up to an optimal value before eventual degradation. This trend was general for films after modification but it did not hold for etching of reverse-graded reference controls.

Table II. Effects of Etching Procedures after Gallium-only Surface Modification.

#	Etchant	Voc (V)	Jsc (mA/cm^2)	Voc (V)	Jsc (mA/cm^2)	Remarks
		Surface Modified		**Ref. Control**		
1	$HCl:HNO_3$	**0.57**	10	0.49	31	Gallium enrichment is apparent. High voltage jump +80-100mV
2	HCl	**0.50**	**34**	0.45	29	Removes extraneous material, low voltage jump +20-50mV
3	$Br_2:H_2O$	0.46	24	0.46	34	Degrades near-surface composition
4	HCl / $Br_2:H_20$	0.45	30	0.43	31	Back to statistically insignificant

Upon closer inspection, etch 1 produced our highest open-circuit voltage to date of 570mV which represents 80–100 mV improvement from reference controls. The currents however were quite unimpressive. Etch 2 on the other hand, maintained small voltage gains but it also slightly improved the short-circuit currents (Jsc). HCl is known to have an almost negligible effect on CIGS chalcopyrite with an etching rate in the tenths of Å/min.[4] We believe our etching procedure polishes our modified surface composition to help stabilize device currents, while maintaining statistically significant enhancement in the open-circuit voltages.

2.2.6 Efficiency Improvement

It can be argued that Voc gains from these surface treatments were a result of the formation of some limited, but desirable quaternary CIGS phase formation. However other defective binary phases (Ga-Se binaries) and ternary phases ($CuGaSe_2$) remaining at the surface are likely responsible for the dramatic voltage increases and current losses (Table I, Etch 1). We stipulate that the presence of a semi-infinite gallium source at the surface promotes rapid Cu diffusion into the surface adlayer. In a hydrogen selenide ambient, the surface adlayer will almost certainly produce ternary $CuGaSe_2$ (CGS) phase as the surface kinetic product in this situation before forming the quaternary CIGS phase which is our target.

It is known that making single phase CIGS from separate $CuInSe_2$ and $CuGaSe_2$ phases is very difficult and in fact hindered in the presence of Se overpressure which can include both elemental Se or hydrogen selenide.[5] By modifying the CIS surface with gallium as the singular group III metal cation, copper diffuses from the underlying $CuInSe_2$ lattice to create defective, lattice mismatched CGS ternary phase. It appears our initial strategy for depositing gallium chalcogenide in the interlayer should require elevated temperatures for the CIS/CGS system to coalesce into single-phase $CuIn_xGa_{1-x}Se_2$ at the near surface. Marudachalam *et.al.* demonstrated that solid solubility of the CIS/CGS interface is possible below 600°C [5] however as we will show, we have worked out a better solution to the problem of forming single phase surface chalcopyrite without extended reaction times which becomes costly from the manufacturing standpoint.

We adjusted our solution-spray method by adjusting the composition and thickness of Ga compounds as precursors. Using the usual post-modification selenization and light surface etching, we immediately produced a statistically significant Voc jump with stabilized current collection and fill factors. We observed an expected tradeoff in electronic properties between higher voltage and lower current The efficiency enhancement from our reference control was obtained by a characteristic Voc increase (50-70mV) with only minor losses in Jsc (0-2mA/cm^2)

resulting in a new 13.7% champion efficiency. In order to validate our established surface modification procedure, we repeated the treatment on a sister control and obtain similar result. The I-V curves for the modified solar cells are shown below in Figure 3 with device parameters given in Table III.

These results confirmed that by manipulating the surface, we are able to enhance the overall CIGS cell efficiency primarily by increasing the open-circuit voltage. There is still further room for improvement.

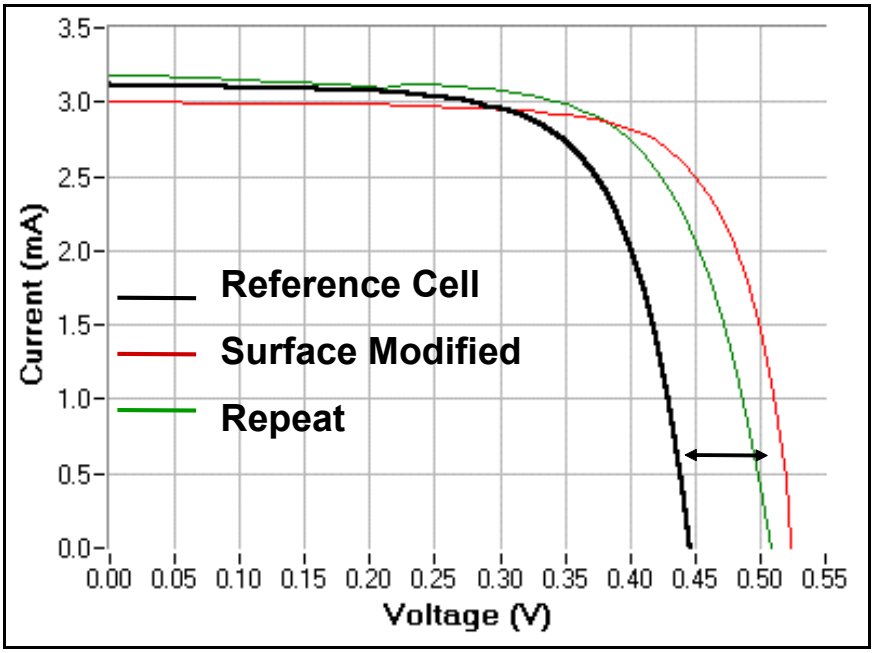


Figure 3. I-V Characteristics of 13.7% Champion Solar Cell by Surface Modification. Devices are without anti-reflection coating under AM1.5 illumination.

Table III. Overview of CIGS Solar Cell Parameters with Surface Modifications

Device Parameters	Ref. Control	Surface Modified	Repeat
Voc (mV)	446	**524**	**508**
Isc (mA)	3.12	3.00	3.19
Jsc (mA/cm^2)	37.09	35.74	37.92
FF	0.69	0.73	0.68
Pmax (mW)	0.96	1.15	1.10
Eff (%)	**11.4%**	**13.7%**	**13.0%**
Area (cm^2)	0.084	0.084	0.084
Irrad (mW/cm^2)	100	100	100

2.2.7 When Cell Efficiency Can be Improved

We find that stoichiometric control over the final Cu/(In+Ga) ratio by surface modification is highly sensitive to the thickness of the Ga surface layer deposited with a tolerance of only a few tens of nm. As expected, minor thickness variations in the thin to ultrathin region can have a dramatic effect on the final semiconductor composition. Attempts to incorporate gallium rich adlayers at the surface are successful at boosting Voc only when extraneously deposited Ga-containing material does not exceed a critical thickness range defined by the following:

(i) the starting I/III composition, with slight copper rich side being more desirable,
(ii) the density and relative thickness of adlayer to bulk absorber film, and most importantly,
(iii) time of reaction.

We have developed an understanding on the role of kinetics governing the extent of Ga incorporation at the surface. First, we have shown by simulation that while there may be semi-infinite thickness combinations of adlayer:bulk capable of producing photoactive $CuIn_xGa_{1-x}Se_2$ front-graded film compositions (where x varies through the depth of the film), there is a very narrow operating regime in a surface modification strategy to give an adequate depth distribution that produces any beneficial effect of Ga-grading. As a consequence, this limits the starting copper concentration and defines the cross section of wide band gap layers that can be externally grown.

- When the modification layer exceeds the critical thickness, net gains in Voc are coupled with systematic losses in Jsc and FF with no overall efficiency improvement.

- When the modification layer is within the critical thickness, net gains in Voc are preserved (subject to near surface composition) with stabilized Jsc and FF producing a net efficiency increase.
- When the modification layer is below the critical thickness, no statistical gains in any cell parameters are observed from the baseline efficiency

We need to develop these ideas further in this work which are of course very route specific. The chemical nature of the gallium precursor will define the rate of formation of target single-phase chalcopyrite versus defective ternaries. So it is the thickness control along with the reaction path and time that will govern the ability to increase the efficiency.

Our strategy of surface band gap engineering requires that the surface produces wide band gap material to increase Voc, yet is thin enough to allow lower band gap material deeper within the absorber to absorb lower energy photons and maintain values of Jsc. This approach to band gap tuning by Ga-incorporation may avoid bulk effects of voltage-dependent current collection observed by Shafarman *et. al.* in which current losses offset gains in open-circuit voltage to argue that efficiency is independent of the band gap for non-graded CIGS films.[6] Our approach to band gap tuning has already given us a 1% to 2% efficiency improvement from baseline efficiency.

2.2.8 Future Tasks to Support High Efficiency Processing

The operating domain established for surface modification is highly sensitive to the adlayer thickness and reaction time, which dictates final semiconductor composition and depth distribution. In fine-tuning the graded composition band gap, we need to continually optimize adlayer composition with reaction time. We have subsequently discovered that copper must diffuse to the surface from the bulk and that extraneous addition of copper at the surface forms defective material.

We have demonstrated our solution-spray method as a versatile, scalable method that will modify the surface of CIGS films to stoichiometric control. However since the surface composition changes with Ga content, the resulting amount of gallium incorporated into chalcopyrite lattice is consequently controlled by counter-diffusion of copper.

As a consequence, the process of Ga-incorporation is limited by the diffusion of copper and the homogenizing force governed by Fick's Law which washes out concentration gradients. Copper depletion at the surface is a major challenge since it leads to defective material and degradation in cell parameters stemming from possible type-inversion. ***As a practical***

matter, there is a dynamic competition between surface diffusion and over-selenization.

Additionally, we have some indication that by removing sodium from the bulk of the absorber, we may enhance the diffusivity of Ga in CIS along grain boundaries.[7] This however, should be countered by sequential addition of Na after modification.[8-9] We are continually building a body of knowledge on CIGS surface treatments to increase solar cell output. This activity will lead us to our 15-16% goal by non-vacuum processing.

2.3 PROCESS IMPROVEMENT, CONTROL & RECYCLING ISSUES

In parallel with surface modification, we concentrated efforts on optimizing our reduction and selenization steps for process scale-up. By investigating reaction kinetics under our goal of large-scale production, we were able to make changes which have led to both a larger size and quantity of high efficiency CIGS solar cells. Our efforts directly impact process throughput and yield capability.

2.3.1 Recirculation of H_2/N_2 Gasses

In phase I we set up a recirculation system for the large area reduction furnace with the objective of reducing the amount of gas which is used during each run. This system was designed to re-circulate the internal gases, while siphoning out both H_2O and oxygen. The chamber is filled with a hydrogen/nitrogen mixture, and then the gas is circulated through a liquid nitrogen cold trap, which freezes any water in the gas system. The water-free gas mixture is then fed through a moisture/oxygen trap, and again flowed over the sample being reduced. The flow of gas over the sample using the circulation pump is greater than that of gas being fed via a compressed gas cylinder, so the rate and degree of reduction of the Cu-In-Ga oxide films increases, allowing us to process a large number of substrates uniformly. Initial experiments have demonstrated that this concept is very effective in the conversion of the Cu-In-Ga oxides to the metal alloy. The highest efficiency of a CIGS solar cell reduced via a recirculation reduction scheme was 8.8 %, and its I-V characteristics are shown in Figure 4.

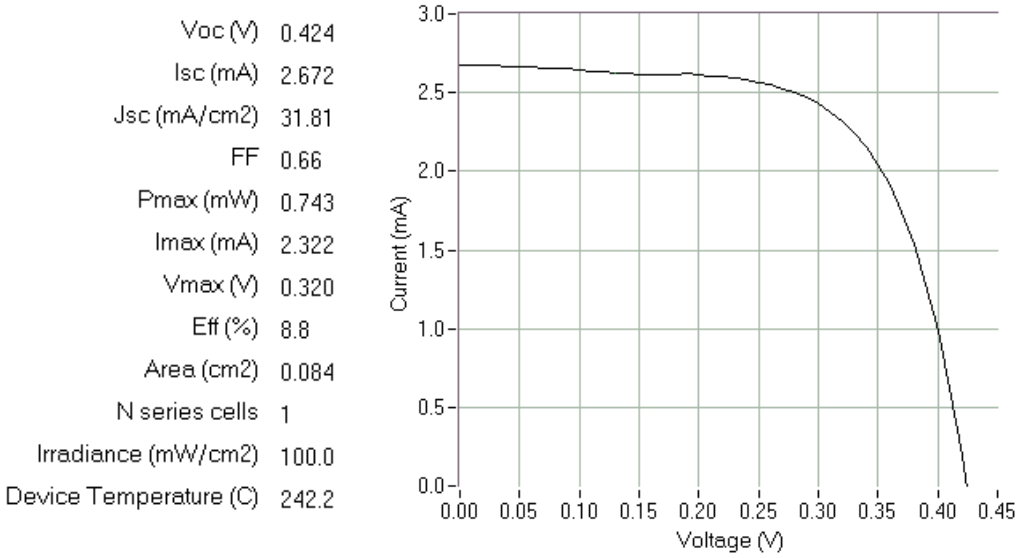


Figure 4. I-V Characteristics of Best Cell using Recirculation of Gases in Reduction.

2.3.2 Processing of Large Area Devices

We are currently processing large area samples for both the reduction of Cu-In-Ga oxides to alloy and selenization of the alloy to CIGS. The largest single sample that can be processed in one run is 13.3 cm x 28 cm and has been demonstrated on molybdenum foil. Figure 5 is a typical sample size which is cut from the single large device for processing and testing.

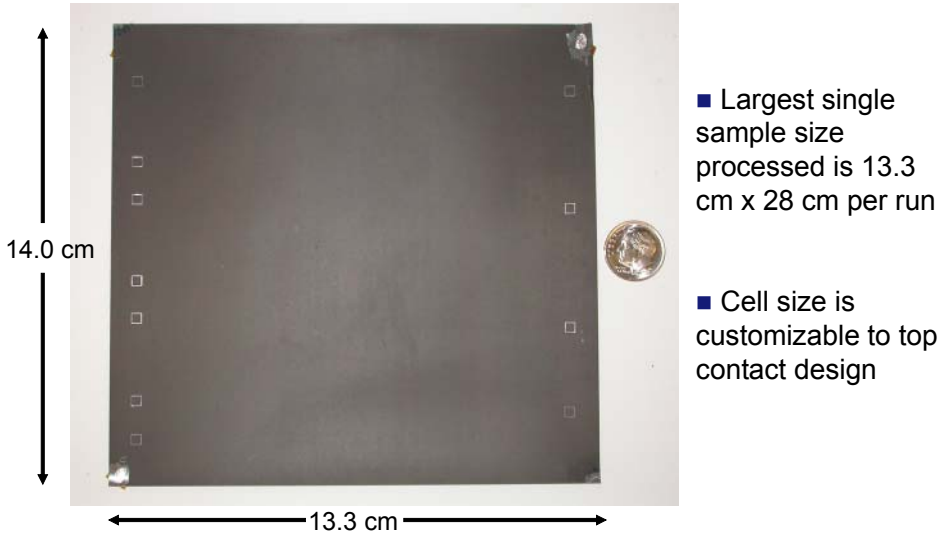
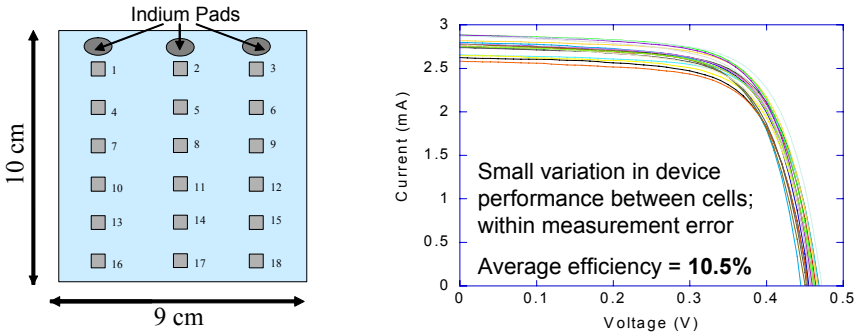


Figure 5. Typical Large Area Samples Processed.

2.3.3 Uniformity of Large Area Devices

In Phase I we demonstrated high efficiencies for samples produced in our large area furnaces. As a quality control check in Phase II, a study was conducted to investigate the uniformity of the samples. A section of a large area sample was cut to 9 cm X 10 cm and multiple devices were tested over the entire area. The sample showed high uniformity over the entire cell area with a normal distribution. Cells had high efficiencies averaging 10.5% (AM 1.5). Figure 6 illustrates the individual I-V curves and data taken for each device.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Voc	0.465	0.456	0.469	0.455	0.462	0.468	0.461	0.462	0.472	0.460	0.461	0.463	0.459	0.450	0.466	0.458	0.452	0.445
Isc	2.76	2.78	2.75	2.62	2.75	2.66	2.65	2.75	2.87	2.88	2.77	2.88	2.88	2.78	2.82	2.78	2.74	2.80
Jsc	34.47	33.07	32.69	32.80	32.77	31.61	33.09	32.77	34.18	34.33	32.94	34.34	34.26	33.04	33.56	33.07	34.23	34.96
FF	0.69	0.69	0.69	0.68	0.68	0.69	0.68	0.68	0.69	0.68	0.66	0.68	0.67	0.67	0.69	0.69	0.68	0.68
Pmax	0.88	0.87	0.89	0.81	0.86	0.86	0.83	0.86	0.94	0.91	0.84	0.91	0.89	0.84	0.91	0.87	0.84	0.84
Eff	**10.99**	**10.35**	**10.54**	**10.14**	**10.28**	**10.27**	**10.39**	**10.28**	**11.16**	**10.78**	**10.05**	**10.87**	**10.57**	**10.00**	**10.84**	**10.42**	**10.53**	**10.52**

Figure 6. Device Uniformity Study with an Average Efficiency 10.5% (AM1.5)

2.4 MODULE INTEGRATION

Under the current "Lab to Large Scale" transition contract, ISET is developing a non-vacuum monolithic integration scheme for depositing top contacts on its CIGS solar cells. In this scheme we are evaluating epoxy based silver inks that can be screen printed on top of the ZnO window layer to form top contacts. Silver top contacts are more advantageous over ZnO layer, both for current collection and for monolithic integration. On a cell level the significantly higher conductivity of the silver contacts lowers the series resistance of the cell, there by resulting in higher fill factors and higher currents. On a module level since cell to cell connectivity is through the silver pattern, it relaxes the conductivity requirements on the ZnO layer, thereby allowing us to deposit thinner layers. Thinner window layer permits greater light transmission to the p-n junction which in turn increases the short circuit current of the solar cell. Moreover, monolithic integration via silver pattern somewhat immunizes the cell from changes in the

properties of the ZnO layer over a longer period of time. Increased resistivities of ZnO as a result of window layer degradation will have a minimal impact on the properties of the cell or module since the current collection over larger areas is primarily via the silver pattern. Similarly, degradation of ZnO layer conductivity will also not affect the cell to cell connectivity in a module.

During Phase I, the primary focus of this task was to identify commercially available silver inks that could meet the minimum criteria necessary for forming good contacts to the top ZnO layer of ISET's CIGS solar cells. Unlike silicon solar cells where the top contacts are processed at above 600°C, top contacts on CIGS solar cells cannot be processed above 200°C as that will destroy the photoactive junction. This implied that the inks had to be polymer/epoxy-based and curable below 200°C. In addition to the temperature limitation, a successful ink should meet two criteria. First, it should exhibit minimal contact resistance in contact with the TCO layer. Second, it should have minimal resistive losses for current conduction within the silver grid pattern. In phase I, over 50 inks from several vendors were screened for the above criteria and based on their listed bulk/sheet resistivity specifications followed by in-house testing, 20 inks qualified for further testing on the CIGS solar cell.

During Phase II, as the experiments below describe in detail, the inks were screen printed onto high efficiency CIGS cells and the I-V properties of the resulting devices were evaluated. Based on the I-V properties of the printed contacts and their long term stability we have now been able to narrow down the choice to 4 inks. While the primary focus of this task was to develop the top contacts, towards the end of phase II efforts were also directed towards lamination and module formation.

2.4.1 Stability of CIGS Solar Cells at 200°C

Until the beginning of Phase II, one of the assumptions that had never been investigated, at least at ISET, was the stability of the CIGS/CdS junction to exposure at high temperatures. At ISET, deposition of ZnO by Low Pressure OMCVD necessitates the exposure of the p-n junction to 150-190°C for times ranging from 10-30 minutes. The need for curing the ink further increased this high temperature exposure to >3 hrs. We realized that these process conditions were unique to ISET and others doing OMCVD deposition of zinc oxide. Several other labs working with CIGS cells use other techniques to deposit their TCO layers which do not require exposing the samples to temperatures above 100°C. Moreover, they do not deposit silver top contact which in our case makes additional exposure of the cell to high temperatures necessary.

2.4.2. Effect of Time of Sample Exposure at 170°C on I-V properties

Based on literature reports, our original assumption was that the p-CIGS/CdS junction was stable up to 200°C for a significant period of time. However experiments done in this Phase II gave results that

indicated otherwise. In one experiment samples with multiple CIGS solar cells *without contacts* were heated on a hotplate at 170°C for up to 90 minutes. The samples were periodically taken off the hotplate, cooled to room temperature and their I-V properties were measured. Figure 7 shows the I-V characteristics of three CIGS samples with multiple small area (0.084 cm^2) cells scribed on each sample.

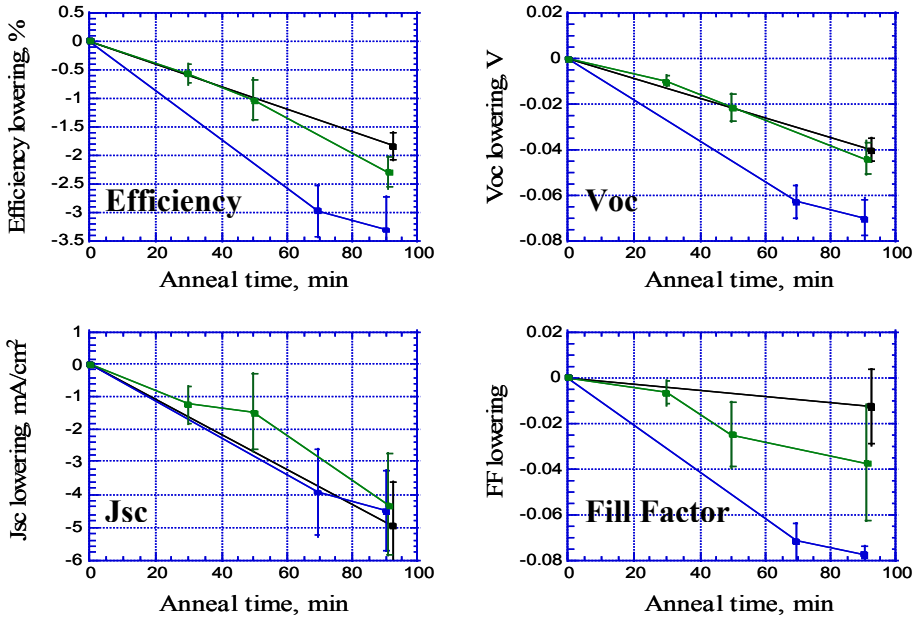


Figure 7. Degradation of Device Properties as a Function of Exposure Time at 170°C. The black, green and blue curves each represent a sample with multiple identical CIGS cells. In each graph, the data point on each curve shows the average **absolute** lowering of value (Efficiency, Voc, Jsc, FF) measured from all the cells on that sample and the error bars show their scatter.

The results show that <u>all</u> the parameters of the cell degrade when held at 170°C in air for an extended period of time. In each graph, the data point on each curve shows the average value (Efficiency, Voc, Jsc, FF) measured from all the cells on that sample and the error bars show their scatter. By using three samples which were taken off the hotplate at different times, it is clear that *the degradation is cumulative and worsens with increased duration of exposure*. More importantly, the *extent* of degradation is of significant concern. The three samples tested lost **an average of 2-3 absolute %** in efficiency as a result of this exposure to high temperature.

2.4.3 Effect of Temperature on the I-V Properties of CIGS Cells

Next, we evaluated the temperature at which the cell degradation started. A sample was held for 30 min each at successively higher temperatures to see how much the cell properties degraded at each temperature. After each

exposure the sample was cooled to room temperature to measure its I-V properties.

The results, shown in Figure 8 indicates that the efficiency, Voc and FF decrease as the sample is successively exposed to higher temperatures. Initially the Jsc also decreases as the sample is exposed up to 130°C. Further heating of sample at higher temperatures lowered the Jsc loss, bringing it closer to pre-anneal values. The cause of this behavior in Jsc is presently unknown. Overall, however, **the data reveals that the degradation starts at temperatures as low as 100°C and gets worse at higher temperatures.**

Together, the exposure time and temperature experiments show that the CIGS solar cells are not stable at around 170°C. The ramification of these observations is that in order to suppress cell degradation, the contacts must be cured at or below 100°C. Furthermore, the curing time should be minimized so as to limit the high temperature exposure.

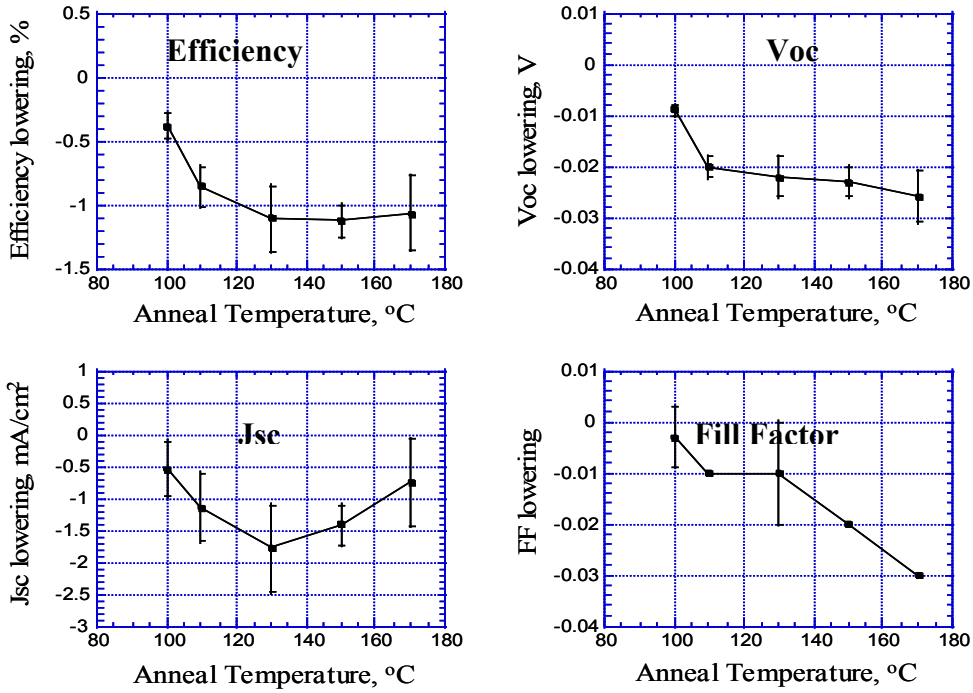


Figure 8. Degradation of Device Properties as a Function of Anneal Temperature. Starting at 100°C, the solar cell was successively held at each temperature for 30 minutes**.**

With the stability limit of the CIGS/CdS junction lowered to 100°C, we had to iterate back to validate the curability of the selected silver inks at 100°C. Some more experiments were done to re-establish whether i) the inks could be cured at 100°C to achieve bulk resistivities specified by their

manufacturer and ii) whether the contact resistance of inks cured at 100°C was low enough to make good ohmic contacts to ZnO.

2.4.4 Can Inks be Cured at 100°C?

Even though most of the inks we are testing have recommended curing temperatures well above 100°C, we nonetheless evaluated their curing properties at 100°C. Identical patterns of the various silver inks were deposited on glass and cured for increasing lengths of time at 100°C. Table IV shows the thickness of the test patterns used, the vendor specified resistivity of the 'cured' inks and the measured resistivity as a function of the curing time. In general, the resistivity went down as the inks were cured longer.

As the numbers indicate, however, different inks behaved differently. Some inks (#1, 7, 8, 9, 19 and 20) initially exhibited very high resistivity and even after four hours of curing did not reach their specified 'cured' resistivity limit. Other inks (#2, 3, 5, 12, 14, 15, 18) exhibited resistivities that were near or below their specified 'fully cured' values only after 30 min of curing and improved even further with increased curing time. This observation was very encouraging because it indicated that the desired 'in-pattern' conductivity was achievable even at 100°C.

Table IV. Measured Resistivity of Silver Inks Cured at 100°C.

Ink #	**1**	**2**	**3**	**5**	**7**	**8**	**9**	**12**	**14**	**15**	**18**	**19**	**20**
Pattern thickness, microns	18	16	29	17.5	34	22	18	16	42	20	28	28	16.5
Vendor Specified Resistivity, μ-ohm-cm	<51	35	<200	30	25	25	<38	50	116	51	<100	7	25
Cure time, minutes	**Measured Resistivity, micro-ohm-cm**												
30	65	39		19		35	122				107	11883	31
60	60	37	87	20	77	34	113	24	95	50	102	1467	29
120	57	36	83	20	73	32	108	23	82	46	99	710	28
240	53	35	79	20	72	30	103	21	75	44	95	38	27

2.4.5 Stability of CIGS Cells at 100°C

Having established that several inks could be cured at 100°C, we evaluated the degradation of the CIGS solar cells at 100°C. Two small area (0.084 cm^2) CIGS cells (without silver contacts) were annealed at 100°C and I-V properties were measured every hour to measure performance loss. As shown in Figure 9 the cell efficiency seemed to improve marginally initially for up to 2 hrs of annealing at 100°C and then started dropping down.

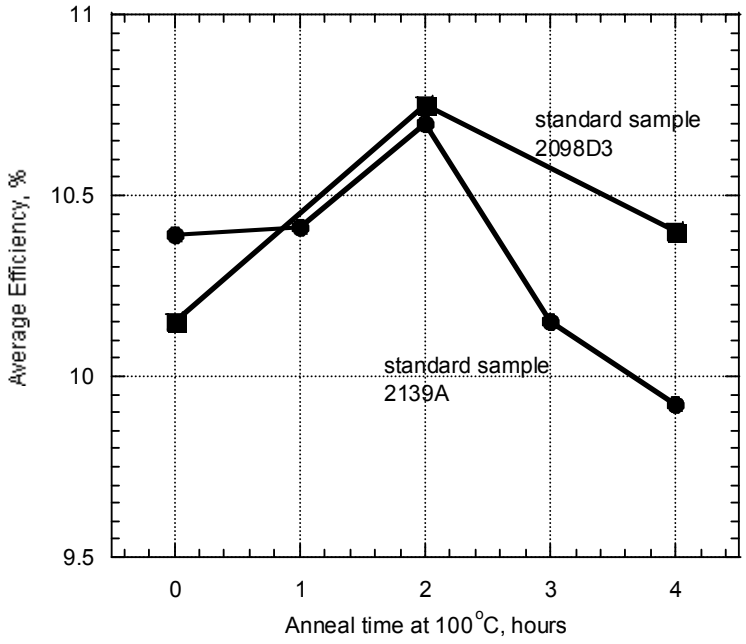


Figure 9. Change in Cell Efficiency as a Result of Heating at 100°C for up to 4 Hours.

In the follow up experiment the number of samples was expanded to get some statistical measure of change in I-V properties when the samples were annealed at 100±10°C for up to 2.5 hours. I-V properties of 21 small area (0.084 cm^2) CIGS cells (without silver contacts) measured before and after annealing showed that the average loss in efficiency was only 0.4% (absolute). In fact, in some samples there was no loss of efficiency observed after annealing. This number is significantly less compared to the data in Figure 7 in which the samples lost 2-3% efficiency when heated only for 90 minutes at 170°C. In essence, we can safely say that **there was no significant degradation in cell efficiency when the cells were annealed at 100°C.** The efficiency loss observed in this experiment set up a basis by which to differentiate the effect of 'contact resistance' from the effect of solar cell degradation when evaluating the cells with silver contacts.

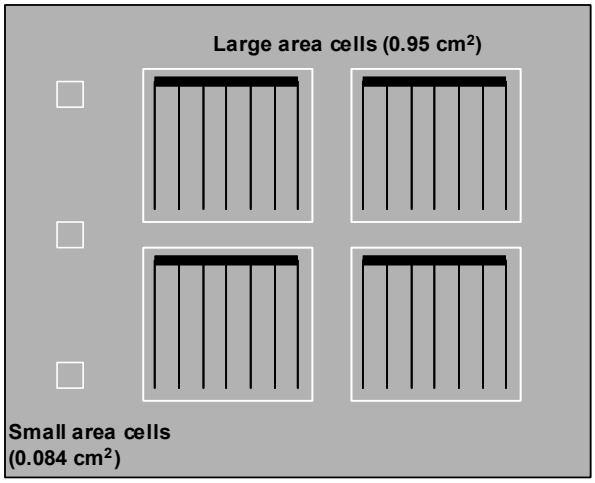


Figure 10. Schematic of a CIGS Sample Used for Contact Resistance Tests. Each sample contained several large area (0.095 cm^2) cells with contacts printed from one ink and small area (0.084 cm^2) cells with no contacts.

2.4.6 Contact Resistance of Screen Printed Inks Cured at 100°C

To evaluate the 'quality' of the contact between the silver ink and the ZnO layer, contacts were screen printed on completed solar cells as shown in Figure 10. Twenty one such device samples were made - one for each ink. Each sample had several identical silver patterns printed on it with one ink (for quasi-statistical purpose). Cells of approximately 0.95 cm^2 area were isolated around the silver patterns. In addition, several small area (0.084 cm^2) cells were also scribed on the same sample. The small area cells had no silver patterns on them. Each sample was annealed on a hot plate for 2.5 hours at 100±10°C to cure the silver ink patterns. After annealing, the samples were cooled to room temperature and I-V properties were measured both on small and large area cells.

Table V compares, for each ink/sample, the I-V characteristics of the best large cell and of the best small cell on the same sample. The large cells have the printed top contact whereas the small cells do not because the conductivity of the ZnO is sufficient for the small cells. Since the small cell data mentioned here is also taken *after* annealing, any changes (degradation or improvement) in the I-V properties arising from the cell are common to both the small and the large cells. Hence, the *difference* in the performance, outlined in table IV is solely due to the 'quality' of the contacts.

Table V. Comparison of Large and Small Area Cells Scribed on a Sample.

Group	Ink #	**Best Small Cell** 0.084 cm^2 (**without** Printed Contacts)					**Best Large Cell** 0.95 cm^2 (with Printed Contacts)			
		Eff %	**Voc** V	**Jsc** mA/cm^2	**FF**		**Eff** %	**Voc** V	**Jsc** mA/cm^2	**FF**
I	12	11.3	0.492	35.0	0.66		**12.3**	0.489	40.1	0.63
	15	10.0	0.482	30.7	0.68		11.9	0.484	**42.3**	0.58
	9	10.4	0.500	33.7	0.61		11.7	0.494	36.9	**0.64**
	8	10.2	0.491	33.9	0.61		11.3	0.493	39.2	0.58
	19	10.2	0.475	32.8	0.65		11.1	0.484	35.9	**0.64**
	20	10.3	0.485	33.3	0.64		11.0	0.479	35.8	**0.64**
	3	9.6	0.478	32.1	0.63		10.7	0.473	35.9	0.63
	1	9.7	0.491	29.9	0.66		10.6	0.486	38.4	0.57
	2	9.8	0.475	32.2	0.64		10.2	0.478	35.5	0.60
	14	9.9	0.475	31.7	0.66		10.1	0.463	39.4	0.55
II	11	10.9	0.477	35.1	0.65		9.7	0.487	34.0	0.58
	13	10.9	0.513	35.7	0.59		9.6	0.496	38.8	0.50
	10	11.7	0.505	34.5	0.67		9.6	0.504	35.2	0.54
	5	11.2	0.497	34.1	0.66		8.2	**0.507**	35.3	0.46
	18	9.5	0.471	31.7	0.64		7.0	0.465	32.3	0.47
	6	10.1	0.484	33.3	0.62		6.5	0.478	37.5	0.36
	22	10.9	0.504	34.9	0.62		6.0	0.502	36.4	0.33
	17	11.2	0.486	34.3	0.67		5.3	0.485	33.8	0.33
	7	11.3	0.478	35.5	0.67		4.4	0.456	35.4	0.27
	16	10.3	0.487	32.5	0.65		4.3	0.481	34.0	0.27
	4	11.3	0.514	36.9	0.60		0.7	0.466	9.4	0.17

The large cells have printed contacts and the small cells do not. The highest values for each parameter measured on the large cells are given in bold.

Comparing the large cells with the small cells several interesting observations can be made:

- **Voc:** On average the Voc differ by less than 5 mV indicating that the same p-n junction is determining the I-V characteristics in both cases.
- **Jsc:** The Jsc in large cells is, on average, 3 mA/cm^2 *higher* than in small cells. This is a testament to better current collection through the silver prints as compared to the ZnO layer. It also confirms that inks can be sufficiently cured at 100°C to make a good ohmic contact with the ZnO layer.
- **FF:** The FF is the critical factor differentiating the 'good' inks from the 'bad' inks. It incorporates the combined effects of the Ag/ZnO 'contact' resistance and the 'in-pattern' conductivity of the ink. 'Good" inks are those where the difference in FF is positive (greater FF in the large cell) or, at worst, is marginally negative. 'Bad' inks are those where the FF of the large cell is significantly worse than the FF of the small cell.

- **Efficiency:** The behavior of the inks can be broadly classified into two groups. The first group is those where the large cells are *better* than the small cells. Several inks fall in this group (group I) and all are viable candidates for further testing. The second group (group II) is where the performance of the large cells is worse than that of the small cell. These inks were not tested further.

Figure 11 shows the I-V characteristics of the best large area cell made so far with the screen printed contact **with an efficiency of 12.3% (AM1.5)**. As the data in Table V suggests, these cell characteristics are limited by the performance of the underlying p-n junction and not by the properties of the top silver contact.

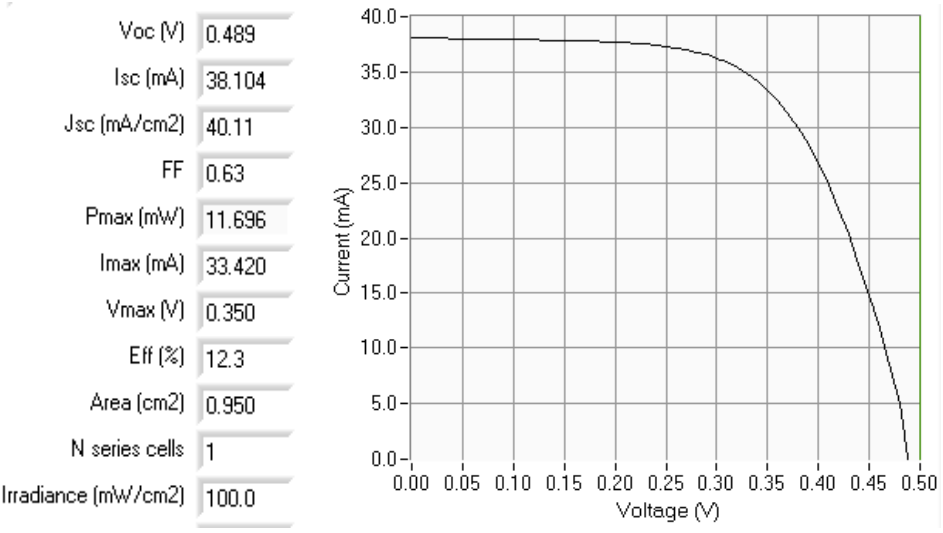


Figure 11. I-V Curve of a CIGS Solar Cell with a Screen Printed Top Contact.

2.4.7 Long Term Stability of Screen Printed Contacts

Long term stability of printed contacts is a critical factor in determining the best ink for making contacts. To determine the long term stability of the silver ink-ZnO junction, CIGS cells were evaluated at several weeks' intervals on samples that had been cured at 100°C. Data was collected on the large cells with the printed contacts to evaluate the overall change in both the silver/ZnO interface as well as the underlying cell. Data was also collected on small cells that did not have the contacts to get a baseline measurement on how the underlying cell itself was changing with time. Difference between the two yielded information on the evolution of silver/ZnO interface with time.

Evaluation of small cells on eleven different samples indicated that there was typically a 0.5-1.5% loss in efficiency when the cells were left (unencapsulated) under ambient conditions for almost three months. In

contrast, the cells with silver contacts lost 1.5% or more in efficiency in the same time period. Looking at the difference between the two, it was clear that there was some degradation of the contacts when the samples were left in air. The 'best' inks were determined to be those that showed least loss in efficiency compared to the underlying cell. Figure 12 shows the observed change in efficiency of the best four samples.

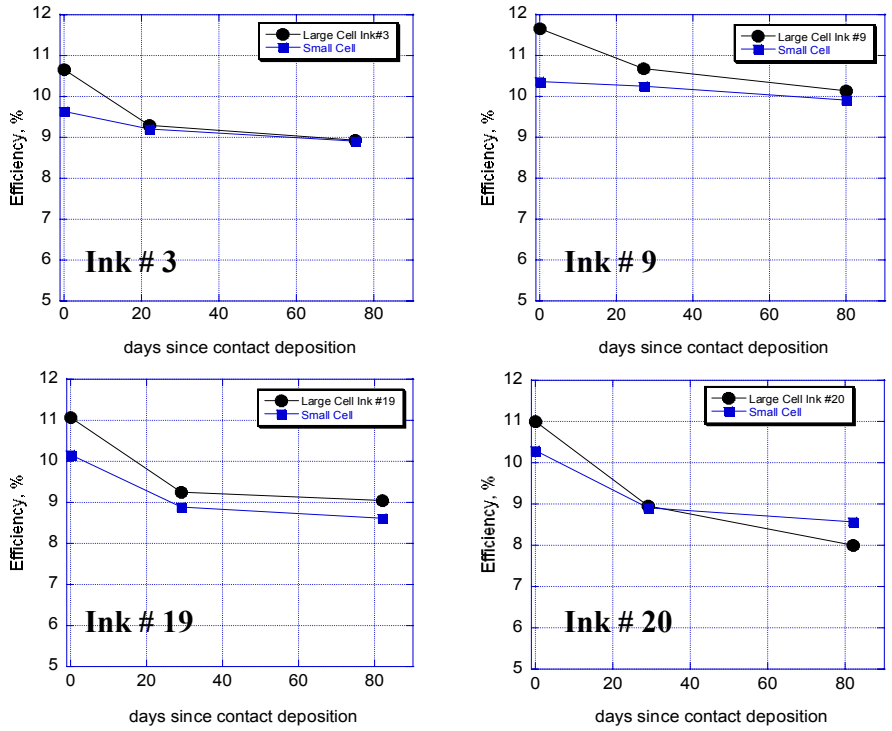


Figure 12. Stability of CIGS Cells with and without Screen Printed Silver Contacts. Blue squares represent efficiencies measured on small area (0.084 cm^2) cells with probes placed on the ZnO. Black dots represent efficiencies measured on large area (0.95 cm^2) cells with probes placed on the screen printed silver prints.

2.4.8 Module Fabrication

In the second half of Phase II, in parallel with the development of screen printed contacts, efforts were also directed at fabrication of modules. 8 cm X 10 cm modules containing 8 cells were fabricated on glass as well as on non-conducting Upilex substrates. The (rigid) modules on glass were made on patterned Mo on which the absorber was deposited and processed. Upon device completion, areas were opened up to expose the back Mo. The entire silver pattern was then screen printed in such as way that the pattern formed the front contact on each cell as well as connection to the back Mo of the neighboring cell. In this manner, monolithic integration was achieved in parallel with top contact deposition.

The flexible modules were made from individual Mo cells that were cut to size from a large Mo sample and then pasted onto a Upilex backing. Areas were opened up in the cell where the silver ink would make contact with the Mo. As with the module above, the entire silver pattern was then screen printed to form the module. Figure 13 shows the I-V curve of a flexible module made in this manner. The low overall module efficiency is in part due to the low efficiency of some of the individual cells in this module. Segments of this module gave overall efficiencies that were almost twice as high as that shown below for the entire module.

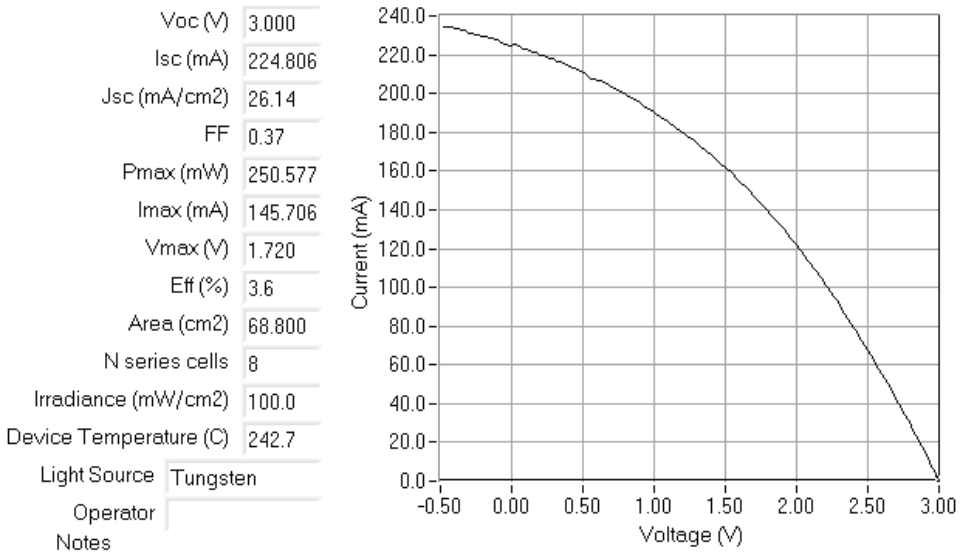


Figure 13. I-V Characteristics of a Flexible CIGS Module.

This is ISET's first foray into fabrication of modules using monolithic integration involving metal top contacts. Hence we are undergoing a sharp learning curve as we fabricate these modules. During the several trials we found that the contact points where the silver ink pattern jumps over from one cell to the other was the weakest link and often broke when the sample was handled. We have now introduced backing support underneath where the contacts are, to ensure that much of the stress is handled by the support. We are varying the design of the top contacts to improve contact reliability. Further improvements are expected as we gain more experience in integrating the cells.

In addition to module formation, we have also started lamination of modules. Vacuum lamination and roll lamination are both being tried and the time-temperature conditions are being optimized to get good quality lamination.

2.4.9 Summary of Work on Screen Printed Contacts

Overall Phase II was very productive in advancing ISET's understanding and ability to form top contacts on the CIGS cells. Several commercial silver inks were screened and a couple of them were able to form good quality contacts to the ZnO layer even at a lowered curing temperature of 100°C. We discovered that the stability limit of our CIGS cells was at a lower temperature than expected. **Using silver top contacts we were able to make a 12.3% efficient cell.** We also performed some preliminary evaluation of long term stability of the contacts and the results were promising.

2.5 FUTURE TASKS

Continuing research efforts will focus on building up main tasks outlined in this report. We will focus on surface modification strategies to improve the solar cell efficiency by increasing open-circuit voltages to achieve 15% cell efficiency. We will push to make CIGS solar cells with screen-printed contacts and carry over the process to produce monolithically integrated modules with printed contacts.

In Phase III several tasks have been identified to achieve the ultimate goal of module fabrication. The observation of cell degradation at temperatures above 100°C has given rise to the issue of "thermal budget" of the cell. Is there a certain combination of heating time and temperature beyond which the CIGS cell starts to degrade? The process elements which comprise the "thermal budget" are ZnO deposition, contact deposition and lamination. Can either of these processes be done with equal effectiveness at a lower temperature or in shorter duration? Are there alternate means of affecting either of these steps that does not require raising the device temperature above 100°C. For example, can the ZnO deposition be made at a lower temperature or in a shorter duration? Can we develop alternate methods for top contact deposition e.g. electrodeposition of contacts. Can the lamination be done at a lower temperature (e.g. using alternate materials) or faster.

In Phase III, a lot more effort will be spent on module interconnection and lamination. We will continue to develop our proprietary low cost scheme for patterning back Mo contacts. Top contact patterns will evolve to ensure interconnect reliability. Lamination will further assist in increasing the robustness of the interconnects. We also believe that lamination will improve the long term stability of the contacts and the cells.

2.6 PHASE II SUMMARY

The overall philosophy of this work is to carry out R & D in areas that directly impact the cost of production of modules in a manufacturing plant such as module power output i.e. watts/ft^2, overall process yield and materials utilization. To make the non-vacuum process suitable for large scale production, we address key

issues in a complete module fabrication process and collect the necessary data so that the *Lab to Production* transition will be made with no surprises. The data and information collected in this study will be used to design scaled up process equipment for large volume production.

Focus on Efficiency
The main focus presented for improving the cell efficiency is to perform the composition gradation on the surface of CIGS absorber layers such that there are Ga rich regions in the front near the junction coming from surface treatments. This Ga profile in the absorber layer may be able to take advantage of both a back surface field reflector (from our selenization scheme) for better current collection and at the same time higher V_{oc}'s from gallium rich regions near the junction resulting in higher efficiency solar cells.

In the first year we evaluated various approaches for gallium surface treatments and narrowed the field to identify a suitable approach for adaptation into a large scale manufacturing of CIGS modules. We have demonstrated higher cell efficiencies by surface treatment, and are developing the science necessary that will take us to our goal of 15% at the cell level. We will continue improving the efficiency of solar cells throughout the entire duration of this contract by way of surface treatments.

Focus on Process Improvement, Control and Recycling
We have initiated kinetics and engineering studies of the reduction and selenization process, effects of temperature, pressure and gas flow regimes leading to a design of production furnaces suitable for processing large area substrates. We have brought online these new larger capacity furnaces, and have transferred our process with optimized profiles to produce high efficiency solar cells using our nanoparticle, ink-based fabrication scheme. Our new larger-capacity design includes the development of a recirculation system for the recycling of gases; sensors, detectors and traps for process control. Our efforts directly impact process throughput and yield capability with higher materials' utilization. We were able to make changes which have led to both a larger size and quantity of high efficiency solar cells with high device uniformity.

Focus on Monolithically Integrated Modules
The major challenge lies in finding proper conducting and insulating inks that could be screen printed with the kind of precision that we will need for monolithic integration of modules with *printed* contacts. We identified several commercially-available inks and are in the process of lowering the contact resistance for monolithic integration that will be the focus of Phase II and III of this contract. We also performed some preliminary evaluation of long term stability of the contacts and the results were promising

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REPORT DOCUMENTATION PAGE

Form Approved
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1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
January 2005	Phase II—Annual Technical Report	August 2003-July 2004

4. TITLE AND SUBTITLE
Lab to Large Scale Transition for Non-Vacuum Thin Film CIGS Solar Cells: Phase II—Annual Technical Report, August 2003-July 2004

5a. CONTRACT NUMBER
DE-AC36-99-GO10337

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
V.K. Kapur, A. Bansal, O.I. Asenio, M.K. Shigeoka, P. Le, B. Gergen, M. Rasmussen, and R. Zuniga

5d. PROJECT NUMBER
NREL/SR-520-37284

5e. TASK NUMBER
PVB55101

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
International Solar Electric Technology, Inc. (ISET)
8950 Lurline Avenue
Chatsworth, California 91311

8. PERFORMING ORGANIZATION REPORT NUMBER
XCQ-230630-30

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSOR/MONITOR'S ACRONYM(S)
NREL

11. SPONSORING/MONITORING AGENCY REPORT NUMBER
NREL/SR-520-37284

12. DISTRIBUTION AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

13. SUPPLEMENTARY NOTES
NREL Technical Monitor: Harin S. Ullal

14. ABSTRACT *(Maximum 200 Words)*

The purpose of this subcontract, as part of the R&D Partners category is to: (i) identify the challenges that International Solar Electric Technology, Inc. (ISET) may face in the process of making a “Lab to Large Scale” transition for its ink-based non-vacuum process in production of thin-film CIGS solar cells and modules, and (ii) develop workable solutions for these challenges such that they can readily be implemented in a large-scale processing line for CIGS modules. The primary objective of this research is to streamline ISET’s ink-based non-vacuum process for fabricating efficient CIGS modules to lower the cost of module production << $1.0/watt. To achieve this objective, ISET has focused R&D efforts on investigating topics that directly impact the ultimate cost of processing CIGS modules. These topics of concern include (i) module output, and therefore, the solar cell and the module efficiency, (ii) overall process yield which requires developing a process that offers a very high degree of repeatability for every manufacturing step, and (iii) a process approach that maximizes the utilization of the materials used. In accordance with the above, this report will cover activity during Phase II in the investigation of methods for low-cost manufacturing and process development. Specific tasks cover four broad areas: (1) solar cell efficiency, (2) process control, (3) module integration, and (4) enhanced material utilization by reduction of waste stream.

15. SUBJECT TERMS
PV; module; solar cells; manufacturer; thin film; ink-based non-vacuum process; large-scale transition; photoactive junction; open-circuit voltage; nanoparticle precursors; screen-printed contacts;

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			19b. TELEPONE NUMBER (*Include area code)*
Unclassified	Unclassified	Unclassified	UL		

Standard Form 298 (Rev. 8/98)
Prescribed by ANSI Std. Z39.18