March 2005 • NREL/SR-520-37718

Subcontractor Report

High Efficiency Narrow Gap and Tandem Junction Devices

Final Technical Report
1 May 2002–31 October 2004

A. Madan
MVSystems, Inc.
Golden, Colorado

National Renewable Energy Laboratory
1617 Cole Boulevard, Golden, Colorado 80401-3393
303-275-3000 • www.nrel.gov

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1. Introduction

The work reported in this report uses a modified pulsed PECVD technique which has been successfully developed to fabricate state of the art nc-Si materials and devices. Specifically we have achieved the following specific benchmarks.

1. nc SiH device with an efficiency of 8% achieved at a deposition rate of ~1A/s.
2. nc SiH device with an efficiency of 7% achieved at a depostion rate of ~5A/s.
3. Large area technology developed using pulsed PECVD with uniformity of +/-5% over 25cm x 35cm.
4. Devices have been fabricated in the large area system (part of phase 3).
5. An innovative stable four terminal (4-T) tandem junction device of $\eta > 9$ % fabricated. (It should be noted that the 4-T device fabricated with existing technology base and with further development can reach stabilized η of 12%).
6. With improvement in Voc ~ 650 mV, from the current value of 480mV can lead to stable 4-T device with $\eta > 16\%$. Towards this objective, modified pulsed PECVD was developed where layer by layer modification of nc-SiH has been achieved. It should be noted that the due to budget cuts at NREL, this project was curtailed by about one year.)

2. Pulsed PECVD technique for the deposition of nano (or micro-)-crystalline Silicon (nc-Si).

Numerous techniques have been used to deposit nc-Si:H solar cells, such as PECVD [1,2], VHF-PECVD [3], gas Jet [4] and HWCVD [5]. All of these techniques have resulted in η of 7-9% and the so called "micro-morph" cell using the PECVD technique has resulted in an initial efficiency, $\eta \sim 13\%$ at a deposition rate (DR) of ~1 Å/s [6]; as the film thickness requirement in the device (for nc-Si:H) is in the range of 1-3 μm, this is then an impractical approach. Using a similar deposition approach and device configuration, Kaneka Co. has reported large area modules with a stabilized, η of ~10% [7]. Using the HWCVD technique, Klein *et al.* [5] have reported $\eta \sim 8\%$ stable device, but at a DR ~1 Å/s. Using VHF-PECVD technique, the DR has been increased to 5 Å/s with $\eta \sim 7\%$, in a single junction configuration. Using a conventional PECVD (high pressure and low substrate temperature) technique, $\eta > 9\%$ [1,2] has been achieved, but these process conditions are not conducive for production due to potential yield problems. The scale up with of VHF-PECVD is problematical [3] as would be expected for the Jet deposition technique also. Hence all of the techniques, so far studied, confront the low DR, dust formation, and/or the compatibility issue of large area deposition.

Of all the deposition techniques studied so far in the development of nc-Si:H materials and devices, pulsed PECVD technique offers a promising approach [8]. In this, the plasma is modulated in the range of 1 to 100 kHz and with an ON-time to OFF-time ratio of 10-50%. The time averaged plasma properties when so modulated also differ markedly from those generated using normal continuous wave (CW) excitation used in the PECVD approach. Because the discharge in the plasma is not in equilibrium, time modulation permits tuning of processing conditions, often for the better.

3. Some experimental aspects

We have used a proprietary modified Pulsed PECVD technique to deposit nc-Si:H absorber intrinsic layer. Two types of systems have been used, small area cluster tool system which is capable of depositing on to 10cm x10cm sized substrates and a large area cluster tool system which is capable of depositing on to 30 cm x40cm. (It should be noted that these types of systems are manufactured by MVSystems Inc., and at the time of writing, MVS had shipped and installed over 70 systems which are located in 18 countries.)

The devices discussed in "superstrate" type (glass/TCO/ZnO/nc-p/nc-i/a-n/Ag or glass/ZnO/nc-p/nc-i/a-n/Ag) configuration, while the doped layers (nc-p and a-n^+) were grown using the normal CW (fixed frequency of 13.56 MHz) technique. The structural studies were performed on actual p-i-n devices grown simultaneously on c-Si wafer using XRD (D. Willamson of Colorado School of Mines), FTIR and cross sectional TEM. The minority carrier diffusion length (L_d) was estimated, (V. Delal of Iowa State University) from a reverse bias quantum efficiency (QE) experiment after determining the depletion width from capacitance-voltage (C-V) measurements.

4. nc-Si materials developed in a small area cluster tool system- substrate size: 10cm x10cm.

4.1 Intrinsic layer: there are several factors which determine the opto-electronic properties of nc-Si:H such as the orientation and passivation of grains, oxygen concentration, voids, crystalline fraction etc. From a device point of view the critical factors is the minimization of the incubation layer, control of interfaces, effect of textured substrate, etc.

Fig. 1 shows the dark conductivity,σ_d, and DR as a function of deposition pressure while Fig. 2 shows the XRD spectra of p-i-n devices grown at a different deposition temperature, T_H, on c-Si wafers. nc-Si:H films consists mostly of (220) oriented grains with a size of ~ 15 – 18 nm and crystalline fraction of ~ 80%. However, the integrated intensity ratio [(220) to (111)] I_{220}/I_{111} varies with T_H. The high efficiency (~8%) films discussed below are

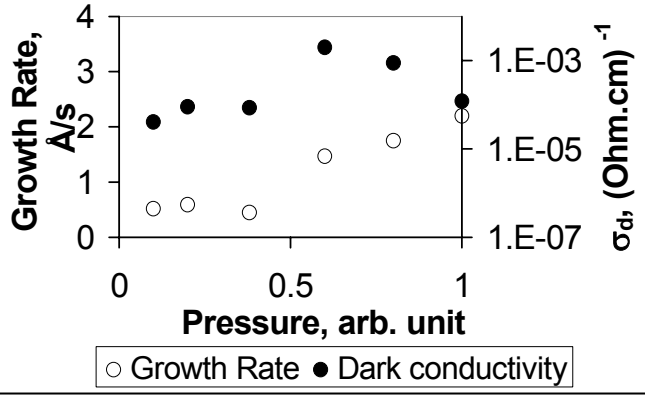


Figure 1: Deposition rate, dark conductivity vs. deposition pressure (arbitrary units) for nc-Si:H films. Typical thickness of films , ~0.5μm.

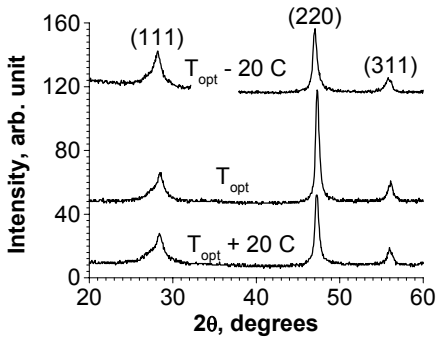


Figure 2: XRD spectra of p-i-n devices grown at different T_H.

(220) oriented with I_{220}/I_{111} ratio of ~2.0. It should be noted that there is general consensus that for solar cells, the preferred orientation is 220.

Fig.3 shows that from the FTIR spectra, no change in the hydrogen content (~7 at%) in the film with T_H was observed. The Si-O peak (~1090 cm^{-1}) intensity, however, increases with an increase of T_H, which implies an increase in the porosity of the film at higher T_H. There is a large body of evidence that the control of oxygen plays a crucial role in the transport properties of the material. For instance, oxygen is known to act as a donor (O^{3+}) in a-Si:H [9], i.e. O of about 10^{19} cm^{-3} increases σ_d to about 10^{-9} $(ohm\text{-}cm)^{-1}$ from its normal value of $\sim 10^{-10}$ $(ohm\text{-}cm)^{-1}$. Similar effects in nc-Si:H have also been noted in which the mobility of electrons (as determined by the Hall effect) remained constant at about 1 $cm^2/(V\text{-}s)^{-1}$ while the electron carrier density increased from 10^{13} to 10^{14} cm^{-3} (i.e an increase in σ_d) when the O concentration increased from 10^{18} cm^{-3} to 10^{19} cm^{-3} [10]. It was surmised that the O may segregate at the grain boundaries and hence the O^{3+} donors lead to an increase in the recombination at the surface, i.e. high surface recombination velocity. With the use of appropriate process conditions a passivation reaction,

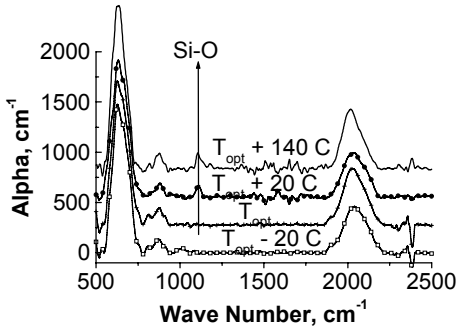


Figure 3: FTIR spectra of p-i-n devices grown at different T_H. The Y-scale is shifted for clarity.

such as $O\text{-}Si_3^+ + H \rightarrow Si\text{-}O\text{-}Si + Si\text{-}H$ can take place [11], which promotes passivation of bonds at the grain boundaries with the result that there is a minimization of recombination at the grain boundaries and an improvement in the properties of the material. Evidence for this also provided by the related work on fine grained (size ~0.25 μm) poly-Silicon thin film transistors (TFT's) [12]; in this, the ON/OFF characteristics, V_{th} (threshold voltage), field effect mobility are improved when the as-deposited TFT is subjected to H, O and H+O plasmas, with the latter exhibiting the best characteristics. For a gate voltage, $V_g > V_{th}$, the technique allows the investigation of transport of carriers above the conduction band and across the grain boundaries. Hence, the appropriate parameter to measure is the activation energy of such transport as any impediment to its flow will be reflected in its changes. It was shown that the activation energy (for $V_g\text{-}V_{th}$ = 10 volts) was the lowest (< 30 meV) for the O + H plasma treatment while in the as-deposited TFT, the activation energy > 140 meV. This study would lend support to the suggestion of the passivation reaction discussed above, leading to good passivation of the grain boundaries.

Dr. V. Delal of Iowa State University has measured L_d in an actual solar cell configuration made by us, using C-V technique at a frequency of 100 Hz. At such a frequency, all states in the intrinsic layer of the cell up to ~0.5 eV below the conduction band should respond to the capacitance signal. Fig. 4 shows the C-V curve and the slopes of the curves give values of 2.1×10^{15} cm^{-3} near the p layer, and 7.6×10^{15} cm^{-3} at a distance of 0.7 μm from the p layer. Knowing the depletion width from C-V measurements, L_d can be estimated from a reverse

bias quantum efficiency (QE); this involves deposition of ITO on the n^+ layer, and the measurement of QE from a 500 nm light beam at different bias. At this wavelength, as most of the photons are absorbed within < 0.1 μm, then the holes are generated essentially at the back surface of the intrinsic layer. By varying the bias voltage, the depletion width is changed, and therefore, the field-free distance that the hole diffuses before it is swept away by the depletion field also changes. By matching this curve with a simple exp ($-x/L_d$) relationship for carrier collection, where x is the thickness of the field free region, and he has estimated the diffusion length, L_d of ~1.2 μm.

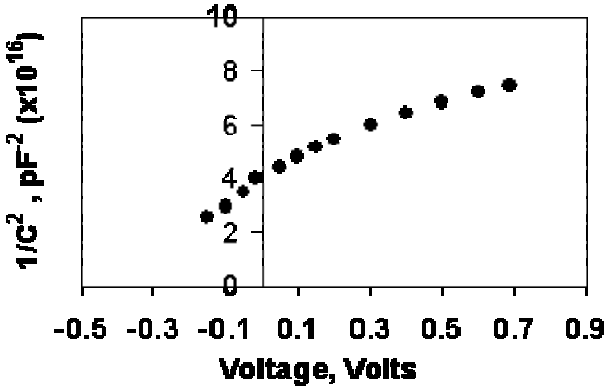


Figure 4: $1/C^2$ (estimated from C-V measurement) vs. applied reverse voltage for a typical pulsed PECVD grown device.

4.2 p- , p/i interface and incubation layer.

The p/i interface, in a superstrate-type (p-i-n) device, plays a crucial role in determining the device performance, as nc-Si:H often starts with an amorphous incubation phase, the extent of which sensitively varies with the film growth conditions. Fig. 5 shows $\sigma_d \sim 0.3$ $(ohm.cm)^{-1}$ (lateral conductivity) of nc-p layer (using tri-methyl boron (TMB) as a dopant gas) and that it increases by several orders of magnitude in the thickness range of 20 – 30 nm, suggesting the presence of amorphous incubation phase in the nc-p layer deposited on glass.

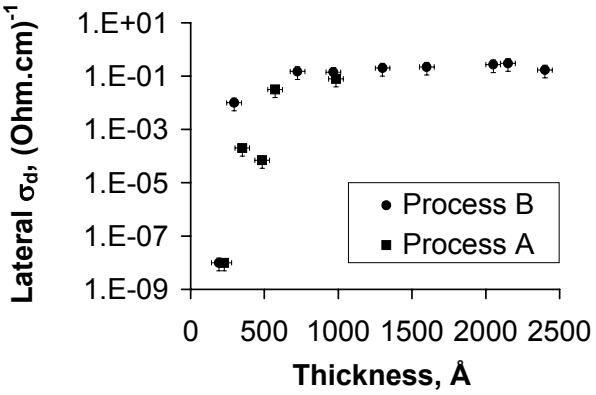


Figure 5: Variation of lateral dark conductivity uisng TMB as the dopant gas for different film thicknesses.

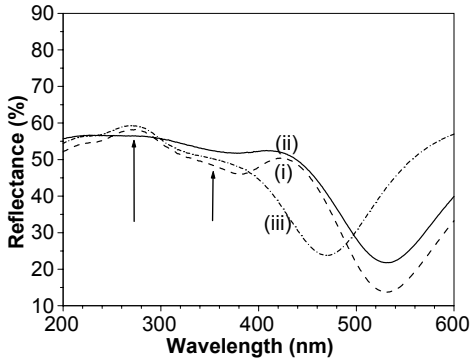


Figure 6: Reflectance spectra of (i) nc-p, (ii) nc-p/7 nm nc-i, (iii) nc-p/ST/7 nm nc-i. Two arrows indicate the location of shoulder in reflection due to crystallinity.

Apart from the p/i interface defects and boron in-diffusion in the overlying i-layer, a careful examination of the film structure at the p/i interface is necessary for producing high efficiency nc-Si:H p-i-n devices. To gain an insight into the structure of the film at p/i interface (initial growth of nc-i layer on fully nucleated nc-p), we studied the reflectance spectra at UV region (surface sensitive). An additional reflection (at 365 nm and 275 nm) appears due to the presence of any crystalline phase in the film (please see the reflectance spectra for a-Si:H and nc-Si:H in Fig. 6). Such an additional reflectance in nc-Si:H films arises due to the specific values of pseudo dielectric constant of crystalline Si, which is often studied by ellipsometric measurements. The reflectance spectra for (i) nc-p layer, (ii) 7 nm nc-i layer on top of nc-p, (iii) 1 min of ST (involving a Hydrogen plasma treatment) and the fabrication using a *modified* pulsed PECVD for nc-p followed by 7 nm nc-i layer are compared in Fig. 6. The curve (i) in Fig. 6 clearly shows the shoulders in reflectance spectra at 365 nm and 275 nm indicative of good crystallinity in nc-p layer (well nucleated). However, 7 nm nc-i layer directly grown on nc-p appears amorphous [curve (ii)]. Even 1 min of ST of nc-p layer using *modified* pulsed PECVD results in a significant increase in the crystallinity of the overlying nc-i layer [curve (iii)]. Either or both of the following reasons would result in such an initial nucleation of the nc-i after ST; (a) The treatment procedure modifies the nc-p surface resulting a high-density of nucleation sites for subsequent nc-i growth, (b) removal of surface oxygen, which may form during inter-chamber (dope-to-intrinsic) transfer, on nc-p film by ST leading to a better nucleation of nc-i.

Fig. 7 shows the illuminated J-V characteristics of nc-Si:H p-i-n devices with and without ST performed on the nc-p layer. As shown, without the ST process, the device is very poor with a low fill factor (0.47). However, FF (0.66) improves dramatically for the device when ST is performed and is primarily due to the reduction or elimination of the amorphous incubation layer at the p/i interface, as revealed from the UV reflectance spectra shown in Fig. 6.

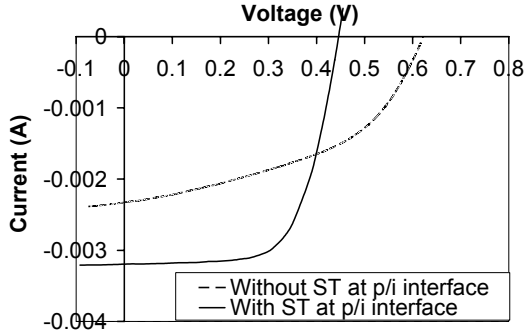


Figure 7: Illuminated I-V curves for nanocrystalline Si p-i-n devices with and without surface treatment at p/i interface.

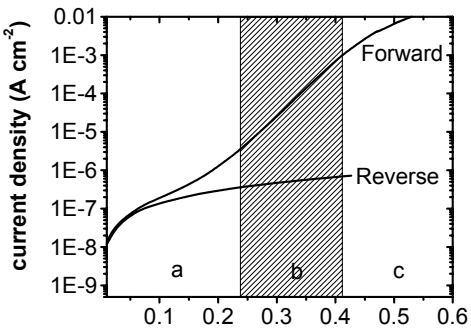


Figure 8: Typical dark J-V characterictics for nanocrystalline p-i-n device. The diode quality factor (n) and dark saturation current density (J_0) was estimated from the shaded region (b) in forward voltage.

Fig. 8 exhibits a typical dark J-V characteristics of a nc-Si:H device with ST using *modified* pulsed PECVD method at the p/i interface. The diode quality factor (*n*) and the dark saturation current density (J_0) were estimated from the shaded region (region "b") of forward voltage in Fig. 8. The dark current density (J_{dark}) under forward voltage (*V*) is given by,

$$J_{dark} = J_0\left[\exp\left(\frac{eV}{nkT}\right) - 1\right] \qquad (1)$$

where, *e*, *k*, and *T* are the electronic charge, Boltzmann constant and temperature respectively. Fig. 9 shows the variation of n and J_0 as a function of i-layer thickness of nc-Si:H p-i-n devices grown on three different substrates, namely Asahi "U"-type TCO (coated with 30 nm ZnO to protect SnO_2 from H_2 plasma), AIST ZnO (textured ZnO supplied by

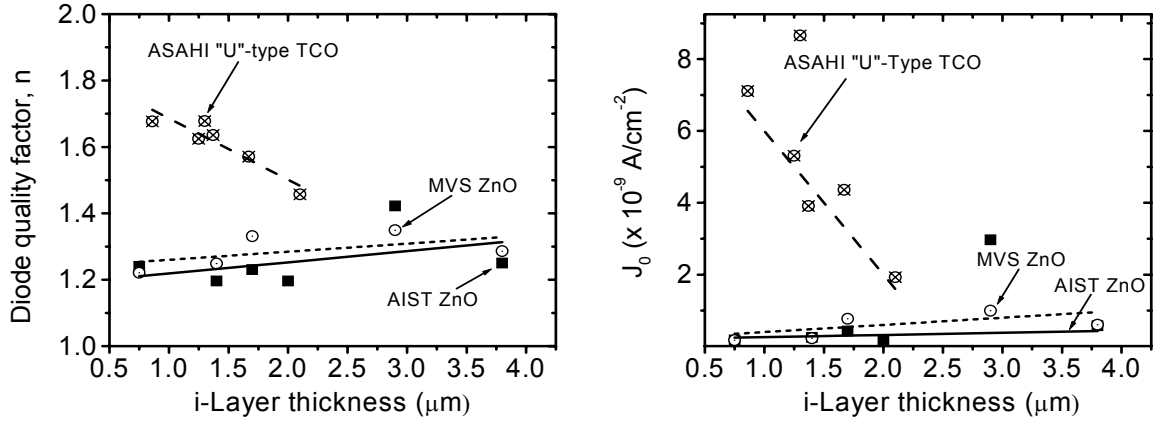


Figure 9: Variation of diode quality factor (*n*) and dark saturation current density (J_0) as a function of i-layer thickness for nc-Si:H p-i-n solar cells deposited on three different substrate (20 nm ZnO coated Asahi "U"-type TCO, AIST supplied textured ZnO and MVS developed textured ZnO).

AIST, Japan), that the values of *n* and J_0 for the devices grown on Asahi "U"-type TCO decreases as the device thickness increase from 0.7 μm up to ~4 μm. It has been noted that a decrease of n for the thicker i-layer is indicative of lower recombination in the bulk and that nc-Si:H material properties improves with thickness [8,13]. Also, as discussed below (see Fig. 14), the cross sectional TEM data reveals that the texture of Asahi "U"-type TCO is not optimal for nc-Si:H film growth as it leads to grain collision and hence a void rich and defective region results in the vicinity of the collision area. However, the "AIST ZnO" and "MVS ZnO" with a different texture leads to a decrease in grain collisions leading to a larger current density from a similar device produced on "Asahi TCO". Fig. 9 shows an insignificant variation of n and J_0 with device thickness from 0.7 μm to 3.8 μm for the device grown on "suitably textured" ZnO substrates. The rather insignificant change in n suggests that the dark J-V characteristics are not dominated by bulk recombination.

It should be noted that a large variation of n values (from 1.2 to 1.8) has been observed with ST, as function of time, performed at the p/i interface. Fig. 10 shows the variation of open circuit voltage (V_{oc}) and *n* as a function of ST time at p/i interface. The device without any ST at the p/i interface shows a high V_{oc} (>600 mV) and a high n value of 1.8. Such a high Voc may arise due to the fact that the nc-i layer initially grows with an amorphous incubation layer (which is evident from the UV reflectance spectra as shown in Fig.6) and the subsequent i-layer with a lower crystalline fraction. The large value of n indicates a defective i-layer quality and/or a

defective p/i interface. It should be noted that even with a short (30 s) ST process at the p/i interface, leads to an improvement in the light and dark device characteristics and n reduces from 1.8 to 1.3 which remains almost constant up to the ST time of ~ 5 mins. For a longer ST time (6 mins), V_{oc} drops sharply and n increases significantly, which essentially suggests that the underlying nc-p layer may have become damaged. To gain

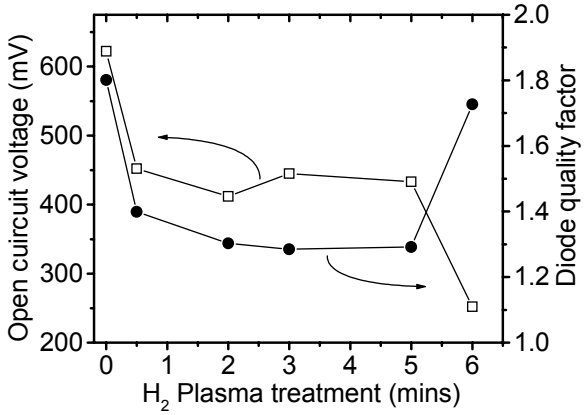


Figure 10: Variation of open circuit voltage (V_{oc}) and the diode quality factor (*n*) as a function of surface treatment time at p/i interface for the nc-Si:H p-i-n solar cells deposited on to MVS developed textured ZnO.

a better insight into what may be the cause, we have also studied optical emission spectroscopy (OES) during the nc-i layer growth. Fig. 11 shows the ratio (SiH_4^*/H^*) of 414.2 nm emission peak (due to SiH_4^*) to 656 nm emission peak (due to H^*) as a fucntion of deposition time. OES study shows that at the beginning of the nc-i layer (t=0) deposition without ST, the SiH_4^*/H^* ratio starts with a high value of 1 and tends to stabilize at a value of ~ 0.7 over the deposition time of ~ 250 s. On the contrary, with ST perfomed at the p/i

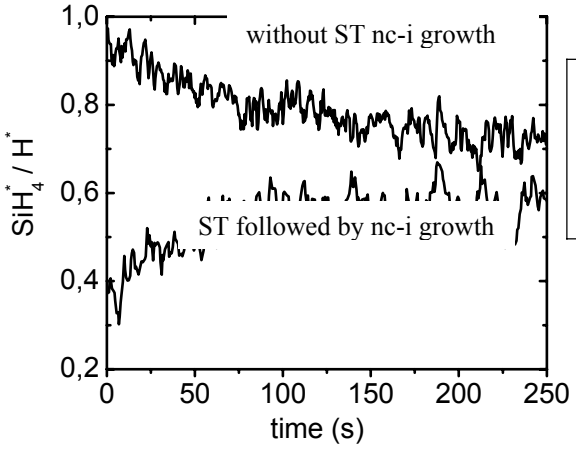


Figure 11: Ratio (SiH_4^*/H^*) of 414.2 nm emission peak (due to SiH_4^*) to 656 nm emission peak (due to H^*) observed by OES as a function of deposition time.

interface, the SiH_4^*/H^* ratio starts with a lower value of 0.4 and stabilizes to ~ 0.6, in ~ 250 s. It would therefore appear that there is a basic difference in the plasma conditions and hence the type of radicals and growth precursors within the first 250s of nc-i layer growth. Initial high value of SiH_4^*/H^* without ST leads to the growth of a-Si:H layer at the p/i interface, which corroborates the UV reflectance measurement (Fig.6) and the device performances with and without ST (Fig.7).

4.3 Nano-crystalline Silicon: single junction solar cells

4.3.1: devices fabricated on Asahi SnO2 substrate: using "Asahi U-type TCO" substrate Fig. 12 shows the nc-Si:H p-i-n device performances (V_{oc}, J_{sc}, FF and efficiency), under AM1.5 illumination, as a function of deviation from optimum heater temperature (T_{opt}) of nc-i layer growth. V_{oc} and FF exhibit an optimum at a particular value of T_H. In this series of experiments, we had achieved $\eta \sim 7.5\%$ (FF of 0.69) with an i-layer thickness of ~ 1.4 μm using and a simple Ag back reflector. Fig. 14, shows a TEM for one of these devices. It should be noted that "Asahi U-type TCO" substrate has been optimized for a-Si:H devices and is not appropriate for use in nc-SiH type devices as the grains tends to grow perpendicularly to the substrate leading to collisions as shown (indicated by two arrows) with the neighboring grains [14].

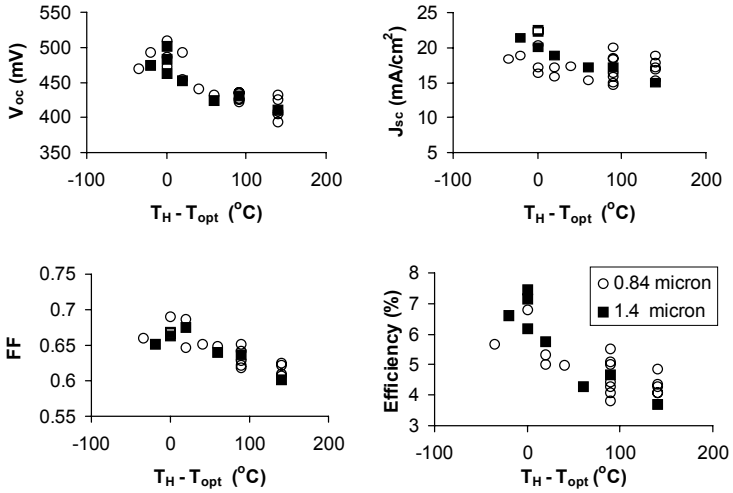


Figure 12: Variation of open circuit voltage (V_{oc}), short circuit current (J_{sc}), fill factor (FF) and efficiency as a deviation from optimum heater temperature (T_{opt} - T_H) during nc-Si:H i-layer growth.

4.3.2: devices fabricated on textured ZnO substrate: by substituting "Asahi U-type TCO" substrate with texutured ZnO and using the configuration, glass/etched ZnO/nc-p type/nc-Si:H- i-layer/amorphous-n^+/ZnO/Ag, with nc-SiH layer of 1.5μm in thickness, we have improved the devices and have obtained, $\eta \sim 8\%$ (V_{oc} of 0.48V, FF of 0.7, J_{sc} ~ 24 mA/cm^{-2}), as shown in Fig. 13 [8,15]. It should be noted that there are several key issues: (a) as shown in the TEM photographs in Fig. 14(a) and noted above, the deposition of nc-SiH devices on "Asahi SnO_2:F coated glass" leads to grain collisions within the bulk which would increase recombination losses; this is further corroborated by the results of Fig 9(c) where we show that such devices exhibited a large diode quality factor, > 1.6. By replacing the "Asahi substrate" with a textured ZnO, the grain collisions were avoided (Fig. 14(b)) and the devices now exhibit a lower diode quality factor of <1.3 (see Fig. 9(c)) even when the device is of 3.8μm in thickness: (d) use of a double reflector layer (ZnO/Ag), leading to an increased reflection at the red end of the spectrum.

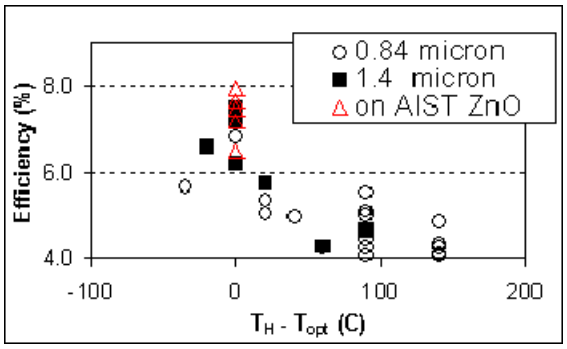


Figure 13: variation of the conversion efficiency of a nc-Si:H constructed in a pin configuration as a deviation from optimum heater temperature (T_{opt} - T_H) during the nc-Si:H i-layer growth. T_H ~170C.

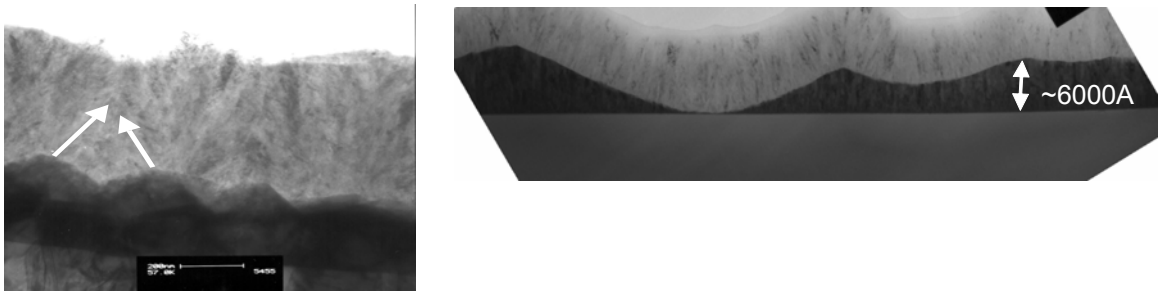


Figure 14; TEM photographs of ncSiH pin grown on (a) Asahi SnO_2:F (left) and (b) textured ZnO (above) substrates.

4.4 High deposition rate nc-SiH devices and comparison of nc-Si H device η measured at NREL, MVS solar simulator and outdoor

In Table I, we compare the performance of devices measured at NREL, at MVS using its Xe lamp solar simulator and under outdoor tests. The data can be summarized as follows.

(i) There is close correlation (+/- few %) between the outdoor tests (on sunny days and corrected for100mW/cm^2 intensity) and those measured by NREL. The highest η as measured in the outdoor test was 7.95%.

(ii) Device with η ~7% has been obtained at a deposition rate (DR) of ~5A/s using the pulsed PECVD technique.

(iii) There is a significant discrepancy for device #1124 and #1126. NREL elected to use rubberized contacts in order to prevent damage to the devices which led to a contact resistance and a lower FF than measured by MVS who used gold tipped probes.

(iv) The MVS solar simulator (Xe lamp) consistently underestimates η in comparison with NREL measurement; this is because the solar simulator has been designed [1] (with filtering) for a-

[1] MVSystems Inc. manufactures solar simulators which are specifically designed for the amorphous silicon market. Prior to delivery of these systems to customers, NREL have in the past calibrated the units and the accuracy of the simulator is within+/-7%- in comparison with the global AM1.5 spectrum -see www.mvsystems.info

Si:H devices where the spectrum over the range (400nm-700nm) is relevant while nc-SiH devices respond over a wider range 400-900nm.

Table I

	I-layer	Dep.	Type of	MVS Xe solar simulatior				NREL J-V test				Outdoor test		
	Thick	rate	substrate	Voc	Jsc (mA/	FF	Eff. (%)	Voc	Jsc (mA/	FF	Eff. (%)	Voc	Jsc (mA/	Eff. (%)
Device #	(um)	(A/s)		(mV)	cm2)			(mV)	cm2)			(mV)	cm2)	indoor FF
NRCT 525	0.9	~1	Asahi TCO	432	12.65	0.622	3.4	**468**	**15.88**	**0.65**	**4.8**	-	-	
NRCT 916	0.72	~1	Asahi TCO	493	12.602	0.687	4.27	**514**	**14**	**0.65**	**4.69**	498	14.9	5.10
NRCT 919	1.2	~1	Asahi TCO	452	15.04	0.675	4.6	**487**	**18.27**	**0.65**	**5.82**	467	18	5.67
NRCT 922	1.7	~1	Asahi TCO	466	15.89	0.674	4.98	**487**	**19.226**	**0.65**	**6.06**	475	18.9	6.05
NRCT 950	1.4	~1	Asahi TCO	501	17.987	0.663	5.98	**519**	**19.323**	**0.64**	**6.38**	506	19.4	6.51
NRCT 959	2.1	~1	Asahi TCO	481	18.52	0.665	5.92	**502**	**20.997**	**0.65**	**6.81**	486	20.5	6.63
NRCT 1077	1.4	~1	AIST ZnO	473	18.1	0.627	5.36					490	22.9	7.04
NRCT 1078	1.4	~1	AIST ZnO	440	18.2	0.69	5.48					480	24	7.95
NRCT 1124	1.7	~1	AIST ZnO	466	15.861	0.668	4.93	**490**	**21.275**	**0.53**	**5.52**	500	22.9	7.65
NRCT 1126	1.7	~1	AIST ZnO	465	16.06	0.667	4.98	**485**	**21.123**	**0.54**	**5.57**	490	22.8	7.45
NRCT 1133	1.7	~1	MVS-ZnO	474	17.392	0.649	5.35					490	23.4	7.44
NRCT 1135	1.7	~1	Asahi TCO	0.457	14.43	0.669	4.42					482	21.94	7.07
NRCT 1135	1.7	~1	MVS-ZnO	0.453	16.005	0.672	4.87					468	23.2	7.30
NRCT1172	1.4	~5	MVS-ZnO	0.469	14.814	0.669	4.64					484	21.8	7.06
NRCT1201	1.5	~5	AIST ZnO	0.427	14.113	0.683	4.11	**0.448**	**18.519**	**0.67**	**5.53**	460	19.6	6.16

5. Nano-crystalline Si materials and devices using a large area (substrate size: 30cm x 40cm) cluster tool.

We have extended the above work to large area deposition of nc-Si:H layers ametarils and devices which were deposited in a commercially available PECVD cluster tool system (capable of handling substrate of size 30cm X 40cm) specifically designed for the thin film semiconductor market and manufactured by MVSystems, Inc. and shown in Fig. 15 [16]. The pulsing (between 1-100 kHz) was superimposed onto a 13.56 MHz signal applied to the RF plate. The process conditions for nc-Si:H depositions were, RF power, 40-300 Watts, a flow rate of silane gas, 2-50 sccm, hydrogen dilution of 90-99%, deposition pressure, 200-9000 mTorr and the heater temperature (T_H) during film growth, 100 °C-450 °C.

Using the PECVD technique, nc-p type materials with a uniformity of ~ +/- 5% over the area 25cm x 35cm have been obtained. Fig. 16 shows the dark conductivity of nc-p type layer as function of thickness which compares well with that the results obtained from a small area cluster tool (substrate size; 10cm X 10cm) shown in Fig. 5. We have also developed, using the pulsed PECVD technique, uniform films of nc-Si:H type materials, with a uniformity which is also similar to that attained for nc-p player (i.e. ~ +/- 5% over the area 25cm x 35cm). Fig. 17 shows a study, of nc-Si:H films properties when the SiH_4 gas flow rate (diluted in H_2) is altered during the deposition; we plot dark conductivity, crystalline

Figure 15: large area sluter tool with multiple PECVD and sputtering chambers. Substrate size: 30cmx40cm.

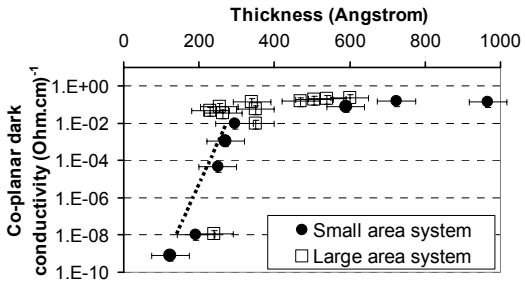


Figure 16: Variation of lateral dark conductivity using Boron as the dopant for different film thicknesses.

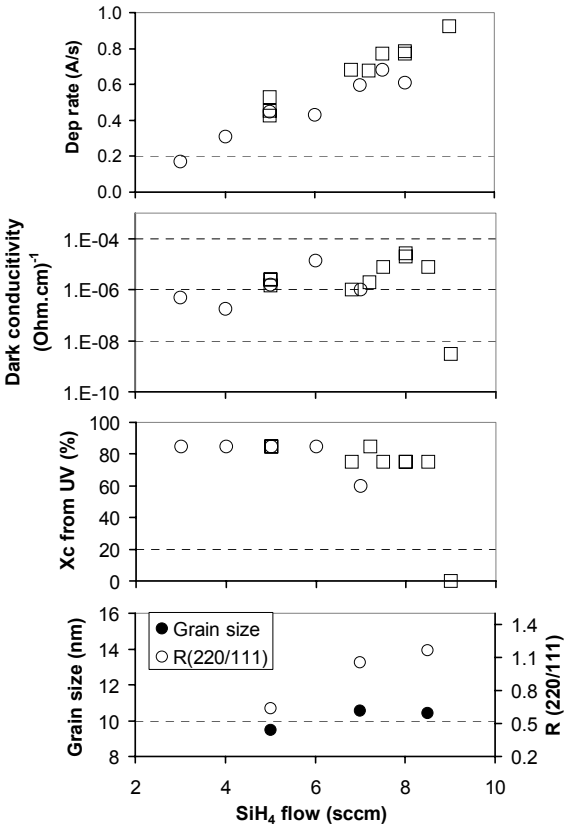


Figure 17: Deposition rate, dark conductivity, crystalline fraction (Xc), grain size, ratio of (220)/(111) as a function of SiH_4 flow rate during deposition.

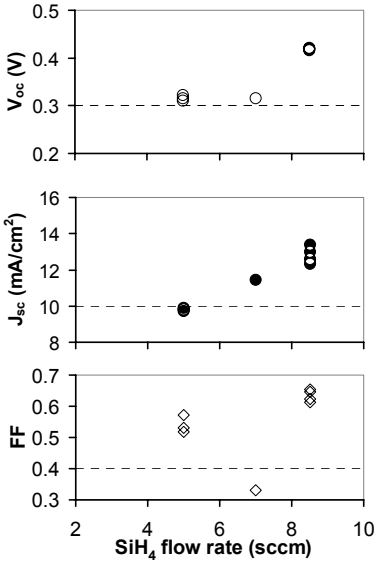


Figure 18: Open circuit voltage, short circuit current density, fill factor of devices (area, 0.25 cm^2) as a function of SiH4 gas flow rate during deposition.

fraction, grain size and orientation (as determined from XRD) and to effectively calibrate the system and compare the properties with that of the small area system, discussed above. We note that as the SiH_4 flow rate increases to beyond about 8.5sccm during the deposition, a transition occurs to an amorphous silicon phase; interestingly, prior to this transition, the films become increasingly (220) orientated.

As discussed above, one of the prerequisites for obtaining a good device is the crystallinity at the p/i interface and the elimination of the incubation layer. Table II, shows the crystalline fraction as a function of position over the large area substrate; the positions designated as 1, 2 and 3 are samples situated equidistant along the diagonal of large area substrate of 30cm x 40cm. It should be noted that the results of crystalline fraction are similar to the ones obtained from the small area system.

Position #	1	2	3
Thickness (A)	610	570	550
Xc (%)	60	60	60

Table II nc-p/nc-i interface study of samples situated along the diagonal of large area substrate of 30cm x40cm. Positions 1, 2 and 3 represent equidistant locations along the diagonal. The intrinsic layer of thickness in the range of 80-100 A^o was used.

Fig. 18 shows a series of solar cells fabricated on Asahi SnO_2/ZnO coated glass with the structure of the devices constructed as nc-p/nc-i layer/a –n+ with nc-Si:H of thickness < 1μm and the improvement in the solar cell device performance that results, as the nc-Si:H process conditions are made to approach the transition region. Fig 19 shows the diode quality factor, n, and compares that with the n obtained form the small are a cluster tool and shows s milir trend as discussed above.

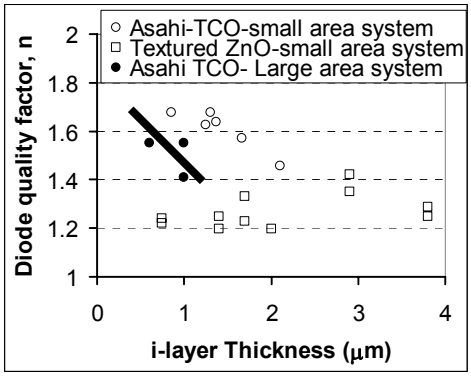


Figure 19: Diode quality factor as a function of nc-Si:H i- layer thickness for devices produced in, (a) small area cluster tool system using Asahi SnO_2 textured glass and textured ZnO and (b) large area cluster tool system using Asahi SnO_2 coated glass.

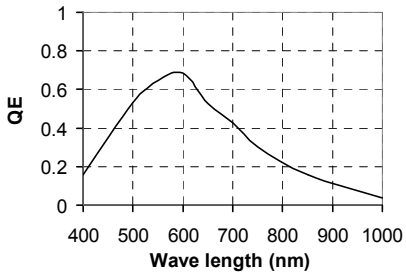


Figure 20: Quantum efficiency of a solar cell constructed just prior to the transition to amorphous silicon phase.

In order to improve the device performance to η~8%, as obtained in the small area cluster tool system discussed above, there are various improvements required. For instance, the QE (quantum efficiency) of the device, shown in Fig. 20 and from a series of runs of Fig. 18, reveals that there is a large loss at the blue end of the spectra and is of course recognized that this is due to the very thick layers of nc-p used. By further optimization and in devices fabricated on " MVS textured ZnO", we show QE of a recent device in Fig. 21 which exhibits Jsc of 19.91 mA/cm^2. Apart from the optimization of nc-p layers in devices, the material property of the i-layer will need to be optimized with respect to flow rates, pressure during deposition, power, modulation frequency and anode - cathode distance. The devices would also require the utilization of the back reflectors, such as ZnO/Ag, and the use of thicker devices (>1.5μm). It was these procedure that had led to η~8% devices in the small area system. On its accomplishment, we shall then proceed to the task of increasing the deposition rate >5-10A/s as already accomplished in the small area system.

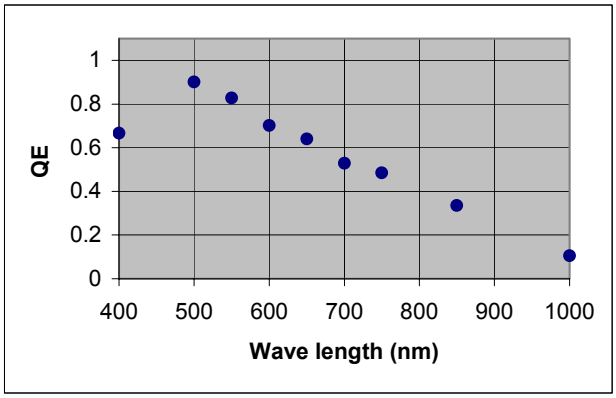


Figure 21: Quantum efficiency of a solar cell constructed on " MVS textured ZnO".

6. Tandem junctions, "micro-morph solar cells" and stable 4 terminal devices.

Light induced degradation remains an impediment for large scale deployment of amorphous Silicon (a-Si:H) based solar panels. The degradation is strongly dependant on the thickness of the device used and can be circumvented to a certain extant by the use of multi-junction (MJ) at the expense of complexity in fabrication. MJ type devices use several cells stacked on top of each other with differing band gaps (and thickness) to absorb a wider portion of the solar spectrum (e.g. a-SiH/a-SiGeH/a-SiGeH) [17]. As this two terminal (2-T) MJ device structure requires the same current from each constituent cell, it necessitates the use of relatively thick a-SiH junctions (~2000 Å) and the device generally degrades by ~20%. Further, the fabrication of a-SiGe:H requires GeH_4 gas **which is prohibitively expensive** and since the gas utilization during production is normally <10%, **the cost reduction of such PV panels may be difficult to realize.** Hence the use of 2-T MJ solar cell with *stable* micro-(or rather nano-) crystalline Si (nc-SiH) as the bottom cell and a-Si:H as the top cell is attracting attention (termed as "micro-morph") [18]. Such MJ (or tandem) solar cells can produce an initial η of ~14.5% in a small area (3 cm^2) and ~12% in large area modules. However, this structure also contains a thick (~4000A) a-Si:H junction (due to the current matching) and as a result majority of the

power (~ 70%) emanates from the unstable thick a-Si:H portion with an inevitable degradation under light.

We have developed [15,19] a simpler 4 terminal (4-T) thin film Si based MJ solar cell configuration in which the current matching constraint is released from each constituent cell, e.g. two cells (a-SiH and *stable* low band gap material, such as nc-SiH)) are separated via an insulator. This allows the use of ultra-thin (<1000A) a-Si:H solar cell where instability is no longer an issue. This *stable solar 4-T MJ design*, has the potential to attain η >16%.

6.1 4-T thin film Si stable solar cells - background.

To circumvent the instability problems in a 2-T MJ device structure, we propose a much simpler 4 terminal (4-T) thin film silicon based MJ solar cell configuration, as shown in Fig. 22, in which the current matching constraint is released from each constituent cell. For example, two cells (a-Si:H and stable low band gap nc-Si:H cells) are separated via an insulating material (e.g. glass, plastic or SiNx).

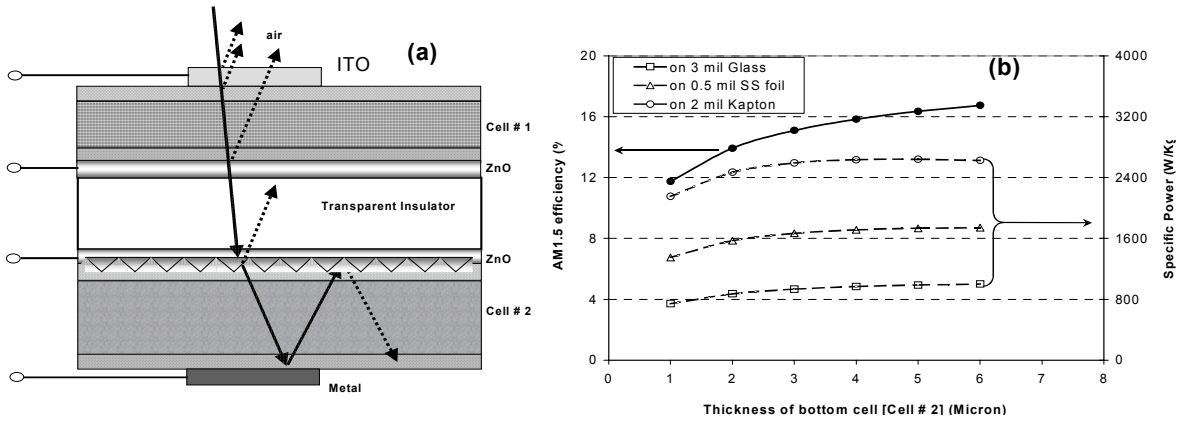


Figure 22. (a) schematic representation of a 4-T solar cell. Cell #1 is constructed as ultra thin a-SiH (<1000A) and cell #2 is constructed from nc-Si:H material. (b) estimated (under Global AM1.5) efficiency and the specific power using three different substrates as a function of bottom cell (cell # 2-nc-Si:H) thickness. The band gap of top cell was assumed to be 1.9 eV.

device can be made thin enough (<1000 Å) to eliminate the degradation; importantly, and in contrast to the 2-T "micro-morph" cell structure, most of the power is now generated from the stable (nc-Si:H) bottom cell. In this it is assumed that the open circuit voltage of the nc-Si:H device can be improved to >650mV which is the voltage normally obtained in large grain multi-crystalline Silicon [24].

6.2 Ultra thin a-Si solar cells and their stability; ultra thin (<1000A) a-Si:H solar cell device, under illumination, should not exhibit instability. It is known that the depletion width of a pin junction using a-Si:H is about 3000A [20]. Further, the density of defect states within the a-S:H layer increases (with illumination) by about an order of magnitude and saturates to about 10^{17}

cm^{-3} [21]. As L_d is small (<0.2μm) [22], it is the charge separation of the photo generated electron- hole pairs from within the depletion width which contributes to the majority of the J_{sc}. Hence to a first order approximation, after the defects have reached a saturation level, the depletion width would shrink to about 1/3 of its original value and should remain larger than the thickness of the device, which in this case would be <1000A; the device would remain fully depleted with the consequence no degradation would be apparent. Fig.8 shows the stability data of the a-Si:H cell of about 900A in thickness with Al and Ag as the back contact. Al contacted device reveals that, at least in the first 50 hours of illumination, the device remains stable. The figure also shows the quantum efficiency (QE) remains the same before and after 50hour of illumination. It should be noted that within this time frame, thicker a-SiH devices which are normally used in a 2-T MJ solar cell configuration usually degrade by about 10 % and eventually saturate with a power which is about 15-25% lower from its initial value [23]. Fig.24 shows the stability data of the a-Si:H cell of about 900A in thickness with Al and Ag as the back contact. Al contacted device reveals that, at least in the first 50 hours of illumination, the device remains stable. The figure also shows the quantum efficiency (QE) remains the same before and after 50hour of illumination. It should be noted that within this time frame, thicker a-SiH devices which are normally used in a 2-T MJ solar cell configuration usually degrade by about 10 % and eventually saturate with a power which is about 15-25% lower from its initial value [23].

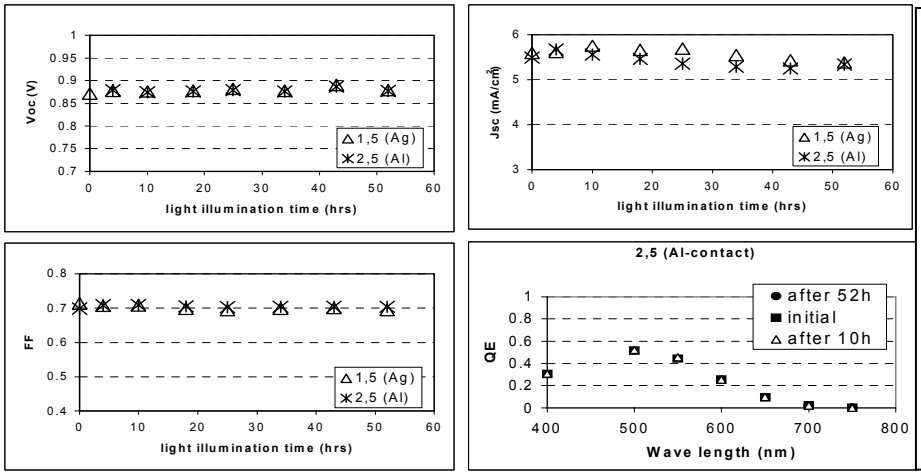


Figure 23: variation of FF, J_{sc}, V_{oc} and the quantum efficiency (Al contact) of 900A thick a-Si:H as a function of illumination (intensity-100mW/cm^2) time (hours).

6.3 a-SiH & nc-SiH cells constructed in a 4-T structure.

As a first step to examine the feasibility of the 4-T approach [15], we have merely joined together two separate devices a-Si:H (cell #1) and nc-Si:H (cell #2) constructed on glass substrate and obtained η >9% as shown in Table III. It should be noted that in comparison with the 4-T structure, shown in Fig. 1, this structure has many losses. (i) There are additional reflection losses which arise from the two additional air/glass interfaces; these losses would be absent in a real 4-T device of Fig. 1. (ii) Cell #2 did not possess a ZnO/Ag as the back reflector but only Ag, which usually provides an enhancement of the current at the red end of the spectra. (iii) a-Si:H (cell #1) was completed with ITO contact, and the FF is considerably lower than a corresponding device finished with evaporated Ag contact which exhibits 0.75. With further optimization of the ITO process (including improving its transmission at the blue end of the spectra), we expect to achieve a similar FF of 0.75 and an improved current from this portion of

the 4-T device structure. (iv) We have used soda lime glass as the substrate which absorbs > 10% of the light in the range of 600-1000 nm. As shown in Fig. 22, to increase the overall efficiency of the 4-T junction, it is necessary that the band gap of the cell #1 be increased to allow more of the light to enter cell #2. By changing the H_2 dilution in i-layer fabrication, we have increased the band gap of the i-layer to ~1.9eV leading to single

		Vo (volts)	Js mA/cm2	FF	Efficiency %
Amorphous Silicon	cell #1	0.836	8.4	0.702	4.93
Nano- crystalline Silicon	cell#2	0.445	14.99	0.63	4.20
Total 4-T					**9.13**

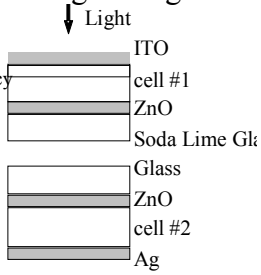
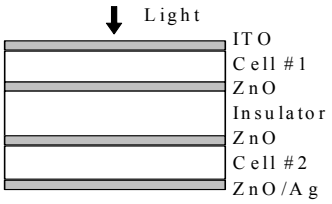


Table III. V_{oc}, J_{sc}, FF and efficiency of cell # 1 (amorphous Si) and cell #2 (nano-crystalline Si) are given together with a total conversion efficiency of the 4-T solar cell structure

junction solar cell with V_{oc} to 0.93 V, FF~0.75 and J_{sc} ~7 mA/cm^2 (device thickness ~900 Å). With further optimization, it is realistic to expect that V_{oc} ~1V , FF~0.75 and J_{sc} of ~8 mA/cm^2 with the result that cell #1 of the stack should yield stable cells with $\eta \sim 6\%$. With the inclusion of ZnO/Ag back reflector in cell #2, there would be an increased response at the red end of the spectra and it should be possible to achieve J_{sc} ~ 20mA/cm^2 from cell #2, with V_{oc} ~0.45-0.47 and FF ~0.7.

In an integrated 4-T MJ structure, it is possible to attain η>12% as shown in Table IV and it should be mentioned that there are no insurmountable barriers but requires, as discussed below, optimization of several layers and careful consideration of light management. With an improvement in Voc to beyond 650mV and use of antireflection coatings, stable device efficiency > 16% are possible.

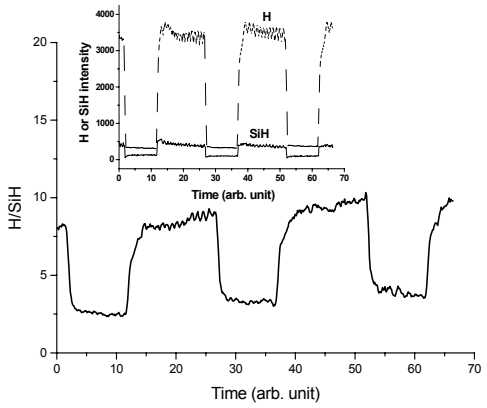
Table IV		Voc (volts)	Jsc mA/cm^2	FF	Efficiency %
Amorphous Silicon	cell #1	1	8	0.75	6.00
Nano- crystalline Silicon	cell#2	0.45	20	0.7	6.30
Total 4-T efficiency					**12.30**



7. Modification of the pulsed PECVD technique to improve the nc-SiH material: currently, stable nc-SiH devices are fabricated with V_{oc} ~500mV; devices which exhibit Voc>500mV are generally unstable. It should be noted that V_{oc} > 650mV can be routinely obtained in multi-crystalline Si solar cells [24]. Further it should be recognized that in fine grained (size of ~2500A) poly-Si with passivation techniques (discussed below) lead to a high performance TFT (thin film transistor) with large field effect mobility's of carriers >40 cm^2/s^{-1}V^{-1} [25]. In contrast, when a TFT is made with nc-SiH materials, the mobility's of carriers are significantly lower, ~1 cm^2/s^{-1}V^{-1} [26]. As may be expected, the small grain size (~200A) in nc-Si:H and their passivation would in turn dictate the transport of carriers and hence affect the solar cell performance.

We have modified the pulsed PECVD technique further such that, it can alter the film growth in a rapid way, (via deposition/etching cycles) to control the structure and the elimination of weak bonds [15]. In this technique, hydrogen, halogens or argon can be used as a diluent gas

with the source gas SiH_4. Atomic hydrogen and or halogens during the film growth act to modify the film properties over a wide processing range (e.g deposition pressure, flow rates etc.); the etching effect acts to reduce the defect density in a-Si:H films and change the film structure from completely amorphous to nano-crystallites embedded in amorphous matrix. The optical emission spectroscopy (OES) studies of the modified pulsed PECVD technique (Fig. 24) show that the concentration of atomic hydrogen in the plasma can be modulated very rapidly (microsecond level) during the film growth, which enables a modification of the growing film surface in an layer-by layer fashion. Figure 25 shows the x-ray diffraction pattern of two nc-Si:H films deposited by this technique for two different plasma conditions. The figure clearly shows predominantly two different crystal orientation (one with (111) orientation and the other is (220) orientation) in the films. The ability to alter the growth in layer by layer fashion should have an impact in the improvement of solar cell and specifically in Voc. To improve Voc beyond 650mV, as obtained in multicrystalline solar cells, it will be necessary to understand the limitation to the grain size, their passivation which in turn dictate the transport process.



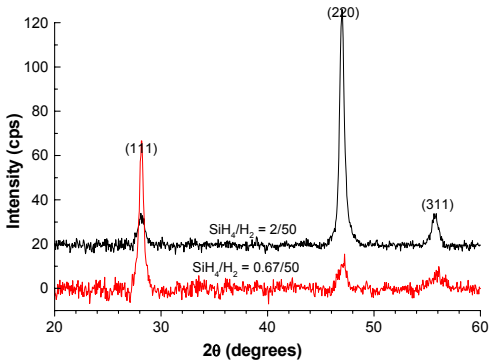


Figure 24. Variation of H* and SiH_4* intensities and their ratio as observed by optical emission spectroscopy in a modified pulsed PECVD technique.

Figure 25: X-ray diffraction pattern of nc-Si:H films deposited using modified pulsed PECVD technique at two different plasma conditions.

Acknowledgements: the following personnel, other than the PI, have worked on these projects, U. Das, Jian Hu, S. Morrison, R. Curry, G. Jones, E. Valentich, D. Zhong, Huon Dong. We are grateful to the collaborations with many team members, including C. Taylor (Utah), Eli Sutter and Don Willamson (both of Colorado School of Mines), V. Delal (Iowa Sate) who provided valuable data on samples supplied by MVS- specifically TEM, XRD, ESR and minority carrier diffusion length measurements mentioned in Sections 2.2.1- 2.2.3

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REPORT DOCUMENTATION PAGE

Form Approved
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1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
March 2005	Subcontractor Report	1 May 2002–31 October 2004

4. TITLE AND SUBTITLE
High Efficiency Narrow Gap and Tandem Junction Devices: Final Technical Report, 1 May 2002–31 October 2004

5a. CONTRACT NUMBER
DE-AC36-99-GO10337

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
A. Madan

5d. PROJECT NUMBER
NREL/SR-520-37718

5e. TASK NUMBER
PVB55101

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
MVSystems, Inc.
17301 W. Colfax #305
Golden, CO 80401

8. PERFORMING ORGANIZATION REPORT NUMBER
ZDJ-2-30630-31

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSOR/MONITOR'S ACRONYM(S)
NREL

11. SPONSORING/MONITORING AGENCY REPORT NUMBER
NREL/SR-520-37718

12. DISTRIBUTION AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

13. SUPPLEMENTARY NOTES
NREL Technical Monitors: Bolko von Roedern

14. ABSTRACT *(Maximum 200 Words)*

The work described in this report uses a modified pulsed plasma-enhanced chemical vapor deposition (PECVD) technique that has been successfully developed to fabricate state-of-the-art nc-Si materials and devices. Specifically, we have achieved the following benchmarks: nc SiH device with an efficiency of 8% achieved at a deposition rate of ~1 A/s; nc SiH device with an efficiency of 7% achieved at a depostion rate of ~5 A/s; large-area technology developed using pulsed PECVD with uniformity of +/-5% over 25 cm x 35 cm; devices have been fabricated in the large-area system (part of Phase 3); an innovative stable four-terminal (4-T) tandem-junction device of η> 9% fabricated. (Note that the 4-T device was fabricated with existing technology base and with further development can reach stabilized η of 12%); and with improvement in Voc ~ 650 mV, from the current value of 480 mV can lead to stable 4-T device with η>16%. Toward this objective, modified pulsed PECVD was developed where layer-by-layer modification of nc-SiH has been achieved. (Note that due to budget cuts at NREL, this project was curtailed by about one year.)

15. SUBJECT TERMS
PV; module; solar cells; manufacturer; device; nano-crystalline silicon (nc-Si); continuous wave (CW); quantum efficiency (QE); tandem junctions; large area

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			19b. TELEPONE NUMBER (*Include area code)*
Unclassified	Unclassified	Unclassified	UL		