

# Advanced CIGS Photovoltaic Technology

**Final Technical Report**  
**15 November 2001 — 13 February 2005**

A.E. Delahoy and L. Chen  
*Energy Photovoltaics, Inc.*  
*Princeton, New Jersey*

**Subcontract Report**  
**NREL/SR-520-38356**  
**August 2005**

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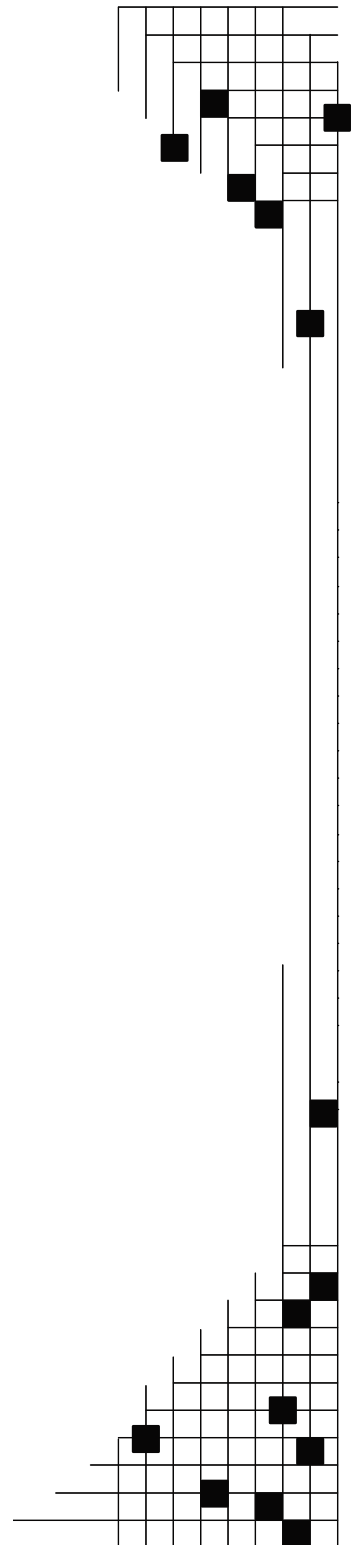
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## *Preface*

Technically, thin-film PV technologies have advanced considerably in the last few years. The leading thin film technologies are, broadly, a-Si (and variations), CdTe, CIGS, c-Si film, and dye-sensitized. At the time of writing, the leading commercially-available thin film technologies have demonstrated the following record aperture area efficiencies and powers for large area modules:

CIGSS	13.1%	64.8W	Shell Solar GmbH (glass)
CIGS	13.0%	84.6W	Würth Solar (glass)
CdTe	10.2%	67.4W	First Solar (glass)
a-Si/ $\mu$ c-Si	10.0%	38.0W	Kaneka (glass)
CIGS	10.1%	71.2W*	Global Solar (ss)
a-Si/a-SiGe/a-SiGe	7.6%	70.8W*	United Solar (ss)
CdTe	7.3%	52.3W	Antec Solar (glass)
a-Si	6.4%	100W	Mitsubishi Heavy Industries (glass)
a-Si/a-Si	6.1%	33.3W	RWE (glass)
a-Si	6.0%	48.6W	Kaneka (glass)
a-Si/a-si	5.8%	43.3W	Energy Photovoltaics (glass)

\* assembly of cells (not monolithic)

Even higher module efficiencies have been demonstrated by some companies that currently do not use the technology commercially, e.g. 13.4% for CIGS by Showa Shell, and 11% for CdTe by BP Solar and Matsushita. Within each thin-film semiconductor technology category, various deposition methods have been devised, and many are represented in the above table. While a high module efficiency is desirable, module efficiency figures do not tell the whole story. The long term commercial success of the various approaches is not automatically assured, but is dependent on a combination of module efficiency, manufacturing cost and market niche. For example, the manufacture of thin-film c-Si modules in the efficiency range 8-10% can be approached by depositing and recrystallizing a-Si:H. Indeed, prototype modules have been produced and the process used has been described in the literature. It is instructive to analyze this thin-film c-Si process, and to compare it to CIGS processing. The analysis reveals more complex processing than is required for CIGS (about 20 steps versus 12, exclusive of encapsulation), a high cost for the borosilicate glass, high capital costs, and extensive use of indirect materials in multiple etching processes. It is not clear that it offers a viable pathway to cost-effective manufacturing. Amorphous silicon, on the other hand, is of lower efficiency, but can be manufactured with high yield and at the lowest \$/W of all the technologies mentioned. CIGS continues to hold the efficiency record, but the technology, although having entered the realm of manufacturing, is arguably not yet sufficiently evolved to be cost-competitive for production of standard power modules.

One further factor that will eventually emerge as a strong driver of success for PV technologies in the energy market is the specific energy for module production. For PV to continue growing at 30% per year for the next 30 years so that it can take its place as a significant energy source on the world stage, modules will have to be made in a more energy-efficient manner. At this growth rate, for a new PV factory to generate a positive energy return in less than 10 years, the specific energy for module production must be less than 18MJ/W<sub>p</sub> [1]. If a particular PV technology cannot meet this condition, it may be questioned whether large quantities of energy will in practice be expended to manufacture modules using such a technology. The published range of total energy requirements to produce wafer-based modules is 20-100 MJ/W<sub>p</sub>. For a-Si the figure is 12-15MJ/W<sub>p</sub> (EPV), while for CIGS the figure is 11MJ/W<sub>p</sub> (Shell Solar).

From the above discussion we see that the driving forces for CIGS are compelling: potentially high efficiency and low specific energy for production. To these we may add the broadly advantageous properties of most thin-film PV processes relative to wafer-based PV: monolithic design and large substrates (leading to reduced parts handling), low consumption of both direct and indirect materials, and fewer process steps.

Energy Photovoltaics, Inc. (“EPV”) is a solar energy company that primarily designs, develops, manufactures, and markets thin-film photovoltaic (PV) modules and Integrated Manufacturing Systems to serve the growing international PV marketplace. The strategy being pursued by EPV is premised on a fundamental belief that, for PV to be successful as more than a specialty source of electricity (with growth stimulated by government incentive programs), it must deliver electricity at the lowest possible cost. In this vein, EPV continues to ship its EPV-40 tandem junction, amorphous silicon PV modules manufactured at its headquarters in Lawrenceville, NJ. The modules are UL-listed and have IEC 61646 certification. The production is fully sold out for 2005. On the IMS front, EPV completed a 2.5MW a-Si module manufacturing plant for the Tianjin Jinneng Solar Cell Corp. in China in April 2004. The plant met all production rate and quality deliverables and is in full production. EPV is also supplying an a-Si IMS rated at 11MW to Heliiodomi, S.A. of Thessaloniki, Greece.

In parallel with a-Si production, Energy Photovoltaics, Inc. is also developing technology to be able to cost-effectively manufacture much higher efficiency CIGS modules. EPV has consistently pursued a vacuum-based approach to CIGS production, and has developed novel linear thermal source technology to supply materials to heated, moving, soda-lime glass substrates. It has also deliberately chosen to develop processing methods with worker safety in mind. These strategically-important choices offer a low-cost substrate, control over layer homogeneity and purity, and production without significant hazards. Although such approaches help to minimize the processing costs of CIGS, further advances appeared necessary in order to improve both ease of production and yield. One such advance, the introduction of Cu sputtering, was accomplished under the NREL **Thin-Film Photovoltaics Partnerships Program (TFPPP)**.

To facilitate the development of CIGS, CdTe, and Si-based thin-film technologies, NREL operates the Thin-Film Photovoltaics Partnerships Program. The long-term objective of the TFPPP is to demonstrate commercial, low-cost, reproducible modules of 15% aperture-area efficiency [2]. As a Technology Partner within this program, EPV has performed research under a three-phase, cost-shared subcontract entitled “Advanced CIGS Photovoltaic Technology” and

participates in the National CIS Team Meetings. One of the main objectives of this subcontract (RDJ-2-30630-21) was for EPV to demonstrate its capability to produce reasonably efficient CIGS modules at a substrate size of 4300 cm<sup>2</sup>. The processing also needed to be reproducible with good controllability. This goal was successfully accomplished by the development and utilization of a new hybrid process for CIGS growth during the three year contract period. This final technical report mentions highlights of the first and second phases of the subcontract, and describes in detail results obtained during the third phase of the subcontract.

The benefits accruing from the hybrid process raises the obvious question of whether process and equipment development does more to advance PV technology than the more traditional research into materials and devices.

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## **1.0 Introduction**

This is the Final Technical Report for EPV's cost-shared subcontract ZDJ-2-30630-21 **Advanced CIGS Photovoltaic Technology** awarded under the Thin Film Photovoltaics Partnership Program (TFPPP). The work period covered by this final report is from November 15, 2001 to February 13, 2005.

As part of the Thin Film Photovoltaics Partnership Program, EPV has conducted research to help generate a technology base for production of CIGS PV modules using vacuum deposition of CIGS onto glass. This strategy is consistent with the observation that, despite there being several approaches to forming device quality CIGS, vacuum deposition has maintained the world record for the highest efficiency CIGS device. This record currently stands at 19.5% (692mV, 35.2 mA/cm<sup>2</sup>, FF 79.9%) for 0.41 cm<sup>2</sup> device grown at NREL by the three-stage process [3]. To overcome barriers to manufacturing CIGS by vacuum deposition, EPV has developed vacuum equipment incorporating novel linear evaporation sources and magnetron sputtering cathodes designed for uniform coating of large (0.43m<sup>2</sup>) moving substrates [4]. The use of elemental selenium avoids the need for gaseous H<sub>2</sub>Se.

### **Project Objectives**

The principal objective has been to develop the best CIGS large area module process based upon capability of implementation on EPV's large scale processing equipment. The first requirement was to develop recipes for CIGS, junction formation and a high quality ZnO window that together are capable of producing small area devices with efficiencies in excess of 13%. The second requirement was to significantly improve the uniformity of all layers (Mo, CIGS, CdS and ZnO) on large area substrates. Thirdly, patterning procedures needed to be improved to generate an interconnection with the lowest possible contact resistance, to eliminate possible shunting paths, and to reduce the dead area. The processes should have good reproducibility and therefore be easily controllable. Finally, having assembled all of these aspects mentioned above, the goal was to fabricate large area, monolithic CIGS modules with efficiencies in the range 7 - 10%. A study of module reliability and long-term stability would be conducted to establish the foundation and confidence for embarking on future manufacturing.

### **Approach**

Process development and process verification for CIGS are conducted initially in the Hercules 4-source system (an R&D system with a capability of six 5cm x 10cm stationary substrates per run) for the purpose of proof of concept. As soon as good device and mini-module performance are achieved and repeated, the basic process concept will be transferred to our large area system Zeus that is fitted with a 4 linear-source head and that handles a single 4300 cm<sup>2</sup> moving substrate per run. In the latter system, which is load locked, source materials are delivered downwards to the moving glass using custom-built, linear evaporative sources, the source axes being perpendicular to the direction of glass travel. This approach allows a wide range of vacuum-based CIGS recipes to be implemented. Copper can be supplied either by thermal evaporation or by planar-magnetron sputtering in the Zeus system, or by sputtering in a separate in-line deposition system. During the period covered by this Final Report, we focused on a so-

called hybrid process utilizing evaporation of In, Ga and Se and sputtering of Cu to take advantage of improved plate uniformity and the flexibility of forming a Ga profile. After verification of process transfer, all further optimization of the CIGS process was conducted in the Zeus system. Film and device characterization were realized through in-house laboratories containing ICP-AES, SEM, computerized QE, and indoor/outdoor IV facilities. Some samples were sent out to NREL and IEC for further analysis.

For junction formation, EPV relies on CBD CdS on a day-to-day basis, and from time to time explores alternative methods in parallel. Other methods include buffer layers applied by evaporation (e.g.  $\text{ZnIn}_2\text{Se}_4$  or other materials), by spray deposition, or by hollow cathode sputtering. A proprietary surface treatment of the CIGS is routinely used in our device and module processing and new processes for surface treatment are being explored. For ZnO deposition, two planar-magnetron sputtering systems are available (Airco and large area, in-line system or ILS) and are fitted with ceramic ZnO targets. New transparent conductors produced by reactive-environment hollow cathode sputtering are also being explored. Module encapsulation is accomplished using glass-glass vacuum lamination with EVA, with processing similar to that used in the commercial EPV-40 amorphous silicon module. For long-term outdoor testing, a Campbell Scientific datalogger is available.

## 2.0 Highlights of Phases I and II [5,6]

- A hybrid CIGS process (involving Cu deposition by sputtering) was explored in the R&D Hercules system in Phase I, with the goal of improving the uniformity of both CIGS thickness and composition. The remaining elements, In, Ga, and Se, continued to be delivered by evaporation.
- An improved thickness distribution on large area plates produced in Zeus was realized in Phase I for CIGS produced by the hybrid process.
- An extensive survey of post-deposition treatments of CIGS was made. A useful wet treatment was identified in Phase I that improved the performance of devices.
- Optimization of EPV's procedure for CBD CdS was conducted. Improved device performance was realized in Phase I after a change from Cd acetate to Cd sulfate.
- Using the hybrid CIGS process, post-deposition treatment, and the improved CBD CdS recipe, cells up to 13.5% efficiency (569 mV, 32.3 mA/cm<sup>2</sup> without ARC, FF 73.5%) were produced in the R&D Hercules system in Phase I. The devices were found to improve upon light soaking.
- Using EPV CIGS prepared by evaporation of all elements, a 10.1% cell was produced in Phase I using an evaporated zinc indium selenide (ZIS) buffer layer, and an 8.6% cell using evaporated  $\text{In}_2\text{S}_3$ .
- A mini-module with laser-scribed Mo and mechanically-scribed CIGS and ZnO was produced using Hercules CIGS with an aperture area efficiency of 9.0% in Phase I.

- The concept of CIGS prepared by a hybrid process that involves evaporation of In and Ga and sputtering of Cu was successfully transferred to large area Zeus system in Phase II. The process shows good reproducibility, and shows promise for being manufacturable.
- Both in-situ and ex-situ sputtering of the Cu have been successfully utilized to form high quality CIGS by the hybrid process in Phase II.
- Diagnostic devices formed on large area (0.43m<sup>2</sup>) CIGS plate in Zeus by the hybrid process have been produced in Phase II with V<sub>oc</sub>s as high as 659mV, and efficiencies up to 11.8%.
- 10.1% devices were prepared by an exploratory process that involves evaporation of IGS compound and Cu sputtering in Phase II.
- The CBD process for CdS was improved through adoption of a slow reaction in Phase II. This improved uniformity.
- Improved ZnO properties were obtained at elevated substrate temperatures in Phase II.
- The type of ZnO best suited to the ZnO/Mo interconnection has been investigated and important rules have been developed in Phase II.
- Large area module processing was restored, and reasonably reproducible 1ft<sup>2</sup> modules were produced relatively quickly in the 5.0 -5.5% efficiency range in Phase II.
- A 15.5% cell (with CdS) was fabricated by EPV on bare NREL CIGS, and a 13.3% cell was fabricated using no CdS but with hollow cathode sputtering of the ZnO.
- An 8.2% cell (with CdS) was fabricated on EPV CIGS using IMO instead of ZnO.
- Water immersion tests indicated superior stability of IMO relative to ZnO.

### 3.0 CIGS Optimization and Device Results

#### 3.1 Composition and Cu rich regime

During the period of Phase III, the CIGS team at EPV mainly focused on device optimization, and especially on the formation of the CIGS absorber. This focus follows from the realization that CIGS quality is the single most important factor contributing to module efficiency. Optimization of the hybrid process was conducted in the large area, pilot-line system using 0.43 m<sup>2</sup> substrates. We examined the necessity of letting the CIGS formation process pass through a Cu-rich (Cu/(In+Ga)>1) stage. This had been reported to enhance the growth of high-quality, large-grained films via the utilization of Cu<sub>x</sub>Se as a liquid fluxing agent at sufficiently high substrate temperatures (>523 C) to promote lateral grain growth [7], but remained controversial. We found that processing a Cu-rich precursor (Cu/(In,Ga)<sub>2</sub>Se<sub>3</sub>) is clearly more robust in repeatedly producing high-quality CIGS films and yielding better devices. Listed in Table 3.1 are some samples produced from Zeus during CIGS optimization.

Table 3.1. Deposition conditions and resulting composition and device performance

Sample ID	Se Temp [°C]	Cu ratio 1 <sup>st</sup> IGS +Cu	Cu & Ga ratio of CIGS		V <sub>oc</sub> [mV]	J <sub>sc</sub> [mA/cm <sup>2</sup> ]	FF [%]	Eff [%]
			Cu	Ga				
Z1559-2*	550	0.87	0.86	0.31	351	27.2	52.4	5.0
Z1559-1	550	0.87	0.63	0.31	483	26.5	64.4	8.2
Z1559-6	525	1.27	0.68	0.26	529	23.1	64.7	7.9
Z1559-5	550	1.27	0.71	0.28	558	26.9	72.7	10.9
Z1665-3	580	1.4	0.89	0.30	554	30.7	70.6	12.0
Z1728-5	600	1.43	0.92	0.30	560	32.3	68.6	12.3
Z1730-5	600	-	-	0.32	543	33.4	70.1	12.7

\*Z1559-2 was made in a two-step process without the last IGS finishing layer

The third column indicates the ratio of Cu to In+Ga measured with ICP AES after the first IGS and Cu depositions. The values in the third column are all greater than one (Cu-rich precursor) before the last IGS layer is deposited except for sample Z1559-1 & 2. A comparison of the V<sub>oc</sub> and FF of Z1559-5 versus those of Z1559-1 (both have the same selenization temperature T<sub>ss</sub> = 550°C), reveals the benefit of passing through a Cu-rich regime in the three-stage hybrid process.

### 3.2 Selenization temperature

Despite the improvement of both V<sub>oc</sub> and the overall efficiency by passing through a Cu-rich regime, the QE response for Z1559-5 (550°C) shown in Fig 3.1 was clearly unsatisfactory, especially the poor collection at long wavelengths.

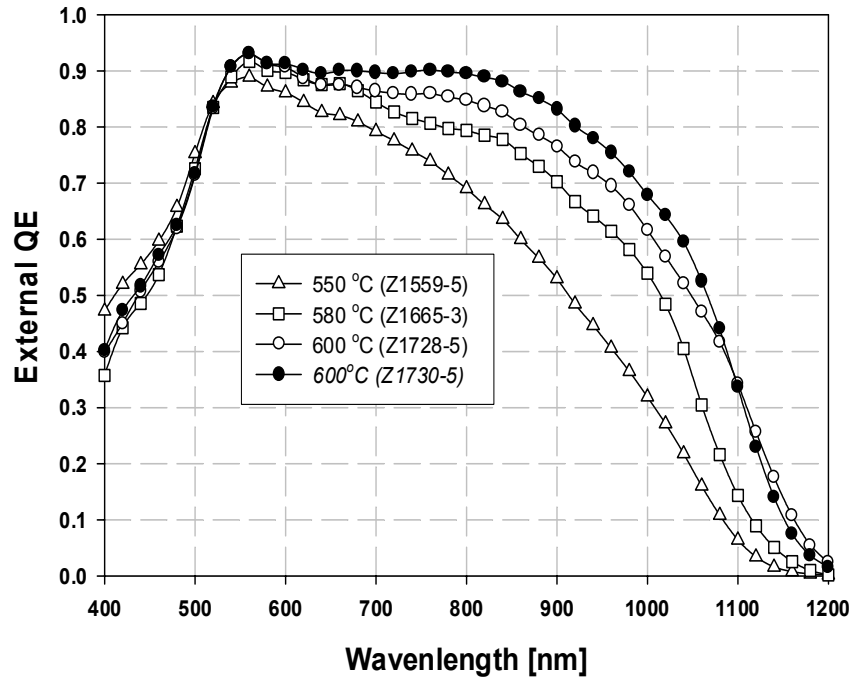


Fig. 3.1. QE curves for devices made at different CIGS temperatures.

It was thought that poor bulk properties of the CIGS film limited the current collection. Therefore, the influence of selenization temperature  $T_s$  on CIGS films and devices was studied. By increasing the selenization temperature from 525°C to 600°C, the short-circuit current density  $J_{sc}$  and the collection of photo-generated electrons at long wavelengths were indeed significantly improved (see Table 3.1 and Figure 3.1). It is worth noting that the real substrate temperature might be slightly lower than the values in the Table 3.1 since the substrate is moving during the deposition and the temperature sensor is static and located closer to the heaters.

### **3.3 Ga distribution and bandgap profile**

That the Ga distribution in a CIGS film, and thus the bandgap profile, will affect CIGS device performance has been known for a long time [8]. (Indeed, a similar concept has been applied to a-SiGe cells for more than a decade. Various graded in, graded out, and notch structures were tested and modeled [9].) Creating a higher bandgap material in the rear part of the CIGS layer by increasing the Ga concentration is thought to form a back-surface field, which will tend to drive photo-generated electrons (minority carriers) away from the rear interface and towards the front, which should be beneficial to  $J_{sc}$  and FF. Device Z1730-5 in the last row of Table 3.1, compared with Z1728-5, is an example of such a design. Its improved performance is consistent with the concepts just described. A further refinement might increase to some degree the Ga ratio (and thus bandgap) within the depletion region and towards the junction which should boost  $V_{oc}$  without presenting a conduction-band barrier to electron collection. A lower bandgap region deeper within the absorber can help absorb long-wavelength photons to retain high  $J_{sc}$ .

### **3.4 Other parameters**

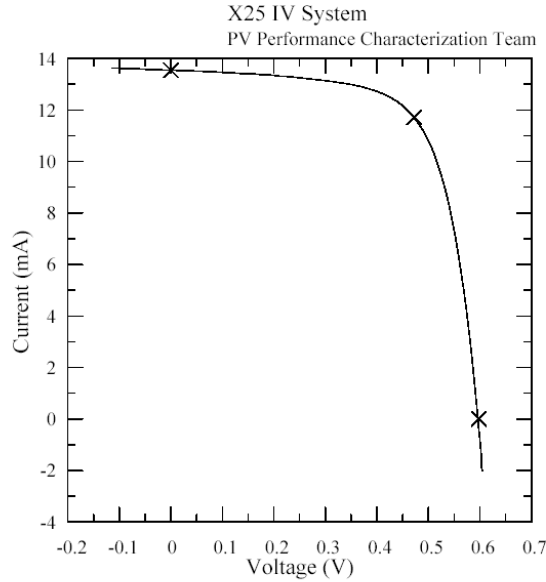
Among the many other process parameters pertaining to the formation of CIGS films, we found the substrate moving speed and deposition rate for the final evaporated IGS layer are sensitive parameters for the hybrid process. As currently implemented, the substrate undergoes multiple scans under the linear sources. It seems that the CIGS surface morphology can in this way be influenced, which we will illustrate below.

### **3.5 Device performance**

After deliberately optimizing everything mentioned above, we were able to achieve an efficiency of over 13% for hybrid CIGS devices made in the large area system Zeus [10]. One such device, Z1699-1, was sent to NREL for verification. Plotted in Fig. 3.2 is the JV curve for cell #5, as measured at NREL. The PV parameters are: 598mV, 32.2mA/cm<sup>2</sup>, FF 68.3%, efficiency 13.1%.

**Energy Photovoltaics**  
**CdS/Cu(In,Ga)Se<sub>2</sub> Cell**

Device ID: Z1699-1 #5                      Device Temperature: 25.0 ± 1.0 °C  
 Jul 26, 2004 10:30                      Device Area: 0.421 cm<sup>2</sup>  
 Spectrum: AM1.5-G (IEC 60904)              Irradiance: 1000.0 W/m<sup>2</sup>



$V_{oc} = 0.5978 \text{ V}$	$I_{max} = 11.713 \text{ mA}$
$I_{sc} = 13.545 \text{ mA}$	$V_{max} = 0.4722 \text{ V}$
$J_{sc} = 32.173 \text{ mA/cm}^2$	$P_{max} = 5.5309 \text{ mW}$
Fill Factor = 68.30 %	Efficiency = 13.1 %

Storage state after 30 minutes soak at  $V_{oc}$ .

Fig. 3.2. J-V curve of Z1699-1 #5 measured at NREL (efficiency 13.1%).

## 4.0 CIGS Film Analysis

### 4.1 Scanning electron microscopy

Some of the samples listed in Table 3.1 were sent to NREL for morphology analysis. SEM micrographs show that the grain structure of the CIGS films changes dramatically as  $T_{ss}$  and the Cu ratio of the precursor are changed (see Fig. 4.1). The film Z1730 formed at  $T_{ss} = 600^\circ\text{C}$  from a Cu-rich precursor (right-hand micrograph) shows columnar grains with typical grain size around 1.0  $\mu\text{m}$  [11]. But for the film Z1559-1 (mislabelled as S1559-2 in the left-hand micrograph) formed at  $T_{ss} = 550^\circ\text{C}$  from a Cu-poor precursor, the grains are smaller and do not grow continuously from the Mo to the top layer. Thus, photo-generated electrons may need to pass through several grain boundaries, affecting their collection. This observation concurs with device performance, and confirms that a Cu-rich precursor and a sufficiently high substrate temperature are important in processing.

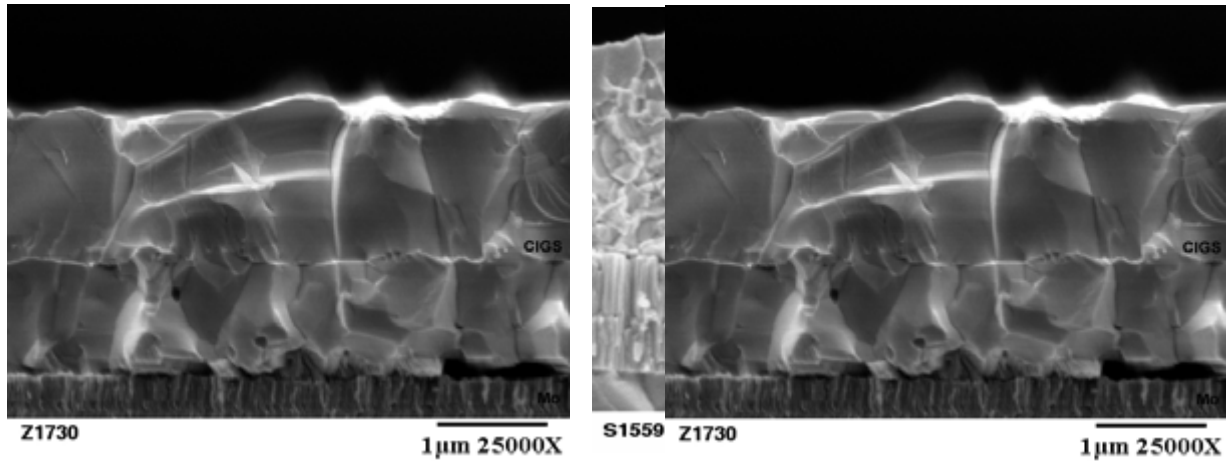


Fig. 4.1. SEM cross-section images of Z1559-1 (left) and Z1730 (right).

#### 4.2 Depth profiling by Auger electron spectroscopy

Depth-profile analyses of CIGS films were carried out by AES. Figure 4.2 shows the Ga/(In+Ga) ratio *versus* film depth for three films listed in Table 3.1. Z1559-2 was made at  $T_{ss} = 550^{\circ}\text{C}$  from a Cu-poor precursor without the In, Ga, Se finishing layer. A very sharp transition is seen with Ga considerably depleted in the surface region. Z1665 was made from a Cu-rich precursor at  $T_{ss} = 580^{\circ}\text{C}$ , and the Ga distribution is fairly uniform. For these two films, the In and Ga fluxes were delivered simultaneously.

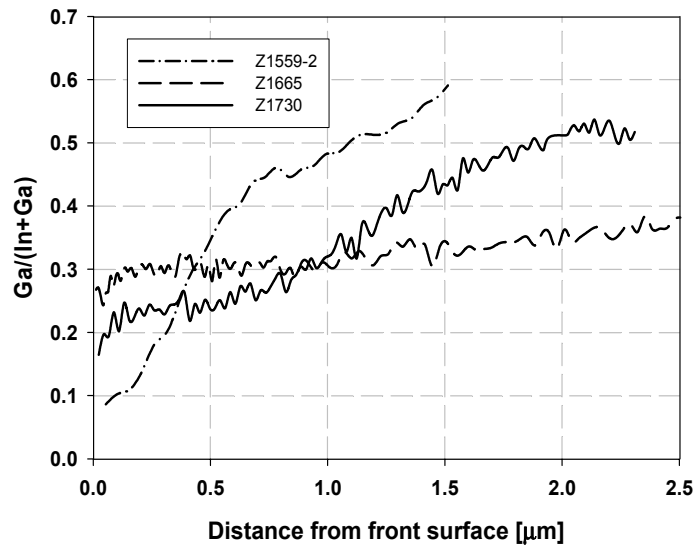


Fig. 4.2. Ga/(In+Ga) vs film depth as determined by AES for three films shown in Table 3.1.

There are two possible phenomena regarding the In, Ga diffusion during the conversion of the  $\text{Cu}/(\text{In,Ga})_2\text{Se}_3$  precursor to CIGS. One is the out-diffusion of In, Ga accompanied by in-diffusion of Cu. The out-diffusing In, Ga reacts with Cu and Se to form new unit cells, contributing to the growth in thickness. As In has a larger atomic radius than Ga, the strain energy of the film is lowered by preferential In out-diffusion relative to Ga, and the additional

film become Ga depleted. On the other hand, when excess Cu and Se and high temperatures result in liquid-phase  $\text{Cu}_x\text{Se}$ , the diffusion due to the concentration gradients of In and Ga are increased via the  $\text{Cu}_x\text{Se}$  at grain boundaries. Consequently, the Ga/(In+Ga) gradient decreases. The uniform Ga distribution of our films under those conditions might indicate that the time spent in the Cu-rich regime is too long.

In run Z1730 the conditions were adjusted to form a precursor with a higher initial Ga content by intentionally changing the Ga flux during the first  $(\text{In,Ga})_2\text{Se}_3$  layer. From Fig. 4.2, a graded Ga distribution for this sample is seen. The fabricated device exhibited increased efficiency with superior current density and QE (see Table 3.1 and Fig. 3.1). The improved electron collection, especially for electrons generated by long wavelength photons, can be attributed to the graded Ga distribution.

### 4.3 X-ray diffraction

Although a graded Ga distribution with a higher Ga content towards the Mo back contact was achieved, the Ga content at the surface of the CIGS films is still low. This might be one of the reasons that the devices do not have exceptional  $V_{oc}$ . Another factor contributing to lower  $V_{oc}$  might be from CIGS surface morphology. In some samples, for example Z1699, we found flake-like morphology with some crevices at the top. It was reported that the hexagonal  $\text{Cu}(\text{InGa})_5\text{Se}_8$  film also has a layered structure [12]. In order to examine if there is another phase in the top layer of the film, XRD (Cu-K $\alpha$ , 35kV, 20mA) and GIXRD (Cu-K $\alpha$ , 40kV, 40mA,  $\Omega$  =1 deg, sampling depth ~300 nm) measurements were carried out, and the patterns are shown in Fig. 4.3.

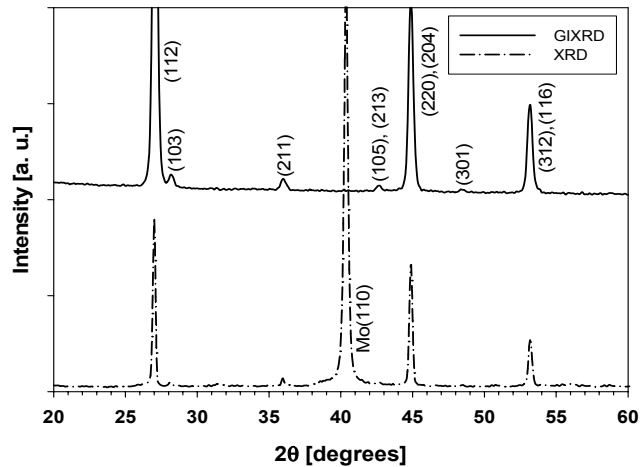


Fig. 4.3. XRD patterns for CIGS film Z1699.

The GIXRD pattern is the same as that from XRD, and all peaks can be indexed based on a tetragonal  $\text{Cu}(\text{In}_{0.7}\text{Ga}_{0.3})\text{Se}_2$  unit cell (JCPDS card #35-1102). This means that no additional phase could be identified, and the cause of the layered morphology is not clear, nor is it known how it affects junction properties. It is hypothesized that the crevices in the top layer result from migration due to a non-uniform  $\text{Cu}_x\text{Se}$  distribution during the conversion of  $\text{Cu}_x\text{Se}$  into CIGS during the final In, Ga, Se delivery [13]. The total extent of Cu-richness during growth would



then be a factor that could improve this, so the maximal tolerable Cu ratio for a Cu-rich precursor needs to be investigated.

#### 4.4 Activation energy

Another possible cause for unexceptional  $V_{oc}$  of devices could be reduced band bending resulting from a higher than desirable activation energy of the CIGS film. To investigate this possibility, measurement of the activation energy  $E_a$  for conduction was carried out during this Phase. Plotted in Fig 4.4 is conductivity vs. reciprocal of temperature for a CIGS film from a Zeus run. The activation energy extracted from this data shows a noticeably high value of 0.36 V. So far it is not clear if there is a strong correlation between  $E_a$  and device  $V_{oc}$ . It should be noted that the measured  $E_a$  was deduced from the lateral conductivity of the CIGS film. Further measurements and comparisons are planned for the next contract.

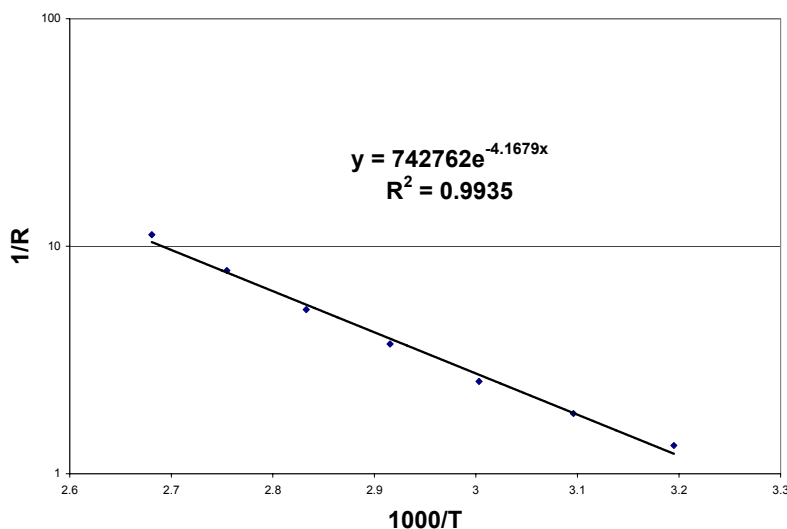


Fig. 4.4. Activation energy for CIGS of 0.36 V calculated from linear fitting.

## 5.0 Full Size Module Process and Performance

### 5.1 CBD CdS process in full size tank

A module aperture area efficiency of 5.5% in an area of 1 ft<sup>2</sup> was achieved in Phase II. At that time, the only missing equipment required for processing full size (0.43 m<sup>2</sup>) modules was a new full size tank for CBD CdS. (Use of an earlier full size tank had been discontinued on safety grounds.) We were able to complete installation of a new large area dipping tank for full size CBD CdS processing at an early stage in Phase III. Some of the features of the set up are as follows. The chemicals are contained in a stainless steel tank. Heaters are attached along the length outside the tank in an insulated compartment. A temperature controller is used to obtain and monitor the desired bath temperature. The chemical solution is re-circulated by a liquid pump driven with a digital module to control solution flow. The tank is easy to maintain and clean up. The process area is well vented for safe operation.

Two kinds of verification tests were conducted for acceptance of the process transferred from a well-characterized beaker set up. First, device performance was compared using CdS deposited in the beaker (as reference) and in the big tank. Listed in Table 5.1 is one of numerous comparison experiments conducted to verify that the tank CBD process is as good as that of the beaker.

Table 5.1. Device FF mapping to compare beaker and tank CBD process

<b>Positions</b>	<b>Column 1 from Beaker</b>	<b>Column 2 from Beaker</b>	<b>Column 3 from Tank</b>	<b>Column 4 from Tank</b>
<b>Row 1</b>	68	67	68	69
<b>Row 2</b>	70	68	69	69
<b>Row 3</b>	71	70	67	67

Second, the tank CdS process was further optimized for plate uniformity, which is checked by measuring the transmission at 420 nm and 440 nm of a CdS film deposited on a large area glass with CTO coating. Listed in Table 5.2 is a typical distribution of CdS film transmission.

Table 5.2. Transmission distribution (at 420 nm) of CTO glass coated with CdS film

<b>Width\Length</b>	<b>3"</b>	<b>11"</b>	<b>19"</b>	<b>27"</b>	<b>35"</b>
<b>3"</b>	0.50	0.50	0.50	0.45	<b>0.45</b>
<b>9"</b>	0.50	0.50	0.50	0.43	<b>0.50</b>
<b>15"</b>	<b>0.46</b>	<b>0.50</b>	<b>0.49</b>	<b>0.45</b>	<b>0.45</b>

## 5.2 Investigation of contact resistance between ZnO and Mo

From time to time in our large area module production, we cut a small glass sample from a full size CIGS plate and process it into a 2" x 4" mini-module (using manual patterning and Airco ZnO) to cross-check the processing. For a particular period, we found that mini-modules with Airco ZnO showed normal IV curves while those made with ZnO in the ILS exhibited extremely large series resistance. What puzzled us was that ZnO co-deposited on plain glass in both systems showed almost the same low value of sheet resistance. After a careful series of measurements, we found that while the ZnO resistance on each cell (on CdS) was almost same in both cases, the ZnO/Mo contact resistance on the mini-modules was totally different. Zinc oxide deposited in the ILS yielded a much larger contact resistance than that deposited in the Airco.

This observation led us to thoroughly investigate various issues that might influence contact resistance. In principle, high contact resistance could be caused by:

- Improper CIGS scratch
- Contaminated Mo surface
- Improper ZnO
- Poor step coverage

At first, we paid much attention to the first two potential causes since, having low sheet resistance, we thought we had good ZnO. We adjusted the CIGS scribing speed and pressure to ensure that the CIGS layer was totally removed and the Mo exposed; we tried different scribing

tips with various hardnesses and shapes; we increased the CIGS cutting width to increase the contact area; we also tested ultrasonic cleaning of the substrate in place of the usual glass washer; we annealed the CIGS after CdS deposition to desorb water to prevent contamination. After extensive experimentation, none of these factors was found to be the root cause we were searching for, although contact resistance was influenced by many variables. Finally, we realized our low sheet resistance ZnO deposited in ILS performed well as a front window layer but performed poorly as a contact. Indeed, sheet resistance describes the lateral resistance of a thin film, but does not give any information about resistance homogeneity in the perpendicular direction. This simplified picture is not adequate to control the properties of the ZnO/Mo contact. Once this was recognized, we were able to modify our deposition procedures to routinely obtain good ZnO/Mo contacts with specific contact resistivity  $< 1 \times 10^{-3} \Omega\text{-cm}$  [4]. Along the way, we demonstrated that an unsuitable ZnO layer could even give rise to diode-like behavior at the ZnO/Mo contact. This is shown in Fig. 5.1 below.

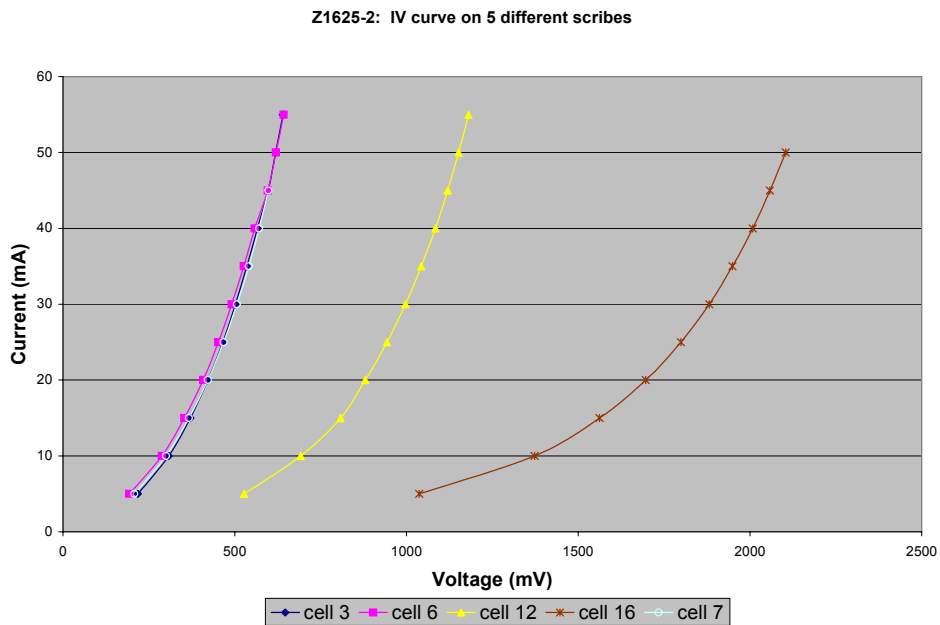


Fig. 5.1. I-V curve for an exceptionally poor ZnO-Mo contact

### 5.3 Uniformity improvement for large area plates

The uniformity of the various layers deposited on large area plates is a central issue in module production. From time to time, rather than completing a module, we measure and map device performance to check the uniformity over the plate. Fig. 5.2 is a contour plot of test device efficiency from Plate Z1653 produced in the beginning of this Phase. Immediate observations are that, while about one half of the plate shows efficiencies in the range 8-10%, a strip of the plate along the bottom edge shows a very significant drop in efficiency to the range 4-7%. As we diagnosed in our previous report, one of the main causes of non-uniformity across the short direction of the plate is non-uniformity of the Ga. The root cause, we found, was due to an asymmetry in the temperature of the two Ga boats.

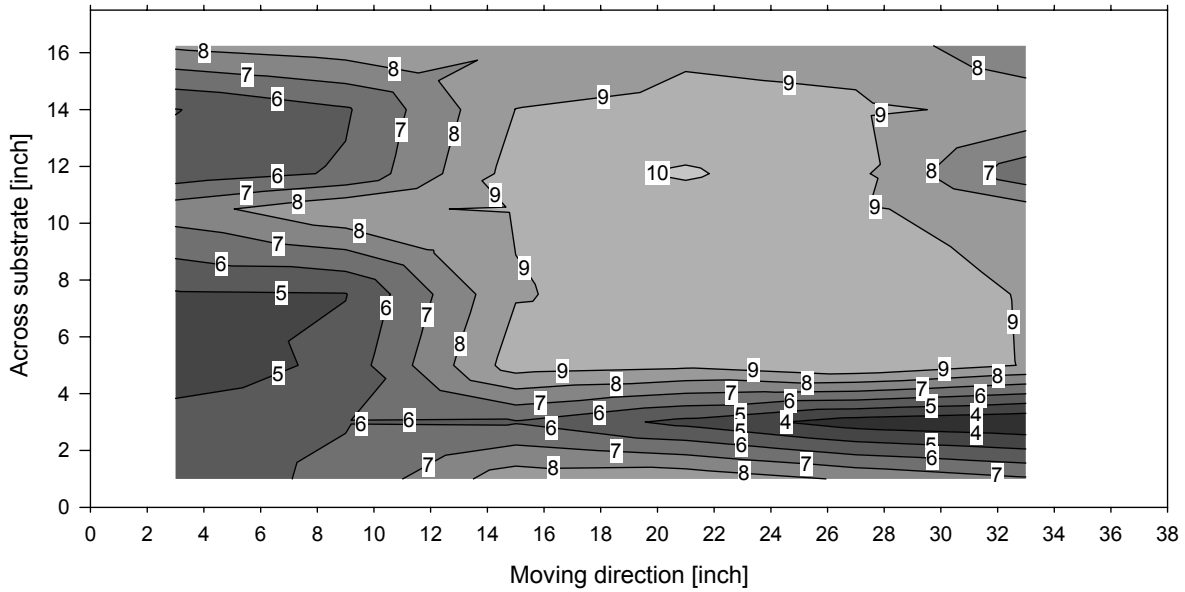


Fig. 5.2. Contour plot of device efficiency for run Z1653 (deposited early in Q2).

In Fig. 5.3 we show the Ga/(In+Ga) ratio in the direction of the linear source. Curve A (data from run Z1660) represents the problematic distribution. Fortunately, instead of rebuilding the whole delivery line and boat assembly, which would have been expensive and time consuming, we found an easier way to balance the temperatures of the Ga boats by adjusting the thermal insulation of one of the boats. Subsequent to that adjustment, the Ga distribution was found to be substantially improved. Curve B (data from run Z1673) is the new Ga distribution after boat temperature adjustment.

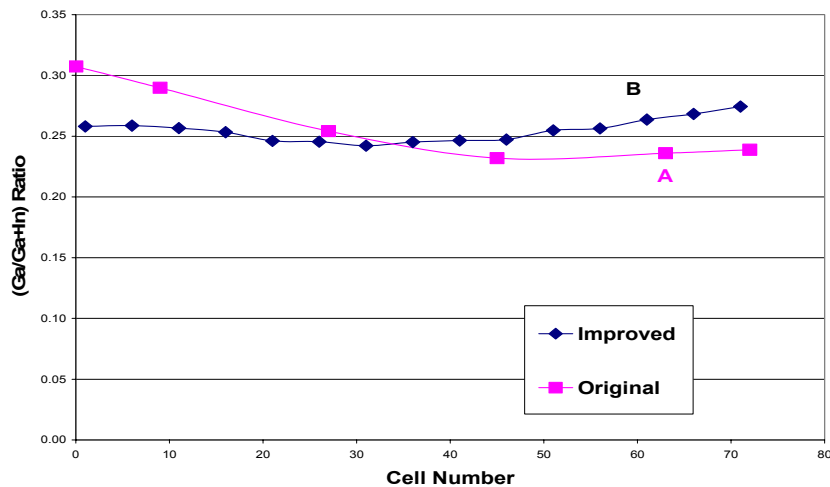


Fig. 5.3. Ga/(In+Ga) ratio versus segment number before and after Ga boat adjustment.

Another factor leading to device non-uniformity arises from the ZnO sputtered in the in-line sputtering system. By mapping out the sheet resistance of the ZnO we obtained the contour plot

shown in Fig. 5.4a. This revealed a surprisingly large range for the sheet resistance, from 8 to 14 ohms/square. In an attempt to improve the situation, we installed a new gas manifold adjacent to the ZnO target to deliver a more uniform gas flow and also adjusted the pumping configuration. The two-dimensional distribution of ZnO sheet resistance resulting from these hardware changes is plotted in Fig. 5.4b. In this run, most of the plate exhibits sheet resistances in the range 12 to 15 ohms/square, representing a tighter distribution.

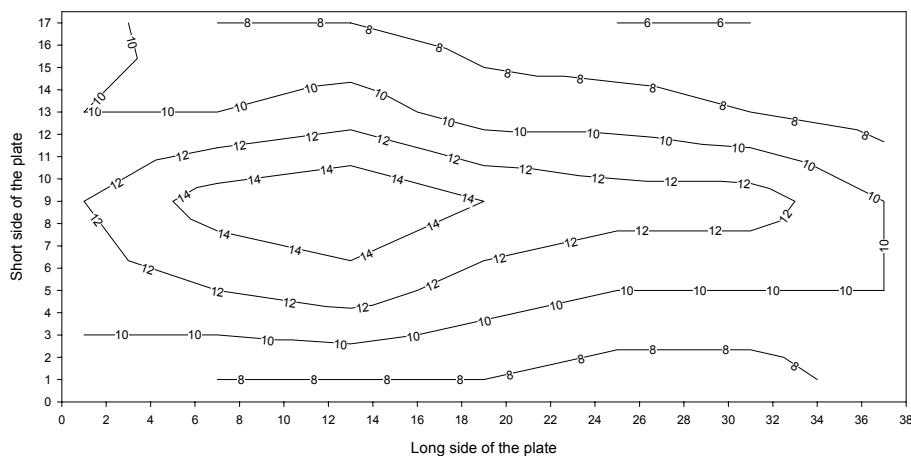


Fig. 5.4a. Distribution of ZnO sheet resistance before ILS modifications.

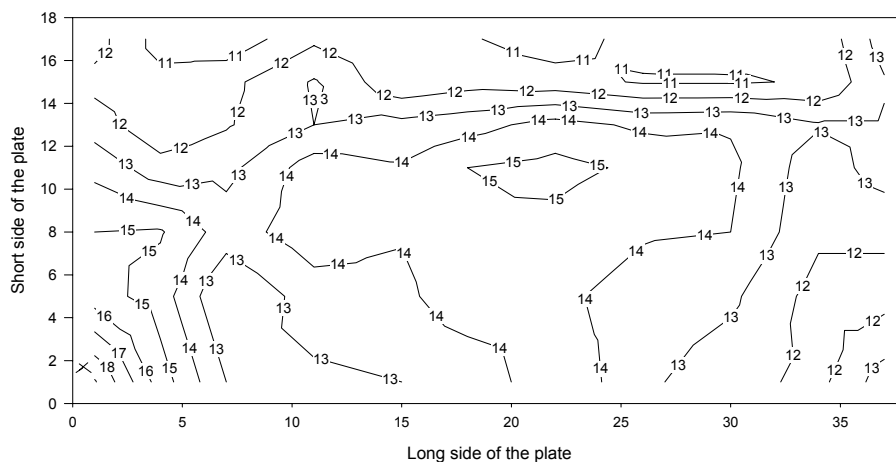


Fig. 5.4b. Distribution of ZnO sheet resistance after ILS modifications.

Finally, thickness mapping of sputtered Mo and sputtered Cu films both show a similar trend in that the films are a little thinner in the middle than at the long edges. This would seem to be due either to weaker plasma in the middle of target or to enhanced deposition near the ends of the racetracks. Therefore, we redesigned the magnetic field distribution for the Cu cathode. Very encouraging indeed, the uniformity of sputtered Cu films after redistribution of target magnetic field is significantly improved. Plotted in Fig. 5.5 is a graph of normalized thickness of Cu film versus position before and after the improvement. In this figure, the thickness measured on three strips oriented along the target direction, but at different locations in the moving direction

(namely 10, 20 and 30 inches from one edge), are measured and normalized. Hollow symbols (and light lines) in the plot represent the normalized thicknesses before improvement, while solid symbols (and heavy lines) represent those after improvement. The uniformity along the target direction is improved on all three strips, with the dip near the center of the target being reduced to 5% from 10%. However, non-uniformity along the moving direction still remains. This effect is related to the pumping port position and the gas delivery. We hope to work on this problem in the near future.

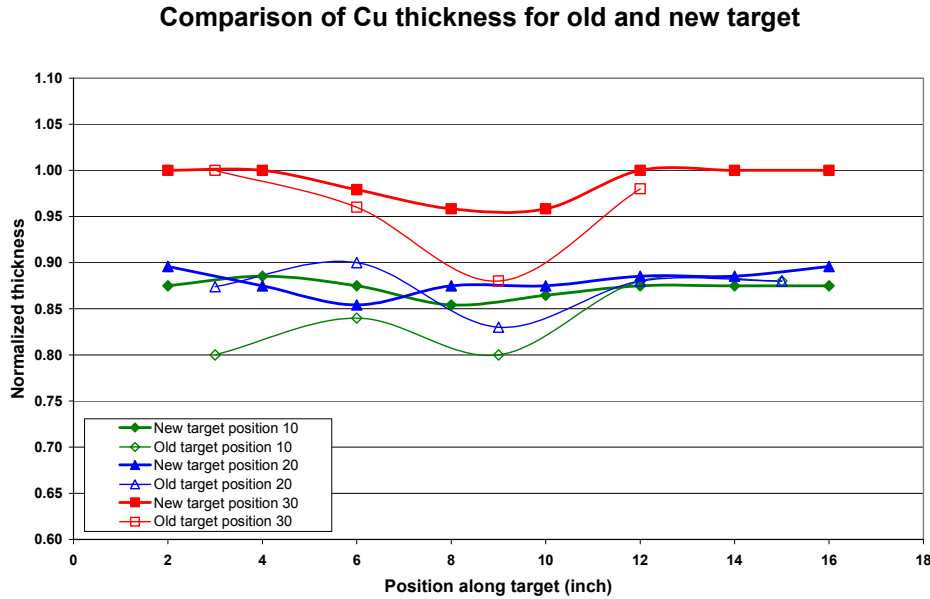


Fig. 5.5. Normalized thickness distribution along Cu target direction

After these many adjustments, modules recently made at EPV show improved uniformity. For example, plotted in Fig. 5.6 are the diagnostic cell distributions of  $V_{oc}$  and FF for plate Z1677, measured in the direction of the sources. The distribution of  $V_{oc}$  is very good, while that for the FF is acceptable, but with some variations whose origin has yet to be pinned down.

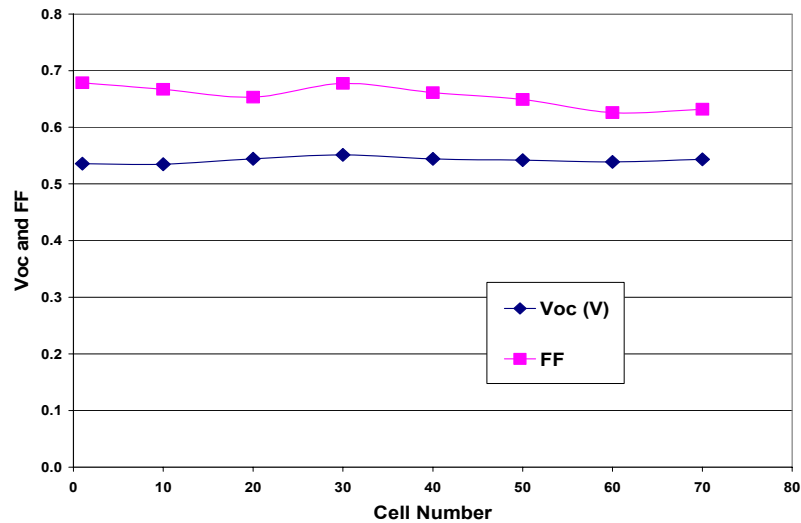


Fig. 5.6. Device performance distribution from plate Z1677.

## 5.4 Module performance

During Phase III, after incorporating the above process improvements and better process control, we were able to produce full size modules almost all of which have STC power of 20 W and above after lamination. The most reliable performance measurements were taken in sunlight with the module mounted on an orientable outdoor rack at EPV, and with 4-wire I-V curves acquired by an indoor computer. The short-circuit current  $I_{sc}$  is normalized by measured light intensity to a one-sun value, while  $V_{oc}$  is normalized to a 25°C value by measuring module temperature and applying a -2 mV/degree/cell temperature coefficient. Listed in Table 5.3 is part of our module inventory. Two of the modules, Z1652 and Z1668, were sent to NREL for efficiency verification, and both NREL results were very close to or a little higher than EPV's outdoor measurement.

Table 5.3. Performance of modules made during the Final Phase

ID	$V_{oc}$ (V)	$I_{sc}$ (A)	FF (%)	Power (W)	Efficiency (%)	Segment #	$V_{oc}/cell$ (mV)	Ap. area (cm <sup>2</sup> )
Z1652	41.3	1.02	49.4	20.9	6.2	71	582	3343
Z1655	40.3	1.10	48.8	21.7	6.1	71	568	3550
Z1657	37.7	1.08	48.1	19.6	5.8	71	531	3355
Z1667	37.9	1.23	54.1	25.1	6.7	71	534	3740
Z1668	38.5	1.20	56.4	26.0	7.5	71	542	3454
Z1670	37.7	1.33	47.2	23.7	6.3	71	531	3770
Z1673	36.1	1.23	47.1	20.8	5.9	71	508	3500
Z1674	36.0	1.20	52.4	22.6	6.0	71	507	3737
Z1677	39.0	0.95	58.5	21.7	6.5	71	549	3366
Z1678	34.9	1.14	50.5	20.1	5.5	71	492	3650
Z1683	34.4	1.11	52.0	20.0	5.4	71	485	3660

While accumulating the inventory represented by Table 5.3, we continued to experiment with CIGS process parameters. Regardless of this experimentation, all modules were functional, and the results in Table 5.3 demonstrate that EPV now has a controllable, large area hybrid CIGS process. A relatively high yield was also achieved, but this has not yet been consistently demonstrated over long periods of time. It does, however, lay down an excellent foundation for further systematic improvement. Once a module efficiency in excess of 9% is achieved, it will become worthwhile to examine the manufacturing potential of the technology. Fig. 5.7 is a copy of the I-V data for module Z1668, as measured by NREL. The  $P_{max}$  of this module was 26.0W, with an average voltage per cell of 542mV.

## Energy Photovoltaics CdS/Cu(In,Ga)Se<sub>2</sub> module

Device ID: Z1668  
May 06, 2004 14:26:20 MT  
Ref. Spectrum: IEC 60904

Device Temperature = 25.5°C  
Device Area = 3453.9 cm<sup>2</sup>  
Irradiance = 1000.0 W/m<sup>2</sup>

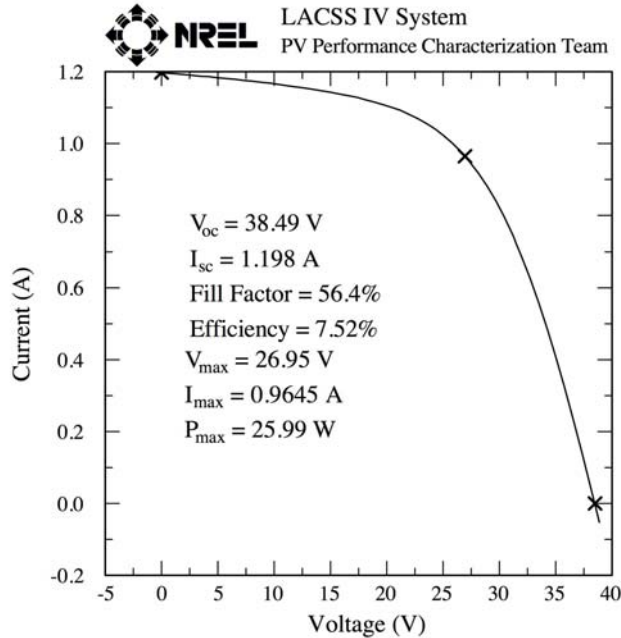


Fig. 5.7. I-V curve for a 26W, 7.5% module, as measured by NREL.

### 5.5 Long-term stability of EPV module

A laminated sub-module, Z1658 8-13, having a dimension of 6" x 17" and cut from full size plate Z1658, has been mounted on a south-facing, outdoor rack. It is periodically measured using the four-wire scheme mentioned above. The module has so far kept excellent stability for more than nine months. Plotted in Fig. 5.8 are normalized  $V_{oc}$  (by temperature), normalized short-circuit current  $I_{sc}$  (by one-sun irradiance), FF, and normalized efficiency (by both temperature and irradiance) derived from outdoor measurements without spectrum correction. The observed fluctuation in  $V_{oc}$  and FF is about 2 percent, and that in  $I_{sc}$  and efficiency is about 3 percent, which seems reasonable given that spectrum and wind speed are not monitored. It is interesting to observe that the normalized efficiency after long-term outdoor exposure shows a slight upward trend resulting mostly from improvement of fill factor and to a lesser extent current. It is not uncommon for CIGS devices and modules produced at EPV to improve in performance after light soaking, and indeed, with the current hybrid process this is the general rule. However, this is the first time we have done long-term outdoor exposure with a consistent measurement protocol.



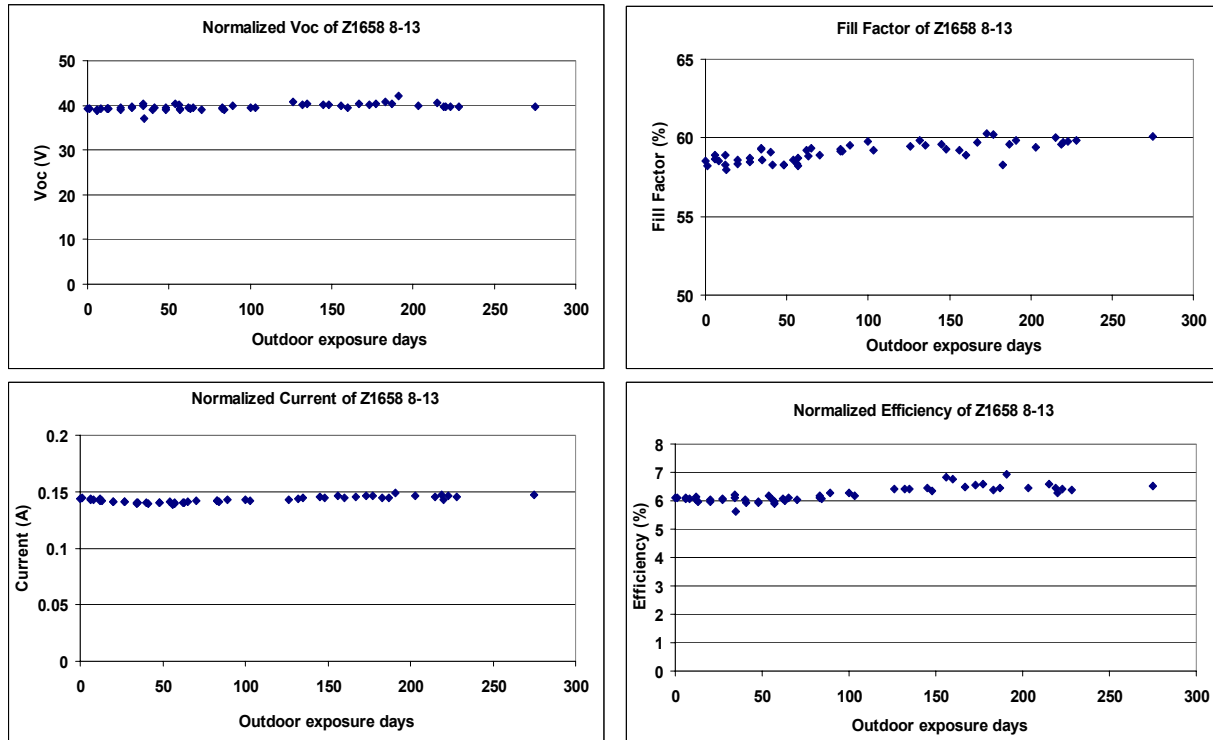


Fig. 5.8. Outdoor stability of CIGS sub-module Z1658 8-13.

## 5.6 Process control and database

Process controls for module production have been implemented at each individual station for quite a while. However, process parameters and measurable control values were separately located in individual databases. To better organize information, and to be able to grasp a picture for the entire process, we developed in the later period of Phase III a whole-process database linked to all of the databases for the individual process steps. In this way, all historical processing information can be easily accessed. Such a database is extremely useful to help identify problems and to analyze data for statistical studies.

## 6.0 Surface Treatment

At EPV, we have found that post-deposition treatment of the CIGS is an important step to improve device and module performance. Therefore, a 'standard treatment' has been implemented as one of EPV's routine processing steps. Nevertheless, we have continued searching for better and easier ways to treat CIGS plates. Some recently developed treatments show encouraging results. Listed in Table 6.0 are some data measured lately. The data in Table 6.0 show that newly developed test treatments are comparable with, and in some cases better than, our standard process.

Table 6.0. Device performance with various surface treatments

Sample ID	Treatment	V <sub>oc</sub> (mV)	FF (%)	J <sub>sc</sub> (mA/cm <sup>2</sup> )	Efficiency (%)
Z1730-25	Standard	504	65.4	32.8	10.8
Z1730-26	Test 1	550	70.8	31.9	12.4
Z1730-27	Test 2	557	70.0	33.0	12.9
Z1730-28	Standard	545	70.0	32.0	12.2
Z1730-29	Test 1	539	68.2	32.0	11.7
Z1730-30	Test 2	501	67.9	34.0	11.5
Z1730-31	Test 1	550	71.3	31.8	12.5
Z1730-32	Test 3	556	71.3	31.1	12.3
Z1730-33	Test 1	543	70.2	31.6	12.0
Z1730-34	Test 3	522	66.7	32.3	11.2
Z1730-35	Standard	545	68.2	32.7	12.2
Z1730-36	Test 3	540	71.5	32.4	12.5
Z1730-37	Test 1	546	70.0	30.9	11.8
Z1730-38	Test 3	547	71.2	31.7	12.4

## 7.0 Development of New TCO Window Layers

The application of new types of TCO produced by reactive-environment hollow cathode sputtering to CIGS devices and modules is one of our innovative efforts during this final Phase. Using RE-HCS, we have produced high-quality films of ZnO:B, In<sub>2</sub>O<sub>3</sub>:Mo (IMO), In<sub>2</sub>O<sub>3</sub>:Zr, and In<sub>2</sub>O<sub>3</sub>:Ti (ITiO) [4, 13-15]. Representative properties of these materials are shown in Table 7.0. While conventional ZnO:Al has an electron mobility of 20-25 cm<sup>2</sup>/Vs, ZnO:B produced by RE-HCS has a mobility of 38 cm<sup>2</sup>/Vs, and IMO and ITiO films produced by RE-HCS have mobilities up to 80 cm<sup>2</sup>/Vs. All three of these latter films have an IR transmission superior to that of ZnO:Al.

Table 7.0. Properties of TCO films made by RE-HCS

Material	T <sub>s</sub> °C	t μm	T %	R <sub>sh</sub> Ω/sq	ρ 10 <sup>-4</sup> Ωcm	μ cm <sup>2</sup> /Vs
ZnO:B	110	0.44	96	17.8	7.8	37.8
In <sub>2</sub> O <sub>3</sub> :Mo	254	0.44	85	3.6	1.6	70.2
In <sub>2</sub> O <sub>3</sub> :Zr	250	0.56	87	4.0	2.3	63.3
In <sub>2</sub> O <sub>3</sub> :Ti	300	0.54	87	3.3	1.8	80.6

In Fig. 7.0 we show the optical transmission of an ITiO film (produced by RE-HCS) that is 545nm in thickness. The carrier concentration is 4.25 x 10<sup>20</sup> /cm<sup>3</sup> and the mobility 80.6 cm<sup>2</sup>/Vs, the resistivity being 1.8 x 10<sup>-4</sup> Ω cm. The latter properties are superior to those exhibited by ZnO:Al. Also shown in the figure are modeled curves of transmission for films having mobilities of 20, 50, and 80 cm<sup>2</sup>/Vs. Note that the transmission in the near IR increases with increasing carrier mobility.

Using films of ZnO:B and ITiO produced by RE-HCS as window layers on CIGS devices, we have so far achieved device efficiencies approaching 11% (see Table 7.1). The potential current

gain with ITiO was not fully realized as the deposition temperature had to be reduced below its optimal value (300°C or higher) in order to not damage the CIGS junction.

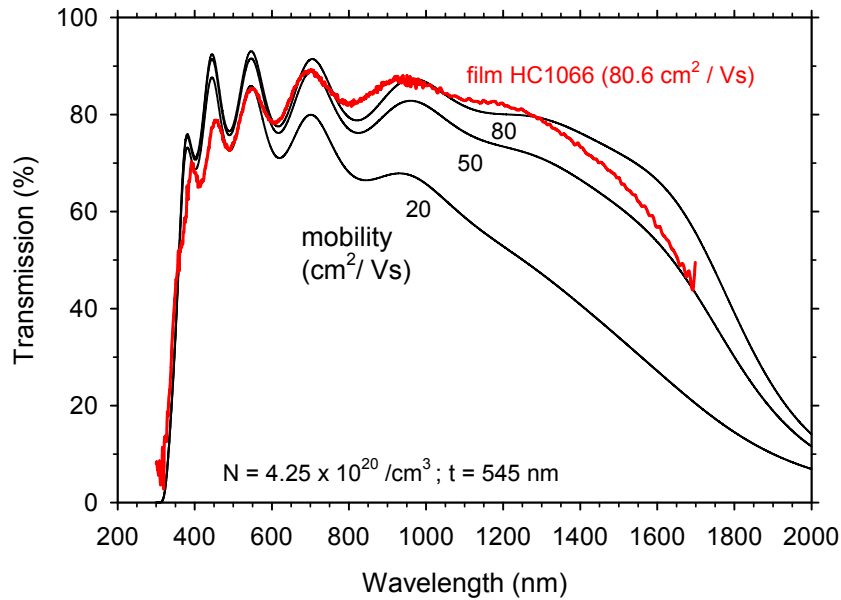


Fig. 7.0. Spectral transmission of a high mobility ITiO film and modeled transmission curves as a function of mobility.

Table 7.1. J-V parameters for cells with RE-HCS window layers

Structure CIGS/...	V <sub>oc</sub> mV	J <sub>sc</sub> mA/cm <sup>2</sup>	FF %	Eff %
CdS/i-ZnO/ZnO:B	564	27.3	70.7	10.9
CdS/i-ZnO/In <sub>2</sub> O <sub>3</sub> :Ti	565	28.4	66.8	10.7

A new, scaled-up hollow cathode system which can handle substrates having widths up to 45 cm is under construction. Most of the installation has been completed, and initial tests with a 12 cm cathode will take place soon.

## 8.0 Future Work

It is hoped that future work can address certain limitations of current CIGS technology. These limitations include module performance and production cost. Module performance is most strongly impacted by basic cell efficiency, and therefore further work to achieve high cell efficiency and more uniform large area deposition is warranted. Cost factors also cast a shadow over future high volume production. Cost can be reduced by simplifying the CIGS growth process, by reducing the thickness of the CIGS from 2.5 μm to 0.5 - 1.0 μm, by invention of a CIGS process that produces device-quality material at lower temperatures, by improved Se utilization, and by many lesser factors e.g. eliminating the need for ceramic targets for TCO production. The use of ultra-thin CIGS would also benefit from the development of a practical light-trapping scheme for CIGS.

## 9.0 Phase III Summary

Energy Photovoltaics, Inc.  
Advanced CIGS Photovoltaic Technology  
Subcontract No. ZDJ-2-30630-21

- Film qualities and device performances for CIGS films produced by the hybrid process (involving both thermal sources and sputtering) have been significantly improved by process optimization including adoption of a Cu-rich precursor, increase of selenization temperature, adjustment of bandgap profile and other parameters. As a result, 0.4 cm<sup>2</sup> devices with efficiency higher than 13% (NREL-verified) have been produced using the large area system Zeus.
- Materials property analysis of CIGS films including ICP, SEM, AES depth-profile, XRD, and activation energy were performed to help understand process parameters and to direct optimization.
- The large area deposition uniformity of the following layers was substantially improved: co-evaporated (In, Ga)<sub>2</sub>Se<sub>3</sub>, sputtered Cu, CBD CdS, and sputtered ZnO:Al.
- A thorough investigation of factors influencing the contact resistance between ZnO and Mo led to improved understanding and excellent interconnections.
- Further reduction of area loss due to patterning operations was realized.
- Dozens of large area modules (up to 4300 cm<sup>2</sup>) were produced in the power range of 20 W and above. The best module had a power of 26 W (under SRC), corresponding to an efficiency of 7.5%, as measured by NREL.
- Process controls are being emphasized at every process step, and a whole process and performance database is being established.
- New CIGS surface treatments are yielding very encouraging results.
- New types of TCO deposited by reactive-environment hollow cathode sputtering (RE-HCS) show excellent optical and electrical properties. In particular, very effective Ti-doping was demonstrated in RE-HCS In<sub>2</sub>O<sub>3</sub>, and electron mobilities of 80 cm<sup>2</sup>/Vs were achieved. The new TCOs have been applied to CIGS devices and show good potential.
- A laminated CIGS module has demonstrated excellent long-term outdoor stability and has slightly improved in power output after more than nine months exposure.
- Overall progress in devices and modules produced by the hybrid process during this subcontract is shown in the figure below.

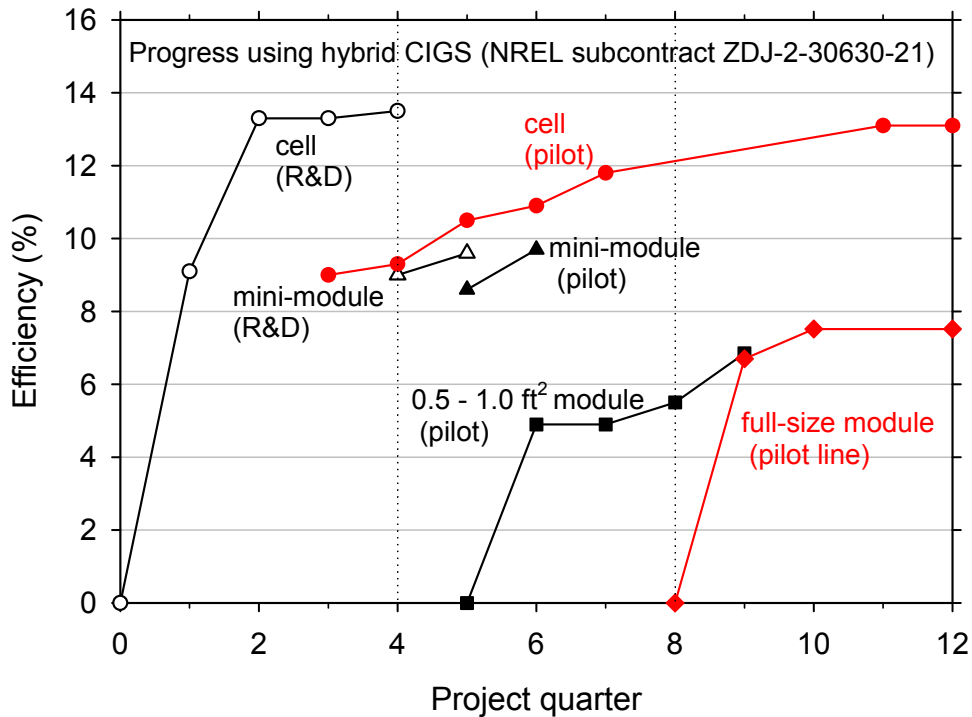


Fig. 9.0 Trajectories of progress with hybrid CIGS during subcontract ZDJ-2-30630-21

## ACKNOWLEDGMENTS

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