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# High Volume Manufacturing of Silicon-Film Solar Cells and Modules

## Final Subcontract Report
## 26 February 2003–30 September 2003

J.A. Rand and J.S. Culik
*AstroPower, Inc.*
*Newark, Delaware*

*Subcontract Report*
NREL/SR-520-38677
October 2005

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NREL Technical Monitor: R. Mitchell
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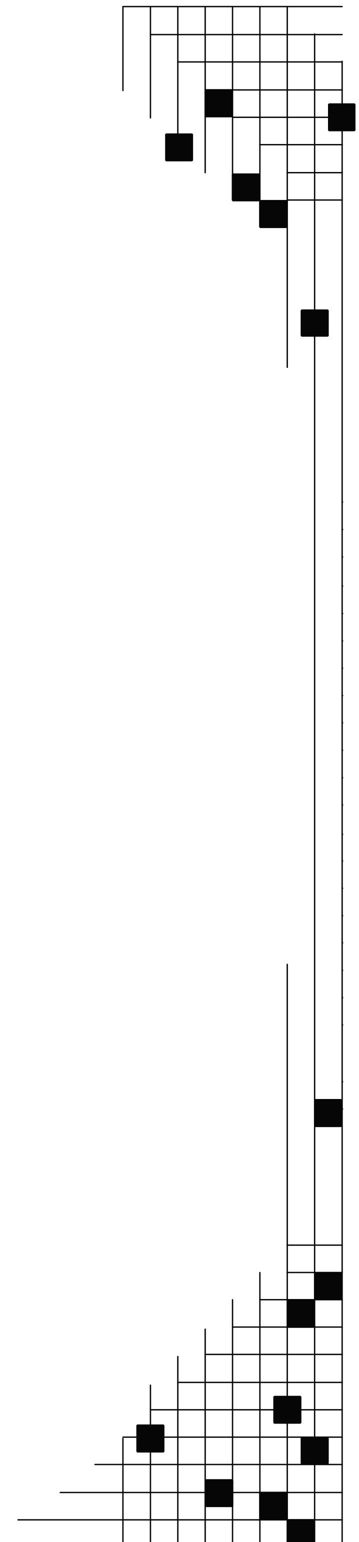

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# 1 Executive Summary

The objective of the PV Manufacturing R&D subcontract was to continue to improve AstroPower's technology for manufacturing Silicon-Film* wafers, solar cells, and modules to reduce costs, and increase production yield, throughput, and capacity. As part of the effort, new technology such as the continuous back metallization screen-printing system and the laser scribing system were developed and implemented. Existing processes, such as the silicon nitride antireflection coating system and the fire-through process were optimized. Improvements were made to the statistical process control (SPC) systems of the major manufacturing processes: feedstock preparation, wafer growth, surface etch, diffusion, and the anti-reflection coating process. These process improvements and improved process control have led to an increase of 5% relative power, and nearly 15% relative improvement in mechanical and visual yield.

Significant progress was made in reducing the amount of silicon consumed by the Silicon-Film process. The introduction of a near net shape wafer formation process has reduced the amount of silicon feedstock used per wafer by 40% and other developments in the feedstock preparation and wafer growth processes promise to further reduce the amount of silicon used per wafer by an additional 15%.

The Silicon-Film process has consistently demonstrated a high tolerance to impurities. Work has been done to understand the impact of impurities on device and growth performance. Experimentation has focused on tuning the growth parameters and optimizing getter sequences to reduce the detrimental effects of these impurities. To take advantage of Silicon-Film's high tolerance to impurities, efforts were made to upgrade metallurgical-grade (MG) silicon to a purity level needed for the Silicon-Film process through the continuous uni-directional solidification (CUDS) process.

Under the PV Manufacturing R&D subcontract a new large area module lamination manufacturing line with a new large area module tester was designed to accommodate the APx-140 modules. In order to reduce module defects, a more rigorous pre-lamination inspection system equipped with an IR inspection station was implemented and improvements in the module design have focused on reducing series resistance losses by increasing the crossectional area of the tabbing. On the system level AstroPower has developed a new method to mount large area APx-140 modules, which promises to be lower cost and more aesthetically appealing than the typical rack mount system.

* Silicon-Film is a trademark of AstroPower, Inc.

# 2 Continuous Large-Area Silicon-Film Solar Cell Processing

## *2.1 Single-Thread Silicon-Film Solar Cell Production Line*

The Single-Thread Silicon-Film solar cell production line is designed to rapidly apply advanced Silicon-Film manufacturing technology to production. Key initiatives include: reducing process time, reducing work in progress, and maximizing mechanical yield. This will be achieved by introducing new technologies that will simplify process sequence, perform in-line real-time monitoring, and minimize wafer handling. The fundamental design principles of the Single-Thread Silicon-Film production line include:

- Maximized electrical yield
- Minimized energy consumption
- Minimized environmental impacts
- Simplified processes
- Improved operator safety
- Improved in-line monitoring
- Easily replicated production units
- Modular production systems that tolerate change
- Eliminated use of plastic cassettes
- Reduced wafer handling
- Single line output of 1500 wafers per hour

The design included three process "modules" located in a 100,000 sq-ft facility with enough utilities to accept at least three paralleled solar cell production lines plus two laminate/module production lines. Within each solar cell process module, there are process sub-modules that are designated as follows:

- Module A1—Caustic surface etching
- Module A2—Junction diffusion

- Module B1—Diffusion oxide etching
- Module B2—PECVD silicon nitride coating

- Module C1—Contact printing and firing
- Module C2—Electrical testing, sorting, visual inspection, packaging

Figure 1. Single-thread Silicon-Film production layout. Lines highlighted in gray indicate the designated locations for future equipment.

The layout (Figure 1) is designed to accommodate the needs of manufacturing to maximize electrical, mechanical, and visual yield. Therefore, it is important that the layout is designed such that work in progress (WIP) and material transfers can be properly managed. There are two types of material transfers between individual process modules and process sub-modules. First, there are critical transfers that should happen immediately. For example, once the wafers are surface etched, they should be diffused as soon as possible so that surface re-contamination is minimized. Therefore, Process Module A1, surface etching, is arranged to flow directly into Process Module A2, junction diffusion. For non-critical material transfers such as the transfer between diffusion and oxide strip (Process Module A and Module B), the equipment can be located a sizable distance apart to permit future expansion of parallel solar cell production lines. This arrangement maximizes facility flexibility as the Silicon-Film solar cell processes mature. In addition to process flexibility, by arranging the processes in this manner

some accumulation of material (WIP) ahead of Module B is possible to allow for differences in operational rates between the process modules.

The manufacturing technologies discussed in the remainder of this section were designed based on the concepts of the single thread production design.

## *2.2 Continuous Non-screen Printed Back Metallization System*

In an effort to increase throughput and lower manufacturing cost, the task was undertaken to develop new methods of applying metals to solar cells. The back of the cell has the least demanding metallization pattern, so this was addressed first. Consequently, a proprietary roller print technology that is capable of printing both the silver back contact stripes and the aluminum on APx-8 solar cells was developed.

With this new ink application method, a solar cell is inserted into the automated machine front side up and the silver or aluminum ink is applied to the back surface of the cell. The cells are then transported to a belt that uses a manifold of perforations that release hot air to dry the ink. The same process is used to apply the silver stripes and the aluminum to the back of the cell.

This alternative print technology offers several advantages. For example, it is expected that the production version of this new printer will demonstrate a higher consistent throughput than can be achieved with typical low cost screen printers. A current prototype manually loaded printer is capable of processing 1200 wafers per hour, and future automated generations of this machine are expected to process over 1500 wafers per hour.

In addition, this new print technology uses less floor space than screen printing. Screen-printed wafers require two printers (one for back contact and one for aluminum back) and two furnaces for drying these inks. The new printer is designed to replace both screen printers and one drying furnace with a six-foot long footprint. With the development of new ink systems, there is the potential to remove the second drying furnace as well. This simplified processing also eliminates the need for use of cassettes and eliminates operator handling, which together reduce the probability of wafer breakage.

Most importantly, the new printer requires much less downtime for problems and preventative maintenance. There are no consumable parts such as screens that need to be regularly replaced. If a wafer breaks during printing, the machine is robust and can virtually not be harmed by a broken cell unlike screens, which can easily rip. Additionally the system includes an automatic ink feeding system, enclosures to capture any emissions, and it is compact enough to be moved into and out of the process area.

The new print technology was tested and qualified through the prototype stage.

## *2.3 Automated Laser Scribing and Cell Breaking System*

AstroPower has long strived to increase solar cell size, with the plan to cut smaller cell sizes as needed at the end of the manufacturing line. Historically, that cutting was done with saws that had poor mechanical yield, required water cooling, and left cracked edges. An effort was undertaken to replace that process with a laser based system.

A new laser scribing system that has the capability to scribe 8" APx-8 wafers into one-third or one-half size cells was designed and installed. Cycle time is 30 seconds per five wafers or 300

per hour. This time could be further reduced and throughput increased with the implementation of an automated loading/unloading mechanism. Other issues with the laser, such as down time and scribe depth, have been addressed.

The main source of down time occurs from dirty optics. Debris from the planks and surrounding atmosphere adheres to the optics and can cause a reduction in the laser power. If not properly maintained, this debris can cause the objective to fail. An air curtain was installed over the protective lens in conjunction with a FUMEX exhaust system to prevent silicon build-up.

Several factors affect the scribe depth including laser power, dirty optics, focus, and thermal lensing. Laser power is directly proportional to the lifetime of the lamp. An inline power meter is used to monitor the laser power before the optics to determine if the bulb needs to be replaced or if the optics need to be cleaned. The focus of the laser beam is important for scribe depth and is changed via a micrometer located next to the objective lens. Poor focus will result in a poor scribe depth and can cause a decrease in the mechanical yield when snapping the wafers from the plank. With proper maintenance and setup of the laser system, the mechanical yield can approach 100%.

When compared to the saw, throughput is approximately half for the laser. However, we are guaranteed an accurately sized wafer every time. Preliminary testing indicates less mechanical yield loss with laser-scribed wafers versus gang-sawn wafers. This could be attributed to the large chips found along the edges of sawn wafers (Figure 2 and Figure 3).

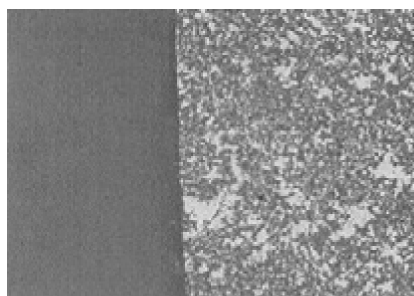


**Figure 2. Laser scribed—back side (typical).**

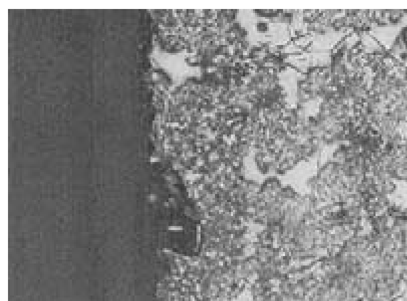


**Figure 3. Saw cut—back side (typical).**

It is clear that there is opportunity to further improve mechanical yield and throughput of the laser scribing process. Detailed specifications for a new automated laser scribing and cell breaking system for APx-8 Silicon-Film solar cells have been design fully developed. This specification document resulted in several concepts and designs for an automated system, including both in-line and rotary table systems. Design concepts included single YAG laser with servo-galvanometer beam steering, single YAG laser with beam splitters and wafer rastering, and multiple lasers. AstroPower is also working with outside vendors to develop an automated high yield, low cost system designed to mechanically break the wafers after laser scribing.

## *2.4 Performance and Yield of the PECVD AR Coating System*

The antireflection coating, ARC, for the APx-8 product was changed from spray deposited titanium dioxide to PECVD (Plasma Enhanced Chemical Vapor Deposition) deposited silicon nitride (SiN). PECVD equipment was acquired from Roth & Rau. This change has increased

the overall cell electrical performance by at least 8% due to the improved uniformity of the antireflection coating and the enhanced surface and bulk passivation by the silicon nitride layer.

Multiple improvements were made in the PECVD process. Initial steps were taken to develop a preventative maintenance schedule and optimize process settings for manufacturability and solar cell performance. Work was done to correct temperature non-uniformity, tune the plasma sources, identify the proper frequency for cleaning the equipment, and changing consumable parts such as O-rings and quartz tubes. Following these steps, multiple parameters having significant effects on the ARC properties were further studied (including belt speed, substrate temperature, gas flow ratio, and the microwave power profile). Many engineering hours were spent experimenting to identify a prime recipe that optimizes the index of refraction, thickness, and maximizes passivation.

Experiments were designed to test the impact of various parameters on performance. FTIR spectroscopy and ellipsometry measurements were used to evaluate the AR quality and composition, with RF lifetime, cell test and quantum efficiency (QE) data used to evaluate bulk passivation effects. These experiments helped in identifying a superior recipe and to narrow the process window defined by composition, thickness and refractive index, to maximize cell power.

Preliminary testing of the process window is represented by three samples with identical bulk characteristics that were run through the silicon nitride process at different times using the same recipe parameters. Ellipsometry was used to determine refractive index ‘n’ and the thickness ‘x’, and FTIR measurements were used to calculate the concentration of N-H and Si-H bonds. These parameters were measured before and after the fire through process (see Table 1).

**Table 1: Optical properties and passivation gain for three samples processed under different conditions.**

| | Before Fire through | | | After Fire through | | | Passivation Gain |
|---|---|---|---|---|---|---|---|
| **Sample** | **x (Å)** | **n** | **N-H/Si-H** | **x (Å)** | **n** | **N-H/Si-H** | |
| A | 874 | 2.09 | 0.43 | 859 | 2.08 | 0.28 | 3.8% |
| B | 1081 | 1.96 | 0.97 | 1024 | 1.99 | 0.66 | 8.6% |
| C | 883 | 2.04 | 0.7 | 880 | 1.95 | 0.38 | 0% |

The process window was narrowed following these initial tests. Improving maintenance scheduling, identifying and repairing equipment in need of reconditioning and making modest recipe modifications achieved higher consistencies. Ellipsometry is used in the manufacturing process to track ARC thickness, x, and refractive index, n, so that variations can be addressed. Figure 4 displays these parameters before and after the optimization of the equipment and process. Process parameters investigated included process time, temperature, gas flows, ratios, and plasma source power levels. The tail end of the ‘After Optimization’ data clearly indicates a need for maintenance.

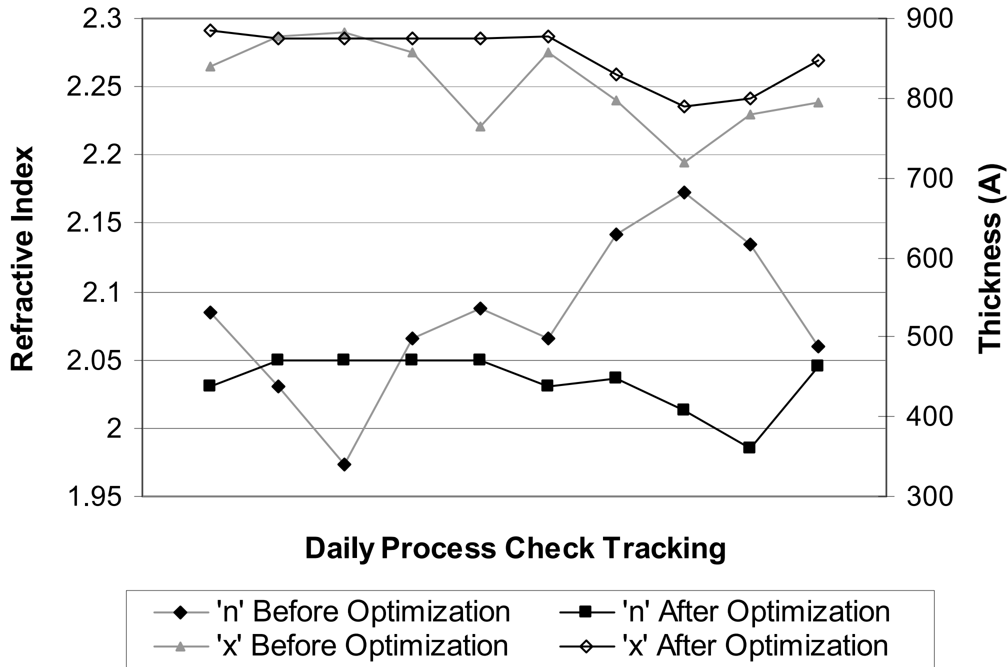
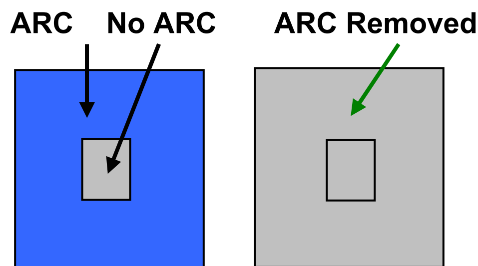



**Figure 4. Monitoring of index and thickness during the manufacturing process shows a narrowing of the process window following process and equipment optimization.**

Recent literature shows how process conditions greatly affect the optical properties and the level of bulk passivation [1, 2]. For this study, bulk passivation is defined as the gain in Isc achieved from the passivation that occurs from the silicon nitride deposition after optical effects are removed. The bulk passivation gain is measured by applying a silicon nitride coating, then removing the coating, and evaluating the quantum efficiency (QE) of the underlying device. This QE data is compared to the QE of a neighboring sample that never had silicon nitride applied. The experiment assumes that the bulk passivation effect will remain in place after the coating is removed. In all cases, theoretical Isc is calculated from the QE data. The illustration of the measurement areas and the quantum efficiency curves for sample C are available in Figure 5 and Figure 6.



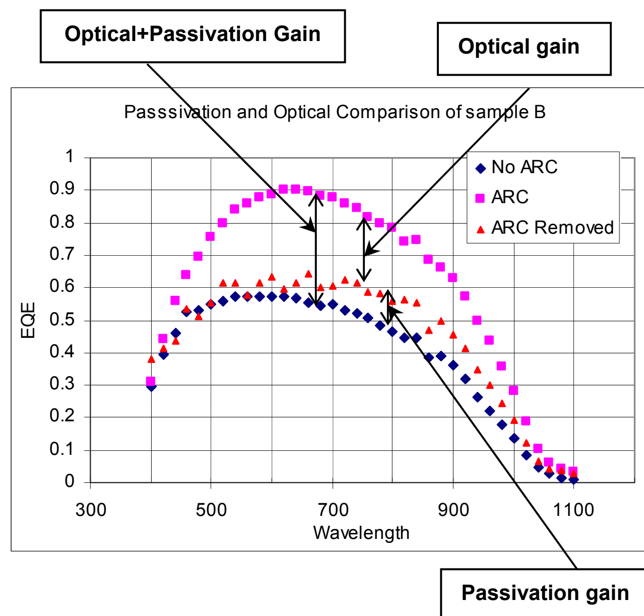




**Figure 5. Visual description of measurement area.**

**Figure 6. EQE curves for sample C indicating 8% Isc passivation gain.**

The work resulted in an estimated 8% boost in solar cell current, as indicated in Figure 6. Further work on process refinement is expected to bring the cumulative effect of a 15% boost in solar cell power.

Cell breakage at the silicon nitride AR step is generally very low. This is primarily due to the fact that this is not a high-temperature step and the processing is low impact. Breakage at this processing step has been under 0.3% for the last three consecutive months.

Improvements to the PECVD silicon nitride deposition equipment and process have resulted in improved visual and electrical yield. In addition, the throughput of the process can be maintained at 500 wafers per hour and the downtime of the equipment for preventative maintenance has been minimized.

## *2.5 Performance and Yield of the Alternative Metallization Sequence*

The antireflection coating for the APx-8 product was changed from spray-deposited titanium dioxide to PECVD deposited silicon nitride. Along with the move to the new AR coating, a change in the front contact metal sequence was evaluated. The historical front metal processing sequence was the following:

1. Post Diffusion Glass Etch
2. Back stripe (Ag) print and dry
3. Back contact (Al) print and fire
4. Front contact print and fire
5. TiO2 AR coat
6. Burnish contacts

In order to streamline the process, and utilize different front contact ink, a fire-through process was developed. The sequence is as follows:

1. Post Diffusion Glass Etch
2. PECVD SiN AR coat
3. Back stripe (Ag) print and dry
4. Back contact (Al) print and dry
5. Front contact print and fire

The fire-through process is simplified since it eliminates the contact burnishing step and it only has a single firing step. The process also has performance benefits including: better AR properties by firing the coating and higher fill factor through the use of a higher-profile ink. The fire-through process has improved mechanical yield due to the simplification of the process and the elimination of the contact-burnishing step.

## *2.6 Investigation of Alternative AR Processes*

Implementation of the PECVD silicon nitride process has been very successful; however, it would still be beneficial to develop a lower-cost, higher-throughput, safer process. Alternative, silane-free, AR coating techniques were evaluated on a lab-scale as potential future replacements for this process.

Experiments using an SiOx layer were performed to evaluate its use as a potential substitute for the PECVD SiN process. The SiOx layer was grown by an outside supplier using their proprietary process. This breakthrough process involves the room temperature fast growth of SiOx films on silicon substrates. The oxide growth could be performed on cells that already had metal contacts in place. The oxide growth process could selectively etch back the silicon that was not protected by metallization; therefore, a cell with high blue response and good contact resistance could be achieved. After a few iterations of processing experimental cells, this process yielded solar cells and modules with relatively good efficiency. Unfortunately, when the modules containing these cells were thermally cycled to simulate environmental stress, the modules severely delaminated and lost significant power. The pursuit of developing this technology was abandoned because this fundamental limitation could not be overcome.

Test cells processed with SiC as an AR coating were also evaluated. The SiC was applied by chemical vapor deposition by an outside supplier. This experimental attempt yielded solar cells with a non-uniform coating and low efficiency, however this was only a preliminary attempt and greater success is expected in subsequent trials. Unfortunately, even if a high performance AR coating is achieved, CVD or PVD (Physical Vapor Deposition) SiC coating methods have not yet proven their ability to passivate Silicon-Film wafers. Downstream plasma technology is therefore being evaluated as a possible method for high-volume passivation prior to any SiC coating step. A heated vacuum test chamber is being constructed to mate with an MKS ASTeX downstream plasma chamber. The MKS plasma chamber is designed and marketed for semiconductor fluorine gas cleaning of process chambers, but theoretically will work equally well in ionizing H2 gas. The process chamber would hold several Silicon-Film wafers at an elevated temperature and be flooded with H+ ions provided by the MKS unit.

# 3 Solar-Grade Silicon

The Silicon-Film process has demonstrated a high tolerance to impurities. This tolerance is based on the near-ideal directional solidification that occurs during the growth process and the engineering of impurities in the final wafer. To fully capitalize on these benefits, work was carried out to upgrade metallurgical-grade (MG) silicon to a purity level needed for the Silicon-Film process.

Work was performed in three areas. One was the development of a continuous, uni-directional, solidification process (CUDS). The process was designed to deliver a directional solidification step in addition to the one experienced in the sheet making process. The other two areas of work involved phosphorus and boron removal explicitly.

## *3.1 Continuous Uni-Directional Solidification Process*

**Background**

Prior to the start of the PV Manufacturing R&D subcontract, a pilot scale CUDS system (Figure 7) was built. This system had the capability to process 5-kg ingots through a melting and recrystallization process. Impurities were then removed by sawing off the last to freeze areas. This established a baseline for purity levels that could be reached with directional solidification alone; these baseline impurity values are shown in Table 2. The data shows that although Al and Ca were sharply reduced, levels of the critical B and P remain largely unaffected.

**Figure 7. Pilot CUDS system.**

**Table 2: Impurity levels before and after purification by directional solidification.**

| | Si Before (ppm) | After Run 1 (ppm) | After Run 2 (ppm) | After Run 3 (ppm) |
|---|---|---|---|---|
| **Al** | > 133 | < 0.1393 | 0.697 | 0.1924 |
| **B** | 7.33 | 7.33 | 7.17 | 7.39 |
| **Ca** | > 354 | 0.385 | 0.698 | 0.527 |
| **Fe** | 26 | < 1.07 | < 1.072 | < 1.069 |
| **P** | 12.4 | 9.15 | 9.17 | 9.11 |
| **Ti** | 2 | < 0.795 | < 0.797 | < 0.795 |

## *3.2 Laboratory-Scale Purification System*

In 2001, another furnace was developed to carry on CUDS experiments (Figure 8). The lab-scale furnace is a closed system, containing only one crucible and ingot at a time. Since it only had one ingot in it at a time, it was very easy to accurately control the growth profile and study different gas chemistries, without worry of synergistic effects of other crucibles and ingots.

AstroPower used this lab-scale system to develop the CUDS "pouring" technology. Faced with scaling the directional solidification process to industrial levels, it was realized after analysis that accurately sawing off all the highly concentrated contaminants from the top of an ingot would be both costly and wasteful. Experiments were performed to demonstrate that molten silicon could be removed by pouring as part of the directional solidification purification process. Pouring had the effect of removing the most impure material, without an opportunity for back diffusion. Additionally, it was shown that the remaining clean silicon could be remelted and separately poured from the system, thus homogenizing the clean silicon and removing it without the need for a release coating. This important development work was the precursor to the development of the production scale system.

Many split lot experiments were run between the static CUDS system (where impurities were removed by sawing) and the pouring system. The silicon produced in the pouring process always outperformed the silicon from the static system in terms of purity and in terms of the resulting solar cell performance after processing into Silicon-Film solar cells.

**Figure 8. Lab-scale purification system.**

## *3.3 Experimentation with Intentional Introduction of Impurities*

In an effort to develop a specification for silicon feedstock for the Silicon-Film program, an effort was begun to measure the impact of impurities on solar cell performance. This effort is a necessary precursor to developing an upgraded metallurgical grade silicon product. To carry out this study, well-controlled impurity concentrations are introduced to the sheet making process. The Silicon-Film process has the benefit of being able to carry out these studies at low cost by involving only a small quantity of material at a time.

**Experimental Results: Common Impurities**

A wide range of impurities occurring in the raw material handling facility at AstroPower, were selected for evaluation by this process. The impact to performance and mechanical yield were measured. In general sodium and calcium compounds cause growth defects with chloride salts being the most detrimental and oxides being acceptable in larger concentrations (notable exception is sodium bicarbonate which causes no significant growth defect up to 100ppmw), Aluminum oxide and clean silicon dioxide cause no growth problems, but Al2O3 does release Al for doping. CaCl2 is very detrimental in very small quantities (1ppmw); <100ppb causes problems in conjunction with high SiOx).

**Experimental Results: Transition Metals**

Recent work has focused on developing detailed specifications for silicon feedstock based on upgraded metallurgical grade (UMG) silicon. We have focused on the behavior of transition metals as well as B and P. We have shown strong segregation effects during our sheet growth, which allows us to tolerate comparatively high levels of transition metals. For testing purposes, silicon was produced by melting clean silicon in a crucible and intentionally contaminating it with common transition metals, B, and P. The contaminated material was then used to determine

the impact of each impurity, as well as their interactions, on the final SF solar cell performance. Figure 9 shows the distribution of Fe throughout the thickness of a SF wafer after 100ppmw of Fe was introduced. It is apparent that Fe has segregated to the back and to a lesser extent the front of the wafer where it can easily be removed.

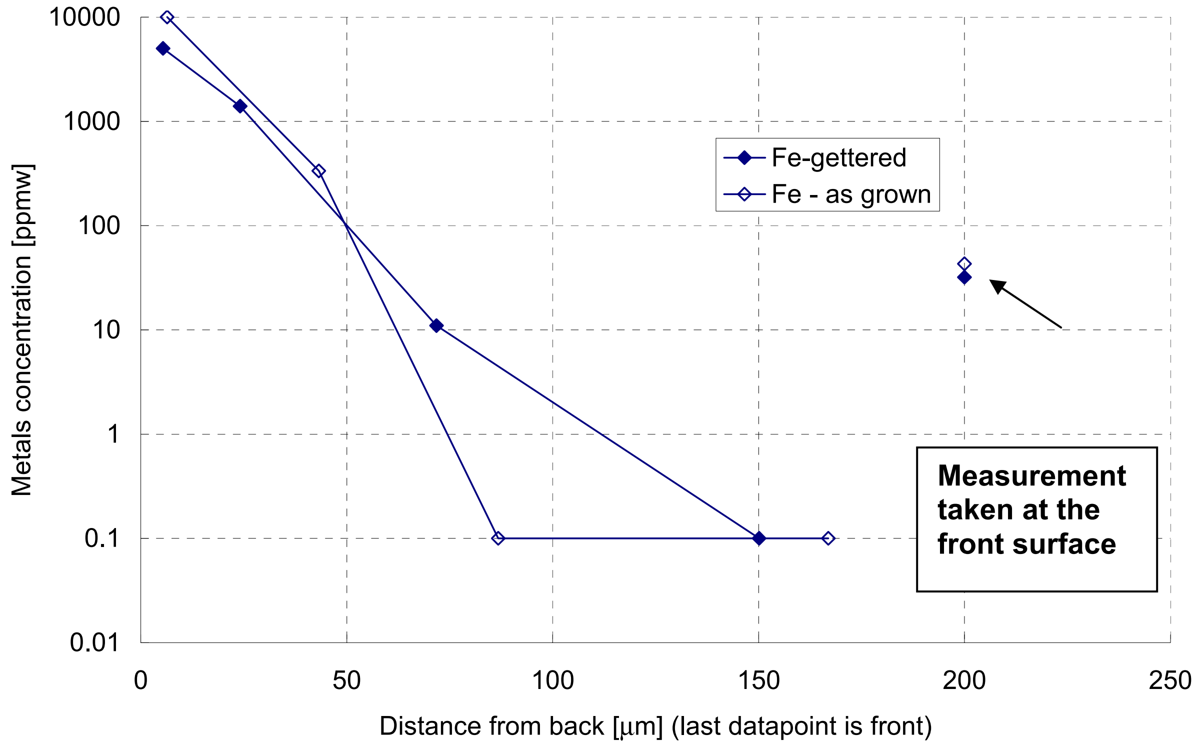



**Figure 9. Fe concentration vs. depth in SF wafer as measured with ICP-OES. The SF wafer was fabricated with silicon intentionally contaminated with 100 ppmw Fe.**

Intentional doping experiments have been carried out with Fe, Al, Ti, Cu, and Ni. Only Ti shows significant impact on performance (Figure 10). We have repeatedly found that 10s of ppm of Fe and or Cu lead to no reduction in performance and in many experiments result in a small (statistically insignificant) increase in performance (Figure 10). Future work will focus on boron and phosphorous as well as on interactions between transition metals, dopants, and dielectric contamination (N, O).

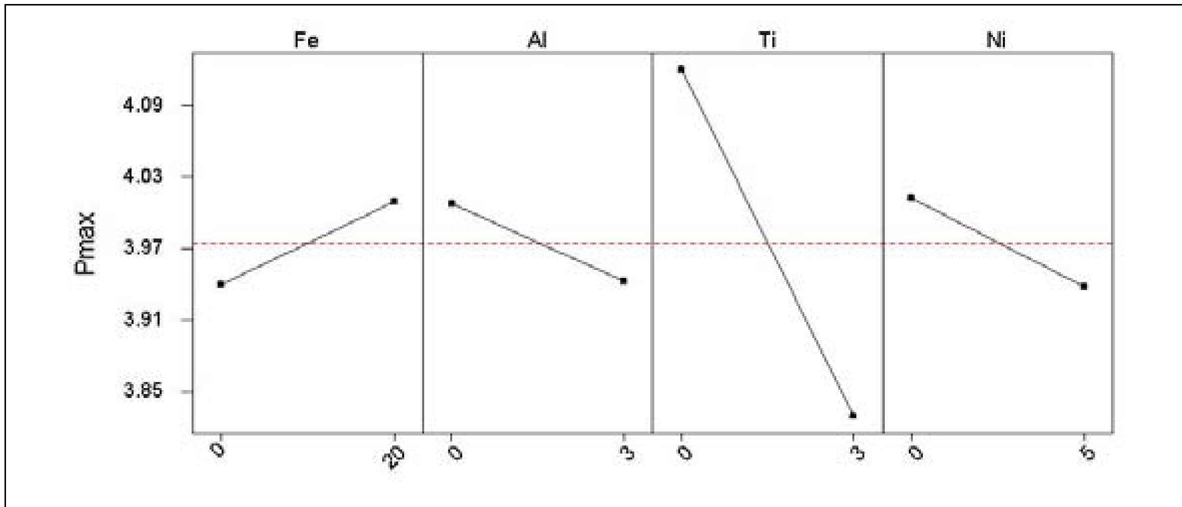



**Figure 10. A main effects plot for solar cell maximum power (Pmax) as a function of impurity level (impurity levels are shown in units of ppmw).**

# 4 Process Monitoring for In-Line Processes

Statistical process control for process monitoring is used in nearly every step in the Silicon-Film process. The SPC practices that have recently been implemented have resulted in substantial yield improvements over the past six months. Table 3 contains a list of all the general parameters that are monitored in the Silicon-Film process.

**Table 3: Parameters that are monitored and controlled in the Silicon-Film Process.**

| Process | Parameter |
|---|---|
| Powder Specification | |
| | Partical size |
| | ICP impurity analysis |
| Wafer Growth | |
| | Bulk resistivity |
| | Wafer weight |
| | Wafer thickness uniformity |
| | Mechanical Defects |
| In-line Surface Etch | |
| | NaOH concentration |
| | SiOx concentration |
| | Bath temperature |
| | Silicon removal |
| Diffusion | |
| | Sheet resistivity |
| | Phosphoric acid flow rate |
| Post Diffusion Anneal | |
| | Sheet resistance |
| Oxide strip | |
| | Wafer hydrophobicity |
| | HF concentration |
| PECVD Silicon Nitride | |
| | Layer thickness and index of refraction |
| | FTIR Spectroscopy |
| | Visual quality |
| Aluminum back | |
| | Ink weight |
| | Visual print quality |
| Front Ink | |
| | Gridline thickness and height |
| | Ink adhesion |
| | Visual print quality |
| Overall Monitoring | |
| | Electrical performace (Pmax, Isc, Voc, FF) |
| | Visual quality |
| | Mechanical breakage |

Recent work specifically focuses on the statistical process control methods used to monitor the *major* manufacturing processes: feedstock preparation, wafer growth, surface etch, diffusion, and the anti-reflection coating process.

## *4.1 Feedstock Monitoring*

**Particle Size Analysis**

For successful wafer growth, it is important that the size of the silicon particles used in the Silicon-Film feedstock powder are uniform and within a certain size specification. A particle size analyzer is used to determine the particle size distribution. The analysis produces a histogram of silicon particle size. Three points are recorded for each measurement based on the histogram data:

- D10—10% of the particles are smaller than this size
- D50—Distribution mean – 50% of the particles are smaller than this size
- D90—90% of the particles are smaller than this size

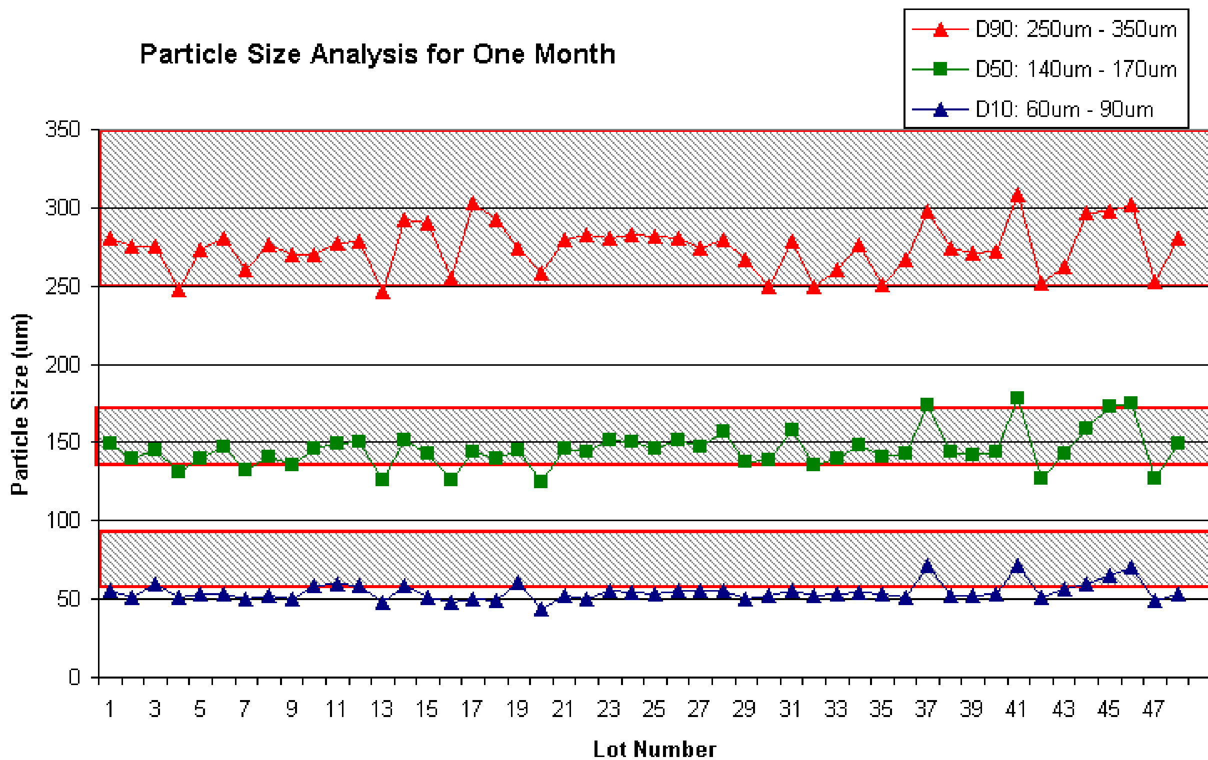



**Figure 11. Data from the particle size analyzer for production data.**

Figure 11 shows powder samples for one month. The control limits are placed on these three parameters determine whether the particle size is suitable at the low, middle, and high end of the distribution. The feedstock is sampled and particle size distribution is measured at least once for each run. In addition, if sheet growth problems spontaneously occur, the particle size distribution is one of the first parameters inspected.

### Impurity Concentration Monitoring

It is important to control the impurity levels of certain elements in the Silicon-Film feedstock. High levels of these impurities can impact cell performance as well as wafer growth and mechanical yield. Limits to these impurity levels have been determined by thorough experimentation. Table 4 provides a list of the impurities that have been discovered to have an effect on wafer growth or cell performance.

**Table 4: Monitored impurities and measurement techniques**

| Impurity | Measurement |
|---|---|
| Calcium | GDMS |
| Copper | ICP-OES |
| Phosphorous | GDMS |
| Boron | GDMS |
| Iron | ICP-OES |
| Carbon | LECO C-200 |
| Oxygen | LECO TC-436 |
| Aluminum | ICP-OES |
| Nickel | ICP-OES |
| Titanium | GDMS |

Currently in-house measurements are made with the Inductively Coupled Plasma – Optical Emission Spectroscopy (ICP-OES) system. Currently the ICP-OES measurement is performed "in-line" on a sample of every batch of raw silicon feedstock before it is processed. If any impurity is detected to exceed the maximum purity spec, the feedstock is rejected. ICP-OES measurements are also periodically performed on as-grown wafers to detect impurities that may be introduced during the wafer growth process.

The ICP-OES tool is limited in that it is not capable of measuring carbon or oxygen. In addition, the measurement resolution is not sensitive enough to detect the lower limit of detrimental levels of titanium, calcium, boron and phosphorus. Therefore, the system for in-line feedstock monitoring based solely on ICP measurements is by no means complete. In order to provide a full analysis of the feedstock, the use of other measurement techniques such as Glow Discharge Mass Spectroscopy (GDMS) and nitrogen/oxygen determination (carried out on LECO Corporation equipment) were necessary. These measurements are not available in house, and due to the expense and lengthy turnaround time they are currently only used on an experimental basis.

In conclusion, the purity limits for Silicon-Film feedstock are still under investigation. To date it has been determined that certain elements that segregate well such as Fe and Cu have very high tolerance limits. We have also found that some compounds such as those with Ca and Na impact wafer growth, but not solar cell performance. The resounding conclusion from our experimentation and characterization is that the purity required for feedstock for the Silicon-Film process is far more lenient than for any conventional Cz, ribbon, or casting process.

## *4.2 Wafer Growth Monitoring*

There are a number of parameters that are control charted for wafer growth process monitoring. Control limits for these processes have been developed by using historical performance data. These parameters are reviewed as the wafers are processed in real time, which allows for immediate reaction to the wafer growth process if parameters are significantly out of control. The parameters monitored are wafer resistivity, wafer weight, edge-to-edge thickness variation, and width-length deviation.

The data is monitored in real time by operators and is reviewed by the engineering group after the conclusion of each run. This data highlights the gradual process drift and can be correlated to any shift in mechanical or electrical data. Figure 12 and Figure 13 are examples of the charts that are reviewed at the conclusion of each run.

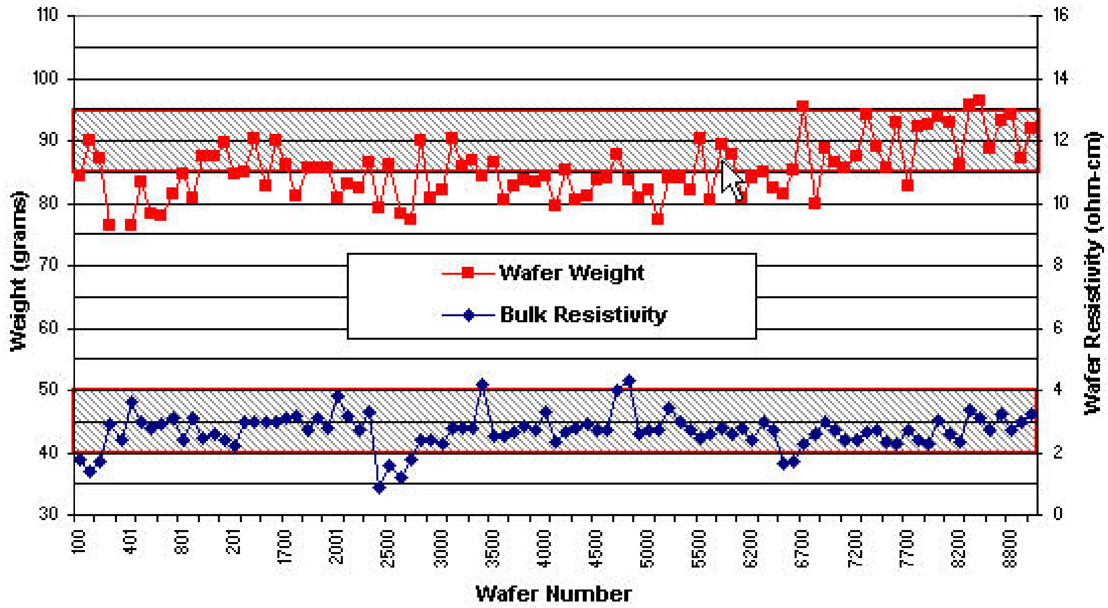



**Figure 12. Control chart of weight and bulk resistivity for one Silicon-Film Run with control limits shown.**

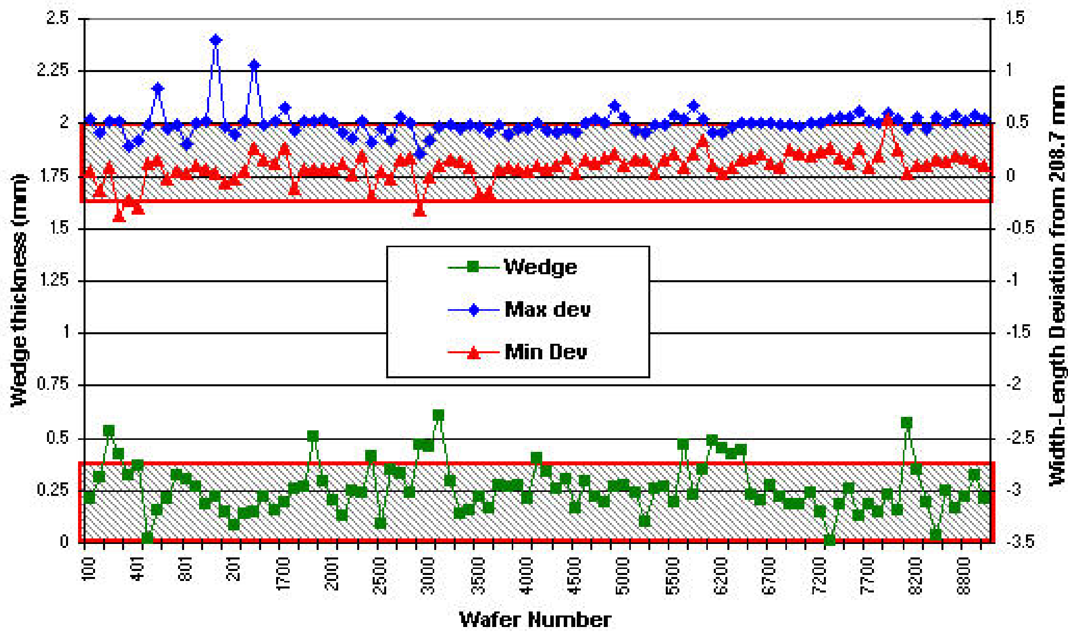



**Figure 13. Control chart of wedge thickness and target width and length for one run with control limits shown.**

### *4.3 In-line Surface Etch Monitoring*

There are a number of parameters that are monitored in-line in the sodium hydroxide etch process; bath temperature; NaOH concentration and silicate concentration. The most important parameter to monitor is the percent concentration of sodium hydroxide by weight. To measure this parameter, a titration is performed on small sample taken from the etch bath once or twice per shift. Figure 14 displays % NaOH concentration for one month of processing.

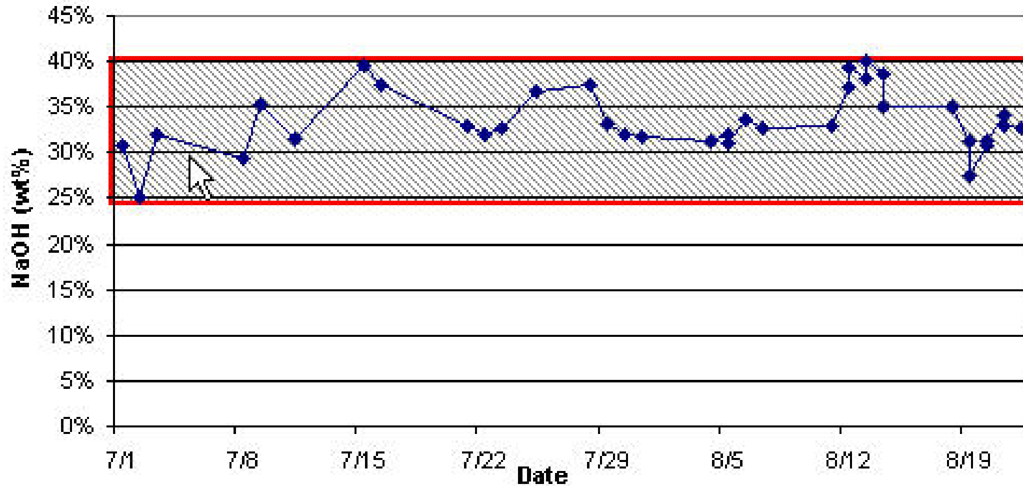



**Figure 14. Daily titration results for tracking NaOH by wt% with control limits shown.**

NaOH concentration is important to monitor so that we can control the etch rate and the etch quality. If this parameter goes out of control, this can affect visual and electrical yield. If the concentration is out of control or is on a trend to be out of control for more than three consecutive measurements an out of control action plan is immediately initiated. The action plan involves investigation of the age of the bath, replenishment rate, temperature, bath level, water dilution rate, and concentration of incoming raw material to troubleshoot the incident.

The temperature of the etch bath is also important to monitor because this has a similar effect on etch rate and etch quality. The target bath temperature is 110 C and the bath temperature is managed by a feedback loop controlled heating system, however the temperature still fluctuates +/- 3C due to variability of the caustic/silicon reaction. The temperature variability is monitored in real time on a periodic basis by the in-line surface etch operators. If the temperature variability exceeds this limitation, appropriate corrective actions are immediately taken such as lowering the caustic levels in the chamber, checking for poor circulation, and troubleshooting heater functionality.

The silicate concentration is monitored periodically because it can vary significantly with bath replenishment rate and the load of wafers going through the machine. High concentrations of silicates have been known to cause detrimental effects to the visual yield and may affect cell electrical performance. It is also critical to maintain silicates within specific limits to avoid solidification of precipitates in piping, pumps and heaters. Figure 15 shows weight percent silicate concentration for the month of July.

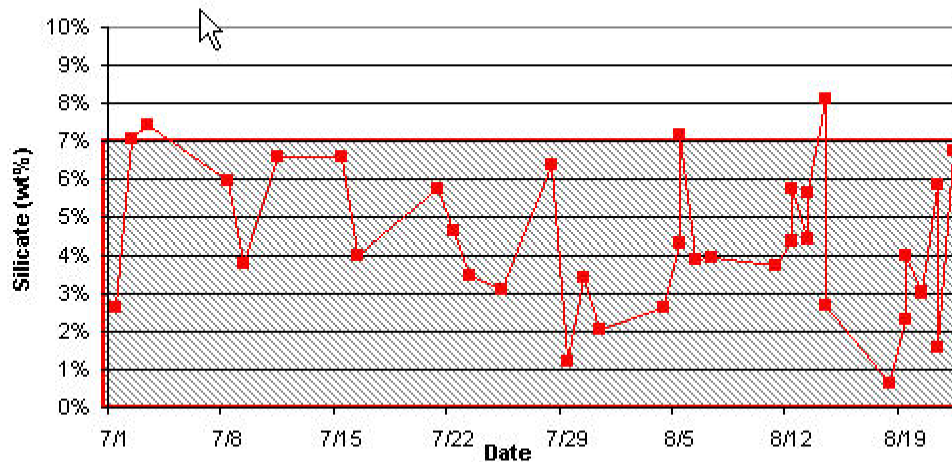



**Figure 15. Daily titration results for monitoring of silicates by wt% with control limits shown.**

When the silicate concentration goes above 7% for two consecutive readings, an out of control action plan is initiated. This plan involves actions that need to be taken to reduce risks associated with the increased silicate levels. For instance, an increase of 7% at the beginning of the five-day bath cycle would indicate fluid circulation and replenishment problems and the process would be shutdown for further investigation.

Since NaOH concentration and temperature both affect etch rate it is difficult to control both parameters at the same time. A third data point, grams of silicon removed (Figure 16), is the most straightforward measurement to determine the amount of Si that is etched. Again, when the amount of Si removed goes out of control or is trending out of control, the appropriate out of control action plan is initiated.

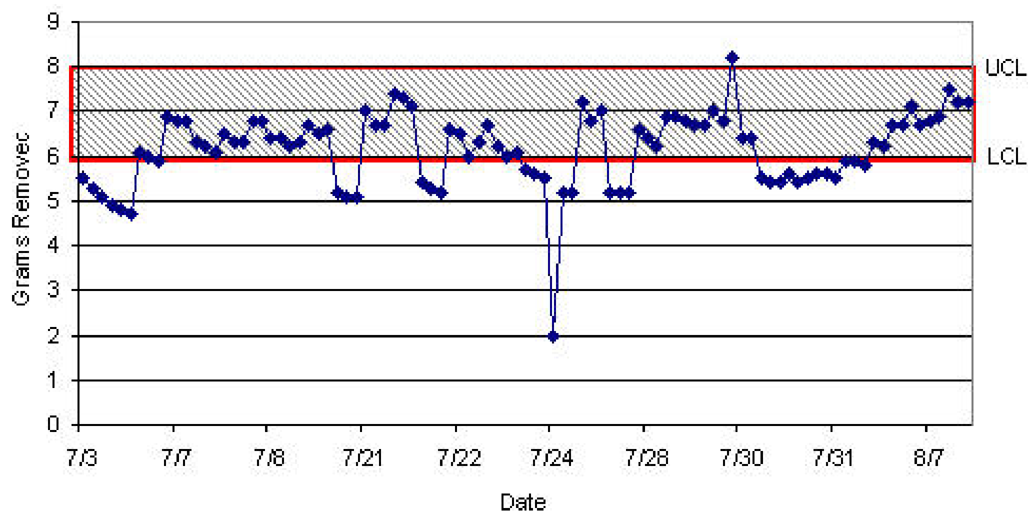



**Figure 16. Daily tracking of grams of silicon removed for in-line surface etch process.**

Through utilization of the process monitoring for in-line surface etch control, we have been able to react to problems and prevent reoccurrences of these problems. This has directly resulted in reduced downtime and reduced variability within the process.

### *4.4 Diffusion Monitoring*

The four-point probe sheet resistance measurement is used inline to monitor the diffusion process. Approximately one wafer is sampled and measured out of every 50 production wafers. It was determined that the best charts to use to track and control the sheet resistance measurements are the X-bar and R charts. The X bar charts allow production to control the variability of sheet resistance wafer to wafer over a period of time. The R chart allows production to control the variability of sheet resistance within a wafer over a period of time. The sheet resistance measurements are monitored in real time by operators who run the diffusion furnace. Operators are given rules to determine when the process is out of control and they react accordingly. In addition, the sheet resistance data is reviewed by engineering on a daily basis to ensure that process drift and excursions are identified.

### *4.5 AR Process Monitoring*

A silicon nitride anti-reflection (AR) coating is deposited on Silicon-Film cells using a Roth & Rau PECVD system. The two fundamental material properties central to obtaining good AR coatings are the index of refraction and the coating thickness. Multiple input parameters on the ARC tool can be adjusted to change these AR film characteristics. Some of these settings include belt speed, substrate temperature, gas flow ratio, and the microwave power profile. Ellipsometry measurements correlated with cell output power were used to define the tool settings that deliver the optimal thickness and refractive index. Optimization activities were covered earlier in the section titled “Performance and Yield of the PVCVD AR Coating System”.

For process monitoring, ellipsometry data is taken 2–3 times per shift to identify process deviations and trends. For instance, in July 2003 we were able to observe how the age of the O-rings and quartz tube plasma sources affect index of refraction and thickness (see Figure 17). The subsequent study determined the maximum effective O-ring and tube lifetime to be 48 hours.

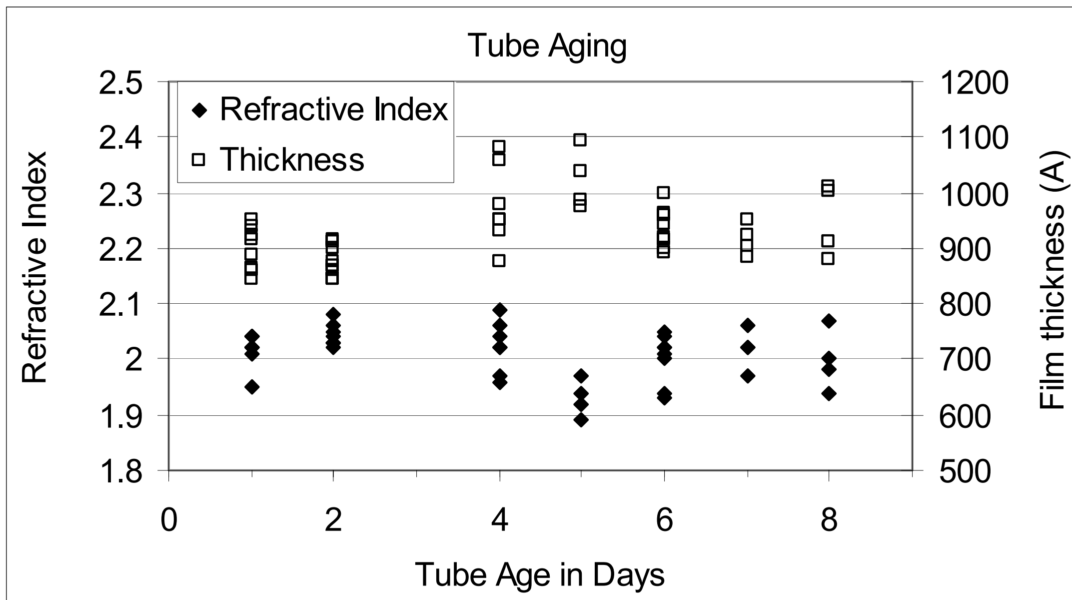



**Figure 17. Refractive index and thickness vs. tube age.**

Measuring index of refraction and thickness of the AR coating to evaluate quality is not enough to monitor the process. SiN AR is also responsible for providing bulk passivation of the Silicon-Film material. Material properties and thickness of the AR coating determine the resulting refractive index and correlate with the effectiveness of the bulk passivation. To improve our analysis capabilities, AstroPower implemented new analytical tools and strategies. The Fourier Transform Infrared Spectroscopy (FTIR) tool is used to evaluate the material properties of the silicon nitride layer. FTIR enables us to track [Si-H], [N-H] bond concentrations and [H] concentrations. This data is then used with the refractive index, film thickness, and cell performance data to develop an understanding of how composition of the thin-film layer affects index of refraction and bulk passivation.

While our initial FTIR work has been fruitful for better understanding the material properties, we believe it could also prove to be useful as an in line quality control measurement. Unfortunately, current FTIR processing is still somewhat time consuming and difficulties in curve fitting limit the translation of compositional analysis. With streamlining of the current FTIR measurement process, and upgrading the software, a system could potentially be implemented for in-line monitoring.

In order to monitor visual defects, every cell is visually inspected post silicon nitride processing. Typical defects include red areas or light areas on all or part of the cell, sliver specs or spots, and areas where the coating has flaked away. These defects are logged and charted, and if there is a large incidence of defects, engineering will react. Typically, about 3–5% of all cells that are manufactured have a visual defect caused by the silicon nitride deposition process. This high fallout is being reduced thanks to improvements in temperature uniformity within a cell and from cell to cell, as well as the introduction of a more rigorous preventative maintenance schedule.

## 4.6 *Process Improvements and Yield Improvements Due to SPC Monitoring*

Implementing statistical process control practices has helped to improve electrical, visual, and mechanical yield. Evidence of this fact is in the following charts (Figure 18, Figure 19, and Figure 20) that illustrate the improvement in these areas over a period of months.

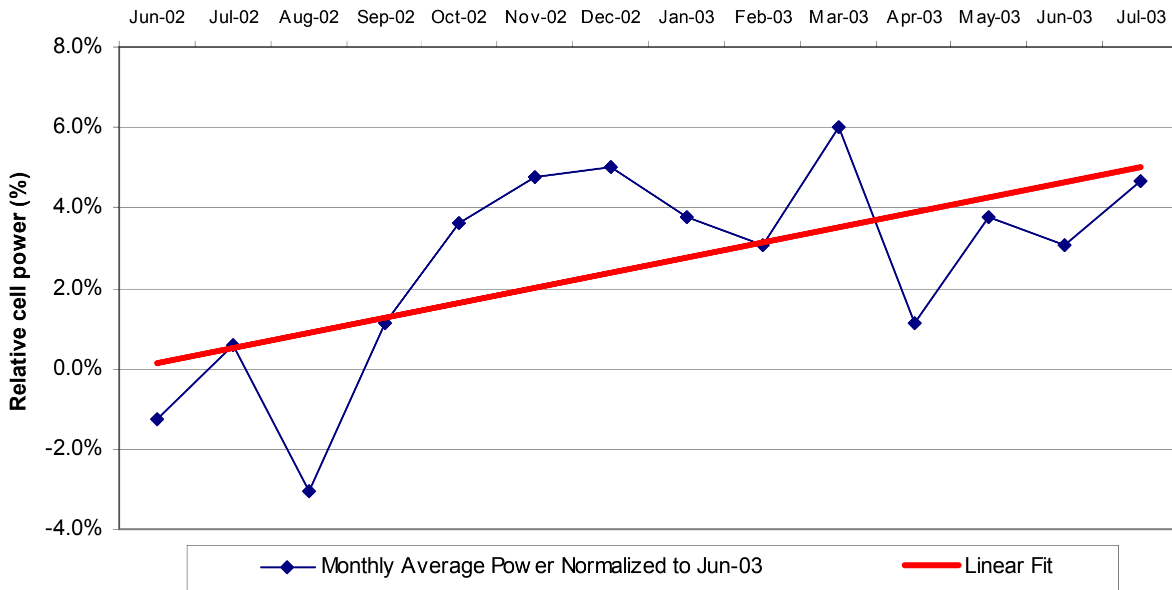



**Figure 18. Relative cell power by month—Improvement 5% relative cell power over one year.**

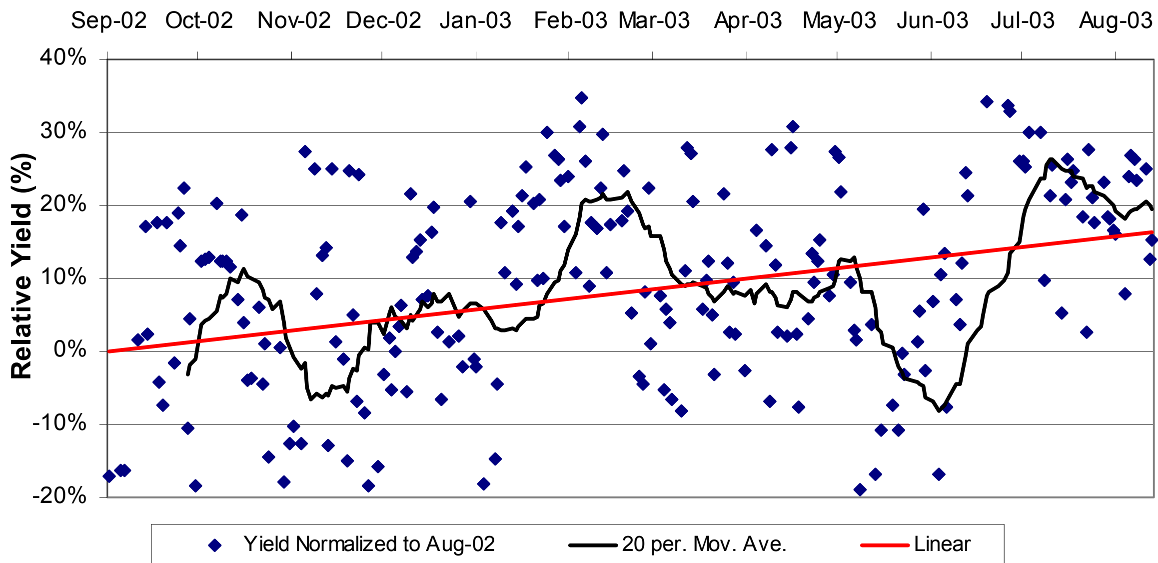



**Figure 19. Visual yield—Improvement 15% relative yield over one year.**

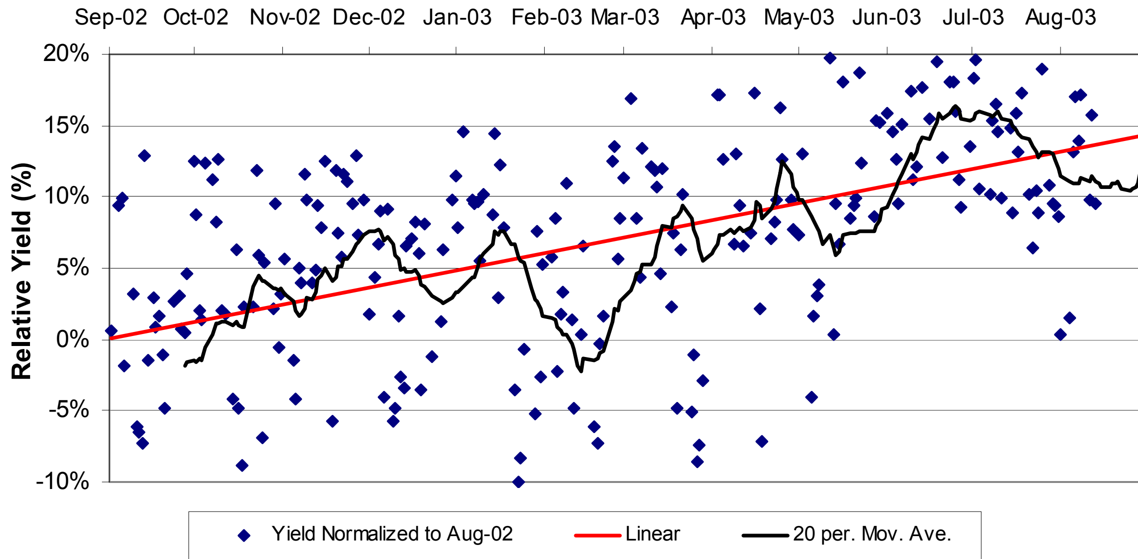



**Figure 20. Mechanical yield—Improvement 14% relative yield over one year.**

# 5 Increase Silicon Utilization and Throughput

Recent efforts to reduce the amount of silicon consumed by the Silicon-Film process have significantly reduced cost per watt of an APx-8 cell. A breakthrough process known internally as the molded wafer process has reduced the amount of silicon feedstock used per wafer by 40%. Other developments in the Silicon-Film feedstock preparation and wafer growth processes promise to further reduce the amount of silicon used per wafer.

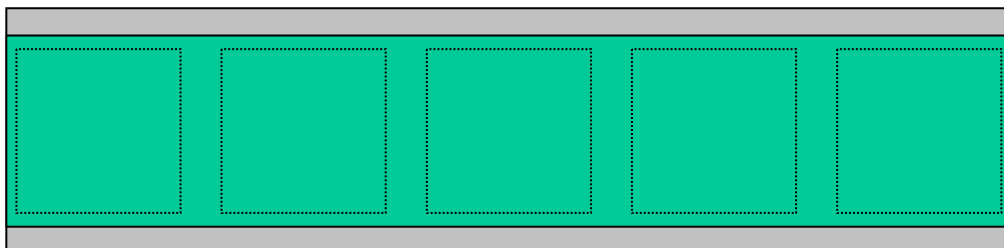
Work is also being done to increase the level of impurities the feedstock can tolerate and still make a good cell. This work will help refine the specification needed for a solar grade silicon product. Efforts have focused on tuning the growth parameters and optimizing a getter sequence to reduce the detrimental effects of these impurities.

In addition, two new processes have been introduced to increase throughput and reduce mechanical yield loss. The first is an edge-grinding tool that combines two steps in one; it achieves wafer symmetry and junction isolation in one step. The second is a change in the post diffusion anneal from a batch to a belt process. The belt process increased throughput, and improved electrical and mechanical yield.

## *5.1 Molded Wafer Process*

The new wafer formation process was put into production in October 2002. The changes lead to a substantial increase in material utilization, mechanical yield, and electrical yield. The majority of the increase in material utilization came from avoiding the waste generated by cutting wafers out of the old continuous sheets (Figure 21a). The old sheet process had an intrinsic yield of only 75%. Intrinsic yield is defined here as the best-case percentage of the sheet ending up as wafers. The new molded wafer process (Figure 21b) has an intrinsic yield of 97%.

**Continous Sheet Process**



**Molded Wafer Process**

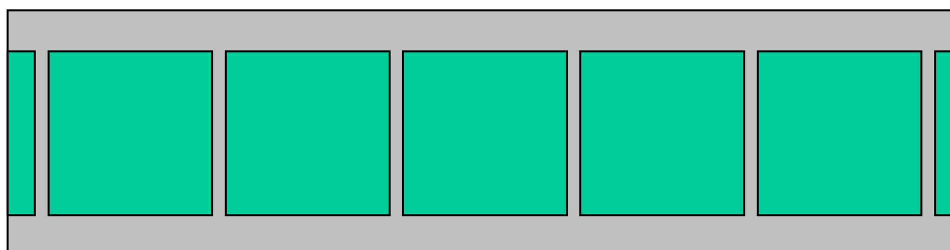


**Figure 21. (a) Old sheet design with intrinsic material yield of 75%; (b) new molded wafer design with intrinsic material yield of 97%.**

When the molded wafer process was introduced on the production line, the amount of silicon used to make one wafer was reduced significantly. The average material used per wafer was lowered 40%. This substantial decrease in silicon utilization consists of all material losses in the wafer including wafer growth yield and reduction in mechanical breakage.

There are additional benefits with the introduction of the molded wafer concept. In the sheet growth process, yield losses often occurred because defects in the sheet would propagate and meter long sections would be lost at a time. In the molded wafer process, defects are contained in the wafer of origin; therefore, propagation is not an issue. As a result, the actual wafer yield was increased from 70.5% in July 2002 to 78.9% in July 2003. In the sheet process, there were also yield losses in the old process due to scribing and sawing defects. The edges on the molded wafers have less edge cracks and chips, leading to better mechanical yield in the subsequent processing. In addition, since the molded wafer process has been instituted, cell power has increased by 5% (see Figure 22).

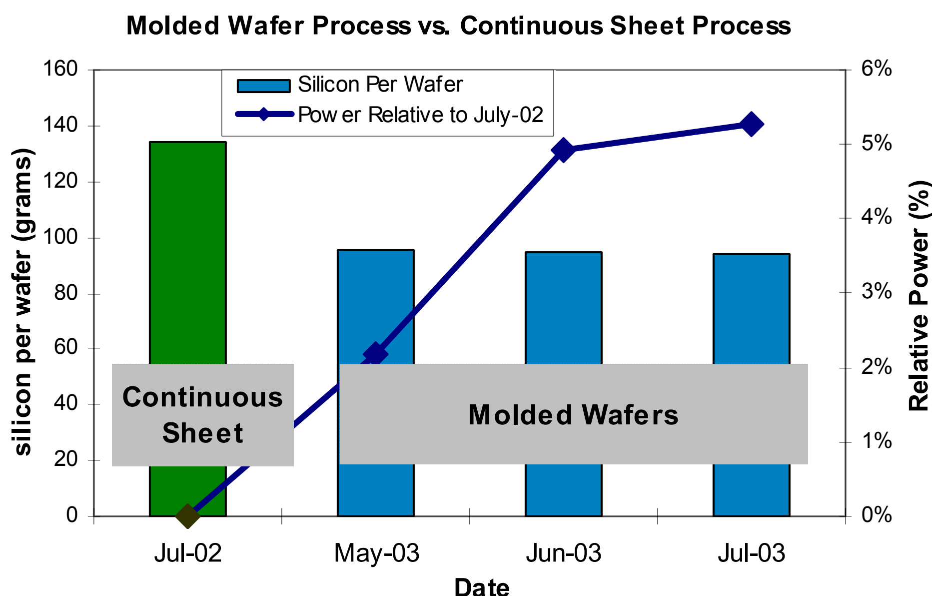



**Figure 22. Reduction of Si raw material and efficiency gains under new molded wafer.**

## *5.2 Increase Impurity Tolerance in Silicon-Film Material*

### Finding Suitable Metallurgical Grade Silicon Source

The Silicon-Film process has demonstrated the ability to tolerate high levels of impurities compared with conventional crystal growth methods. To capitalize on this, AstroPower is aggressively pursuing suppliers of upgraded metallurgical grade silicon that may meet our requirements, or meet our requirements after some additional purification. A survey of the world's metallurgical grade silicon suppliers was undertaken. A typical reading of the impurities is shown in Table 5.

**Table 5: Typical impurity levels of metallurgical grade silicon from various suppliers. Where the value is preceded by a < symbol, the impurity level is below detection limits.**

| Elements | Company A | Company A | Company A | Company A | Company B | Company B | Company B | Company C |
|---|---|---|---|---|---|---|---|---|
| Al [ppmw] | 56.3 | >76 | ~67.3 | ~67.7 | 49.76 | >141.8 | >138.6 | >82.9 |
| B [ppmw] | 4.588 | 3.405 | 2.899 | 3.513 | 4.806 | 5.65 | 5.56 | 3.539 |
| Ca [ppmw] | 2.216 | 28.86 | 12.15 | 14.91 | 2.315 | >437.8 | >425.7 | 13.78 |
| Cr [ppmw] | 11.48 | <1.499 | <1.504 | 1.525 | 10.52 | <2.498 | <2.493 | <1.496 |
| Cu [ppmw] | 2.006 | 1.765 | 1.086 | 1.782 | 0.2249 | <8.07 | <8.05 | <0.2092 |
| Fe [ppmw] | 15.02 | >95.4 | 15.99 | 18.18 | 15.58 | 25.11 | 24.97 | 18.89 |
| K [ppmw] | <2.049 | <2.06 | 2.268 | <2.064 | <2.065 | <2.886 | <2.881 | 2.303 |
| Mg [ppmw] | 3.381 | 0.753 | 0.721 | 0.779 | 2.845 | 0.503 | 0.583 | 0.898 |
| Na [ppmw] | 1.113 | <0.776 | 0.789 | <0.778 | <0.778 | n/a | n/a | <0.774 |
| Ni [ppmw] | <0.731 | <0.735 | <0.737 | <0.736 | 0.746 | <2.352 | <2.347 | <0.733 |
| P [ppmw] | 24.53 | 16.68 | 12.34 | 14.72 | 25.3 | 11.46 | 10.39 | 15.97 |
| Ti [ppmw] | 2.064 | 1.162 | 2.099 | 2.597 | 2.432 | 3.834 | 3.001 | 2.132 |

Table 5 shows samples of upgraded metallurgical silicon from three major suppliers of metallurgical silicon. The impurity analysis of the silicon was performed with inductively coupled plasma – optical emission spectroscopy (ICP-OES) and the difference in detection limits is due to the fact that different systems where used for the analysis. The silicon from Companies A, B, and C have similar levels of transition metals (1–100ppmw) and in general have phosphorus levels greater than 10 ppmw and boron levels less than 7 ppmw. After accounting for purification via directional solidification in the Silicon-Film process, transition metal levels are close to the required levels. Further work is required to reduce the remaining B, P levels through specialized purification steps.

## Improving Effectiveness of Gettering

Gettering can mitigate the impact of impurities on solar cell performance. To assist in optimizing the annealing/gettering process, impurities have been introduced in large amounts and their response to different getter sequences have been studied. The focus was primarily on Fe, a relatively slow diffusing transition metal and Cu, a fast diffusing transition metal. The “altered” heat treatment is a two-stage getter sequence, which is designed to effectively eliminate the impact of both Cu and Fe. No pre-getter treatment (such as P, Al deposition) is required. Table 6 shows results from a study where 30ppm Fe and 50ppm Cu were introduced to the silicon feedstock.

**Table 6: Solar cell electrical data wafers produced with high levels of Fe and Cu intentionally added. There were approximately 70 solar cells in each test sequence.**

| | | | | Standard Getter Sequence | | | | Altered Getter Sequence | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Fe[ppmw] | Cu [ppmw] | | Isc [A] | Voc [mV] | Pmax [W] | FF [%] | Isc [A] | Voc [mV] | Pmax [W] | FF [%] |
| A | 0 | 0 | Med | 11.02 | 555 | 4.20 | 69.0 | 10.76 | 552 | 4.05 | 68.8 |
| | | | Stdev | 0.16 | 4 | 0.18 | 2.3 | 0.15 | 4 | 0.14 | 1.7 |
| | | | Min | 10.60 | 546 | 3.82 | 62.4 | 10.27 | 538 | 3.70 | 64.1 |
| | | | Max | 11.31 | 563 | 4.57 | 73.3 | 10.96 | 556 | 4.44 | 73.8 |
| B | 0 | 50 | Med | 11.13 | 550 | 4.15 | 68.2 | 9.95 | 509 | 3.20 | 62.7 |
| | | | Stdev | 0.15 | 4 | 0.20 | 2.4 | 0.16 | 16 | 0.29 | 3.1 |
| | | | Min | 10.84 | 539 | 3.74 | 62.5 | 9.63 | 467 | 2.67 | 55.4 |
| | | | Max | 11.44 | 555 | 4.44 | 71.5 | 10.37 | 534 | 3.79 | 68.4 |
| C | 30 | 0 | Med | 11.13 | 552 | 4.24 | 69.3 | 10.52 | 543 | 3.83 | 67.2 |
| | | | Stdev | 0.16 | 9 | 0.20 | 2.8 | 0.28 | 13 | 0.28 | 2.4 |
| | | | Min | 10.74 | 509 | 3.77 | 64.2 | 9.74 | 478 | 2.74 | 58.8 |
| | | | Max | 11.33 | 558 | 4.56 | 79.2 | 10.92 | 553 | 4.10 | 70.1 |
| D | 30 | 50 | Med | 11.34 | 553 | 4.32 | 68.8 | 9.84 | 509 | 3.10 | 62.2 |
| | | | Stdev | 0.12 | 5 | 0.13 | 1.9 | 0.16 | 24 | 0.31 | 3.0 |
| | | | Min | 11.05 | 533 | 4.04 | 64.7 | 9.28 | 431 | 2.33 | 55.1 |
| | | | Max | 11.53 | 558 | 4.52 | 74.1 | 10.19 | 535 | 3.76 | 69.0 |

## *5.3 Edge Grinding Tool*

Mechanical yield issues have focused attention on the wafer edges. It is widely known that wafer edge treatment has a profound impact on wafer cracking through the solar cell processing line. To address this a wafer grind process has been designed. The tool employs large diameter fixed grinding wheels to grind wafers produced with a size variation of +1 to +3mm to within +/-20µm while simultaneously performing edge isolation. The equipment build is completed and the tool is ready to be put into production. It has a process capacity of over 600 cells per hour.

# 6 Module Enhancements and Rooftop Systems

Extensive efforts were made to improve the design of the module and the module manufacturing process. A new large area module lamination manufacturing line was designed accompanied by the design of a new large area module tester. In order to reduce module defects, a more rigorous pre-lamination inspection system was implemented. This included the introduction of an IR inspection station that can detect cracked wafers, short circuits, and bad solder connections.

Improvements on the module design have focused on reducing series resistance losses. Due to the large solar cell area, light-generated current levels are high (>10A), resulting in substantial resistive losses in the tabbing and interconnects. Using tabbing and interconnects with greater cross-sectional area significantly reduces losses however this leads to manufacturability and reliability issues.

AstroPower is actively investigating an alternative module lamination processes in an effort to reduce the cost of materials and manufacturing. A continuous lamination process being investigated with a partner company may potentially provide a less expensive module manufacturing process.

On the system level, AstroPower has developed a new method to mount large area APx-140 modules. This mounting scheme promises to be lower cost and more aesthetically appealing than the typical rack mount system.

## *6.1 Large-Area Module Lamination Line*

Specifications for an automated module lamination line for producing large-area Silicon-Film modules were developed and used to produce a system design. The lamination line was specified to occupy a space of less than 5,000 square feet, and was designed to produce 20 Silicon-Film modules per hour based on a 15-minute lamination cycle.

This automated line was specifically designed to eliminate glass and string handling for the large-area Silicon-Film modules. The automation was designed such that once the module glass is loaded into the glass washer, it is transferred from station to station on roller conveyors, with no need for an operator to handle glass until after testing. In a similar fashion, once the Silicon-Film cells are loaded into the system, there is no need for operators to manually handle the long strings. As a result, labor is significantly reduced. Due to the automated lay up, handling damage to the strings should be significantly reduced.

## *6.2 Pre-Lamination Inspection*

Significant efforts have been focused on reducing the number of defective modules produced. In order to minimize cosmetic flaws and defects in workmanship, a more rigorous inspection system was implemented at the laminate assembly step. Assuming that there are no issues with the size or appearance of the solar cells forming the strings, the pre-lamination assemblies are inspected visually for the following prior to lamination:

- Improper assembly (i.e. strings assembled in reverse, or not to the drawing)
- Loose, broken, missing, or misaligned tabbing and/or interconnect
- Broken or chipped cells

- Poor solder joints
- Foreign material
- Inadequate spacing between circuitry (cells, interconnect)
- Inadequate edge spacing (between the frame and circuitry)

The laminates are inspected after lamination as well for such defects as delamination, bubbling (entrapped air), which are created during the lamination process.

## *6.3 Thermal Defect Inspection with an IR Camera*

Solar cell cracking during the module assembly process has historically been a significant problem. Cracked cells that go undetected before lamination can result in power loss and deficient product reliability. Once the product has completed its lamination cycle, it cannot be quickly or efficiently repaired. Thus, a process was developed to inspect cell strings just prior to lamination in order to identify (and repair) cracked cells and other potential electrical problems. This process has been very successful in lowering defective module fallout and has been implemented for all module products.

The inspection procedure requires the solar cells to be connected to a DC power supply and forward biased. The thermal image of the strings captured by an infrared camera is presented on a screen for operators to use as they inspect for “hot spots” or “cold spots” that indicate abnormal current flows. Typical defects that can be seen are:

- Cracked or broken cells (the loss in active area is observed as a cold or dark spot)
- Shorted solar cells (the cell appears cold)
- Poor solder joint at cell (the joint appears hot, or white)
- Poor solder joint at string to buss connection (the joint appears hot)

Cells that appear to be cracked or soldered inadequately are either repaired, or removed and replaced, based on the type and severity of the problem. Consequently, the pre-laminate assembly is re-inspected before proceeding to the lamination process.

## *6.4 Continuous Lamination Trial*

In conjunction with a partnering company, AstroPower is pursuing the development of a continuous module encapsulation process (Figure 23). The continuous encapsulation process involves the use of a proprietary encapsulant to replace the traditional EVA lamination film and Tedlar backsheet. The specific properties of the encapsulant allow for the creation of a module without using a typical vacuum laminator. This method is expected to be more cost effective, have higher throughput, and generate less cell breakage in a module.

The process being developed is a two-step curtain coating method. The first curtain coating (optically transparent) is applied to the glass using conveyor belt transport. This is fed through a brief partial curing step (infrared belt furnace) to thicken or “gel” the encapsulant. The series interconnected PV-“layup” is then picked and placed face down into this clear layer of partially cured encapsulant. A slight string “tilt” is being used to dip each row of cells into the coating, side-edge-first. This tilt method is being developed to eliminate the trapping of small air bubbles under the cells. The second curtain-coat layer of encapsulant is then applied on top of the

traveling lay-up and fed into a second IR belt furnace wherein both layers of the encapsulant are rapidly cured. The second layer of encapsulant can be pigmented to practically any color choice.

**Figure 23. Example of a prototype module made with the continuous encapsulation process.**

A pilot scale manufacturing line has been setup at the partner company's location to more realistically develop the manufacturing process and address the manufacturability issues. Results so far have been moderately successful. Batches of small modules have been manufactured on a lab scale with minimal incidents of bubbles and defects and these modules demonstrated expected power at electrical test. Development work is underway to address air bubbles entrapment between cells and glass and the issues associated with mechanical pick and place of the series interconnected 36-cell "layup" into the partially cured transparent top layer of encapsulant. Formulation development is also underway for increased adhesion, toughness, cut resistance, and improved water vapor transmission rate. When these details are addressed, larger modules and modules with Silicon Film cells will be evaluated.

## *6.5 Reducing Series Resistance Losses in a Silicon-Film Module*

Because APx-8 cells have very high current, module resistive losses are a limiting factor in achieving high module power. Series resistance is a particular problem in the full cell Silicon Film module product where the Imp can be greater than 10 Amps. One way that is currently employed to significantly reduce Rs losses, is to use smaller Silicon-Film cells that are one half, or one third the size of normal 430 cm2 cells. Table 7 outlines the 12 module resistive losses for these current production cells:

**Table 7: Resistive losses in a 36-cell module using different size APx solar cells.**

| Source | Modeled Rs Power Loss |
|---|---|
| Full Cell | 8.3 % |
| Half Cell | 2.3 % |
| Third Cell | 1.1 % |

In the full cells, the biggest losses occur in the copper tabbing that joins cells together and tabbing that joins strings together. Experiments have been ongoing to determine what the optimal width and thickness of the cell tabbing should be. The fundamental limit to this optimization is manufacturability; problems arise with building the module as the interconnects become thicker and wider. With special attention to each manufacturing step, an experimental module was constructed using cell tabbing with 75% more cross-sectional area, and string-to-

string tabbing with 100% more cross-sectional area. Table 8 outlines the resistive losses of the experimental module compared to a standard production module.

**Table 8: Breakdown of resistive losses in a standard module vs. an improved experimental module.**

| | Calculated Power Loss (relative) | |
|---|---|---|
| Source | Standard Production | Experimental Module |
| Front cell tabbing | 3.3% | 1.8% |
| Back cell tabbing | 2.7% | 1.2% |
| Al metallization | 1.0% | 1.0% |
| String to string tabbing | 1.4% | 0.7% |
| Total | 8.3% | 4.8% |

This experimental module provides proof that there is great potential in reducing Rs losses. However on a production scale, there are three impasses to using tabbing with higher cross-sectional area: increased cell breakage in the module, problems with manufacturability (adhesion etc.) and failure during environmental test.

A small-scale test using 17% thicker tabbing was performed. The model predicts that this thicker cell tabbing generate an overall 0.9% relative increase in module power, however experimental trials resulted in a 1.2% relative gain in power measured on APx-140 modules. Unfortunately, the modules with the thicker tabbing had a slight increased incidence of breakage and stringing defects. It is expected that these manufacturing issues can be resolved with minor process improvements. The modules with slightly thicker tabbing have performed well in environmental testing.

## *6.6 Rooftop Integrated Module*

The primary design goal of the rooftop integrated module system was to create an aesthetically pleasing PV array that integrates well with common building materials (thus lowering component and installation costs). With the proposed mounting system, the solar module becomes the primary stressed member, rather than the support structure as found in the rack & post paradigm.

The core component of the mounting system is the bracket shown in Figure 24. The bracket, which utilizes sheet metal construction for low unit cost, is designed to interleave with asphalt composite shingles as they are installed. Sheet metal thickness is minimized so the asphalt shingles will lay flat and remain weather-resistant.

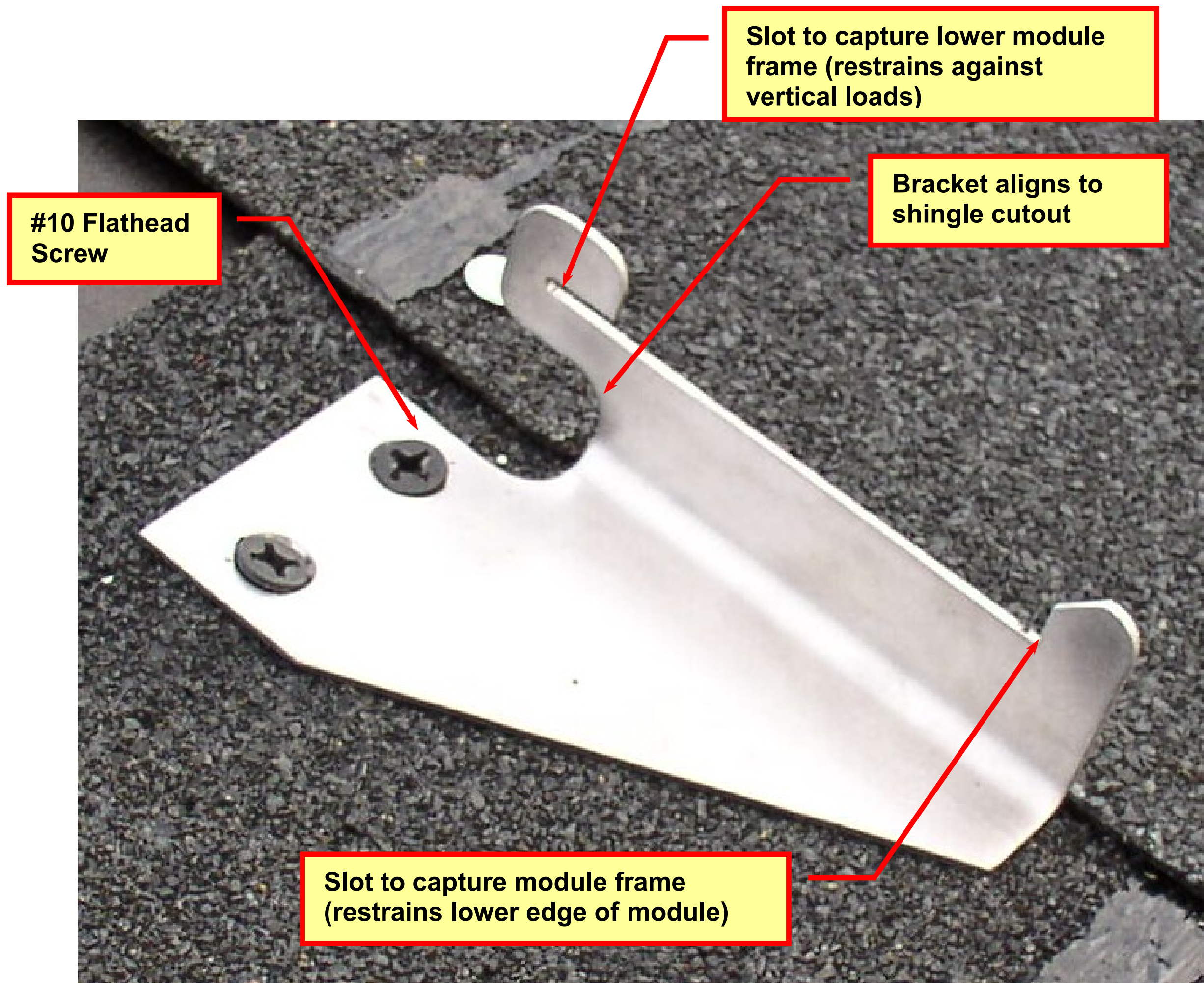



**Figure 24. Rooftop integrating bracket. Critical design features are highlighted. Sample brackets shown here are constructed from a lighter gage than production units would require.**

The shingles determine the location of the brackets, making array layout relatively simple. The bracket can be screwed directly into the roof deck; alignment to rafters is not necessary. The modules are installed on the brackets as pictured below in Figure 25. The lower lip of the module frame is slid securely into the slot on the mounting bracket to restrain the module against vertical loads. The protrusions on the lower portion of the bracket that hold the top of the module in place, also serve as an installation aid since they bear the weight of the module while it is positioned on the upper brackets (this is especially helpful on a steeply-pitched roof).

**Figure 25. First APx-140 module installed on lower bracket.**

Figure 26 depicts the installation of a second module. The “L” bracket attached to the top APx-140 module provides restraint against uplift forces on the module below. In a production unit, the frame would be designed with built-in overlapping flanges.

The lower module is now fully constrained in two dimensions. Lateral forces (parallel to shingle rows) are only partially constrained in this concept demonstrator. These issues will be addressed in the design for production units; possibly by sizing the module and frame so the roof brackets lock into pre-defined locations or by modifying the roof bracket so that it can be screwed into the frame.

It should be noted that this initial design is not a prototype for a production unit but rather a proof-of-concept that could be developed into a commercial system.

**Figure 26. Complete two-module array.**

# 7 Summary

The objective of the PV Manufacturing R&D subcontract was to continue to improve AstroPower's technology for manufacturing Silicon-Film wafers, solar cells, and modules to reduce costs, and increase production yield, throughput, and capacity. As part of this effort, specific technical undertakings were accomplished in the following five areas:

**Cell Manufacturing Upgrades**—New technology such as the continuous back metallization screen-printing system, and the laser scribing system were developed and implemented and existing processes such as the silicon nitride antireflection coating system, and the fire-through process were optimized.

**Process Control**—Improvements were made to the statistical process control (SPC) systems of the major manufacturing processes: feedstock preparation, wafer growth, surface etch, diffusion, and the anti-reflection coating process.

**Silicon Utilization**—The introduction of a near net shape wafer formation process as well as developments in feedstock preparation and wafer growth processes enormously reduced the amount of silicon used per wafer.

**Defect Engineering**—Extensive characterization has been done to understand the impact of impurities on device and growth performance. Experimentation has focused on tuning the growth parameters and optimizing getter sequences to reduce the detrimental effects of these impurities.

**Silicon Purification**—Work was done to upgrade metallurgical-grade (MG) silicon to a purity level needed for the Silicon-Film process through the continuous uni-directional solidification (CUDS) process.

**Module Manufacturing Upgrades**—A new large area module lamination manufacturing line with a new large area module tester was designed to accommodate the APx-140 modules and an advanced pre-lamination inspection system equipped with an IR inspection station was established.

**Rooftop System Design**—AstroPower has developed a new method to mount large area APx-140 modules, which promises to be lower cost and more aesthetically appealing than the typical rack mount system.

These improvements resulted in an increase of 5% relative power, and nearly 15% relative improvement in mechanical and visual yield in the cell manufacturing process. In addition manufacturing cost has reduced significantly due to the over 50% reduction in feedstock utilization. Considerable progress has been made in understanding the impact of impurities in Silicon-Film growth and performance and work was done to improve impurity reduction in the silicon feedstock through directional solidification.

# 8 References

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The objective of the PV Manufacturing R&D subcontract was to continue to improve AstroPower's technology for manufacturing Silicon-Film* wafers, solar cells, and modules to reduce costs, and increase production yield, throughput, and capacity. As part of the effort, new technology such as the continuous back metallization screen-printing system and the laser scribing system were developed and implemented. Existing processes, such as the silicon nitride antireflection coating system and the fire-through process were optimized. Improvements were made to the statistical process control (SPC) systems of the major manufacturing processes: feedstock preparation, wafer growth, surface etch, diffusion, and the antireflection coating process. These process improvements and improved process control have led to an increase of 5% relative power, and nearly 15% relative improvement in mechanical and visual yield. (Silicon-Film* is a trademark of AstroPower, Inc.)

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