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Manufacturing Improvements in Cz Silicon Module Production

Annual Subcontract Report
July 2005 — October 2006

T.L. Jester
SolarWorld Industries
Camarillo, California

Subcontract Report
NREL/SR-520-42418
November 2007

NREL is operated by Midwest Research Institute • Battelle Contract No. DE-AC36-99-GO10337

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NREL Technical Monitor: R. Mitchell

Prepared under Subcontract No. ZAX-5-33628-07

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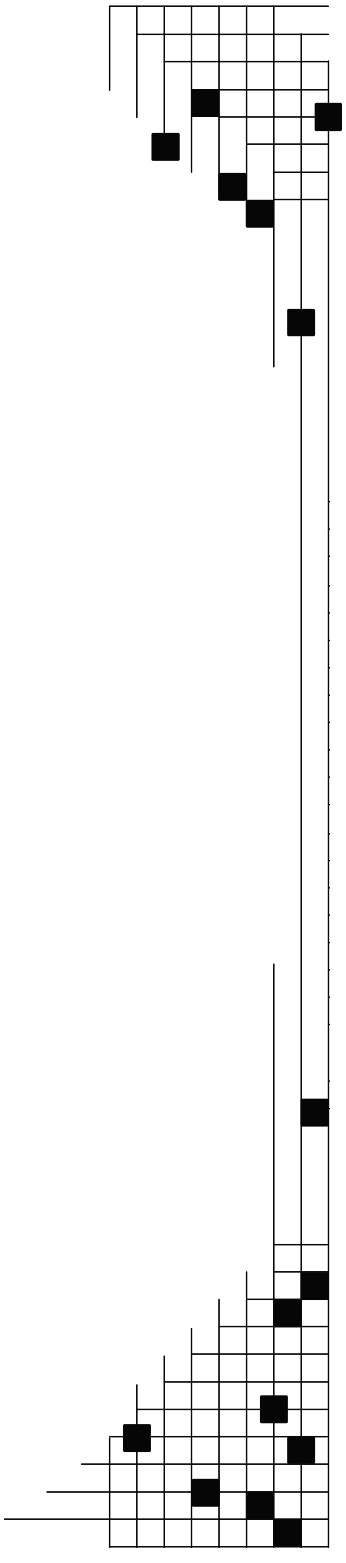

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1617 Cole Boulevard, Golden, Colorado 80401-3393
303-275-3000 • www.nrel.gov

Operated for the U.S. Department of Energy
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Contract No. DE-AC36-99-GO10337

Preface

This report describes work done by SolarWorld Industries America (SWIA) from July 2005 to October 2006 during Phase I of a three-phase Photovoltaic Manufacturing R&D (PVMR&D) subcontract from DOE/NREL. The work focuses on improvements in the cost per watt of Cz modules and improved PV module manufacturing technology. The focus for the three-year program is to implement a 15% efficient, module in production at under $2/Watt manufacturing cost. In addition, the program will develop higher reliability photovoltaic modules.

Acknowledgments

Many people have contributed to the work under this contract. Thanks are due especially to Rick Mitchell, NREL technical monitor, Paul Norum, Jeff Nickerson, Ken Sandland, Chris Fredric, Lisa Mandrell and the engineering staff at SWIA.

This work was funded in part by DOE/NREL Subcontract # ZAX-5-33628-07.

Summary

Work focused on reducing the cost per watt of Cz silicon photovoltaic modules under SolarWorld Industries' DOE/NREL PVMR&D Phase I subcontract is described in this report. Work on cell thickness reduction, the required electrical and mechanical changes to accommodate these thinner cells, higher efficiency process development and improved reliability are all described in this annual report. Table i shows the results of Phase I of the program.

Table i. Program Plans and Results

	Phase I 1st Year	Phase II 2nd Year	Phase III 3rd Year
Module Efficiency	13% efficient module ***14% achieved***	14% efficient module	15% efficient module 18% efficient cells
Cost Reduction*	20% thinner wafers 10% thinner wire ***Complete***	20% thinner wire	25% thinner wire
Improved Reliability	Reduce LID Identify new backsheet ***Complete***	Further reduce LID Implement new soldering technique	Implement new solder technique in production and new backsheet

* Polysilicon at $30/kg

Table of Contents

List of Figures

List of Tables

Introduction

Program Goals

The Photovoltaic Manufacturing Research and Development (PVMR&D) project is sponsored by the U.S. Department of Energy (DOE) through the National Renewable Energy Laboratory (NREL) in order to assist the photovoltaics industry in improvement of module manufacturing and reduction of module manufacturing cost. The objective of the DOE/NREL PVMR&D subcontract with SolarWorld Industries America (SWIA) is to continue the advancement of SolarWorld Industries' photovoltaic manufacturing technology in order to achieve a 33% reduction in module cost. The program addresses the reduction in cost per watt with a three part development contract: a significant reduction in wafer thickness from approximately 300 microns at the start of the program to a finished cell thickness of 180 microns at the end of the three years, a significant increase in module efficiency and an improvement in reliability in module lifetime. This is shown in Table 1.

Table 1. Goals of SolarWorld Industries' PVMR&D Subcontract from DOE/NREL

	Phase I 1st Year	Phase II 2nd Year	Phase III 3rd Year
Module Efficiency	13% efficiency module with improved processes	14% efficiency module	15% efficient 18% efficient cells
$2/Watt cost*	20% thinner wafers 10% thinner wire	20% thinner wire	25% thinner wire
Improved Reliability	Reduce LID Identify new backsheet	Further reduce LID Implement new soldering technique	Implement new solder technique in production and new backsheet

* Polysilicon at $30/kg

Approach

The first step toward reducing cost in this PVMR&D program at SWIA was to reduce wafer thickness. The cost per watt reduction affected through both the PVMR&D program and other programs at SWIA have shown significant progress. A 10% cost reduction has been realized during Phase I.

About half of the cost to produce a solar module is incurred by the time a wafer is produced, and another 20% is added in the cell processing steps. SolarWorld Industries has studied, developed and implemented processes for 240-micron thick wafers in the factory in Camarillo in order to reduce the wafer cost.

Efficiency gains have been significant. SWIA has increased the efficiency of solar cells made in our factory from approximately 15% to over 16.6% during Phase I. This has been done by working on the Boron BSF process, particularly the uniformity of the Boron coating and drive in process.

Module reliability is being improved with continued work on solder joint quality and automation as well as module Light Induced Decay (LID) reduction. New glass and EVA have been implemented which reduced LID by over 2% and increased productivity by over 30% due to faster curing in the lamination process. Plans for Phase II include a new module design, which saves over $0.10/Watt and improves reliability by increasing the rated voltage from 600 Volts to over 1000 Volts.

These three areas of focus, thinner cells, higher efficiency cells and modules and improved module reliability have the potential to drive costs down to under $2 per watt.

High Efficiency Cells and Modules

The work on efficiency at SolarWorld Industries has focused on the optimization and full deployment of a Boron Back surface field process to increase both the voltage and the current of the cell. The Boron BSF has in theory a higher efficiency potential than that of Aluminum back surface fields. While Boron has a better efficiency, the process details are more complex. Traditionally, Aluminum BSF formation is done with printing a back contact. Boron BSF's are usually formed through the deposition of the Boron containing dopant, followed by a thermal drive in at elevated temperatures above 1000 degrees C. This process has proven to be extremely sensitive to variations in coating and with these elevated temperatures. Heating during the drive in process needs to be done in a gradual manner to lessen shock on the cells. The improvement in cell efficiency distribution has been done in parallel to the work on making thinner wafers, which has proven to be an additional challenge.

Back Surface Fields in Production

The need for a Back Surface Field (BSF) to offset the electrical efficiency drop, as wafers are made thinner has been reported in PVMAT 5A2[1]. As cells are made thinner, a loss of efficiency is seen due to surface field effects. Thin cells require better passivation on the rear, requiring additional process steps. As mentioned above, SolarWorld has chosen the Boron Back Surface Field approach in our factory in Camarillo, California. Efforts to improve the Back Surface Field passivation have begun to show significant current and voltage improvements in the cells being produced in the Camarillo factory. Figure 1 shows the improvement in cell efficiency during 2006. As can be seen in the chart, cell efficiency has changed from just under 15% to over 16.6%. This has been done mainly by working on the Boron coating uniformity. The deposition of the Boron dopant is highly sensitive to minor machines changes. Coating wafers at high speed and with high material uniformity has been the main focus. Work on spray nozzle design and coverage has been important in ensuring high voltages and higher currents. The boron coat process is continually monitored for consistency and statistical process control has been an important tool here. Additional controls have been placed on all process steps, particularly the etching processes which prepare the surface of the cells prior to coating. A clean oxide-free surface prior to Boron deposition is required. Additionally, the removal of the Boron glass post thermal processing has been important for good contact formation.

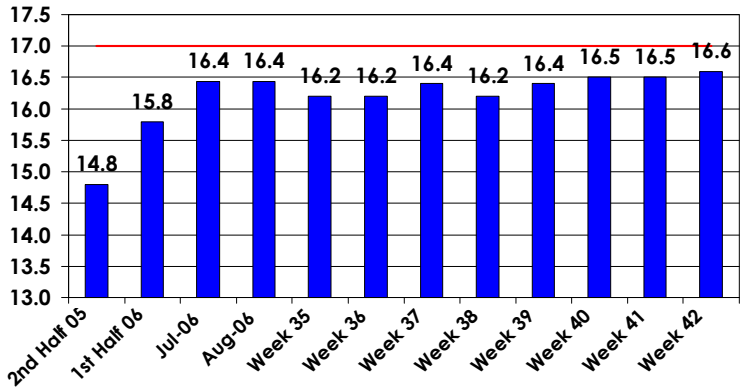
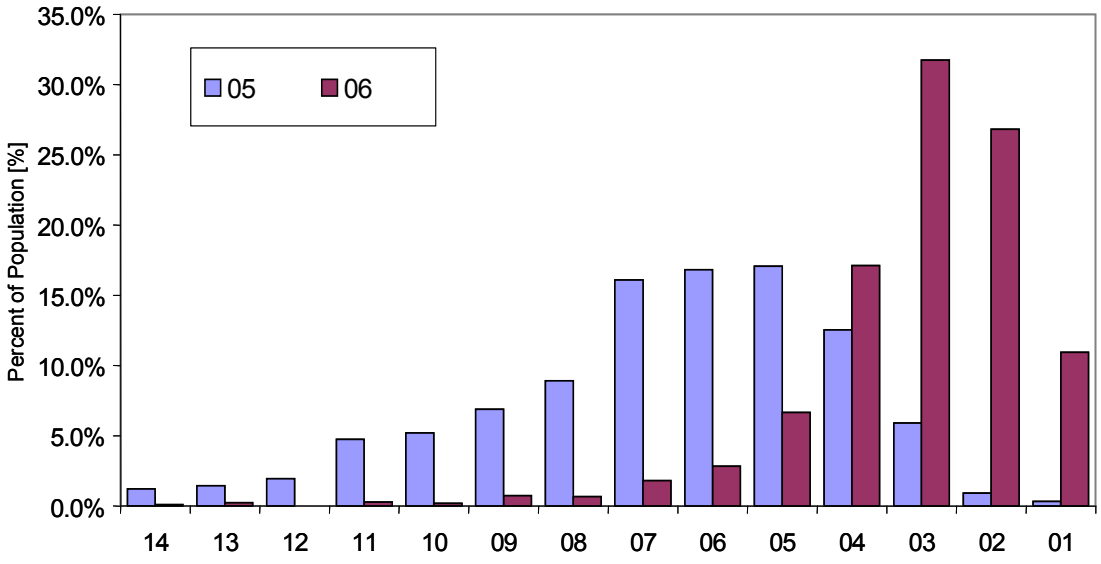


Figure 1. Cell Efficiency

In addition to an absolute improvement of efficiency, the cell distribution has become more repeatable with less variation. Figure 2 shows the improvement in histogram form showing both the shift up and the tightening of the distribution. As mentioned in the prior paragraph, uniformity of deposition has been a key driver for this improvement. Process control monitors have been set up at every step of the production line and have significantly reduced run-to-run variation. This has an added benefit of making production planning more routine with an improved ability to commit shipments to customers. This has also allowed the offering of 175-Watt Modules as the standard product, lowering the overall dollar per watt production cost.

The cell distribution is monitored twenty (20) times per day in the Camarillo Factory. Samples of each "lot of cells" are charted such that voltage, current and fill factory can be reviewed. A chart showing the monitoring of the distribution is shown in Figure 3, where the upper and lower control limit are well defined. Any excursion from nominal data is analyzed and failure mechanisms identified. The tightened control in Boron deposition uniformity has been a key contributor as well as work on the Phosphorous emitter uniformity to produce these better results. Contact firing is continually optimized as wafer thickness is reduced. The contact firing process is controlled daily with thermocouple monitoring of the furnace profile and exhaust settings and is one of the most significant control parameters for consistency of production. Cell processing variation continues to be a major focus in Phase II of the program.

Figure 2. Cell Distribution for 2005 and 2006



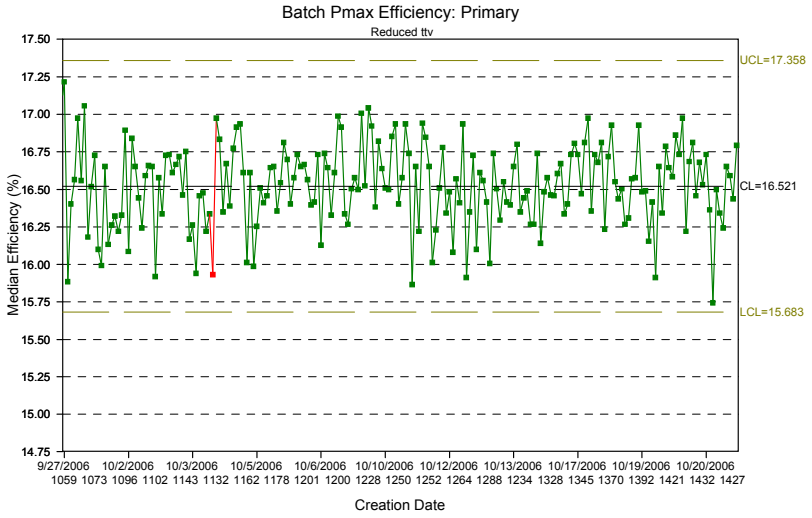


Figure 3. Efficiency Monitoring Chart

The next step in reaching production of a 17.5% efficient solar cell is to improve the emitter surface. A good understanding of the limiting factors on our cells has been important. Analysis has been done by the Georgia Institute of Technology to compare the most recent (16.6%) efficient cells being produced to 17.5% cells produced in the laboratory. Measurement of spectral response for long wavelength Internal Quantum Efficiency has been done comparing the center and the edges of the cells. The spectral response in the longer wavelengths is comparable as shown in Figure 4 where the SSG (red and yellow curves) designate the 17.5% cells, and the SSI (blue and green curves) designate the 16.6% cells. This long wavelength response, from 800-1000 nm shows comparable performance indicating that the back surface field quality is similar in the two samples. This is a direct result of improvements made to the Boron Coat and deposition process.

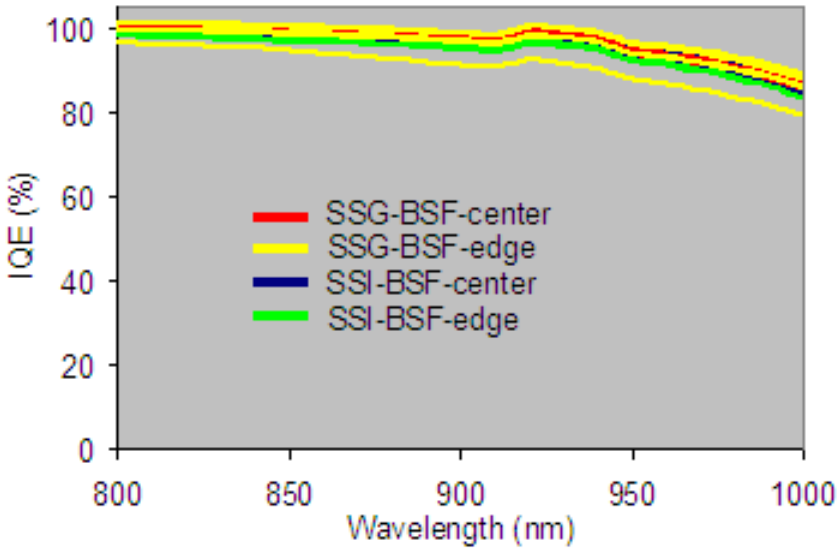


Figure 4. Long Wavelength IQE

Georgia Tech's data in the short wavelength region, 360-560 nm shows a significant difference between the two samples where the 17.5% lab cell has better low wavelength response. Further, there is a different response from the center of the 16.6% (SSI) cell to the edge, indicating a uniformity problem on the emitter. This has been further confirmed by sheet resistance measurements on the samples. This finding indicates that the uniformity of the phosphorous diffusion needs to be improved to better capture the low wavelength light. This data is shown in Figure 5.

Experiments have been launched to investigate the cause of the non-uniformity. This difference in emitter performance can be due to a thermal non-uniformity in the process, because of wafer position or load in the furnace tube. A series of experiments has been carried out to better understand the impact of higher and lower processing temperatures, impact of load size and gas flow. All experimentation is analyzed using the measured sheet resistance. It is best to look at the sheet resistance data across the wafer and across the tube using Weibull plots. Several different experiments can be shown on one chart with this analysis. Figure 6 shows the result of experiments to improve the uniformity of sheet resistance in the phosphorous diffusion. The graph shows the probability plots of sheet resistance variation (range of sheet rho across the wafer and tube) for various process changes. As a reference, the green data is the sheet rho uniformity for 17.5% efficient cells measured at SolarWorld, this variation averages approximately 10 ohms/cm^2. The pink data is the baseline production condition, showing a variation of approximately 15 ohm/cm^2. Changes to the formation of the Boron BSF were made to see if there is an affect on the Phosphorous emitter process, this data is shown in red, showing no effect. On the other end of the chart, the black data is a cell process without Boron BSF, which provides the most uniform sheet rho. This indicates that the presence of the Boron is affecting the Phosphorous uniformity. As this was discovered, several additional experiments were carried out, testing the physical placement of cells in the tube. The last two sets of data shown in Figure 6 (the yellow and the blue) are process changes to the phosphorous diffusion, mainly in how the wafers are spaced next to each other. Further experimentation is ongoing, with collaboration with Georgia Tech to improve our emitter performance.

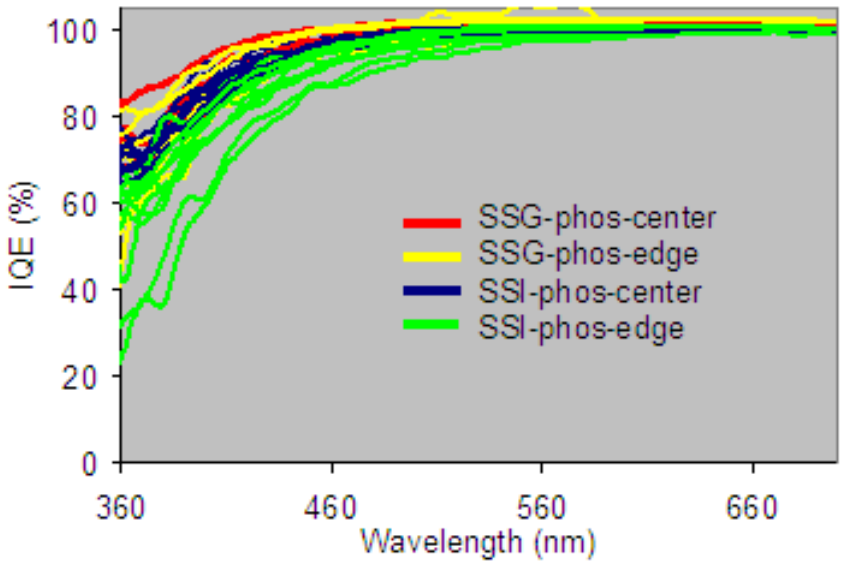


Figure 5. Short Wavelength IQE

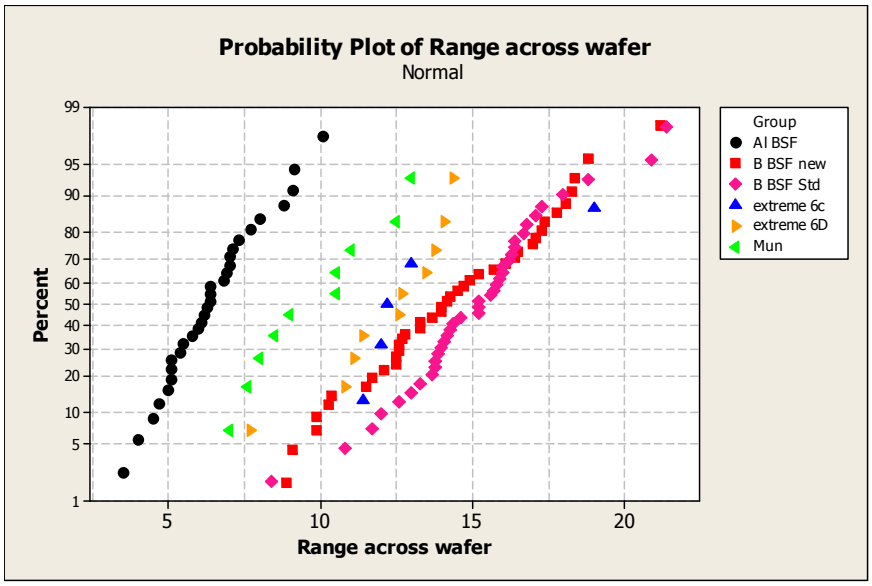


Figure 6. Sheet Rho Variation Across Wafer

As the cell efficiency has improved, so has the module power distribution. Figure 7 shows the improvement in modules power from 2005 to 2006 as a result of the changes in cell efficiency. Again, both a change upward and a narrowing of the distribution have been achieved with the improvements in cell processing. An absolute power gain of 10 watts has been achieved, improving module efficiency by 7% relatively. As mentioned above- a predictable and stable cell efficiency distribution allows for routine planning of module shipments. The main module product being offered at SolarWorld today is the 175 Watt product.

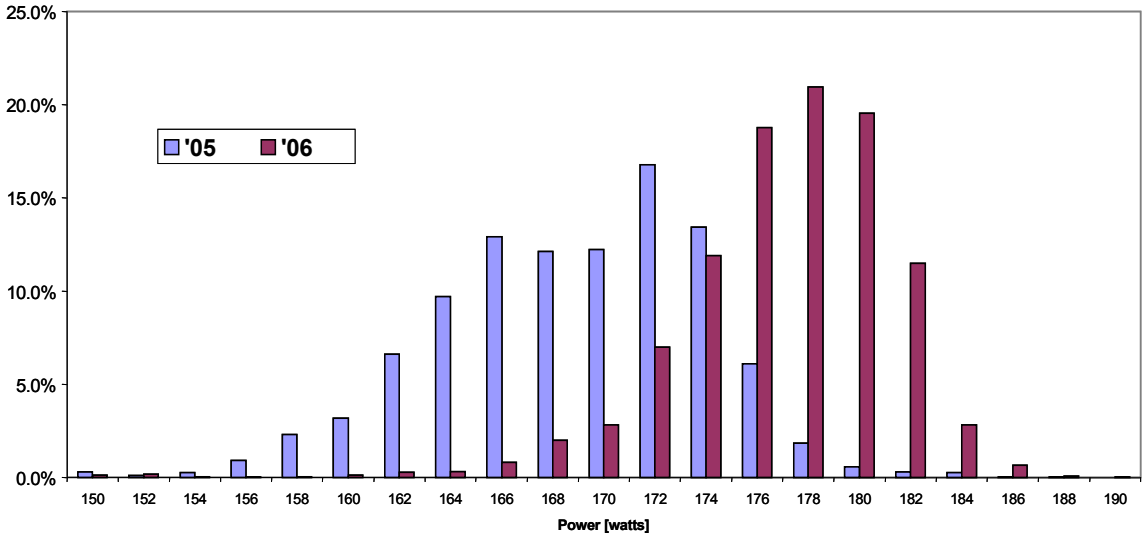


Figure 7. Module Distribution 2005 and 2006

Modules have been sent to NREL for efficiency verification. A representative module is shown in Figure 8 where the measured total area efficiency is equal to 14%. This satisfies a major milestone in Phase II as described in the Introduction section of this report.

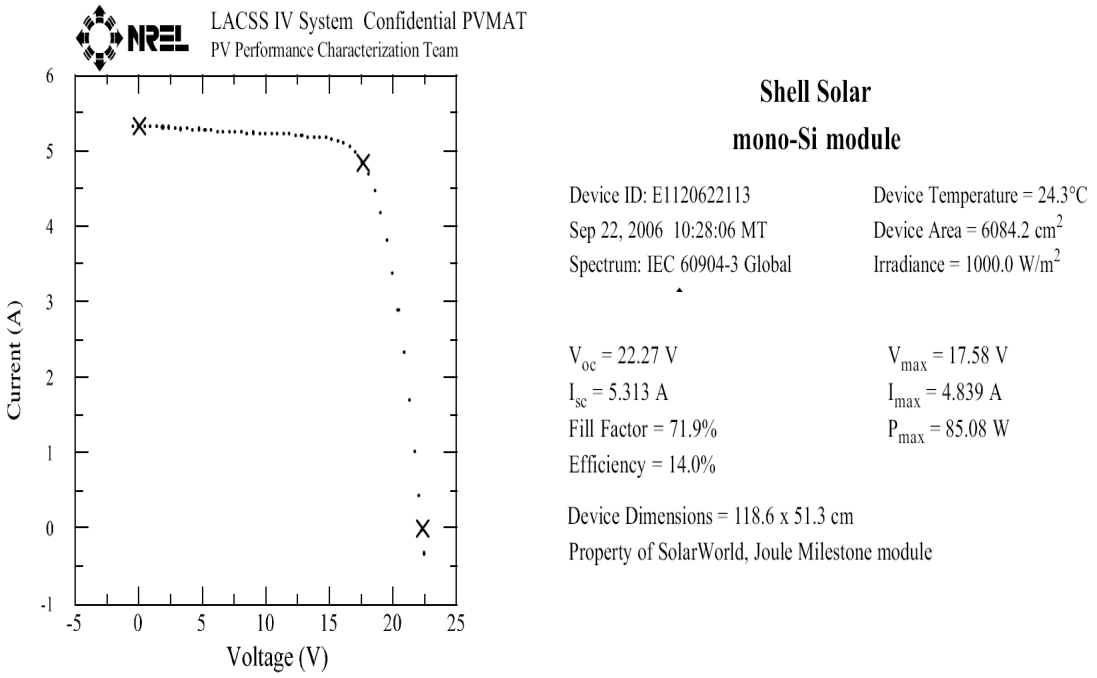


Figure 8. NREL Measured Module at 14% Efficiency (Total Area)

The next development activity in module efficiency improvement will be to understand the gains possible by making the interconnect ribbon thicker, lowering the resistance and improving the fill factor. Initial testing of different ribbon is described in the Cost Reduction section of this report

Cost Reduction

The work performed at SolarWorld during Phase I of the contract has resulted in an improvement in silicon utilization efficiency to over 120 watts produced per kg input of polysilicon, less than 8 grams of silicon used per watt. This important metric is shown in Figure 9 and is a leading indicator of cost performance. The less silicon used per watt, generally the lower the cost to produce This gain in productivity has been a result of implementing thinner wafers, thinner cutting wire, and better yield in all areas: wafer production, cell production and module assembly. Additional cost reduction efforts have been made in silicon recovery from cutting. This evaluation is described in later paragraphs.

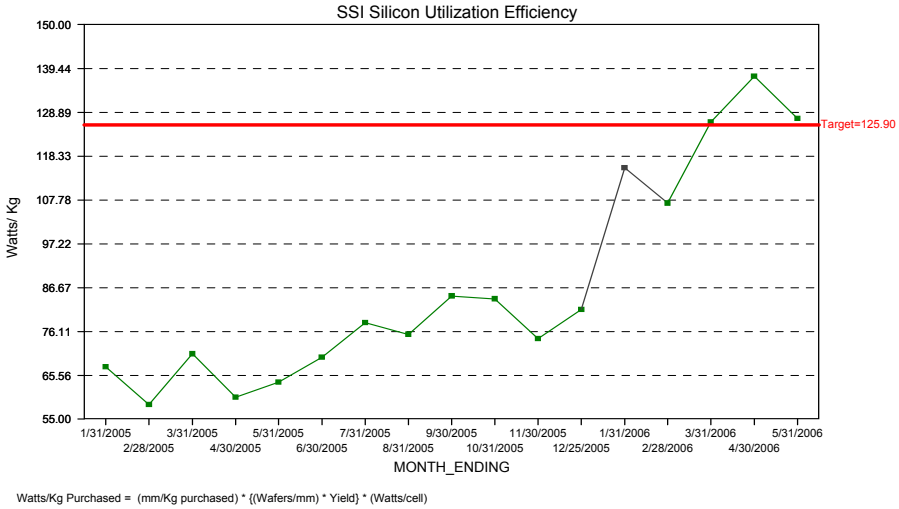


Figure 9. Silicon Utilization

Thin Wafer Production

The making of thinner wafers and cells in the manufacturing process has a large cost advantage. During PVMaT 5A2, significant yield losses were identified as wafers were cut thinner[1]. Figure 10 shows the original test data as reported during that program. As wafers were cut thinner, there was a significant decrease in yield. In addition, there was a significant decrease in electrical performance without a Back Surface Field. The benefit of Back Surface Fields is described in the first part of this report, detailing work on cell efficiency improvements.

The making of thinner cells in the manufacturing process has a large cost advantage. This assumes no loss to yield problems. Figure 10 is a summary chart of previous testing done during our PVMaT 4 contract[1], which shows wafering yield loss by part size and thickness. These data were gathered on a pilot run series of three ingots per part size and thickness and followed a systematic trend. In general the bigger the wafer, the lower the yield, and the thinner the wafer, the lower the yield.

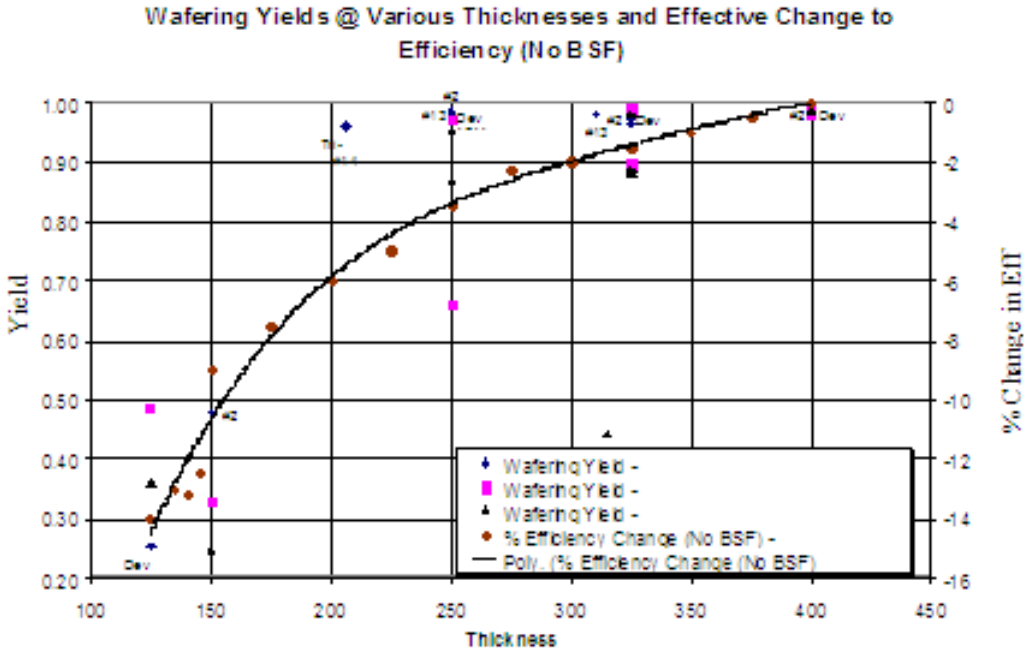


Figure 10. Wafer Thickness vs. Yield and Efficiency

Implementing thinner wafers in this program began with reducing wafer kerf loss during the wire saw process. When the program began, SolarWorld used a wire thickness of 140 microns. Testing showed that 125-micron wire worked well with minimal wire ruptures. Our wire supplier worked to produce 125-micron wire consistently. This really stabilized the yield. As this process was deployed, SolarWorld continued to work with the wire supplier to develop stronger 120-micron wire. As can be seen in Figure 11, the wire thickness reduction took place in two steps where the 125-micron wire was introduced into the production line for four months and stabilized, followed by the next step to 120-micron wire for two months prior to making the wafers thinner. Wafer thickness was reduced from 280 microns to 250 microns, followed by a further reduction to 240 microns. As each step in thickness reduction was implemented, yield issues emerged. Machine settings had to be fine tuned as well as operators trained to handle these thinner wafers. The combination of thinner wire and thinner wafers has resulted in a 26% benefit in ingot usage at the wafer level. In other words a given amount of ingot now produces 26% more wafers than one year ago. This has significantly contributed to the lowering of manufacturing costs. Figure 12 shows the average daily thickness in the manufacturing line and as can be seen, continues to be reduced.

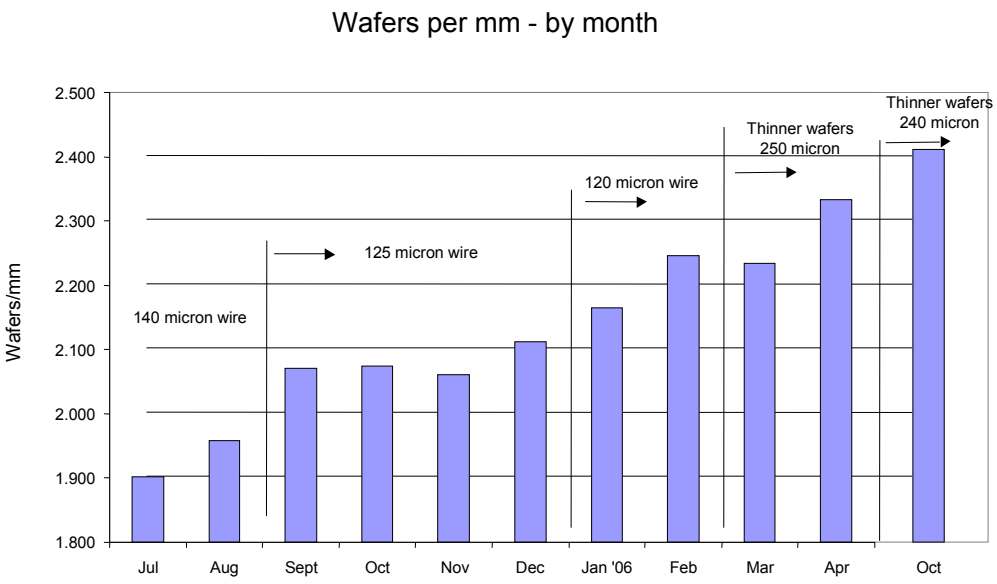


Figure 11. Wafers per mm

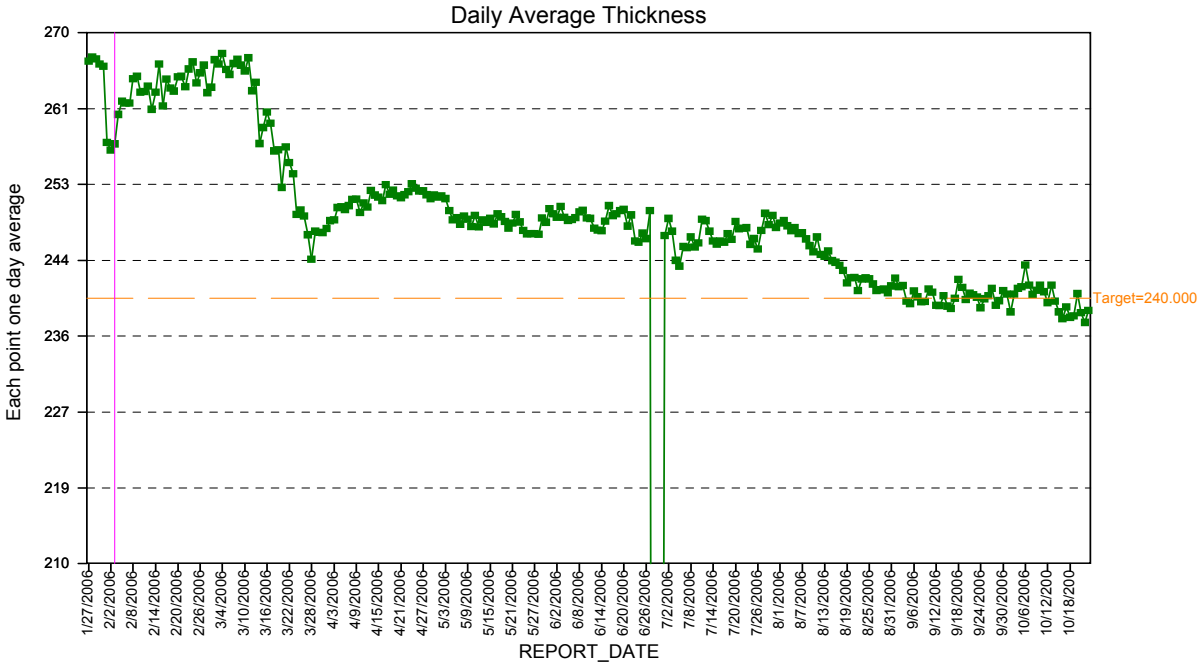


Figure 12. Daily Wafer Thickness

Thin Cell Processing

The processing of thin cells has been a challenge. As the wafers are cut thinner, the cells become even more fragile. As cells are approximately 30 microns thinner than the cut wafers, the handling steps and transferring of cells from one process to another, becomes very critical. Figure 13 shows an example of a process change required with thinner cells. The push/pull speed used in loading the Boron Diffusion furnaces had to be slowed down to improve yield because cells were getting chipped on the edges with the original pull speed (faster). When cells were made thinner, the yield loss or scrap increased. This required the slowing of the push/pull speed. This change actually helped wafer yield in the range of wafer thickness from 250 microns to 280 microns as can be seen in Figure 15 where the yield improved in all cases by slowing down the transfer speed.

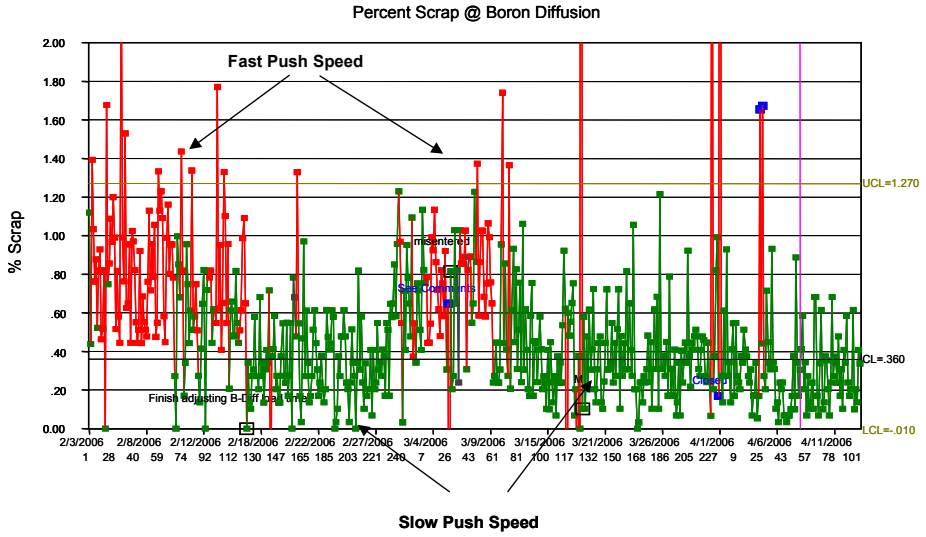


Figure 13. Boron Push/Pull Speed vs. Scrap

The electrical performance of cells has been discussed in the first section of this report. A significant test was run during Phase I to show that the BSF process deployed at SWIA provides enough passivation to offset the drop in efficiency seen in Figure 10. Three groups of cells were processed from wafers 270, 250 and 230 microns thick. The cells processed were 240, 220 and 200 microns thick respectively. As can be seen from Figure 14, the cell performance overlaps completely, showing no decay in cell output as the wafers become thinner. This data provided the baseline to continue with thin cell processing for cost reduction.

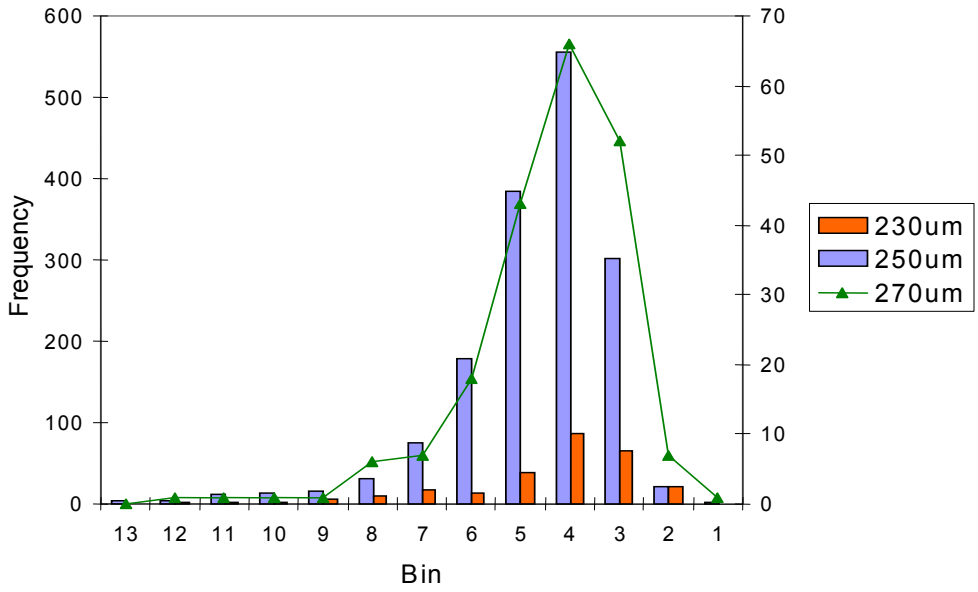


Figure 14. Cell Distribution vs. Thickness

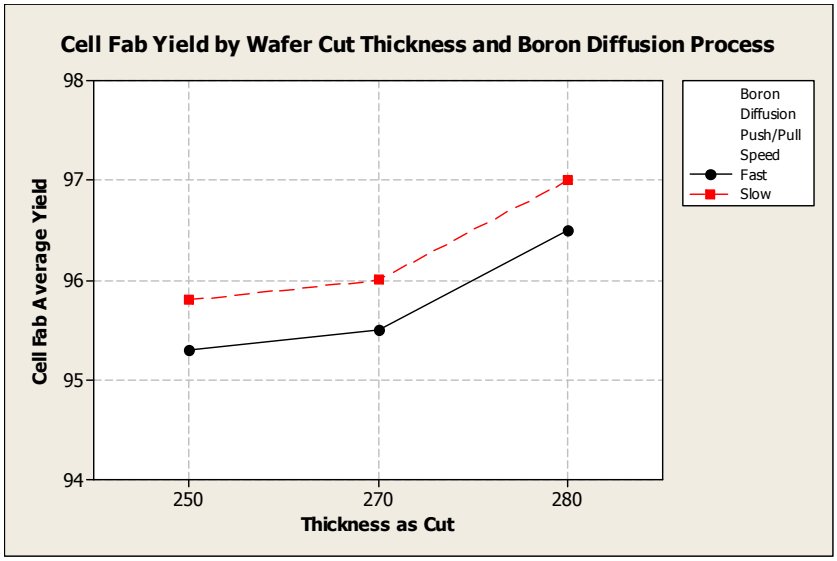


Figure 15. Cell Yield vs. Thickness

As wafers are made thinner, mechanical yield is more of a challenge. We particularly looked at movement of wafers in and out of the boron diffusion process. In reviewing this particular step, the impact of thinning the wafers is shown in Figure 15, where the lower line shows the fast pull speed, the upper line shows the slow pull speed. For all wafer thickness groups, the yield improved by slowing the process speed.

Although the cell distribution remained consistent as the wafers were made thinner, there was an increase in the amount of electrical scrap or cells which produce a minimal amount of power. A look at the wafer total thickness variation (TTV) showed an increase in absolute value as the cutting wire and thickness changes were deployed. As can be seen in Figure 16, the TTV increased significantly. This change in wafer quality was of concern in the ability to fire contacts properly to the solar cell. The amount of cells classified as unusable increased (electrical scrap). An overlay of the electrical scrap vs. TTV measurements is shown in Figure 17, showing strong correlation. Improvements in ttv are being brought about with changes to slurry and Silicon Carbide mixtures and will continue to be a focus for the next phase of the program.

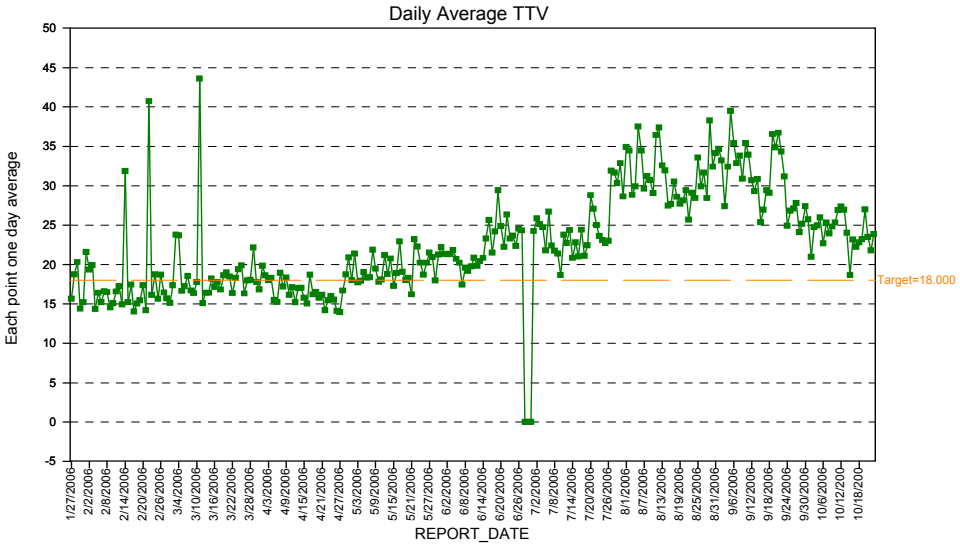


Figure 16. Daily Average TTV

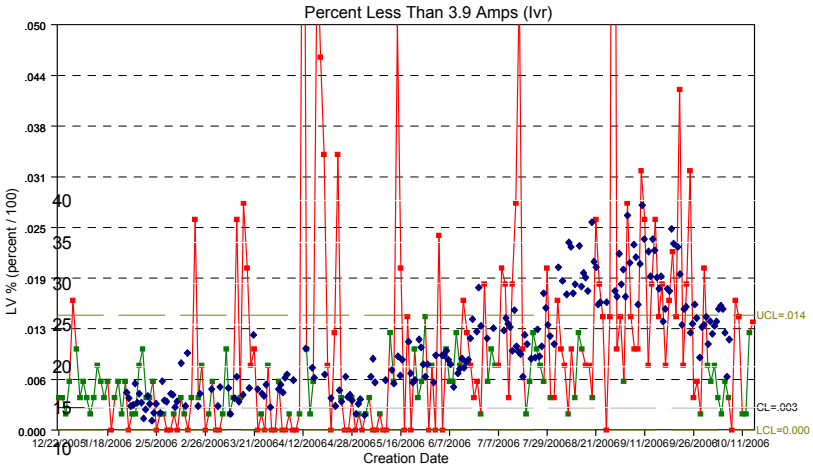


Figure 17. Electrical Scrap Correlation to Wafer TTV

In early 2006 there were several improvement programs underway in the Camarillo facility. The reported yield and daily output numbers were being used as a feedback system to show results of improvement efforts, many of which have been documented in monthly reports issued under this contract. The daily reports issued from the manufacturing information system were inconsistent, although the engineers knew the process was improving. Three important issues emerged. The reports being generated had the following problems:

1) Production performance was not viewed statistically – no separation of special events from the noise of normal operation
2) Too summary in nature- events would be hidden in the noise
3) Not real time – the numbers are already history (often history of "the other shift")

While engineering was working on yield and system improvement solutions, the efforts were disconnected from the line operators. Line operators had "yield improvement" added to their performance reviews, but the expectations of them lacked specificity. Several of the engineers observed that experiments that should have resulted in more scrap resulted in yields that were significantly better than production. It was hypothesized that the experiments increased accountability and the production reporting lacked accountability. The basic shop floor reporting system looked like Figure 18.

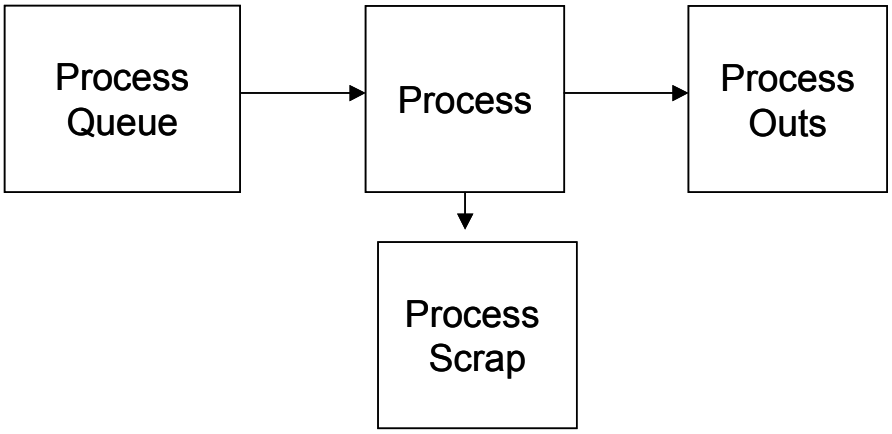


Figure 18: Production reporting system in January 2006

In February 2006, a lot tracking system was introduced in the factory to help improve mechanical yields in thin cell processing. It was agreed to try a batch tracking system that would increase accountability by requiring that individual operators trace material as it moved through the system. Fourteen (14) processes were specified as requiring the implementation of this accountability.

The batch system was launched with a lot or batch tracking sheet.

The system provided a series of SPC charts as shown in Figure 19, which provide feedback every batch (~ every 2 hours) to the operator where all Out of Control points are investigated for special causes.

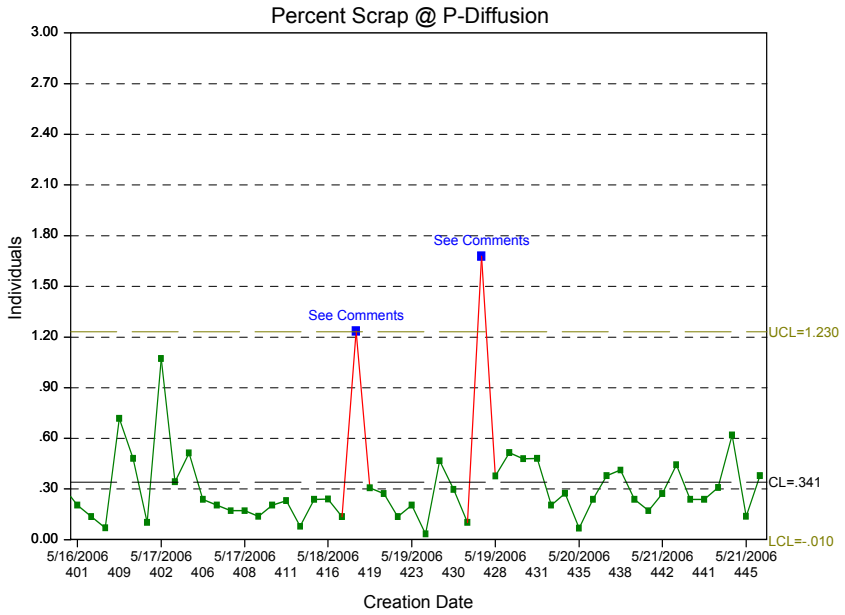
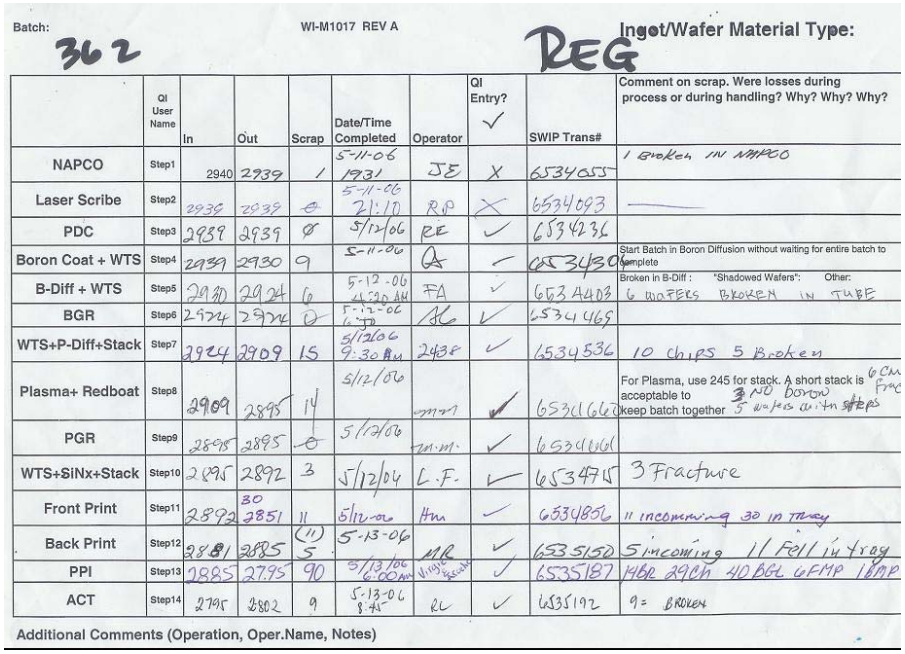


Figure 19. Individual Process SPC chart for Yield

Figure 20 shows an example of a lot-tracking sheet, capturing all of the operations details about that lot. This data is analyzed daily for trends and improvement opportunities.

The result of the implementation of the batch tracking was an immediate improvement in yield. The scrap rate was reduced, and the accountability and problem resolutions were increased. The resultant scrap values are shown in Figure 21, where the only change to the production line was the tracking system. As can be seen by the chart, scrap was reduced by over 3.5% due to this new monitoring method.

Additional information will be added in the future to track individual machines within a process and to track all aspects of production including yield, throughput, set-up time, machine uptime, and other important lot characteristics. This will commence during Phase II.



Batch: 362 WI-M1017 REV A Ingot/Wafer Material Type: REG

	QI User Name	In	Out	Scrap	Date/Time Completed	Operator	QI Entry? ✓	SWIP Trans#	Comment on scrap. Were losses during process or during handling? Why? Why? Why?
NAPCO	Step1	2940	2939	1	5-11-06 1931	JE	X	6534055	1 broken in NAPCO
Laser Scribe	Step2	2939	2939	0	5-11-06 21:10	RP	X	6534093	
PDC	Step3	2939	2939	0	5/12/06	RE	✓	6534236	
Boron Coat + WTS	Step4	2939	2930	9	5-11-06	QA	✓	6534306	Start Batch in Boron Diffusion without waiting for entire batch to complete
B-Diff + WTS	Step5	2930	2924	6	5-12-06 4:30 AM	FA	✓	6534403	Broken in B-Diff : "Shadowed Wafers": Other: 6 WAFERS BROKEN IN TUBE
BGR	Step6	2924	2924	0	5-12-06	JC	✓	6534465	
WTS+P-Diff+Stack	Step7	2924	2909	15	5/12/06 9:30 AM	2438	✓	6534536	10 chips 5 Broken
Plasma+ Redboat	Step8	2909	2895	14	5/12/06	[illegible]	✓	6534666	For Plasma, use 245 for stack. A short stack is acceptable to keep batch together. 3 NO Boron 5 wafers with steps. 6 Cracked
PGR	Step9	2895	2895	0	5/12/06	[illegible]	✓	6534666	
WTS+SiNx+Stack	Step10	2895	2892	3	5/12/06	L.F.	✓	6534715	3 Fracture
Front Print	Step11	2892	30 2851	11	5/12-06	Hm	✓	6534856	11 incoming 30 in tray
Back Print	Step12	2881	2885	(11) 5	5-13-06	MR	✓	6535150	5 incoming 11 Fell in Xray
PPI	Step13	2885	2795	90	5/13/06 6:00 AM	Virgil Escalante	✓	6535187	MBR 29Ch 40BGL 6FMP 18MP
ACT	Step14	2795	2802	9	5-13-06 8:45	RL	✓	6535192	9= BROKEN

Additional Comments (Operation, Oper.Name, Notes)

Figure 20. Sample Lot Tracking Sheet

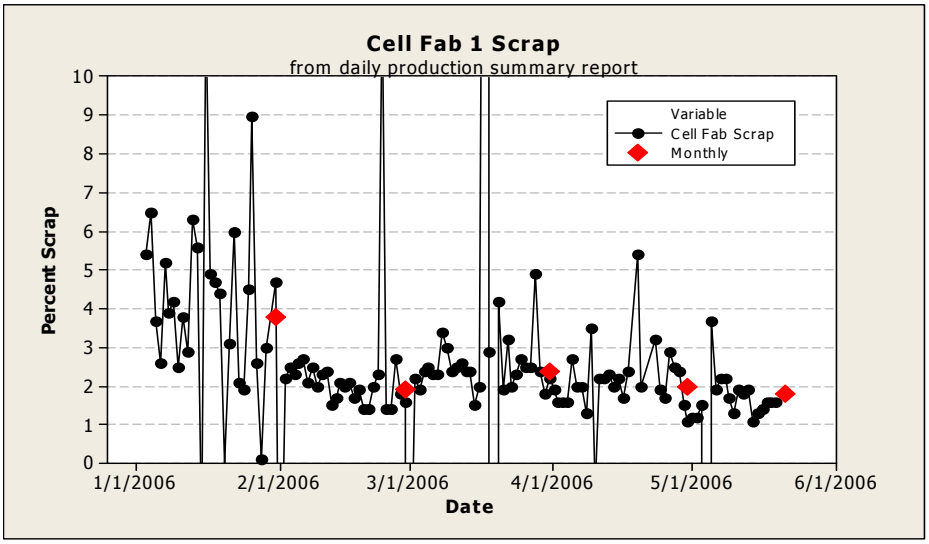


Figure 21. Scrap Reduction after Lot-tracking Implementation

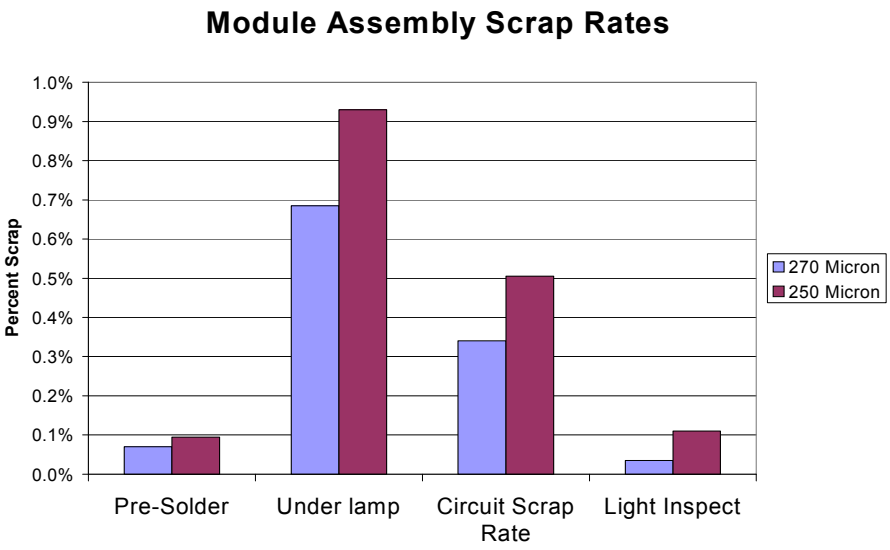


Figure 22. Module Assembly Scrap Rate with Thinner Cells

An increase in scrap at the module assembly process has been seen as cells have been made thinner. The process of soldering cells has been particularly sensitive to changes in wafer thickness. Figure 22 shows the scrap increase with thinner wafers. In each part of the soldering process, belt loading (pre-belt), under the soldering lamp (under lamp), circuit assembly (circuit), and final inspection (light inspection). The total increase in scrap is 0.7%. This 0.7% increase in scrap continues to be worked as different solder processes are evaluated.

Ribbon thickness and hardness are also being evaluated to lessen the effect of thin cell processing. Figure 23 shows the result of experimentation with different ribbons. Ideally the ribbon thickness should increase to reduce the resistive losses in a module. It was also theorized that the ribbon should get "softer" to induce less stress on the cell. The results in Figure 23 contradict these ideas and required keeping the baseline conditions. Work continues to optimize ribbon thickness vs. solder scrap during Phase II.

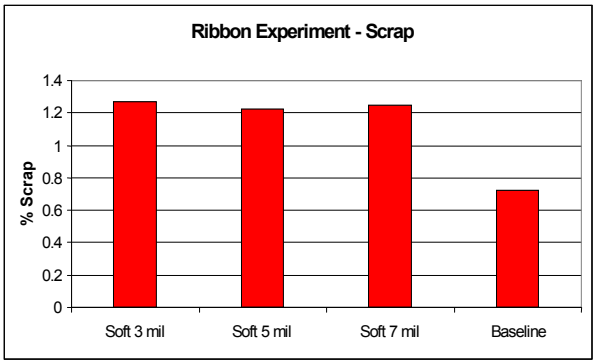


Figure 23. Solder Scrap vs. Ribbon Type

Silicon Recovery

During July and August, 2005, analysis was performed on two types of slurry waste, these were:

1) used slurry from Camarillo saws
2) SiC fines from Camarillo saws

Both samples were subjected to Soxhlett extraction in n-heptane, which yielded clean dry free flowing powders. Powder X-Ray Diffraction (p-XRD) was used for the structural identification of compounds in the two samples.

The following data was reported:

1) This sample consisted of small silicon particles around 1 micron, with significantly larger and 'jagged' particles of silicon carbide with an average size of 5 microns. Furthermore very small iron containing particles were observed. Powder XRD found small amounts of iron oxide and some another iron-containing material that could not be identified. XRF found 4% by weight iron, 70% silicon, 26% carbon and traces of other elements (Cu, Zn, S, Ca, Ti, V, Mn).

2) This sample mainly consisted of smaller SiC particles, silicon and iron containing particles. Powder XRD found small amounts of iron oxide, and a large amount of the unidentified iron-containing material. XRF found about 13% by weight iron, 70% Silicon, 16% carbon and traces of other elements (Cu, Zn, S, Ca, Ti, V, Mn).

The XRD results are as follows:

1) for the powder obtained by Soxlett extraction of "used slurry":
~88%wt SiC
~5%wt Si
~5%wt Fe-Cr stainless steel
~2%wt FeO

2) for the powder obtained by Soxlett extraction of "SiC fines":
~52%wt SiC
~18%wt Si
~28%wt Fe-Cr stainless steel
~2%wt FeO

SiO2 could not be detected with XRD in these samples.

From the above it is clear that in both samples the majority of the material is silicon carbide, whereby the silicon carbide particles are a factor of 5 larger than the silicon particles. Iron is present in oxide form in amounts ranging from 4 to 12% by weight. Since iron is such a lifetime killer in silicon, it was suggested that selective removal be done first before trying to recover silicon from the silicon/silicon carbide physical mixture.

The following was considered: Mild and careful reduction of the iron oxide phase at several hundred degrees in hydrogen under avoidance of high partial pressures of water formed by the reduction, that would tend to promote the nearly irreversible formation of iron silicate from iron and the silica layer covering the silicon particles. Subsequently carbon dioxide can be passed over the sample between 70

and 90 degrees centigrade, which will turn all accessible iron metal into volatile iron carbonyls. If the removal turns out to be complete, tests could begin in subsequent steps. If not, the separation would be very difficult and the whole project should be reconsidered for cost reasons.

After further review, the complexity to recover this material outweighed the benefit. Another approach was outlined, the recovery of broken wafers.

This approach can save up to 5% of the silicon used and is much easier to implement, particularly in the factory in Camarillo.

Work has begun with limited findings. This will be further investigated during Phase II.

Module Reliability Improvement

Development of an LID-free module began with understanding the contributions to LID (Light Induced Decay) from both the cell and module materials[2]. A series of tests were run to look at the decay of Cerium containing glass showing that 1.7% of the LID was coming from glass decay. Figure 24 shows the pre-degradation and post-degradation behavior of the glass vs. wavelength and overlay of the cell performance with respect to wavelength. This glass has been replaced with a new composition glass having no decay in the long wavelength when exposed. This combined with a new EVA formula has resulted in now LID contribution from the module package. These materials were deployed in the Camarillo factory during Q3 and Q4 of 2005.

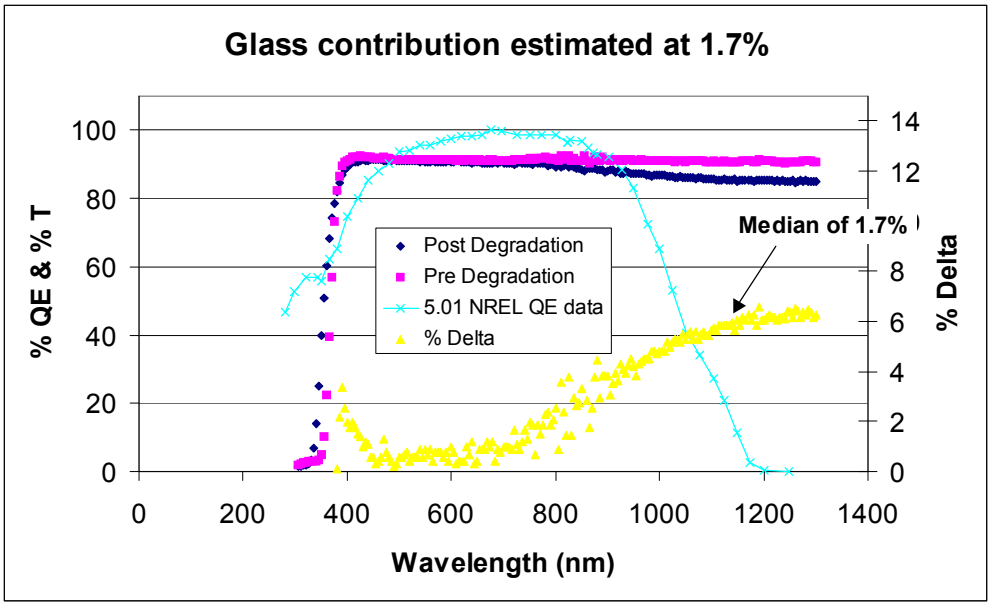


Figure 24. Glass Degradation

Additional experimentation has been done on the cell level LID, particularly with dopants used during Cz crystal growth. Figure 25 shows the degradation (or lack of degradation) where a substitute dopant for Boron has been used. This new dopant has the advantage of being a direct substitute for Boron and can be used safely in manufacturing environments. This promising result is being evaluated further in additional tests at the cell level to ensure that the efficiency of the cell produced is as stable and at or above 16.6%.

Reliability of PV modules is heavily dependant on solder processes used to make modules. Solder joint studies have been done looking at reliability and repeatability. Test data of solder joint strength is shown in Figure 26, a test done every four hours in the factory. The operations personnel perform a measurement using a force gauge to assess solder joint quality. The specification developed is to have joints greater than 200 grams. The chart shows an average joint strength in excess of 360 grams, well above the necessary requirement. As mentioned, the test is performed every two hours to ensure consistency.

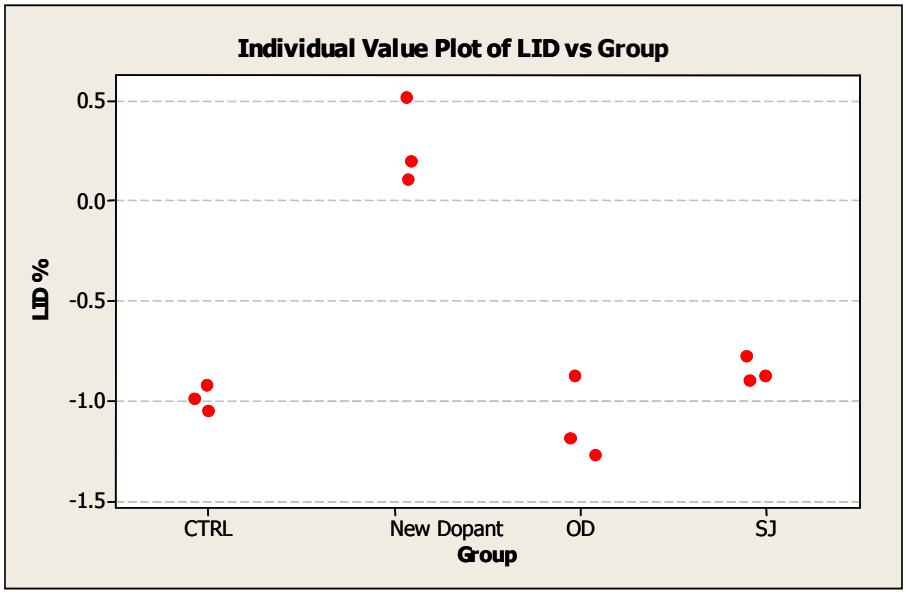


Figure 25. New Dopant Experimental Results

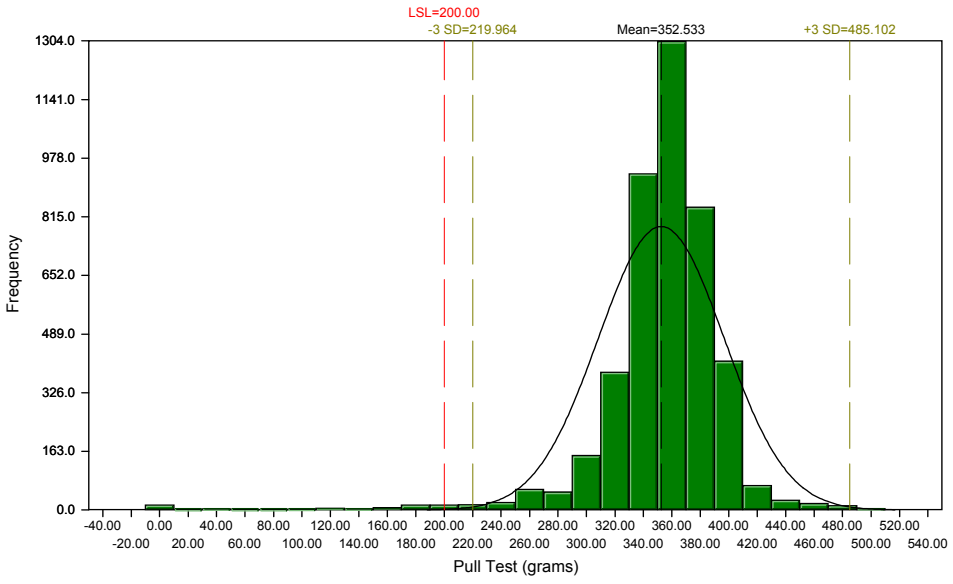


Figure 26. Solder Joint Pull Strength

Additional work on solder joints has been done to asses the quality of the metal bonds. Figure 27 shows SEM analysis of solder joints showing good lead distribution, indicating a uniform and reliable solder process. These data are critical baseline data for comparative studies of different solder techniques and machines being evaluated at SWIA. In deploying new ribbon materials, and new solder techniques, this microscopic evaluation, coupled with solder pull strength will keep joint quality at a high level. More work is planned during Phase II to evaluate new solder techniques and materials.

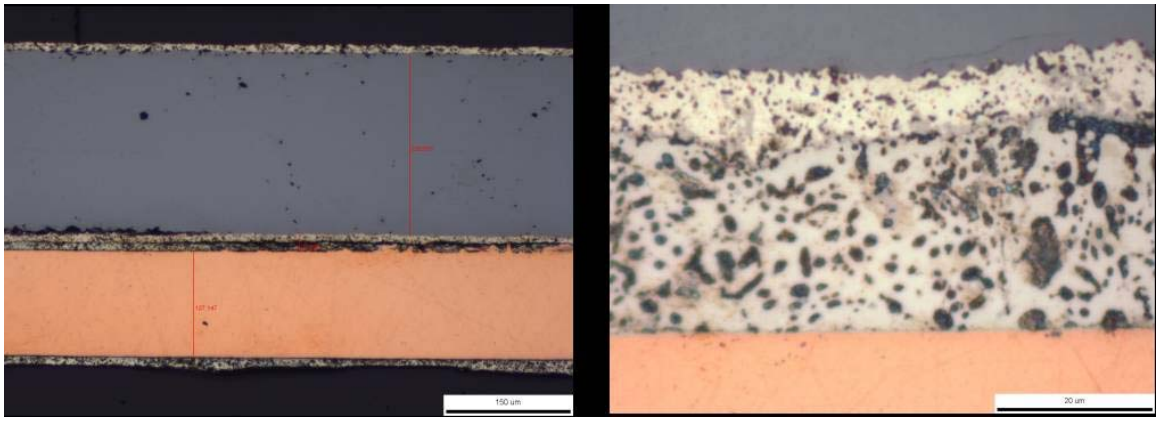


Figure 27. Solder Joint Cross Section SEM

Module Materials Improvement- EVA and Backsheets

Ethylene Vinyl Acetate (EVA) sheet is laminated in the module on both sides of the solar cell, forming seals to the glass front and backsheet of the module. During the lamination and curing process, the EVA crosslinks, forming a chemical bond, which seals the module. To test this crosslinking process, a sample of EVA is physically removed from a suitable coupon, and analyzed by a Gel test. This test is done by measuring the weight loss of a sample of cured EVA after it has been dissolved in toluene for 16 hours. The sample is then dried and the weight is recorded. The ratio of the weight after dissolution compared to the weight prior to dissolution is called the Gel content. The minimum amount of retained weight or gel content is 80%.

At the start of the encapsulation investigation process, the standard encapsulation material being used required a curing time of 60 minutes at 150°C in order to achieve an acceptable level of EVA crosslinking. A new EVA formulation has been deployed, along with a new curing oven, which has reduced the curing time to reach 80% gel content to below 30 minutes. Figure 28 shows cure time vs. gel content, where a cure time of 24 minutes exceeds a gel content of 80%. This has improved the capacity of the lamination and curing process by over 100% and is repeatable and consistent.

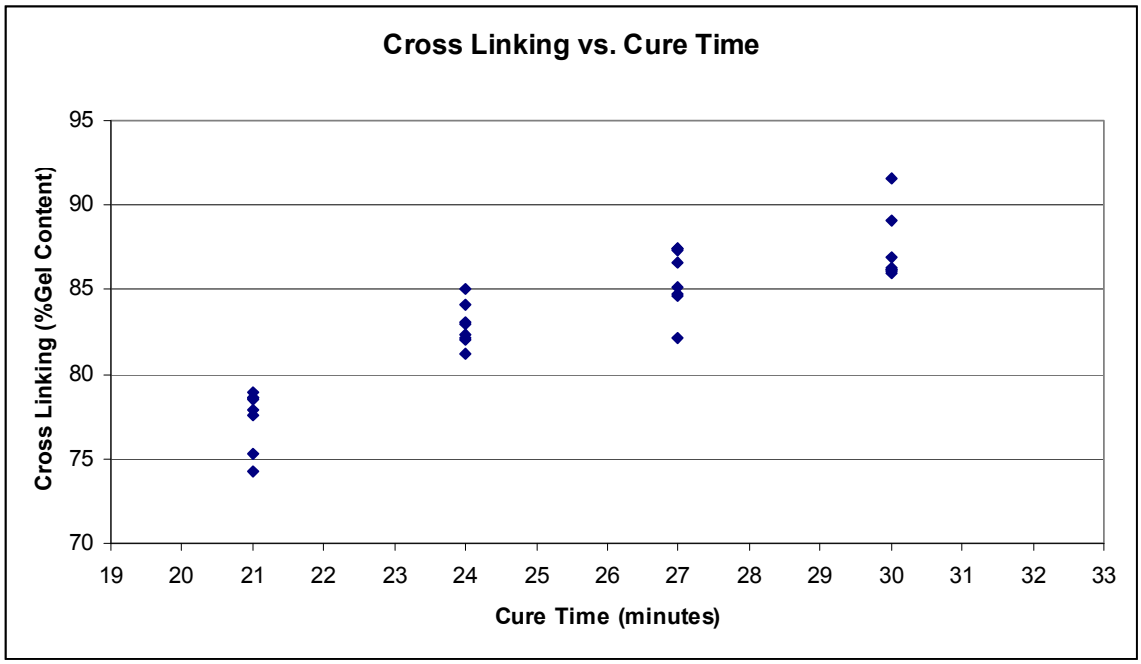


Figure 28. EVA Gel Content vs. Cure Time

The photovoltaic market has used the same backsheet material for many years. This material has proven to be durable, easy to process and reasonably priced. However, recent market pressures have required manufacturers to investigate new materials, which offer the promise of improvements in a number of areas:

- Higher voltage standoff for higher voltage systems
- Brighter for increased module power
- Lower cost
- Greater durability for longer life and higher quality
- Easier processing

A survey of the current market was performed and the following promising backsheet alternatives were identified:

Table 2 . Backsheet Candidates for Investigation

Mat'l	Desc.	Layer 1 Material and Thickness	Layer 2 Material and Thickness	Layer 3 Material and Thickness	Layer 4 Material and Thickness	Mfgr. Code
1	Current	1.5 mil PVF	3 mil Polyester	1.5 mil PVF	none	1
2		1.5 mil PVF	10 mil Polyester	1.5 mil PVF	none	1
3		.8 mil PVDF	3.8 mil Polyester	primer	none	1
4		1.5 mil FP	3 mil Polyester	10 mil EVA	none	2
5		4 mil PET	18 mil EVA	none	none	3
6		.3 mil MPET	6.35 mil WPET	.3 mil MPET	Primer	4
7		Unk.	Unk.	Unk.	Unk.	5

Each of the above materials promises improvements of one or more of the following characteristics:

Table 3. Characteristics of Backsheets under Investigation

Mat'l	Desc.	Voltage Standoff	Brightness	Environmental Durability	Ease of Processing
1	Current	715 V	Off-White	Medium	Medium
2*		1000 V	Off-White	Medium	Difficult
3		840 V	Bright White	Unk.	Unk.
4		1000 V	Bright White	High	Easy
5		Unk.	Bright White	Low	Unk.
6		1000 V	Bright White	Low	Unk.
7		Unk.	Unk.	Unk.	Unk.

* Material offers cost savings in higher voltage systems.

SolarWorld Industries has started evaluation and development programs with the five different suppliers representing six new and different materials. Although some of the materials are similar to the current material in use at SWIA, these are still developmental in nature.

The following materials are in various stages of development:

Table 4. Current Development Stages of Backsheet Materials

Mat'l	Desc.	Development Stage				
		In Development by Supplier	In Test by Supplier	In Test by a Module Mfgr.	Ready for production	In production
1	Current					√
2					√	
3				√		
4				√		
5			√			
6					√	
7		√				

During Phase II, SolarWorld Industries will investigate the benefits of the above backsheet materials including cost analysis, processing comparisons, environmental testing and affects on power.

Summary and Conclusions

The first step toward reducing cost in this PVMR&D was to reduce wafer thickness and wafer cutting wire thickness. The original plan to start piloting wafers at 240 microns showed excessive yield losses. For this reason, the approach was modified to decrease wire thickness first, reducing silicon wasted during cutting. After stabilizing yields with thinner wire, thinner wafers were introduced in two steps, 250 microns then 240 microns. This stepped approach has worked well and has resulted in a 26% improvement in silicon utilization. During Phase I the handling tools, the Back Surface Field (BSF) process, and the confirmation of the environmental integrity of thinner wafers was all accomplished. Efficiency improvement through the use of a Boron Back Surface Field Process has been highly successful producing cells averaging 16.6% with potential to reach 17% conversion efficiency.

Module reliability improvements have begun with lower Light Induced Decay processes being developed and implemented. New glass, EVA and backsheet materials have all been studied with the glass and EVA being deployed in production under Phase I.

These three areas of focus, thinner cells, higher efficiency and more reliable have shown the potential of reducing cost to under $2 per watt.

In summary, the work at SolarWorld during Phase I has progressed well. The goal of $2/Watt (with $30/kg polysilicon) is achievable. The thin wafers and cells, improved efficiency and continued progress on module reliability are all contributing significantly to module cost reductions and improvements. Phase II will continue this work to further develop and implement these improvements.

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1. Jester, T. L. (October 2001). "*Specific PVMat R&D on Siemens Cz Silicon Product Manufacturing Photovoltaic, Final Subcontract Report", June 1998 – September 2001.* Work performed by Siemens Solar Industries, Camarillo, CA.
2. Jester, T. L. (January 2005). "*LID Free Crystalline Silicon Modules", January 2005,* IEEE Photovoltaic Specialist Conference, Orlando, Florida, January 3-7, 2005. Work performed by Shell Solar Industries, Camarillo, CA.

3. Jester, T.L. (October 2001). "*Specific PVMat R&D on Siemens Cz Silicon Product Manufacturing, Final Subcontract Report"*. Prepared under Subcontract No. ZAX-8-17647-14, October 2001

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ORGANIZATION.

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
November 2007	Subcontract Report	July 2005 – October 2006

4. TITLE AND SUBTITLE
Manufacturing Improvements in Cz Silicon Module Production: Annual Subcontract Report, July 2005 – October 2006

5a. CONTRACT NUMBER
DE-AC36-99-GO10337

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
T.L. Jester

5d. PROJECT NUMBER
NREL/SR-520-42418

5e. TASK NUMBER
PVB75301

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
SolarWorld Industries
4650 Adohr Lane
Camarillo, California 93011

8. PERFORMING ORGANIZATION REPORT NUMBER
ZAX-5-33628-07

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSOR/MONITOR'S ACRONYM(S)
NREL

11. SPONSORING/MONITORING AGENCY REPORT NUMBER
NREL/SR-520-42418

12. DISTRIBUTION AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

13. SUPPLEMENTARY NOTES
NREL Technical Monitor: Richard Mitchell

14. ABSTRACT *(Maximum 200 Words)*

This report describes work done by SolarWorld Industries America that focuses on improvements in the cost per watt of Cz modules and improved photovoltaic module manufacturing technology. The focus of the three-year program is to implement a 15%-efficient module in production at under $2/watt manufacturing cost. In addition, the program will develop higher reliability photovoltaic modules. Work on cell thickness reduction, the required electrical and mechanical changes to accommodate these thinner cells, higher efficiency process development, and improved reliability are all described in this annual report.

15. SUBJECT TERMS
PV; silicon; module; manufacturing; cell thickness; high efficiency; cost per watt; wafer thickness; cost reduction; light-induced decay (LID); reliability; back surface field (BSF); Czochralski Si;

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
Unclassified	Unclassified	Unclassified	UL		19b. TELEPHONE NUMBER (*Include area code*)

Standard Form 298 (Rev. 8/98)
Prescribed by ANSI Std. Z39.18