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# Advanced, High-Reliability, System-Integrated 500-kW PV Inverter Development

## Final Subcontract Report
## 29 September 2005 – 31 May 2008

R. West
*Xantrex Technology, Inc.*
*Livermore, California*

***Subcontract Report***
**NREL/SR-520-43839**
**August 2008**

NREL is operated by Midwest Research Institute • Battelle Contract No. DE-AC36-99-GO10337

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NREL Technical Monitor: R.L. Mitchell

Prepared under Subcontract No. ZAX-5-33628-01

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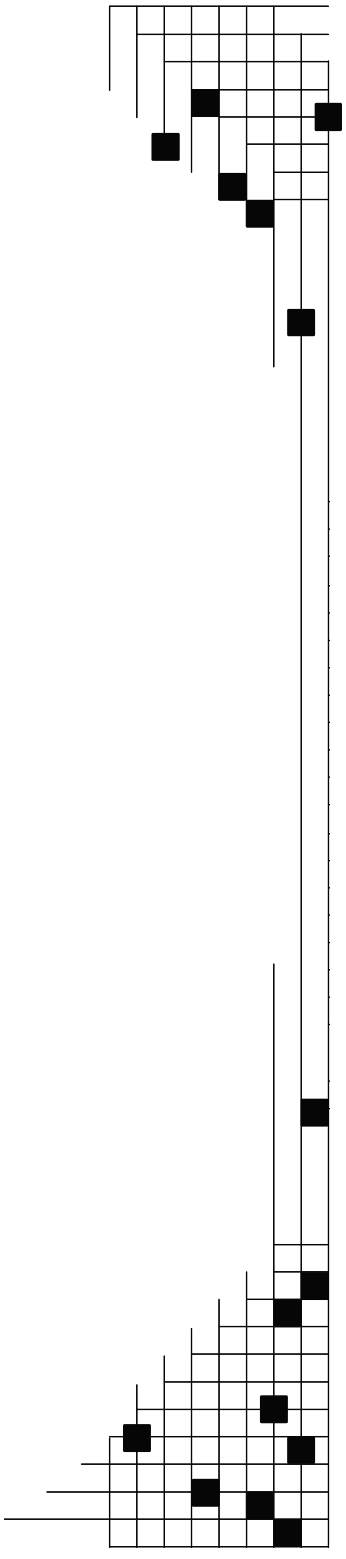

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# 1 OVERVIEW

Under this contract, a prototype 500kW photovoltaic inverter was specified, designed, fabricated and tested. All of the contract goals were met or exceeded. This 500kW inverter is scheduled for commercialization as Xantrex Model GT501.

This Final Technical Report is arranged to first present the outcome of this contract with a brief description of the 500kW inverter, followed by a condensed description of the work accomplished under each of eleven contract tasks.

# 2 500KW INVERTER DESCRIPTION

**Photograph 1 - 500kW Inverter**

## 2.1 CONTRACT ACHIEVEMENTS AND INVERTER FEATURES

| | |
|---|---|
| **Improved Performance** | 44% reduction in power conversion losses |
| **Improved Reliability** | **3**2% extension in mean time to failure |
| **Reduced Cost** | 46% parts cost reduction |
| **Reduced Weight** | 35% weight reduction |
| **Reduced Size** | 56% volume reduction |
| **System Integrated Design** | Includes integrated PV and AC disconnects, PV master combiner, segmented DCGFI, external synchronization for inverter paralleling, 4-circuit array "mover" motor controller, data logging, and multi-format communication interfaces |
| **Optimized for Multi-Megawatt PV Systems** | Designed for direct connection to an external, medium-voltage distribution transformer without the requirement for an internal 60Hz isolation transformer |
| **Plug-and-Play Manufacturing and Repair** | The inverter packaging is based on a number of functional-block subassemblies all interconnected with plug-in cables |
| **High Voltage PV Array Input** | Supports bipolar photovoltaic arrays of up to 1000Vdc pole-to-pole |
| **Advanced Power Conversion Topology** | A patented, multiple bridge power converter topology with interleaved pulse width modulation enables a significant reduction in DC bus and AC line filter components |

The Xantrex PV225 is the basis for all comparisons in this contract except for reliability where the newer Xantrex GT250 was used. All comparisons are normalized per kilowatt, except for reliability. Contract goals were all 25% improvements.

## 2.2 INVERTER PERFORMANCE SPECIFICATIONS

| | |
|---|---|
| Rated continuous power, nominal AC line | 500kW |
| Maximum AC power output, high AC line | 525kW |
| Grid-tie voltage, nominal | 360Vac |
| Maximum AC current | 800 Amps rms |
| CEC power conversion efficiency | 98% |
| | |
| PV array configuration | Bipolar (+ and – ground) |
| Maximum PV open circuit voltage, per monopole | 500Vdc |
| Maximum PV MPPT range, per monopole | 250Vdc to 500Vdc |
| | |
| Maximum PV current | 1000A |
| DCGFI circuits | 4 circuits, ¼ array disable |
| Master PV combiner circuits | 16 x 200A max fuse size |
| Master PV combiner string monitoring | 8 circuits |
| | |
| Dimensions | 8’W x 2’D x 6’H |
| Weight | 1500lbs |
| Cooling | Forced convection |
| Enclosure environmental integrity | Nema 3R |
| Operating temperature range | 0°C to +40°C |
| | |
| Safety design standard | UL1741 |
| Grid interconnect design standard | IEEE1547 |

## 2.3 INVERTER ARCHITECTURE AND PACKAGING

The packaging design of the 500kW inverter is substantially different from state-of-the-art photovoltaic power converters. The approach uses functional-block subassemblies to reduce the cost of manufacturing, servicing and repair. Each functional-block module has a high degree of integration. In contrast, the packaging of all other state-of-the-art PV inverters, employ a myriad of distributed current sensors, voltage sensors, fuse blocks, contactors, power supplies and printed circuit boards all wired together by hand or by the use of hand-made wiring harnesses. Many of these connections are made with *fast-on* or screw terminal type connections that are less reliable than the soldered connections used in the PCB based functional-block approach.

To "build' an inverter using the functional-block approach, subassemblies are mounted into the enclosure shell and then connected with plug-in cables. Power conductors and bus bars are added and the "build" is complete. This method will inherently produce a more consistent, quality-controlled product because the number of possible assembly and manufacturing variables are substantially reduced. This method is also more suited for high-volume manufacturing.

The "functional" part of this descriptive means that each functional-block can perform autonomously to verify subassembly function before being run with other pre-tested subassemblies as a complete system. The way these inverter functions are split is critical and is optimized for field fault identification and ease of subassembly swap-out.

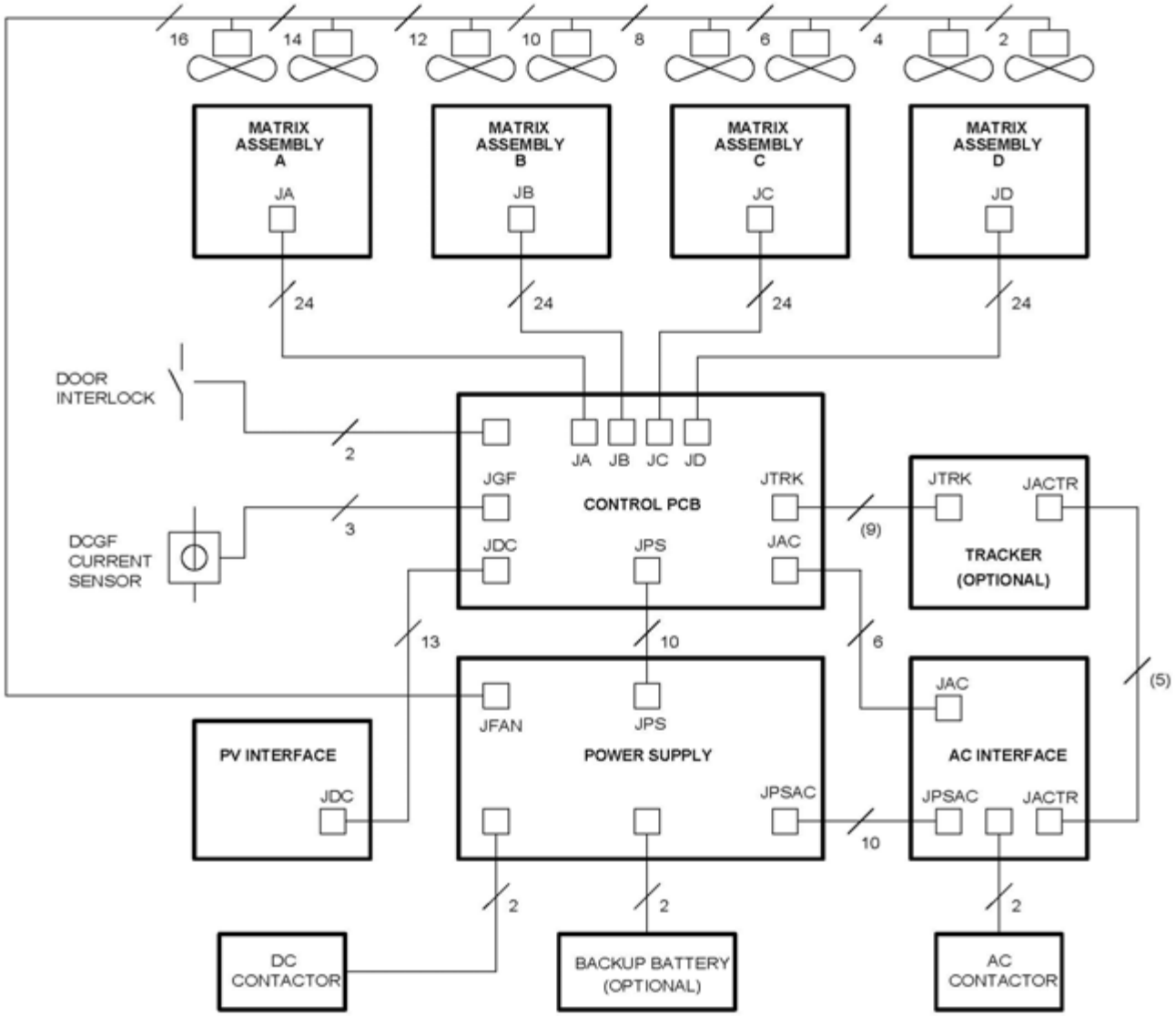



**Figure 1 - 500kW Inverter Functional Block Architecture**

# 3 WORK DESCRIPTION BY TASK

The work on this contract was done in two phases divided into 11 tasks. Phase I includes Tasks 1 through 7 and was dedicated to studies, modeling, calculations, cost estimates and design of the 500kW hardware. Phase II includes Tasks 8 through 11 and was dedicated to control firmware design and the fabrication and test of the 500kW inverter prototype hardware.

## 3.1 TASK 1 - INVERTER ARCHITECTURE

The overall goal of this contract was to determine the added value of a multi-megawatt PV power plant designed to operate at PV open circuit voltages greater than 600 volts and, subsequently, define a higher-performance and more cost-effective inverter architecture. In Task 1 a feasibility study was done by first creating a selection matrix of 288 possible array and inverter topology combinations. Initially 75% of the combinations were rejected by qualitative analysis by lack of comparative value to other options in the matrix. The remaining 25% of combinations were evaluated by engineering and cost analysis. A list of some of the selection matrix variables are presented below:

- Monopolar grounded PV array
- Floating PV array
- Bipolar grounded array
- Use of PV modules with >600V module-to-frame rating
- Use of higher voltage electrical ancillary BOS (excluding inverter) equipment
- Inverter topologies with single voltage boost stage
- Inverter topologies with dual voltage boost stages
- Inverter topologies with 1700V vs. 1200V silicon semiconductors
- Inverter topologies driving dedicated floating Delta connected grid interface
- Transformer-less inverter topologies driving grounded WYE grid interface
- Inverter topologies with multiple vs. single 3-phase bridge(s)
- Inverter topologies with active Voc (PV open circuit voltage) limiting

In the final analysis, an optimum inverter architecture was defined as follows:

- Bipolar grounded array with 1000Vdc max pole-to-pole Voc
- No voltage boost
- 1200V silicon
- Multiple 3-phase bridges
- Delta-connected at low side of distribution transformer

Three proprietary circuits were developed during this contract to greatly enhance the viability and value of this approach.

1. A circuit to allow the inverter to regulate a grossly imbalanced bipolar PV array.
2. A circuit to allow higher efficiency, lower cost 1200V silicon to be used safely with higher open circuit voltage PV arrays to significantly enhance silicon utilization.
3. A power converter topology with four 3-phase bridges operating with interleaved switching frequencies to effectively quadruple the switching frequency of the inverter to reduce the cost, size, weight and losses associated with all power filter components. (US Patent # 7,046,527)

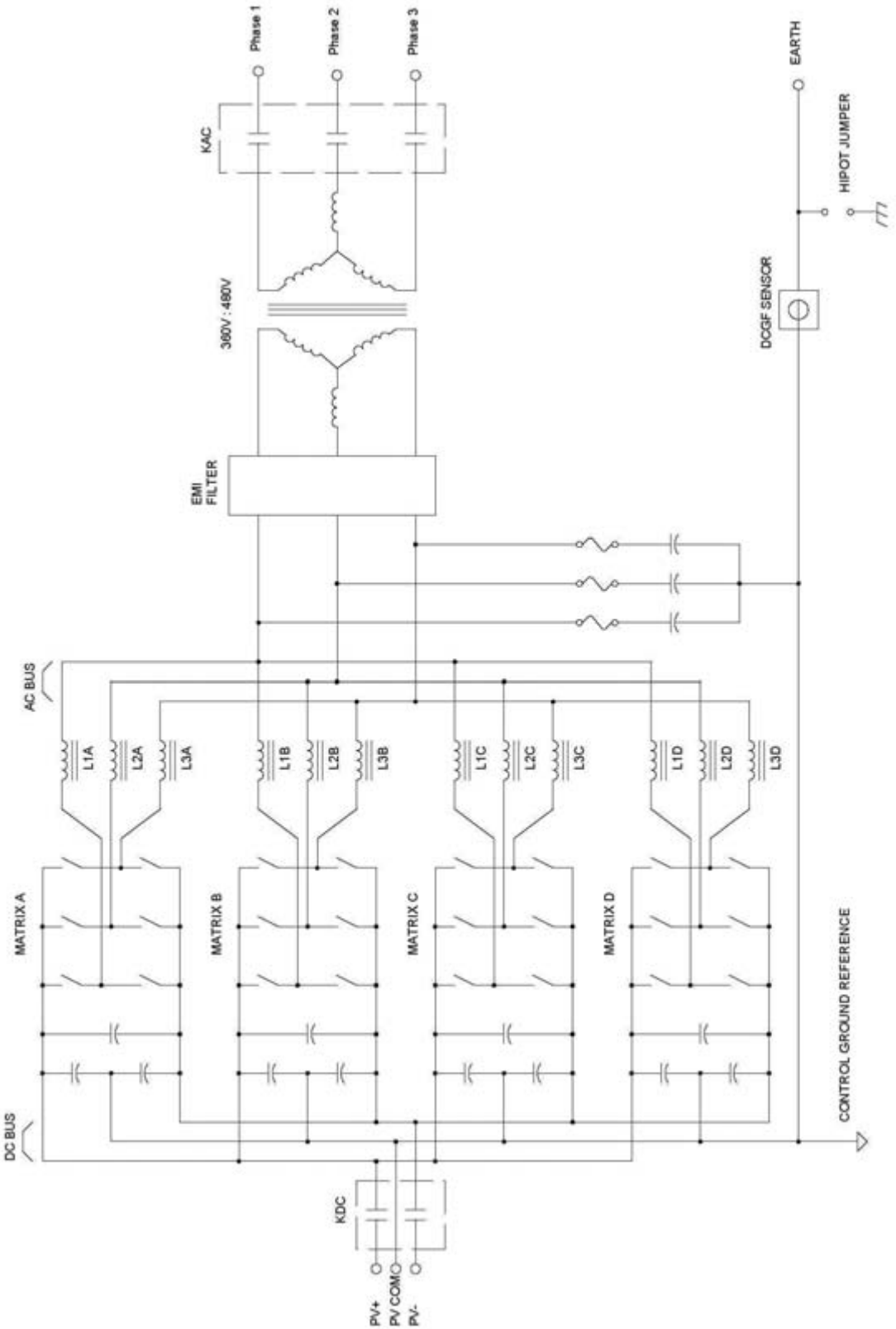



**Figure 2 - Inverter Power Architecture**

## 3.2 TASK 2 - INVERTER PRODUCT SPECIFICATIONS

In Task 2, the form, function and reliability of a 500-kW inverter were defined. Reliability enhancement design rules were established for projecting the mean time before failure (MTBF) with respect to state-of-the-art equipment. IEEE 1547 was reviewed for inclusion in the inverter functional specifications. Also, advanced grid interaction features were evaluated based upon input from potential end users. To ensure that the inverter specification supports typical system requirements, a design for a multi-megawatt PV power plant was completed to further improve the degree of integration between PV, inverter, and non-inverter BOS. A design review meeting was held for all 500kW inverter project participants and contributors. A formal, detailed functional specification for the 500kW inverter was completed to serve as the reference document for all following design tasks. See Section 2.2, Inverter Performance Specification

## 3.3 TASK 3 - HIGH POWER ELECTRONICS AND PACKAGING

In Task 3, the high power portions of the inverter were designed; the bridge matrix subassembly, the line filter chokes and the inverter cooling system. The design of each of these three elements cannot be optimized without considering the impact on the other two and the packaging design as a whole.

### *3.3.1 BRIDGE MATRIX SUBASSEMBLY DESIGN*

Four bridge matrix assemblies are required for each 500kW machine. The bridge matrix is the "muscle" of the inverter and contains three high power, half-bridge IGBT (Insulated Gate Bipolar Transistor) modules, heatsink and mounting panel. Other functions that are typically not integrated on an assembly with the power modules are IGBT gate drives, isolated IGBT drive power supplies, line current sensing and fault detection. Other advancements include isolated *wire* drive signals from the control board in place of six separate fiber optic cables, transmitters and receivers. The wire drive signals are included in the single plug-in cable that contains all of the other required control and sense signals.

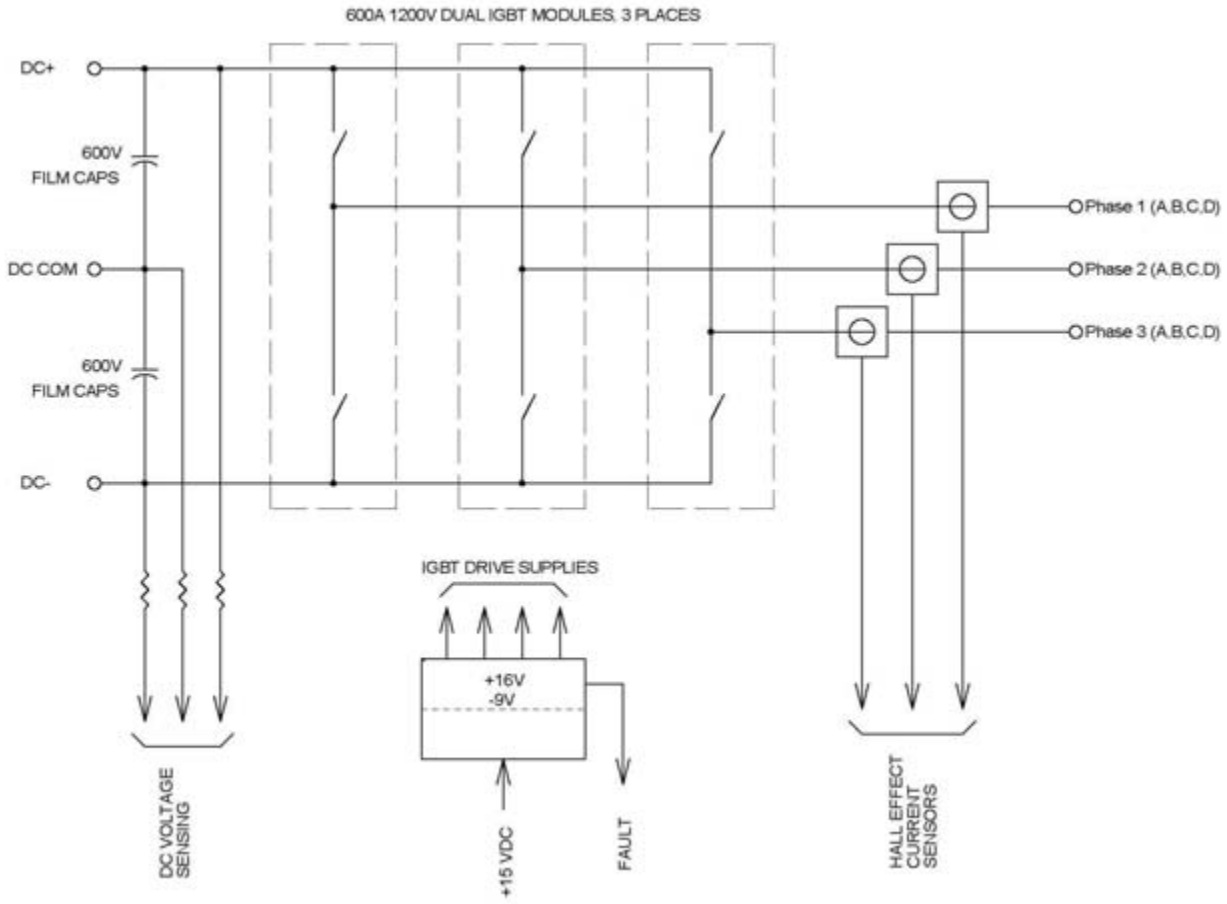



**Figure 3 - Bridge Matrix Assembly Schematic Diagram**

### *3.3.2 LINE FILTER CHOKE DESIGN*

High reliability magnetic components using advanced core materials will be designed. Core materials and configurations for the magnetic components will be analyzed and optimized with respect the contract goals of cost, weight and size reduction.

The 500-kW inverter configuration selected utilizes four 3-phase inverter bridges, each operating at 125-kW. These bridges will be operated in a time-skewed arrangement to provide ripple current cancellation at the point where the four bridges are connected. This arrangement allows each inductor to operate at a higher ripple current while reducing the strain on DC bus capacitors and AC line filter capacitors. This higher ripple current translates into lower inductance, and the opportunity to reduce the size of the inductors.

Four inductor configurations were considered:

- Single-phase E-core
- Three-phase E-core
- U-core
- Toroidal core

Several magnetic materials with low core losses suitable for operation at this power level were considered:

- Amorphous metal tape-wound cut-cores
- JFE steel proprietary high-silicon steel blocks
- Other proprietary cores

Single-phase E-cores for high-frequency inductors may be configured from two sets of C-cores placed side-by-side. Three of these inductors would be required for one bridge, for a total of 12 inductors in the 500-kW inverter.

A three-phase E-core utilizes three coils on one three-leg core. One of these inductors would be required for each three-phase bridge, for a total of 4 inductors.

A U-core may be wound with one or two coils. The two-coil configuration has the advantage of reducing the total length per turn of copper. This in turn reduces the weight and dissipation of the inductor, at the expense of higher manufacturing costs. The two-coil version has been examined for its advantages in weight and dissipation.

Four different combinations of inductor material and construction were analyzed.

| PART | WEIGHT REDUCTION | COST REDUCTION | SIZE REDUCTION |
|---|---|---|---|
| 1-PHASE AMORPHOUS E-CORE | 22% | 41% | 33% |
| 3-PHASE AMORPHOUS E-CORE | 40% | NA | 51% |
| JFE U-CORE | 26% | 33% | 29% |
| TOROIDAL CORE | 40% | 26% | 38% |

**Table 1 - Inductor Comparison Summary**

Other design goals for the new 500-kW inverter are to achieve the lowest possible audible noise while maintaining the highest possible conversion efficiency. The toroidal inductor meets this goal while also meeting the goal of a 25% reduction in weight, cost, and size. The higher cost of the toroidal inductor, compared to the u-core inductor, amounts to a premium of $3.55 per Watt, which is less than the $5 to $6 per Watt installed cost of additional the PV modules required to make up the difference in losses.

### *3.3.3 INVERTER COOLING SYSTEM DESIGN*

The 500kW inverter has a power conversion efficiency of 98%. The 2% or 10,000 Watts of power that is not converted into AC power is converted into heat which must be removed from the inverter enclosure. The 500kW inverter heat removal system is an air-cooled, forced convection system. The fans draw air from outside the enclosure through rainproof, screened vents located at the top front of the enclosure. This intake air is first directed through the cooling fins of the power matrix heatsinks. These heatsinks provide heat removal for the IGBT (Insulated Gate Bipolar Transistor) power modules, the most heat sensitive components and the components generating the most heat. Next, this air is directed past twelve line filter inductors, the second highest heat producing elements. From there, the air flows into an expansion chamber and through rainproof, screened exhaust vents on the back of the inverter enclosure.

The bridge matrix assembly contains IGBT modules, the silicon semiconductor power switching elements that do most of the power conversion "work". There are two primary IGBT loss mechanisms, conduction losses and switching losses. The IGBT losses produce approximately ⅔ of the total inverter waste heat or 6,670 Watts. In general, cooling of the IGBT modules drive the design of the entire inverter cooling system.

The second greatest heat producing components in the 500kW inverter are the filter inductors. There are two primary loss mechanisms, core losses and copper losses producing approximately ⅓ of the total inverter waste heat or 3,370 Watts.

A number of variables were considered in the overall cooling system design such as, heatsink type and fin profile, fan type and quantity, intake porting, exhaust porting, plenum and baffle geometries, back pressure, soiling, turbulent (impingement) vs. laminar flow, cost, electrical efficiency, reliability, redundancy and ease of service.

The thermal performance for the 500KW inverter was validated for the specified maximum ambient air temperature of 40°C and with enough thermal margin to allow operation with 50°C intake air. The cooling system design provided balanced margins on the two component groups

generating the most heat, the IGBT modules and the filter inductors. The extensive thermal modeling done in the design phase was key to providing finished hardware that meets and exceeds the requirements of the functional specification and the goals of this subcontract task.

The work on this task resulted in a >25% reduction in the normalized cost, weight, and size of the inverter bridge matrix, magnetic components and heat removal system for the 500-kW inverter when compared to a state-of-the-art 225-kW inverter. In addition, a >25% extension in the Mean Time Before Failure (MTBF) for all critical components was achieved.

## 3.4 TASK 4 - LOW POWER ELECTRONICS AND CONTROL

In Task 4, three low power subassemblies were designed; the power supply, the analog control board and the digital control board.

### *3.4.1 POWER SUPPLY DESIGN*

The power supply is a PCB based subassembly that provides regulated low voltage power to the control board, current sensors and other low power devices not on the control board. The power supply design has multiple SMPS (Switch Mode Power Supply) circuits as well as AC and DC solid state relays for driving inverter system peripherals such as contactors coils and heaters.

### *3.4.2 ANALOG CONTROL BOARD DESIGN*

The analog control board is designed to run all four power switch matrices at full output current and at full bus voltage into a short circuit. The analog control board will have all of the functions required to protect the power hardware and test personnel.

Figure 2 is a block diagram of the analog control board regulation functions.

A proprietary regulation methodology will be used where the pulse width modulation (PWM) of each four power switch matrices is phase shifted by 90º at the PWM switching frequency with respect to the next matrix to achieve a significant cancellation of switching frequency ripple current at the output and summation point of all four matrices. This function is implemented on the analog control board by generating four PWM triangle waves (and clocks) which are out of phase by 90º.

Three sinewave current references are generated digitally using a counter, three PROMs and three digital-to-analog converters. The amplitudes of the three current references are controlled by three multiplier circuits where one multiplicand of each circuit is connected to a potentiometer. The potentiometer is adjusted by test personnel to simultaneously program all output currents from 0-current to full-current.

Each of the twelve analog current regulator circuits compares the feedback from current sensors to the current reference for a given phase on a given matrix. An error signal is generated from the difference of the actual sensor current and the reference current. This error signal is the compared to one of the triangle waveforms creating a PWM pulse train. In this way, the bridge power switches are operated as part a servo loop. A cycle-by-cycle current limit circuit will terminate a given PWM “on” pulse should the current limit be exceeded. This current limit circuit is the primary protection mechanism for the power semiconductor switching devices. Also, latches are included to prevent double pulsing at transitions. Drive signal circuits provide dead-time and cross-conduction protection.

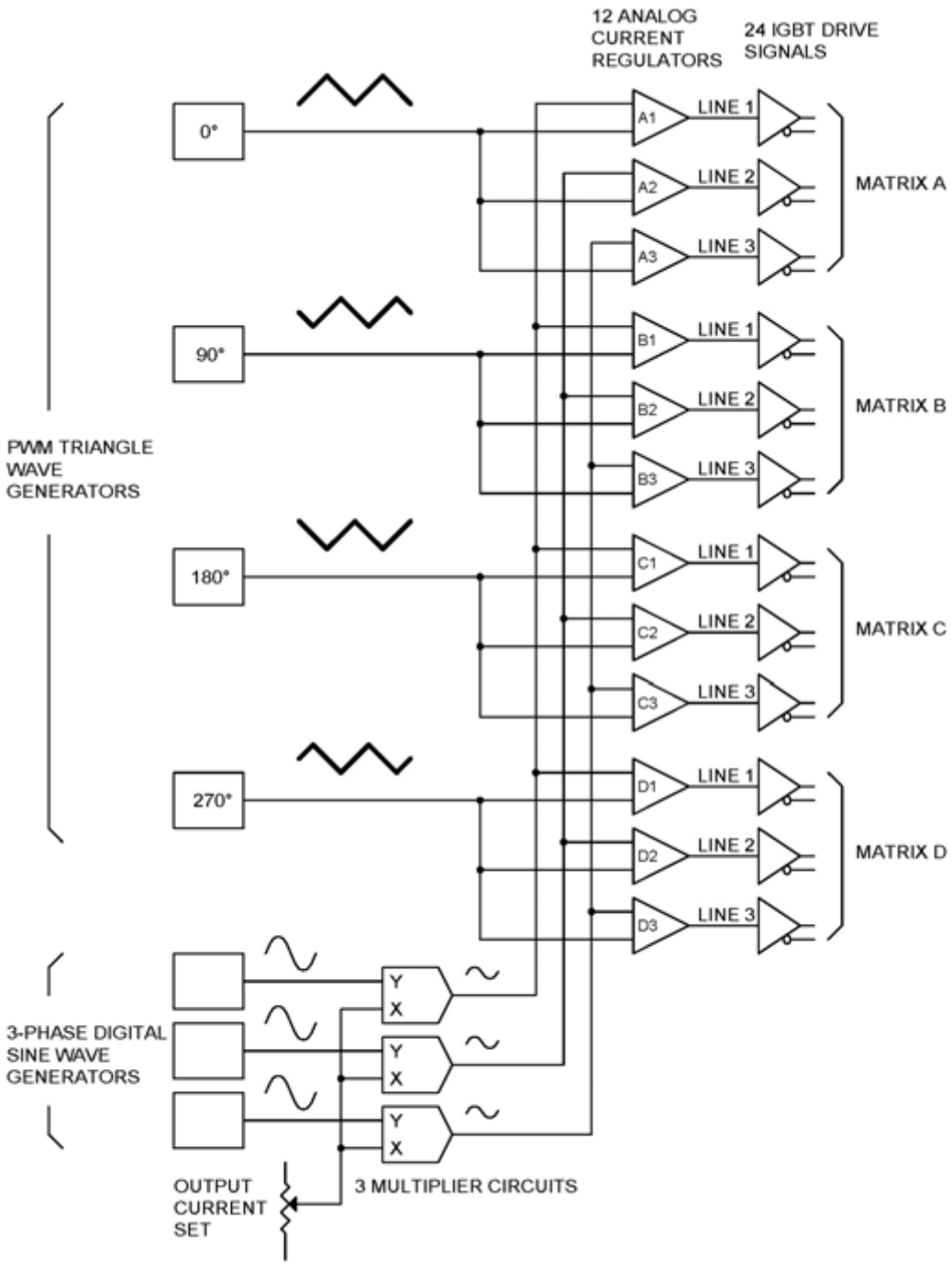



**Figure 4 – Analog Control Board Regulation Circuits**

The analog control board detects and enunciates seven distinct fault conditions. Any one of these faults will shut down the inverter instantaneously. Each power switching matrix detects undervoltage IGBT gate drive faults and overcurrent faults. The overcurrent faults are sensed by high (desaturated) IGBT collector to emitter voltages. These four faults, matrix faults A, B, C and D, are reported to the control board. DC bus voltages that exceed 500Vdc on either monopole are detected by the analog control board and reported as an overvoltage bus fault. Out of tolerance +/-15Vdc and +3.3Vdc supplies are detected on the analog control board and reported as an undervoltage power supply fault. All matrix temperatures are monitored, the highest temperature is selected and reported as an overtemperature fault should preset limits be exceeded.

All of the fault detection is designed to protect the IGBT semiconductor power switching devices no matter what PWM pulse train is being commanded by the current regulator circuits. The switches are protected from overcurrent by two methods, desaturation and feedback current comparison to a trip level. The overvoltage bus and overtemperature faults insure that the voltage rating or the temperature rating of the switches is not exceeded.

The fault logging is accomplished by seven flip-flops which capture and hold the identity of the fault that has caused the machine to shutdown. LED lamps display the latched information. The fault logging is important for troubleshooting when determining cause and effect relationships.

The master latch is controlled by simple “stop” and “start” pushbutton switches. The control logic will not allow the power electronics to start when any fault is active. The “start” pushbutton clears all fault latches to re-arm the latches for the next possible fault.

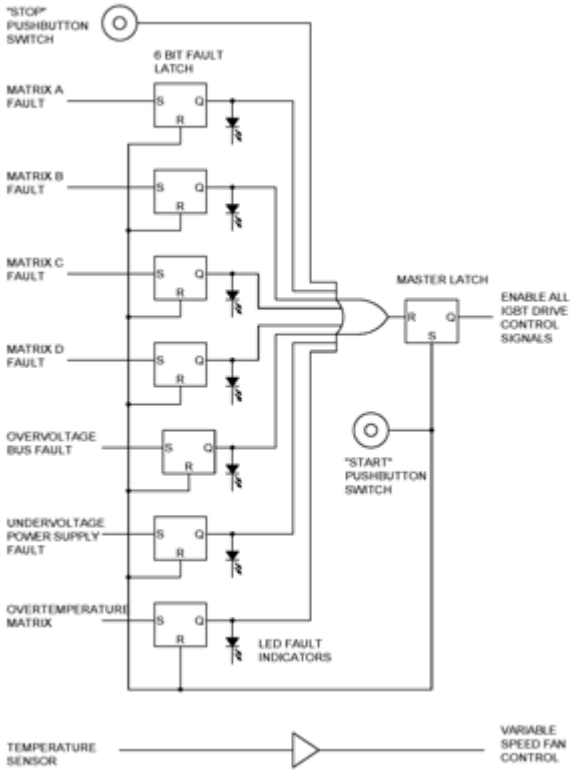



**Figure 5 - Analog Control Board Fault Detection**

### *3.4.3 DSP CONTROL BOARD DESIGN*

The design of a digital signal processor (DSP) based control board was also completed. The digital control board provides all of the regulation and fault protection included on the analog control board plus:

- An inverter state machine
- Automated startup and shutdown
- PV maximum power point tracking
- Anti-islanding
- Serial communications
- Data logging

The DSP board receives operational power from the power supply board. Analog and digital signals arrive to the DSP control board through a variety of sensors. The analog signals are filtered to remove noise and converted to digital form through A/D converter circuitry. Software implemented in the DSP makes the IGBT device control decisions and signals are sent to switch the transistors on and off. Analog control signals are sent through D/A converters. Binary Inputs and Outputs are also implemented.

There are two documents describing the design of the DSP Control board.

- DSP Control Board Functional Specification
- DSP Control Board Hardware Design

A few of the key items from those documents are given in the following sections.

Figure 6 is a block diagram showing the key functions of the DSP control board. The key operational blocks are given in a simplified format that shows “one line” representative signals.

A key architectural decision is to use two separate microprocessors for this control board. One, the DSP, will be used for control purposes and a second chip will be used for communications functions. This was determined to be the optimal solution for software development and allows the decoupling of key control and protective functions from the communications functions. This will facilitate the third party certification of this product and allow enhanced flexibility in future software and functional upgrades.

The FPGA (Field Programmable Gate Array) will also be used to implement some of the glue logic for the interfaces between the processors and their peripherals to minimize the number of integrated circuits on the DSP board. Binary inputs and outputs will also pass through the gate array which will also reduce the chip count and improve reliability.

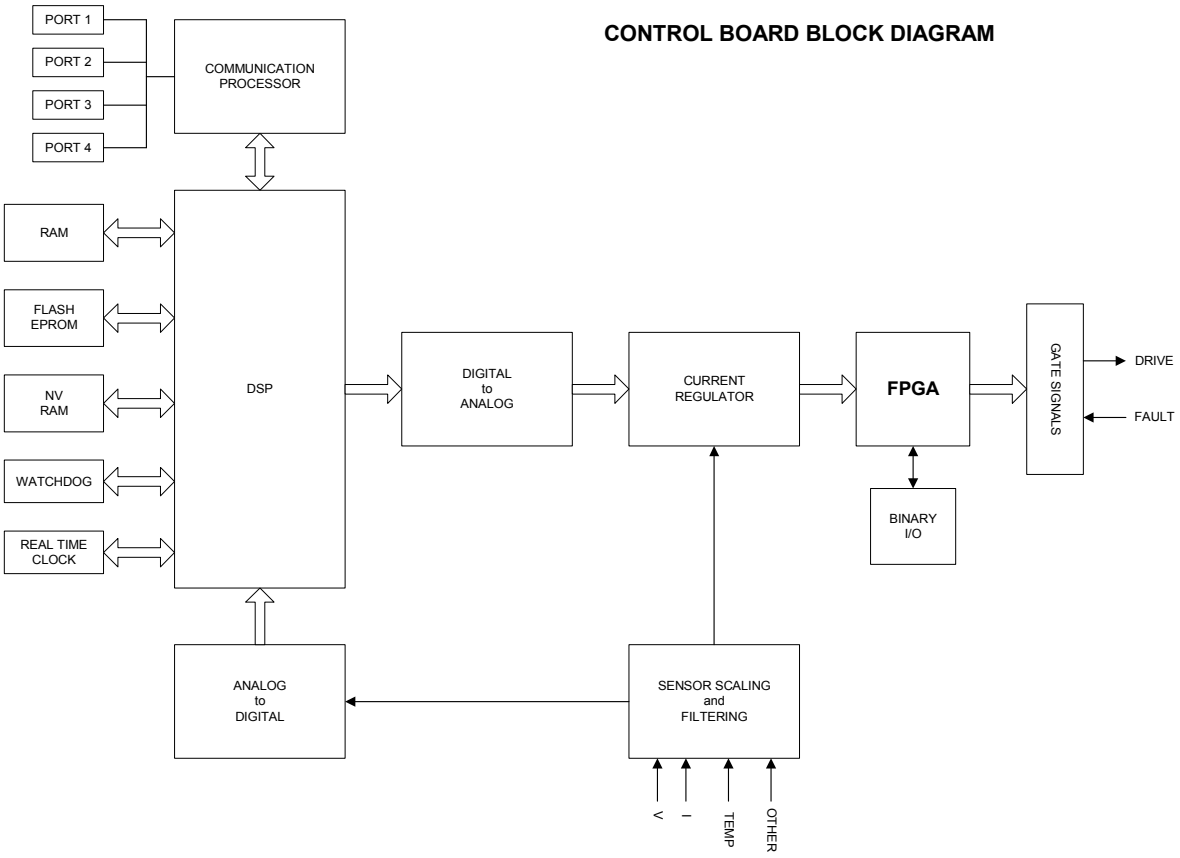



**Figure 6 - DSP Control Board Block Diagram**

The DSP chip that has been selected is the Texas Instruments TMS3206713. This is a high performance Floating Point processor which will allow for advanced algorithms to be efficiently implemented and also provide for future expansion. It is also very reasonably priced. The communications processor will be the Freescale MCF5282 chip from the "Coldfire" family of microprocessors. This is a highly integrated part that has communications ports built in. Development tools for both processors are being procured. The breakdown of functions between the two processors is given in Table 2 below.

| Function | DSP | Communications |
|---|---|---|
| Inverter state machine | X | |
| Fault detection | X | |
| Power Tracking | X | |
| Anti-islanding | X | |
| Phase rotation auto detection | X | |
| Voltages and currents calculations | X | |
| Matrix control | X | |
| Common mode modulation | X | |
| External communications | | X |
| Data recording (NVRAM & RTC) | | X |
| Fault history recording (NVRAM & RTC) | | X |
| Oscillography (NVRAM) | | X |
| Software Downloading | X | X |
| Analog inputs | X | X |
| Analog outputs | X | |
| Digital inputs | X | |
| Digital outputs | X | |

**Table 2 - Processor Task Assignments**

The work on this Task 4 resulted in a >25% reduction in the normalized parts when compared to a state-of-the-art 225-kW inverter. Inverter performance and capabilities were also significantly enhanced.

## 3.5 TASK 5 - DESIGN OF SYSTEM INTEGRATED FEATURES

In Task 5, features and capabilities were designed into the 500kW inverter to enable a low-cost, high-performance, pre-engineered system solution for multi-megawatt PV systems. Three areas were addressed:

(1) A four-channel, single-axis PV array motive drive tracker controller was designed

(2) An optimized AC collection and distribution system for multi-megawatt PV power plants was defined and a synchronization circuit designed to allow parallel-connected inverters to share a common distribution transformer

(3) A DC ground fault interrupt (DCGFI) device was designed for integration with the inverter.

### *3.5.1 SINGLE-AXIS ARRAY TRACKER MOTOR CONTROLLER DESIGN*

The most common mechanical photovoltaic array tracking method is single-axis, east-to-west tracking. In the lower 48 states, single axis tracking provides, on average, a 37% increase in annual energy harvest compared to fixed plate installations. Adding a second tracking axis, north-to-south, will increase annual energy production by an additional 13% over single-axis tracking alone. From a system dollars/AC kilowatt-hour perspective adding second-axis-capability is not often cost effective, especially in locations where the value of the energy produced in summer months exceeds that of winter months.

Dual axis trackers are typically more than twice the cost of single axis trackers. Dual axis trackers must be more mechanically robust because the plane of the array must be located at a higher elevation above grade than single axis trackers and are therefore subject to higher wind loads. Also, dual axis trackers are held at a point instead of a line. Dual axis trackers are more complex and must have two drive motors and two control channels. Dual axis trackers also require significantly more real estate than single axis trackers in multi-tracker systems.

Single axis tracking has been made even more cost effective by using high strength industrial linear actuators to track multiple single axis arrays. The individual single-axis arrays are linked similar to the workings of a Venetian blind. This approach simplifies and reduces the cost of single-axis tracker designs. Furthermore, if the plane of array on each single axis array is coincident with the axis of rotation, a very significant wind load torque cancellation is had that limits the wind-induced tension and compression on the linear actuator for additional cost reductions and/or reliability enhancements.

Fractional horsepower, 3-phase motors, drive the linear actuators used in this scheme. The motors are coupled to the linear actuator through a gear reducer mechanism. A motor run time of 30 minutes would not be atypical to drive an actuator form full retraction to maximum extension.

The 500kW inverter-integrated tracker controller design can drive four linear actuators each capable of positioning a 125kW photovoltaic subarray. The master controller is resident on the inverter control board and is the brain behind the tracker controller brawn. The master controller communicates with the tracker controller over a simple parallel data communication link.

When a photovoltaic installation is commissioned, certain parameters must be programmed into the master controller a user interface keypad. These parameters are site longitude, site latitude, the width of the arrays, the spacing between the arrays, the Greenwich Mean Time and date. The arrays will be positioned on-axis with the sun according to the calculated clock-calendar position of the sun whenever array-to-array shadowing does not occur and within the mechanical limits of the tracking system.

The daily rotation of the subarrays is as follows. During the night, all subarrays are horizontal to prevent array-to-array shadowing at the low angle of sunrise. As the sun ascends, the arrays begin to track west just enough to prevent shadowing. The arrays will track on-axis to the sun in the morning at an angle of approximately 45 degrees. The array position will remain on axis with the sun, through a horizontal position at noon to approximately 45 degrees east in the late afternoon. Just before array-to-array shadowing occurs, the arrays will begin to back track and stop again at a horizontal position for the night.

There are also other tracking options for special conditions. If maintenance or inspection is required on a subarray, manual tracking can be performed by commands entered on the inverter user interface keypad. The inverter master controller may also be programmed to read an anemometer input and stow the arrays horizontal in high wind conditions. The proposed tracker controller is contained within the inverter enclosure to eliminate the mounting, conduit runs and wiring of an external controller. The position of the subarrays must, as with any other tracker, be sensed at the subarray being rotated. The proposed tracker controller uses a simple, effective, accurate, low cost and safe method for tracking a subarray.

The inverter-integrated tracker controller approach will be compared to two other commercially available solutions. There is a prepackage single-axis tracker solution available from Enhancement Electronics called the SolarTrak. Four of these would be required to track the four 125kW sub arrays that make up a 500kW system. This product has been used in a number of commercial PV systems. Another typical solution is to use an industrial programmable logic controller (PLC). This approach has also been used in a number of commercial PV installations.

The costs of the proposed inverter-integrated tracker controller and the two commercial solutions sited are tabulated below.

**Table 3 - Tracker Controller Retail Price Analysis**

| Tracker | Qty Required | Ext Price | Relative Cost |
|---|---|---|---|
| Inverter-Integrated | 1 | $1795 | 1.00 (reference) |
| EEI SolarTrak | 4 | $7200 | 4.01 |
| Square-D PLC | 1 | $8177 | 4.56 |

The contract goal was to demonstrate a 25% cost reduction in PV system single-axis tracking control costs. A cost reduction of 75% to 78% was achieved. The inverter-integrated tracker controller has proven much more cost effective for the following reasons:

By integrating the tracker controller into the inverter enclosure, the cost of a tracker controller enclosure, user interface keypad and micro controller are essentially eliminated from the tracker controller cost equation. These items are already included in the inverter and the burden of these added tracker controller functions on the inverter infrastructure is negligible.

Other system advantages are had with the inverter-integrated tracker controller that are not easily quantifiable in comparison to the other sited solutions:

- The cost of installing a support structure and conduits for a non-integrated tracker controller solution has a negative impact on system installation costs and esthetics.
- The inverter has a comprehensive data acquisition system that can report tracker faults to the PV system's technical monitoring staff. This is a capability not had with the other two tracker solutions.

### *3.5.2 AC COLLECTION STUDY FOR MULTI-MEGAWATT PV POWER PLANTS*

Three AC power collection approaches were considered, each resulting in a system-integrated transformer subassembly design. The transformer subassembly designs each include a distribution transformer, primary and secondary overcurrent protection and a high-side disconnect switch. Three solutions are outlined below for AC power collection in a 2 megawatt PV power plant with four 500kW inverters. Three solutions will be compared for cost, performance and commercial feasibility.

- **Solution #1** - Four 500kVA transformer subassemblies, one for each inverter.
- **Solution #2** - One 2000kVA transformer subassembly with common low voltage winding shared by all four inverters.
- **Solution #3** - One 2000kVA transformer subassembly with four separate 3-phase low voltage windings, one for each inverter.

#### 3.5.2.1 SOLUTION #1

Figure 7 shows a transformer subassembly electrical schematic for Solution #1 where each 500kW inverter connects to a dedicated 500kVA distribution transformer. Figure 8 shows how four inverter-transformer pairs would connect in a 2 megawatt PV system based on Solution #1. Solution #1 is the typical method for AC power collection in multi-megawatt PV power plants. This solution has the advantage of scalability in 500kW increments. This solution also has lower conductor losses because the AC power is boosted to a higher transmission voltage at the source, the inverter.

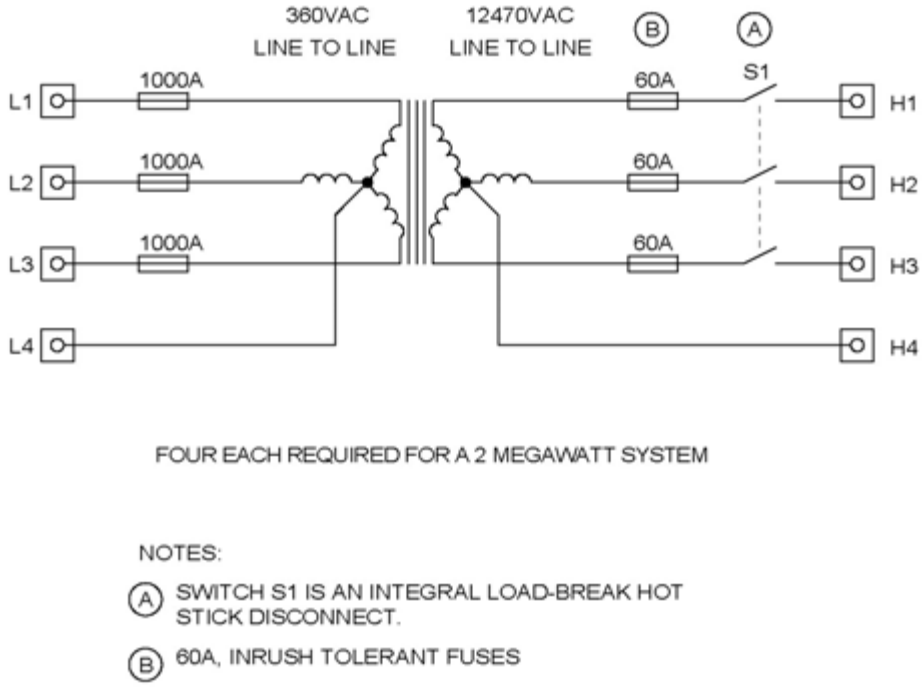



**Figure 7 - Solution #1, 500KVA Transformer Subassembly Schematic**

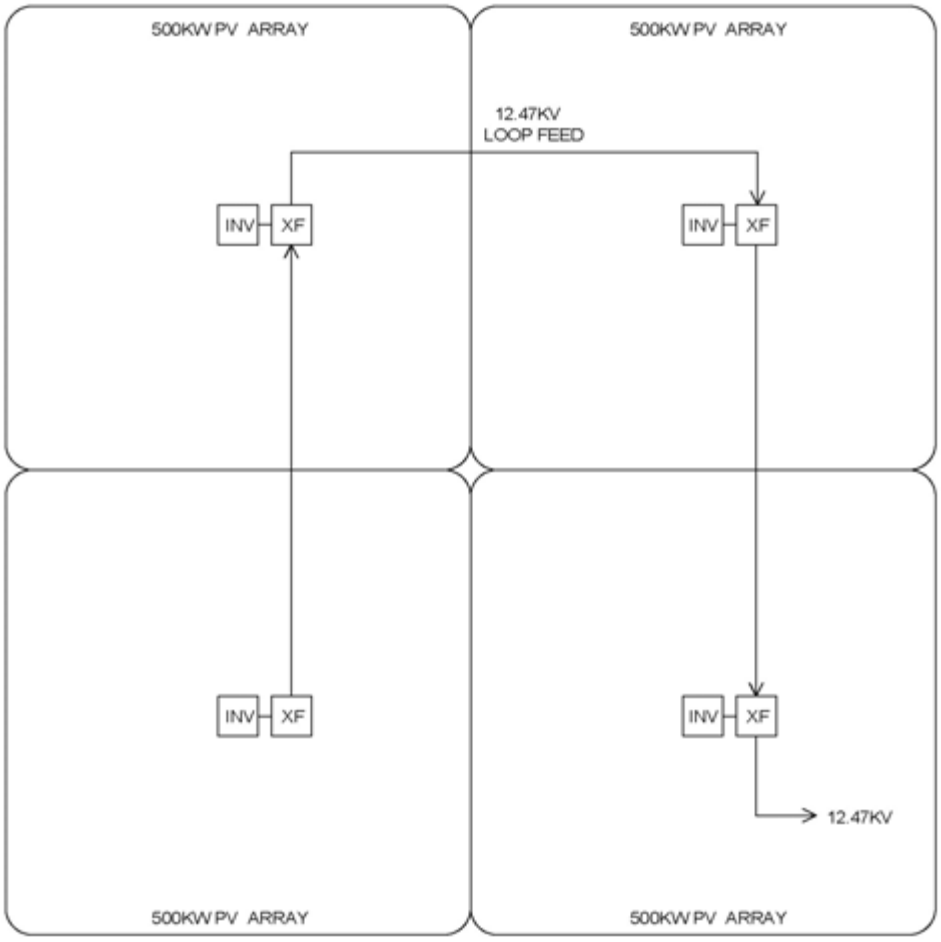



**Figure 8 - Solution #1 Field Layout, 4 x 500KVA Transformers**

#### 3.5.2.2 SOLUTION #2

Figure 9 shows a transformer subassembly electrical schematic for Solution #2 where one 2000kVA transformer is used and where the low side of the transformer subassembly includes a power distribution circuit to protect the 3-phase feeds from the four individual inverters. Figure 10 shows how the one transformer and four inverters would connect in a 2 megawatt PV system based on Solution #2. The Solution #2 advantage is lower transformer subassembly costs for a given power conversion efficiency. With this approach, one transformer, one set of high voltage fuses and one high voltage disconnect are amortized over the entire 2 megawatt system for a 75% reduction in the number of these components when compared to Solution #2. It should also be noted that larger transformers are significantly more efficient, smaller, lighter and less expensive on a normalized, per kVA basis.

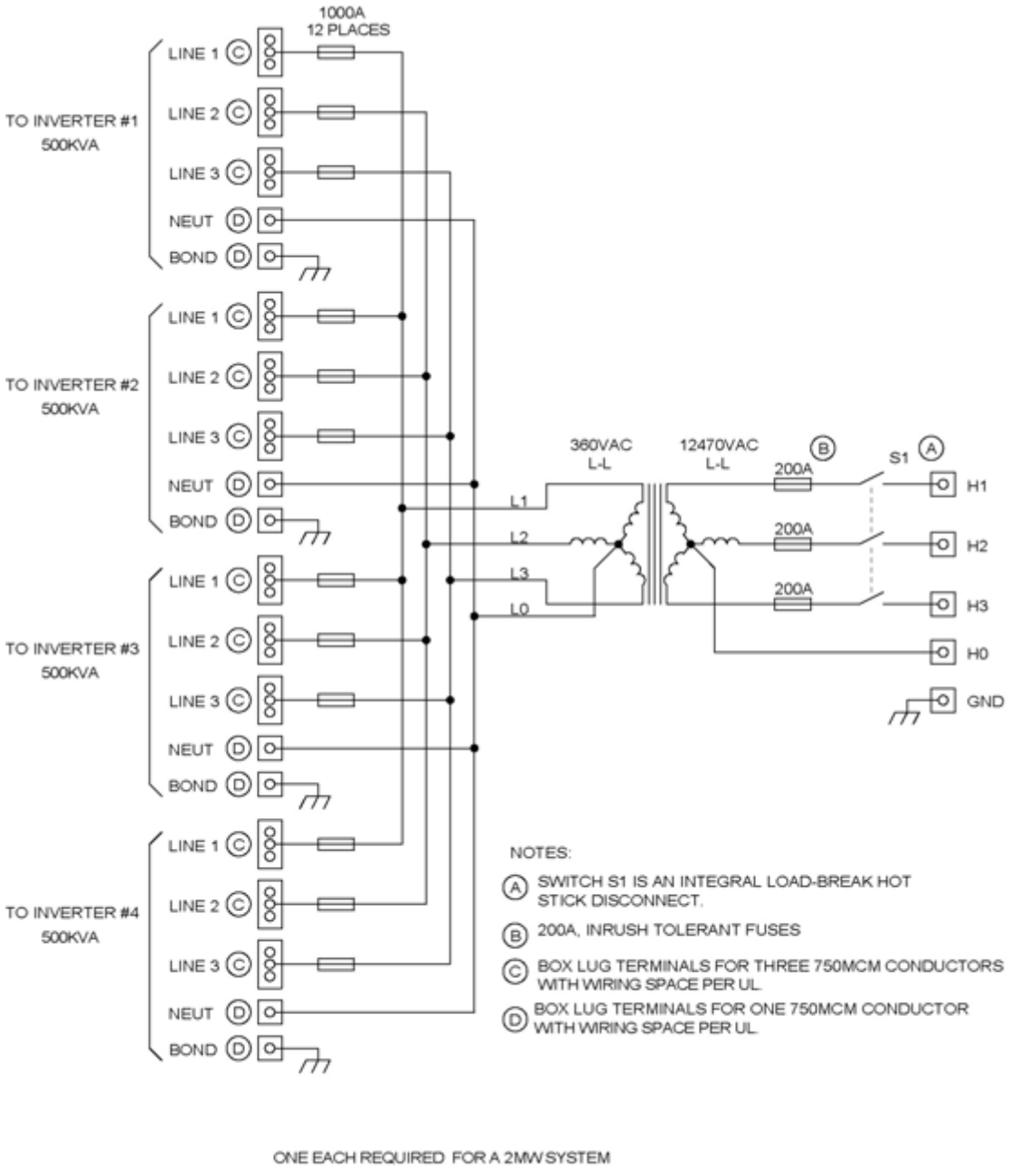



**Figure 9 - Solution #2, 2MVA Transformer Subassembly Schematic**

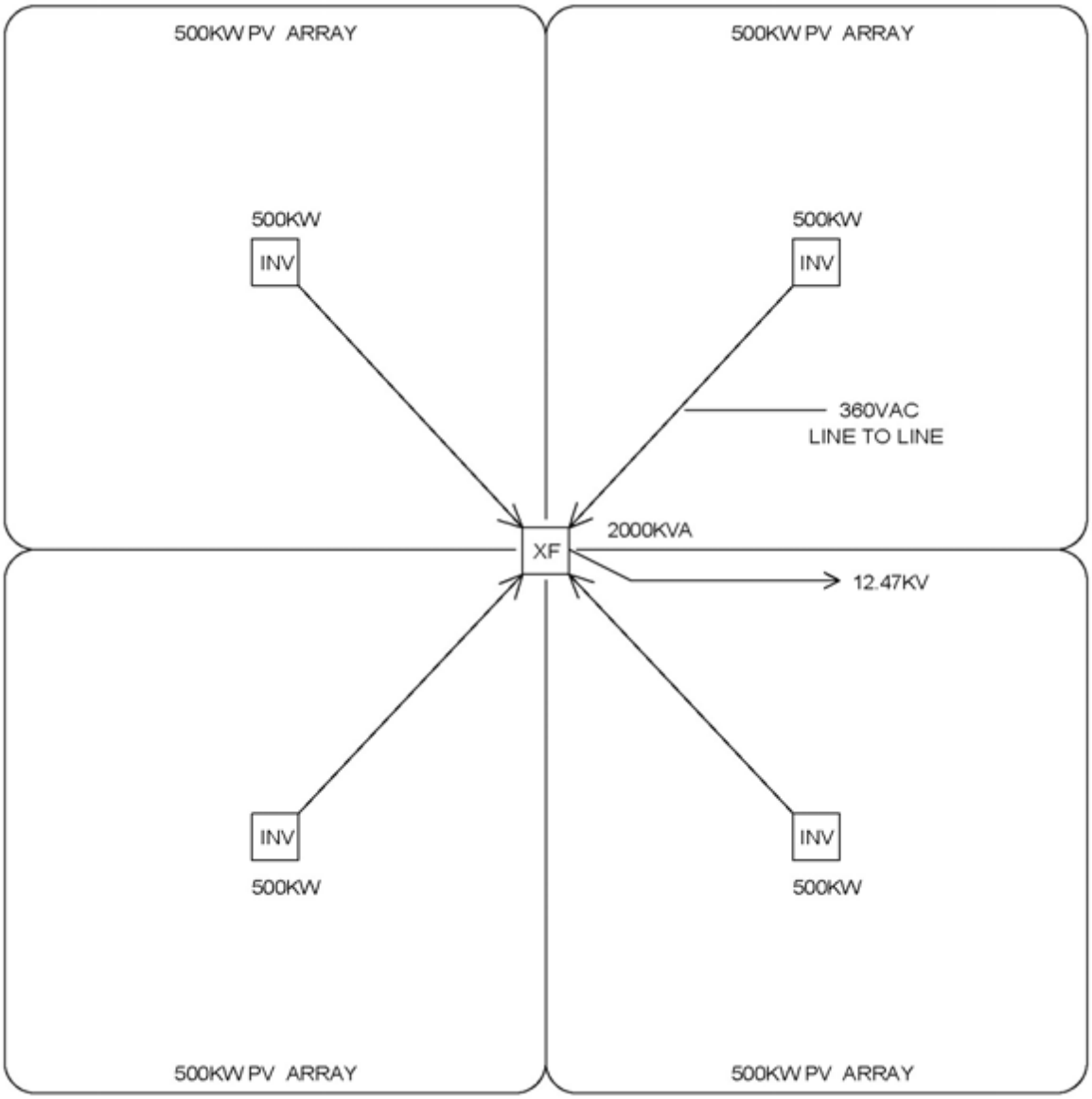



**Figure 10 - Solution #2 Field Layout, 2MVA Transformer**

#### 3.5.2.3 SOLUTION #3

Figure 11 shows a transformer subassembly electrical schematic for Solution #3 where one 2MVA transformer subassembly is constructed with four separate 3-phase low voltage windings, one set for each of the four 500kW inverters. The PV system hookup will be similar to the hookup shown in Figure 9. Solution #3 was originally proposed in the Statement of Work for this subcontract as a viable solution to allow multiple inverters with asynchronous switching frequencies to share a common transformer.

With the synchronization circuit developed for the 500kW inverter, multiple inverters can now be directly paralleled. In retrospect, this was a very good outcome since none of the six transformers manufacturers solicited would quote this 15-winding transformer.

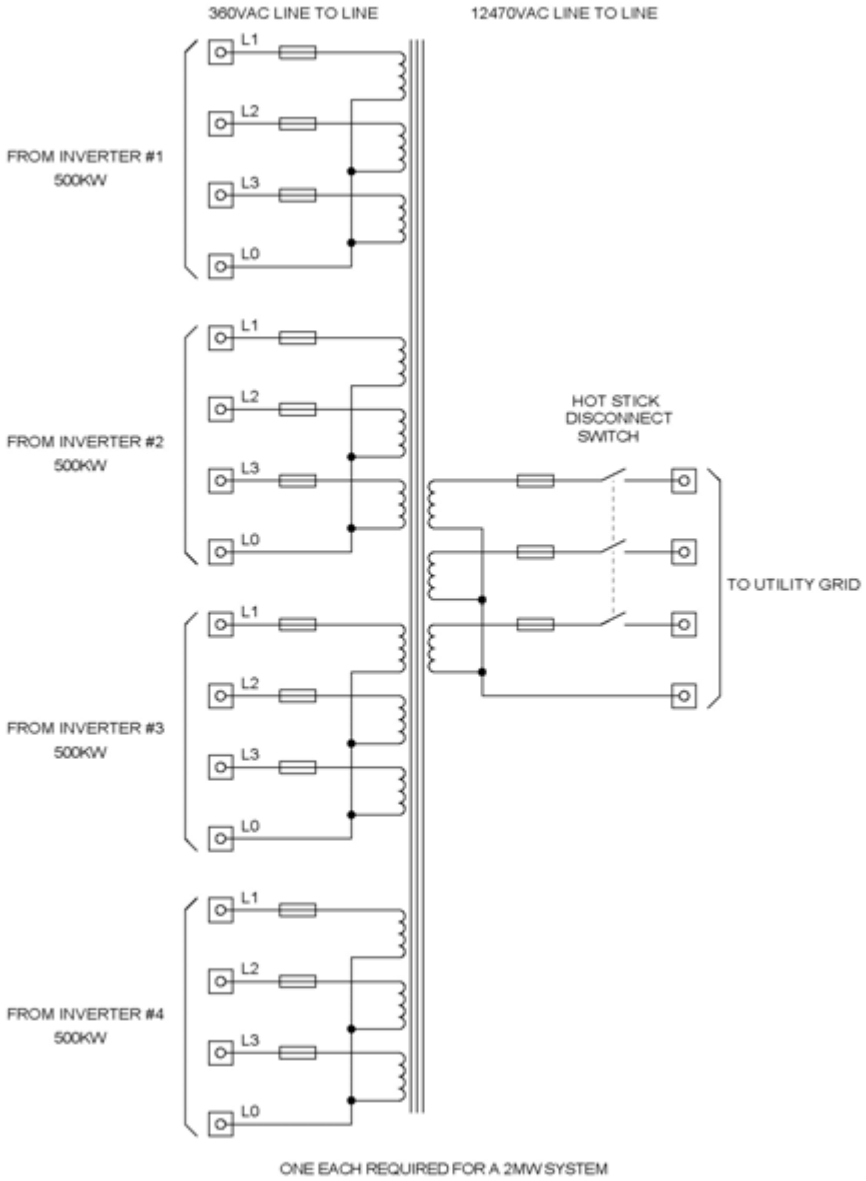



**Figure 11 - Solution #3, 2MVA Transformer Subassembly Schematic**

#### 3.5.2.4 TRANSFORMER COST ANALYSIS

The top U.S. manufacturers of large oil filled distribution transformers were requested to quote on three different transformers, all 3-phase with 360Vac line-to-line, WYE configured, low voltage windings and 12470Vac line-to-line, WYE configured, high voltage windings:

- 500kVA standard efficiency
- 500kVA high efficiency
- 2000kVA high efficiency

The preferred supplier for the 500kVA transformers quoted a ¾ power conversion efficiency of 98.74% for the standard efficiency transformer and 99.46% for the high efficiency version. The difference in power losses at ¾ power is 2700W. From a system cost perspective, this 2700W has a value equal to the installed cost of additional photovoltaic capacity to make up this difference, adjusted for the inverter conversion efficiency of 96% or 2813W. With a cost estimate of $5/installed watt, this 2815W translates to an additional system cost of $14,065. The quoted price difference between the standard efficiency and the high efficiency transformer is $4,877. The value proposition is clearly the high efficiency transformer where a net $9,188 could be saved by using the $12,267, high efficiency transformer instead of the $7,390, standard efficiency transformer.

The evaluation of AC collection Solution #1 vs. #2 is straightforward since the quoted conversion efficiencies of the high efficiency 500kVA and the 2000kVA transformers were almost identical. Although the PV field layouts, as shown in Figures 5 and 7 respectively, have different geometries, the lengths of conductors, conduit and trenching are similar and the delta in the associated costs for these items is negligible compared to the cost of the transformers.

The contract goal is to demonstrating a 25% cost reduction in PV system AC collection and distribution transformer costs. Table 2 shows a 42.5% reduction in the cost of AC power collection for a 2 megawatt PV power plant by using multiple inverters with external synchronization and a common distribution transformer. This analysis illustrates how the commercialization of multi-megawatt PV power systems can be advanced by leveraging transformer economies of scale when used in conjunction with an enabling inverter technology.

**Table 4 - Distribution Transformer Cost Analysis Summary**

| Configuration | Transformer Costs | Quantity Required | Extended Cost | Relative Costs |
|---|---|---|---|---|
| Solution #1 | $12,267 | 4 | $49,068 | 100% (ref) |
| Solution #2 | $28,237 | 1 | $28,237 | 57.5% |
| Solution #3 | No Bid | 1 | ---- | --- |

### *3.5.3 DC GROUND FAULT INTERRUPT STUDY*

During the course of this subcontract, the marketing requirements for the 500kW inverter changed. As such, the design of the 500kW inverter has been augmented to include DCGFI capabilities. The contractual scope of work called out for a paper study only.

The reporting on this task is limited due to the proprietary nature of the technology developed.

## 3.6 TASK 6 - COMMUNICATIONS DESIGN

Figure 12 illustrates the system-integrated communications and DAS designed for the 500kW inverter. The current and voltage sensors are the same sensors used by the inverter for regulation and fault detection. The signals from these sensors are filtered to remove high frequency noise, scaled and offset. The conditioned signals are connected to analog to digital converter inputs of the mixed signal microcontroller. The data processor is part of the microcontroller used to run all the other inverter systems. Being able to leverage the use of existing sensors and data processing capability are the key cost reduction drivers in favor of this approach. All components shown in Figure 12, with the exception of the Gateway, are resident on the 500kW inverter control board in order to obtain a high level of integration.

Multiplexers 1 and 2 are low cost devices which allow the microcontroller analog inputs to process a large number of low frequency bandwidth signals to expand the number of inputs available for data acquisition. Multiplexer 1 handles the metrology inputs and multiplexer 2 handles up to 32 PV string current sense channels. The multiplexer switch closures and timing is controlled by the microcontroller. With a contrary, external data logger solution, the cost of adding channels to emulate this equivalent multiplexer performance would be prohibitive.

Another key element of the system integrated design is the provision for a number of serial communication formats; RS232, RS485, RS485/MODBUS, and a connection to the Internet via a standard Gateway product.

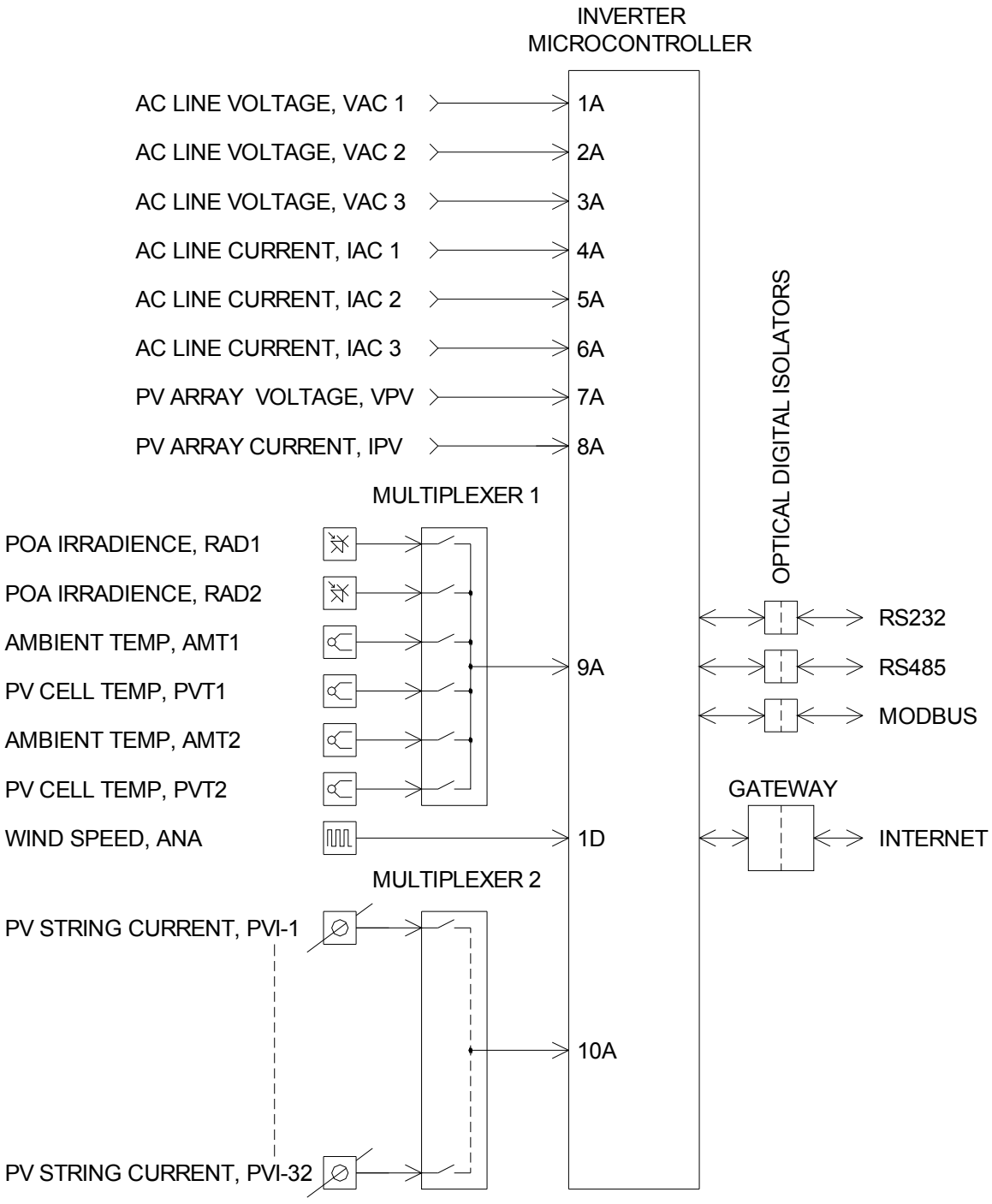



**Figure 12 - System Integrated Communications Design Block Diagram**

The 500kW inverter will allow remote access through multiple communication options. The user will have the ability to control and monitor the status of the inverter through these communication options. The inverter will be programmed to store the time and details of all faults in non-volatile memory. The inverter will also have the ability to notify the user that a fault has occurred.

The inverter will store performance data values and operation metrics for system operational analysis. These values will be stored on the controller board in non-volatile memory and will be accessible by local laptop or remote computer through the remote access serial port on the inverter. These parameters may be user selectable.

**Accumulated Energy**

The system shall calculate and keep in non-volatile memory the accumulated energy delivered by the inverter since commissioning. It shall also allow the user to read and reset the accumulated values individually through any of the communications ports.

**Accumulated Energy Sold Since Commissioning**

Energy is calculated only when the inverter is on-line. Energy is calculated by summing the Power Calculation values for one second and dividing by 60 to create Watt-Seconds, which are accumulated and converted to Watt-hours. The Watt-Hour value shall be stored in NV-RAM and updated every 15 minutes while online, and also updated during any transition out of the on-line state.

**Time and Date**

The system shall be able to read the controller board real time clock. The real-time clock shall be settable through either of the communications ports.

**Data Recording**

The system shall maintain a data log with a capacity of at least 31942 32-bit words. The data log shall be a circular buffer (located in non-volatile memory) and the earliest records shall be overwritten once the capacity of the buffer is exceeded.

**Fault History**

The system shall record an entry, in a 100 record circular buffer, every time a fault occurs. The entry shall have the fault code and a timestamp (mm/dd/yy hh:mm:ss). The buffer shall be located in non-volatile memory and once the buffer is full, the oldest record shall be overwritten.

When comparing the system-integrated solution to the discrete component solution, the benefits of the system integrated solution are:

- Lower costs because dedicated DAS current and voltage sensors are not required.
- Lower costs of the data logger vs. the microcontroller. The microcontroller costs $12 and is already required for other inverter control functions. The amount of firmware development for the microcontroller is however, nontrivial.
- The number of low bandwidth analog inputs are easily expandable and with insignificant cost impacts.
- The throughput rate to the data storage memory is faster by at least an order of magnitude.
- The digital I/O for fault enunciation/reporting and the ability to remotely configure inverter operational parameters is vastly improved because high speed serial data is accessed directly by the microcontroller and does not need to be coded for data logger interface.
- Data logger and modem mounting, power supply connections and signal cables are not required.

The contract goals were exceeded by a very wide margin. A high degree of integration was demonstrated. Data throughput rates were increased by a factor of 10. Although not a specific task goal, component costs were reduced by an estimated 90% compared with a non-integrated solution using external sensors and data logger.

## 3.7 TASK 7 - PHASE I DESIGN REVIEW

In Task 7, a comprehensive design review of the 500kW inverter was completed by the product development team. All of the subcontract design goals in Tasks 1 through 6 were addressed and a consensus was reached that all of the contract goals had been met. All functional specifications; hardware specifications; PCB layouts; magnetics fabrication drawings; mechanical fabrication drawings; electrical schematics; and BOMs were updated so that fabrication of the 500kW inverter hardware could begin in Phase II.

## 3.8 TASK 8 - SOFTWARE DESIGN

The reporting of this task is somewhat limited due to the proprietary nature of technology developed. In Task 8, four major software modules for the 500KW inverter were designed:

(1) Regulation
(2) State machine
(3) Data acquisition and communications
(4) Single-axis array tracker positioning

### *3.8.1 INVERTER REGULATION SOFTWARE DESIGN*

Two nested servo loops are used to regulate the inverter as further explained in Sections 3.8.1.1 and 3.8.1.2.

#### 3.8.1.1 AC LINE CURRENT REGULATION

There are three identical AC line current regulation loops, one for each AC line phase, per bridge matrix assembly. Grid interactive inverters regulate sinusoidal currents into the grid in phase with the grid voltage. The AC grid can be modeled as a perfect voltage source having zero impedance. Each regulator is a servo loop that exactly follows the sine wave reference generated by the microcontroller. This is done by comparing the actual line current from a current sensor to the reference and generating an error voltage that corrects for differences between the two signals. This signal, at the output of the AC error amplifier, is compared to a triangle wave to produce a pulse width modulated (PWM) version of the current sine wave being "constructed". IGBT (insulated gate bipolar transistor) gate drivers cause the IGBT half-bridge to switch in complementary fashion. The resulting PWM power switching is then filtered into a sine wave of current by the series PWM filter inductor.

The microcontroller software is called firmware or program code. This code is designed specifically for this application and is loaded into the microcontroller. The sine wave references are created by sequentially addressing memory locations in a look-up table containing binary coded sine wave amplitude information. The starting point for each sine wave is synchronized with a signal which indicates when the grid voltage crosses zero volts. Each set of digital binary information generated by the microcontroller processing core is converted to analog signals by digital to analog converters within the microcontroller.

#### 3.8.1.2 PV VOLTAGE REGULATION LOOP

The PV voltage regulation loop has a much slower response time than the AC current regulation loops and maintains a constant PV array voltage which is proportional to the PV REF signal generated by the microcontroller. The PV REF signal is incrementally adjusted or perturbed and the resulting change in PV array power output is observed. If an incremental increase in PV REF results in an increase in PV power then the next incremental adjustment in PV REF will be in the same direction. When an increase in PV REF causes a decrease in PV power, the direction of the PV REF step is reversed for the next cycle. This perturb-and-observe algorithm continuously seeks and tracks the maximum power point voltage of the PV array when the inverter is producing power. The range of PV REF, the step size of PV REF and the frequency of PV REF increments are factory programmed but may be modified by the user via the communications port.

The digital value of PV REF is generated in response to a complex portion of microcontroller program code. A 12-bit binary word from the microcontroller is converter to an analog signal by a digital to analog converter. To form the control loop, V REF, the desired voltage of the PV array is compared to the actual value of the PV array voltage. The difference of these two signals simultaneously controls the amplitude of all the three sine wave current references by acting as the common input to three analog multiplier circuits. In this manner, when the PV array is below the maximum power point voltage of the array, the servo loop will command the sine wave current references to a higher amplitude, creating more power into the grid (and out of the array) thereby lowering the PV array voltage. When the PV voltage is above the maximum power point of the array the current reference amplitudes will be decreased.

### *3.8.2 INVERTER STATE MACHINE*

For the following discussion, please reference Figure 13 - State Machine Diagram. These asynchronous states are commanded by the state machine according to the conditions applied to the inverter, compared to the parameters set at the factory and by the user.

**Initializing**

When powered up, and when the key switch is moved from the OFF position to the ON position, microcontroller U1 will invoke the INITIALIZATION state. Upon completion of initialization, microcontroller U1 will transition to the SLEEP State.

**Sleep**

While in the SLEEP state, the inverter will monitor the PV input voltage to determine if it is time to start.

**Wakeup**

After at least 10 seconds and if the PV voltage is greater than the user settable minimum start voltage the state changes to WAKEUP. Adhering to a UL 1741 rev 2005 and IEEE 1547 stipulation, this state is maintained for five minutes. The 5-minute delay is reduced to 10 seconds when the following power-up sequence is followed:

The DC disconnect is switched from the open to the closed position, while the PV voltage greater than the start voltage.

The 5-minute delay will be bypassed when the WAKEUP state has been entered from the 5-minute delay in the FAULT State.

If the PV voltage drops below the Minimum Start Voltage, while in the WAKEUP state, then the state changes back to SLEEP.

After remaining in WAKEUP state exclusively for five minutes, the state will transition to ONLINE.

**Online**

In this state the inverter is energized. Upon transitioning into this state, the following sequence shall be followed.

- Set the output command to achieve minimum current
- Wait settling time
- Enable the matrix
- Wait settling time
- Close the DC contactors
- Wait settling time
- Close the AC contactor
- Set command voltage equal to bus voltage

While in the ONLINE state, if the PV voltage drops below the Minimum Operating Voltage, the inverter matrix stops switching, the AC and DC contactors open, and the state changes back to SLEEP. Maximum Power Point Tracker (MPPT) mode is the default mode in this state. MPPT may be turned off from the user interface, in which case the inverter operating voltage stays at a settable voltage value.

**Shutdown State**

Regardless of which state the machine is in, if the DC disconnect switch is open, the remote shutdown command is asserted from the user interface, or the remote shutdown terminal current loop is opened, the inverter will transition into Shutdown state.

**Diagnostic States**

The following additional states may be set by the user. These states are for diagnostic use, and can only be accessed by use of a suitable communications device.

**Matrix Test**

While the front panel PV Disconnect switch is in the off position, the user can put the inverter into the MATRIX TEST state by setting the inverter's goal state to Matrix Test. This state energizes the drive signals to the matrix by setting an enable bit high while maintaining the contactors in the open position, and sets the amplitude of the sine wave references to zero, for testing of the inverter matrix. This state can only be entered by command from the user interface.

**Manual Current State**

The user can activate the MANUAL CURRENT state by setting the inverter's goal state. In this mode, when the inverter reaches Power Tracking state, it will output the current specified by user settable parameter.

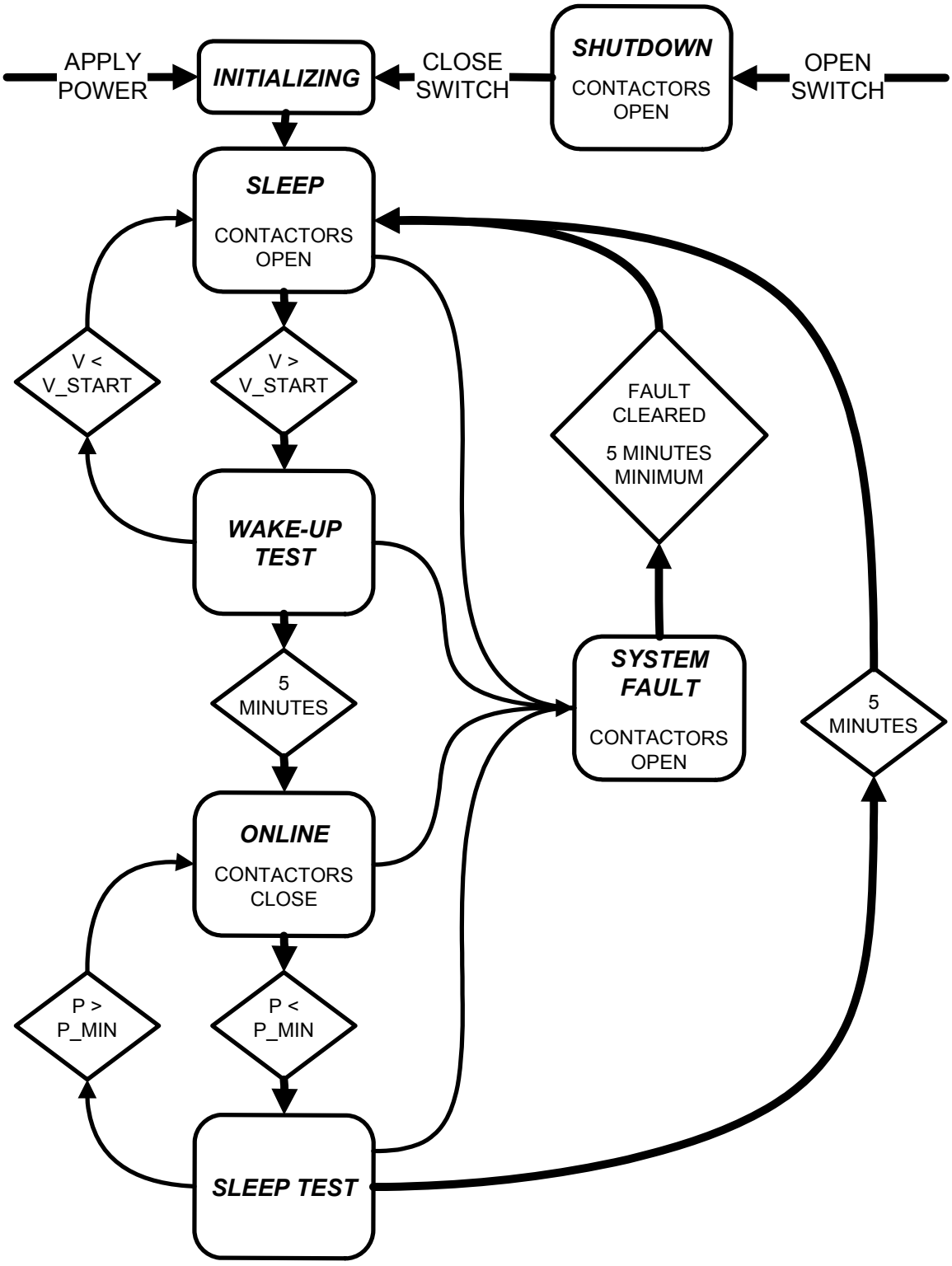



**Figure 13 - State Machine Diagram**

### *3.8.3 DAS AND COMMUNICATIONS SOFTWARE DESIGN*

The GT30 communications, DAS (data acquisition system) and remote control firmware represents approximately one third of the total GT30 microcontroller code. The initial design of this firmware has been completed but will not be fully tested until the target hardware is fully functional. The GT30 uses two Texas Instruments MSP430 mixed signal microcontrollers. The MSP430 achieves maximum code efficiency with its 16-bit RISC architecture, 16-bit CPU-integrated registers and a constant generator. The MSP430 has two universal serial synchronous/asynchronous communication interfaces (USART), and 64 I/O pins to support the GT30 serial communication functions.

Note: "Firmware" is the more common term for imbedded microcontroller code whereas "software" is more applicable to instruction sets used on a personal computer. With respect to this deliverable, *firmware* and *software* will be used interchangeably.

**Processing Unit**

The processing unit is based on a consistent and orthogonal CPU and instruction set. This design structure results in a RISC-like architecture, highly transparent to the application development and notable for its ease of programming. All operations other than program-flow instructions are consequently performed as register operations in conjunction with seven addressing modes for source and four modes for destination operand.

**CPU**

The CPU has sixteen registers that provide reduced instruction execution time. This reduces the register-to-register operation execution time to one cycle of the processor frequency.

Four of the registers are reserved for special use as program counter, stack pointer, status register, and constant generator. The remaining registers are available as general-purpose registers.

Peripherals are connected to the CPU using a data address and control bus, and are handled with all memory manipulation instructions.

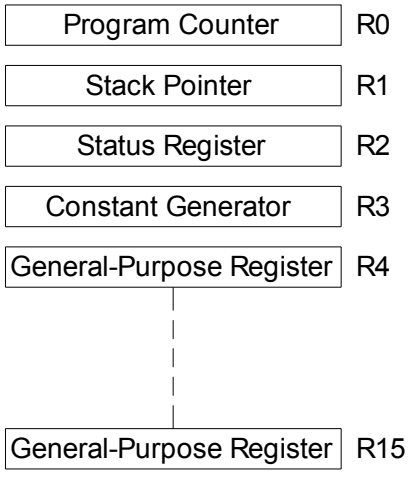



**Figure 14 - CPU Registers**

**Instruction Set**

The instruction set for this register-to-register architecture constitutes an assembler language. The instruction set consists of 51 instructions with three formats and seven address modes:

- Dual operands, source-destination
- Single operands, destination only
- Relative jump, un/conditional

Computed branches and subroutine call instructions use the same address modes as other instructions. These address modes provide *indirect* addressing, which is ideally suited for computed branches and calls. The full use of this programming capability results in a program structure which is different from structures used with conventional 8- and 16-bit controllers. For example, numerous routines can be designed to deal with pointers and stacks instead of using flag-type programs for flow control.

**Operating Modes and Interrupts**

The MSP430 operating modes directly support the GT30 control goals. These goals are achieved by intelligent management during the different operating modes of the modules and CPU states and are fully supported during interrupt event handling. An interrupt event awakes the system from each of the various operating modes and returns to the mode that as selected before the interrupt event occurred.

**Interrupt Vector Addresses**

The interrupt vectors and the power-up starting address are located in a fixed address range. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Special Function Registers**

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple firmware access.

**Boot ROM Containing Bootstrap Loader**

The bootstrap loader downloads data into a flash memory module. Various write, read and erase operations insure the proper download environment.

Protected Functions

All protected functions are executed only when the access is enabled.

- Write/program byte into flash memory; parameters passed are start address and number of bytes.
- Segment erase of segment 0 to segment in n in main memory, and segment erase of segments A and B in the information memory.
- Read all data in main memory and information memory.
- Read and write to all byte peripheral modules and RAM.
- Modify PC and start program execution immediately.

Features of the Bootstrap Loader are:

- UART communication protocol, fixed to 9600 baud
- Port pin P1.1 for transmit, P2.2 for receive
- T1 standard serial protocol definition
- Implemented in flash memory version only

**Flash Memory**

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0-n. Segments A and B are also called *information memory*.
- A security fuse burning is irreversible; no further access to JTAG is possible afterwards.
- Internal generation of the programming/erase voltage.
- Program and erase timing is controlled by hardware in the flash memory - no firmware intervention is needed.
- The control hardware is called the flash-timing generator. The input frequency of the flash-timing generator should be in the proper range and should be maintained until the write/program or erase operation is completed.

**Peripherals**

Peripherals are connected to the CPU through data, address, and control busses, and are handled using all memory-manipulation instructions.

**Oscillator and System Clock**

Three clocks are used in the system - the system clock (MCLK) used by the CPU and the system, the subsystem clock (SMCLK) used by the peripheral modules, and the auxiliary clock (ACLK) used by the peripheral modules. This highly flexible digitally controlled clock system allows the GT30 clocks to be optimized for various modes of operation.

Different tasks and system conditions dictate different system-clock requirement, including:

- High frequency for quick reaction to system hardware requests or events
- Low frequency to minimize current consumption, EMI, etc
- Stable peripheral clock for timer applications, such as real-time clock (RTC)
- Start-stop operation that can be enabled with minimum delay

**Multiplication**

The multiplication operation is supported by a dedicated peripheral module. The module performs 16x16, 16x8, 8x16, and 8x8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

**Digital I/O**

There are six 8-bit I/O ports implemented-ports P1 through P6. Ports P1 and P2 use seven control registers, while ports P3, P4, P5 and P6 use only four of the control registers to provide maximum digital input/output flexibility to this application.

- All individual I/O bits are independently programmed.
- Interrupt processing of external events is fully implemented for all eight bits of ports P1 and P2.
- Read/write access to all registers using all instructions possible.

The seven control registers are:

- Input register 8 bits at Ports P1 through P6
- Output register 8 bits at ports P1 through P6
- Direction register 8 bits at ports P1 through P6
- Interrupt edge select 8 bits at ports P1 and P2
- Interrupt flags 8 bits at ports P1 and P2
- Interrupt enable 8 bits at ports P1 and P2
- Selection (port or module) 8 bits at ports P1 through P6

Each of these ports contains eight bits. Two interrupt vectors are implemented.

**Watchdog Timer**

The primary function of the Watchdog Timer module is to perform a controlled system restart after a GT30 firmware upset has occurred. A system reset is generated if the selected time interval expires.

**USART0 and USART1**

There are two USART peripherals implemented in the MSP430: USAT0 and USART1. Both have an identical function. They use different pins to communicate, and different registers for module control. Registers with identical functions have different addresses.

The universal synchronous/asynchronous interface is a dedicated peripheral module used in serial communications. The USART supports synchronous SP1 (3- or 4-pin) and asynchronous UART communication protocols, using a double-buffered transmit and receive channels. Data streams of 7 or 8 bits in length is transferred at a rate determined by the firmware for depending on that specific task.

Two dedicated interrupt vectors are assigned to each USART module-one for the receive channels and one for the transmit channels.

The GT30 uses two MSP430 microcontrollers for a total of four UART connections, one linking the two processors, one for an external RS232 connection, one for an external RS485 connection and one for and internal, inverter system, RS485/MOD BUS connection.

**Analog-to-Digital Converter (ADC)**

The heart of the GT30 data acquisition system is the MSP430 analog-to-digital converter module. The 12-bit analog-to-digital converter (ADC) uses a 10-bit weighted capacitor array plus a 2-bit resistor string. The CMOS threshold detector in the successive-approximation conversion technique determines each bit by examining the charge on a series of binary-weighted capacitors. The ADC converts all signals form the world outside of the microcontroller to digital format as orchestrated by the GT30 firmware to provide:

- 12-bit converter with ±1 LSB linearity
- Built-in sample-and-hold
- Eight external and four internal analog channels. The external ADC input terminals are shared with digital port I/O pins.
- Internal-temperature sensor for temperature measurement
- Battery-voltage measurement
- Conversion time is selected from various clock sources: ACLK, MCLK, SMCLK. The clock source is divided by an integer from 1 to 8, as selected by firmware.
- Channel conversion: individual channels, a group of channels, or repeated conversion of a group of channels. Conversion of a group of channels is selected the sequence, the channels, and the number of channels in the group can be defined by firmware. For example, a1-a2-a5-a2a2-….
- The conversion result is stored in one of sixteen registers. The sixteen registers have individual addresses and are accessed via firmware. Each of the sixteen registers is linked to an 8-bit register that defines the positive and negative reference source and the channel assigned.

The GT30 uses a number of peripheral data multiplexers to expand the number of analog inputs that can be converted to digital. The firmware controls which external signals are sampled, when they are sampled and how many samples are averaged before the resultant value is used.

### *3.8.4 SINGLE-AXIS ARRAY TRACKER MOTOR CONTROL FIRMWARE DESIGN*

The 500kW is the only commercial PV inverter with an integrated single-axis tracker controller. The 500kW is capable of mechanically positioning four different sub-arrays to track the sun from dawn to dusk. The tracker controller can drive four 1HP, 3-phase, 208Vac synchronous motors and receive feedback signals from tilt sensors mounted on the sub-arrays. The brains of the tracker controller are resident in the system microprocessor on the inverter control board. The muscle of the tracker controller is located on the tracker controller assembly.

The tracker algorithm maintains the plane of array perpendicular to the suns irradiance except when the angle of the sun is low enough that an adjacent row of PV modules would shadow a neighboring row. In this case, the array is tracked off the solar axis to capture the greatest insolation by just staying out of the shadow of the row to the east at sunrise and the west at sunset as illustrated in Figure 1. The tracker controller works on a real-time clock/calendar to determine the position of the sun throughout the year.

Typically, the actuators used to rotate a single-axis array are very robust in order to handle array wind loads. If the actuators are allowed to extend beyond the mechanical stops of a system, catastrophic damage can occur. The GT500 tracker controller employs a redundant over travel protection circuit.

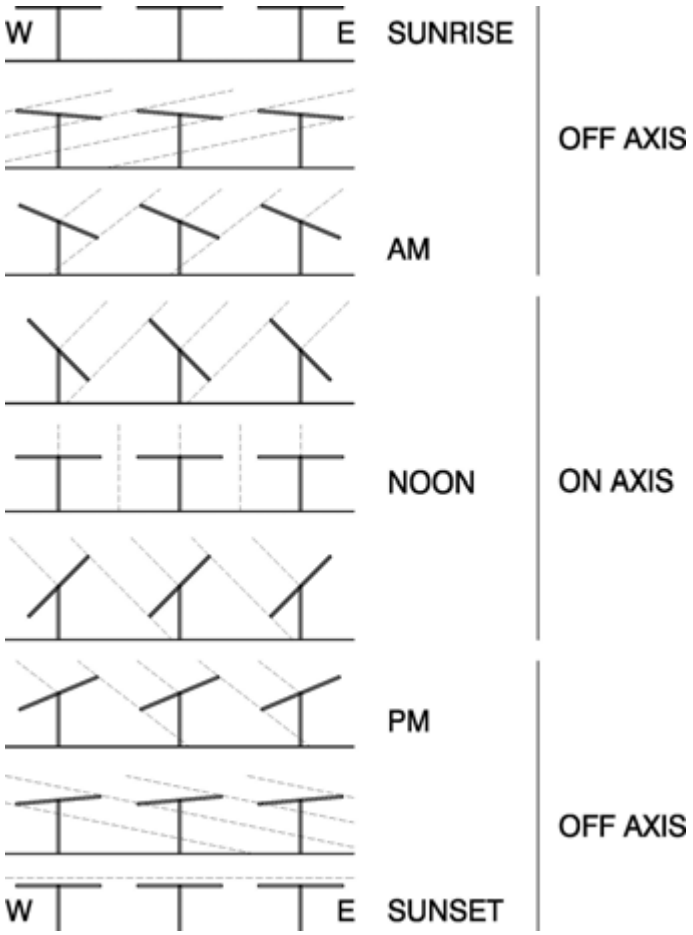



**Figure 15 - Tracker Controller Software Anti-Shadowing Algorithm**

The tracker controller commands the array to start and end the day in a horizontal position. The array tracks on-axis with the sun from 45º east to 45º west from horizontal. Under all other conditions, the array tracks off-axis with the sun to just keep out of the adjacent array shadow.

**User Programming**

When the PV system is commissioned, a number of parameters must be entered, one time, to *describe* the system configuration and location to the tracker controller. The GT500 will prompt the user via the RS232 or RS485 port during the system setup routine for the following parameters.

- Longitude
- Latitude
- Date
- Time of day
- Motor run time to angular displacement ratio (K)
- Array form factor parameters

    R = Radius of array about the rotational axis (axis to edge of panel length)
    H = Height of the rotational axis from grade
    S = Single axis row to row spacing

These three parameters are entered in inches and provide the controller with all the required information to precisely fore track at dawn and backtrack at dusk to prevent row to row shadowing.

In most systems, the 3-phase motor is used to drive a gear-reduced linear actuator or screw jack. The screw jack is in turn connected to a lever arm fixed to the rotational axis of the array. The motor run time to angular displacement ratio, K, can be easily calculated by the motor speed, times the screw jack ratio and the lever arm ratio. Alternately, the time it takes to manually track the array through a given arc can be used to empirically determine this ratio in any system.

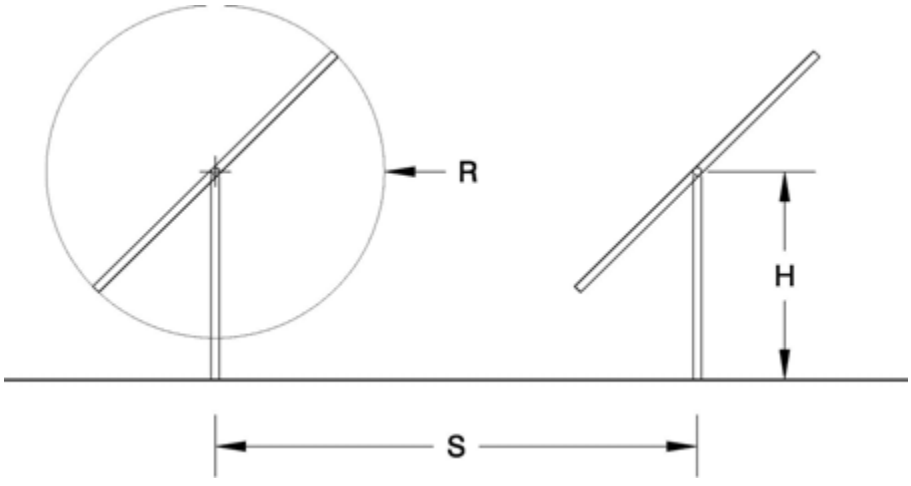



**Figure 16 – Programmable Array Form Factor Parameters**

**Tracking Methodology**

The tracker control is very simple, does not require a real-time position sensor on the rotating array and does not accumulate day-to-day tracking errors. The rotational feedback from the array comes from two mercury tilt switches, one set to open at the eastern rotation limit, the other set to open at the farthest western rotation limit. The limits are set at 45 degrees from horizontal, east and west.

The array is positioned as a function of motor run time. The direction, the cumulative run time and the K factor of a motor is remembered by the tracker controller. Therefore, the position is also known. This system is very accurate because the controller drives the array east every morning and west every afternoon until the respective rotational limit switches open. This function recalibrates the rotational position of the array at a known angle, twice a day, and resets the run time counter.

**Tracking Commands**

There are only four single-bit digital commands from the system control board to the tracker controller assembly, two address bits (TRK A0 and TRK A1) to select which of the four sub-array trackers is active and two command bits (EAST and TRACK) that actively control the movement of the selected sub-array. A logic "1" on the EAST bit arranges the 3-phase motor rotation (via reversible power contactors) to track the subarray in an easterly direction, a logic "0" arranges the 3-phase motor rotation to track westerly. The track bit is active high and commands a power contactor to close connect AC power to the selected motor. All array tracker fault conditions are reported with logic "0" on a single status bit, TRK OK, from the tracker control assembly to the control board.

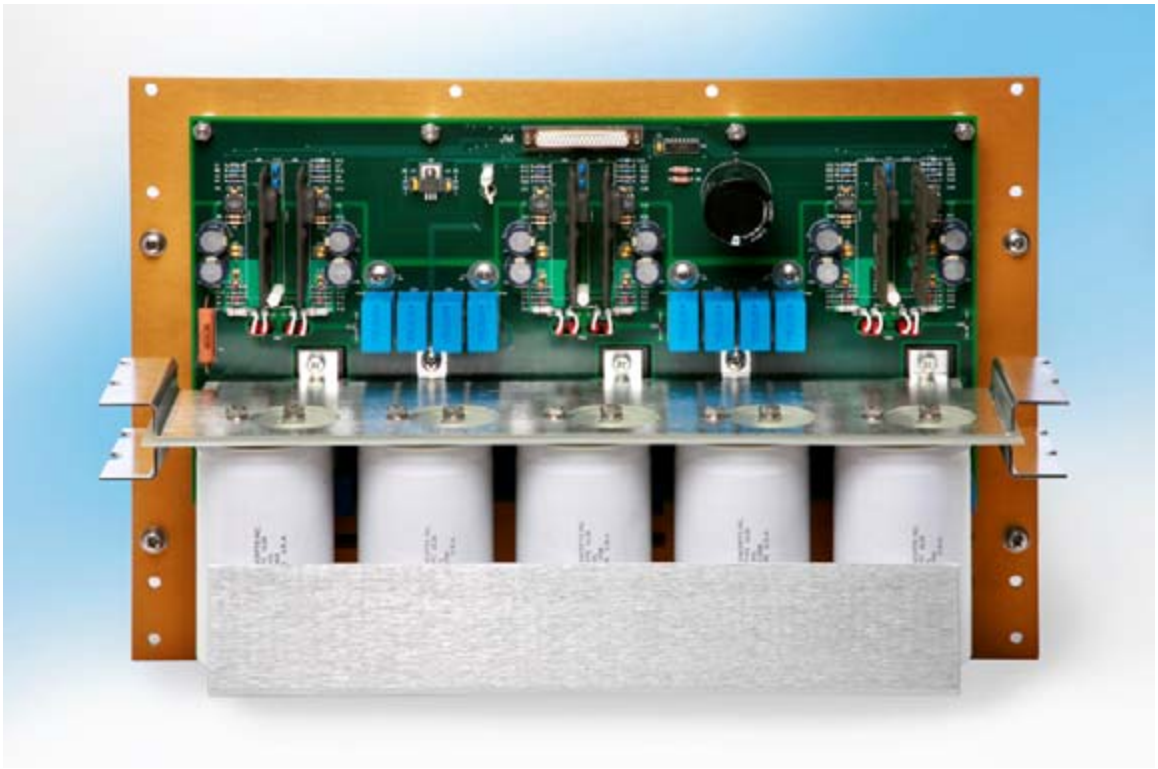
## 3.9 TASK 9 - HARDWARE FABRICATION & UL EVALUATION

In Task 9, all of the hardware for the 500kW inverter was fabricated. In addition, all the documentation required to submit this hardware for construction evaluation according to UL1741 was completed.

In some cases, the hardware shown in the following photos is second-generation where cost, performance or UL1741 compliance goals were not attained on the first attempt.

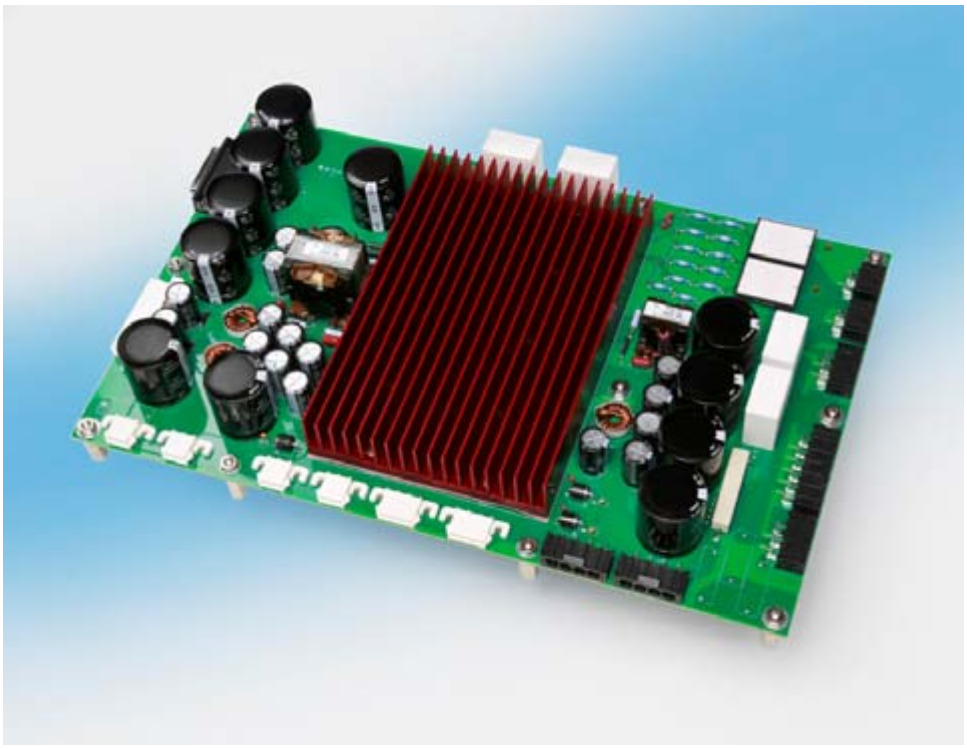
The PV interface assembly shown was not part of the original contract scope of work but was designed, fabricated and included in the final design of the 500kW inverter in order to incorporate the added DCGFI function.

**Photograph 2 - Completed 500kW Inverter, doors open**



**Photograph 3 - Bridge Matrix Assembly, front**
(One of four used in the 500kW inverter)

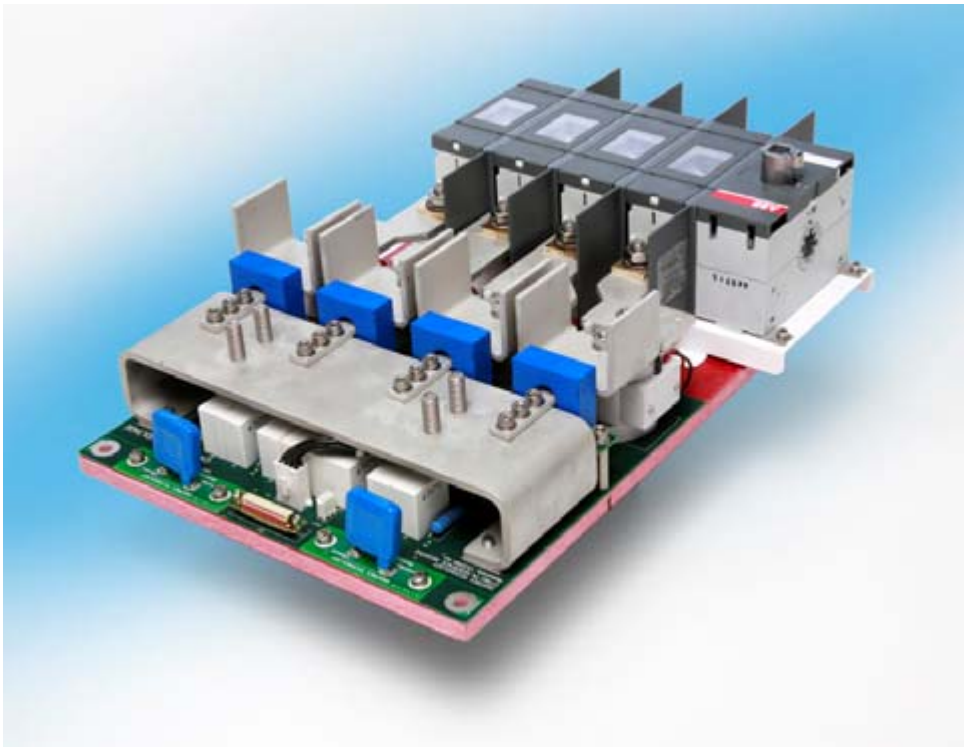
**Photograph 4 - Bridge Matrix Assembly, back**



**Photograph 5 - Power Supply Board Assembly**

**Photograph 6 - Control Board Assembly**


**Photograph 7 - AC Interface Assembly**



**Photograph 8 - PV Interface Assembly**

## 3.10 TASK 10 - INVERTER MTBF RELIABILITY ANALYSES

To verify the increased reliability of the 500kW inverter design, a third-party consultant was hired to perform a Mean Time Before Failure (MTBF) prediction. This prediction is performed by summing the published failure rates of all inverter component parts using a prescribed set of rules to factor in individual component stress levels. These component stress levels are based on the operating temperature and the current and/or voltage, as is appropriate, with respect to the rating of that component and the effective percentage utilization time. To facilitate this analysis, Xantrex engineers worked with this consultant to provide a comprehensive Bill of Materials (BOM), schematic diagrams and information on the individual component operating conditions.

The 500kW inverter has a predicted Steady State Reliability of 68,960 Hours (7.9 years). The state-of-the-art Xantrex GT250, 250kW inverter has a predicted Steady State Reliability of 52,400 Hours (6.0 years) and is used as the comparative "baseline" reference. The subcontract goal of a 25% enhancement in reliability was exceeded by 7% for a total 32% enhancement, on a machine-for-machine basis. Since the power levels of these two machines are not equivalent, an argument can be made that a 500kW system using one 500kW inverter (7.9 years) vs. two GT250, 250kW inverters (6.0/2 = 3.0 years) will be 163% more reliable.

## 3.11 TASK 11 - HARDWARE OPTIMIZATION

In Task 11, all functional-block subassemblies were optimized and low-power operation of the inverter was demonstrated working as a complete system. As part of this task, DVT (Design Verification Test) plans were drafted for each subassembly and for the complete inverter. Data sheets were created to insure that performance results were consistent with the expected results per the Functional Specifications.

Test and optimization was first performed on all of the functional-block subassemblies then the whole inverter. This was an iterative process of troubleshoot, test, modify, retest, modify and retest until the performance of a given assembly was optimized. In some cases more was required. The power supply and the PV interface subassemblies had to undergo complete redesign cycles to meet the performance and cost goals. In other cases, design flaws, assembly errors and operator error during DVT were responsible for additional troubleshoot, rebuild and retest cycles after the occurrence of high-power failures.

The work in Task 11 was a significant portion of the total development effort.

### *3.11.1 OPTIMIZATION OF INVERTER THERMAL PERFORMANCE*

The thermal performance of the inverter was found to exceed the predicted performance. The inverter was run under conditions that will generate the worst-case amount of waste heat. The temperature rise of all temperature sensitive components was monitored and allowed to stabilize. The temperature rise data was then be extrapolated for operation with 40ºC intake air to compensate for the 20ºC ambient test air. If the temperature of these critical components remained below their published ratings and design margins and the heat removal system as be deemed sufficient.

The temperature run was done with the inverter running in an ambient temperature of 20°C at full rated current at medium DC bus voltage and then at high DC bus voltage. The temperature of all the components being monitored was allowed to stabilize at both bus voltages. The "bumps" in the temperature data at 1:30 hours is the result of higher dissipation when changing from medium to high DC bus voltage.

#### 3.11.1.1 TEMPERATURE RUN RAW DATA

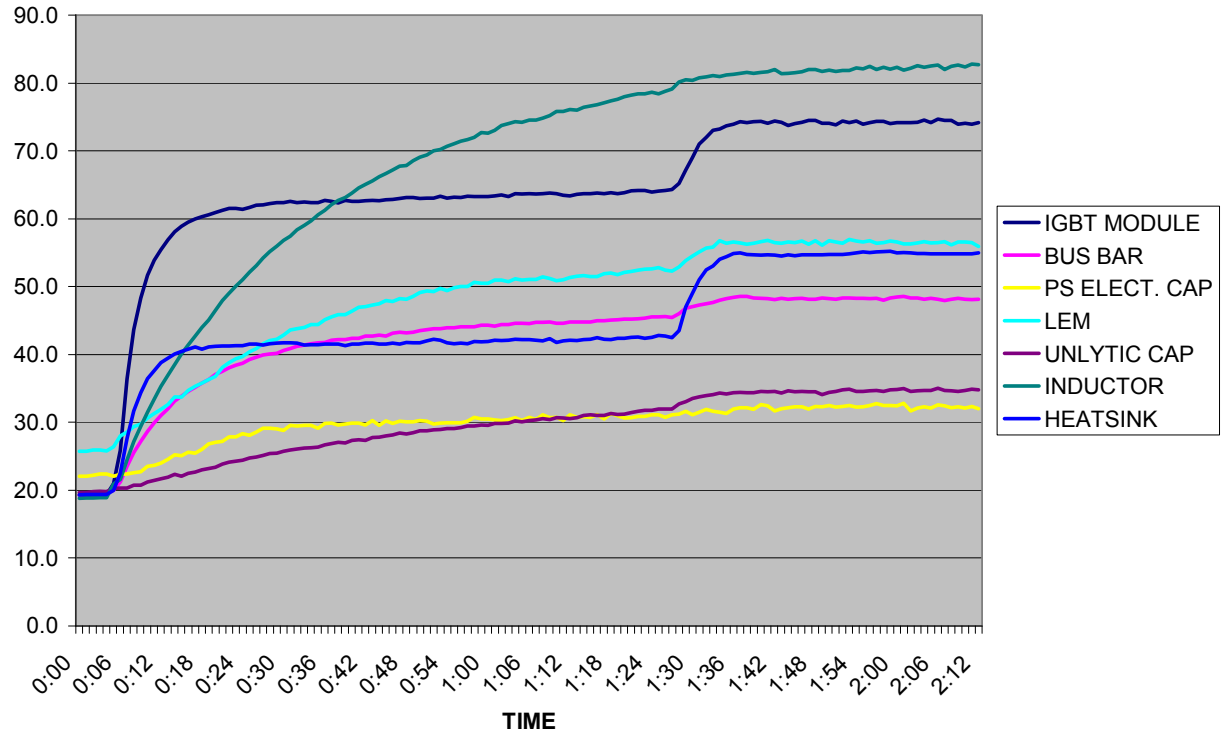



**Figure 17 - Inverter Thermal Mapping Data**

#### 3.11.1.2 TEMPERATURE RUN DATA INTERPRETATION

**IGBT Module**

The IGBT (Insulated Gate Bipolar Transistor) modules are the silicon semiconductor power switching elements of the 500kW inverter and are doing most of the power conversion "work". There are two primary IGBT loss mechanisms, conduction losses and switching losses. The IGBT losses produce approximately ⅔ of the total inverter waste heat or 6,670 Watts. The IGBTs are rated for a maximum silicon junction temperature of 150°C. In general, cooling of the IGBT modules drove the design of the entire inverter cooling system.

The IGBT junction temperatures cannot be measured directly and must be calculated. To do so the module temperature, the amount of power dissipated by the module and the thermal resistance from junction to module must be known. The module dissipation is 6,670W/12 modules or 556W per module, the thermal resistance is .03°C/W (from the IGBT manufacturer's data sheet) and worst case module temperature, from the temperature data above, is 75°C. The junction temperature is therefore 92°C. At 40°C ambient the junction temperature would be 112°C, leaving an acceptable safety margin of 150°C - 112°C = 38°C.

**Filter Inductors**

The second greatest heat producing components in the 500kW inverter are the filter inductors. There are two primary loss mechanisms, core losses and copper losses. The maximum allowable temperature for the filter inductors is 140°C. The extrapolated inductor temperature for 40°C ambient air is 85°C + 20°C = 105°C. This leaves an acceptable safety margin of 140°C - 105°C = 35°C. The margin is well matched with that of the IGBT modules and as such verifies that the cooling of the primary heat producing components is optimally balanced.

**LEM**

There are 12 Hall Effect current sensors used to regulate the AC line currents in the 500kW inverter. LEM is the name of a specific manufacturer. The LEMs are specified for a local ambient temperature of 85°C. An additional 10°C to 20°C of self-heating can be assumed in most applications as a function of the aperture conductor cross section and geometry. The extrapolated 40°C LEM temperature is 57°C + 20°C = 77°C, leaving an expectable margin of 18°C to 28°C at 40°C ambient.

**All Other Components**

All other components exhibit thermal margins well above 35°C and effectively exceed the thermal design requirements by a wide margin.

The thermal performance for the 500KW inverter was validated for the specified maximum ambient air temperature of 40°C and with enough thermal margin to allow operation with 50°C intake air. The cooling system design provided balanced margins on the two component groups generating the most heat, the IGBT modules and the filter inductors. The extensive thermal modeling done in the design phase was key to providing finished hardware that meets and exceeds the requirements of the functional specification and the goals of this subcontract task.

### *3.11.2 INVERTER OPTIMIZATION AT FULL CURRENT AND DC BUS VOLTAGE*

The 500kW inverter was successfully run with all three phases simultaneously producing over 800Amps rms per phase at the rated maximum DC full power input voltage. In addition, the matrix-to-matrix PWM (Pulse Width Modulation) frequency skewing will be illustrated. In both cases verification will be presented graphically followed by a brief technical narrative.

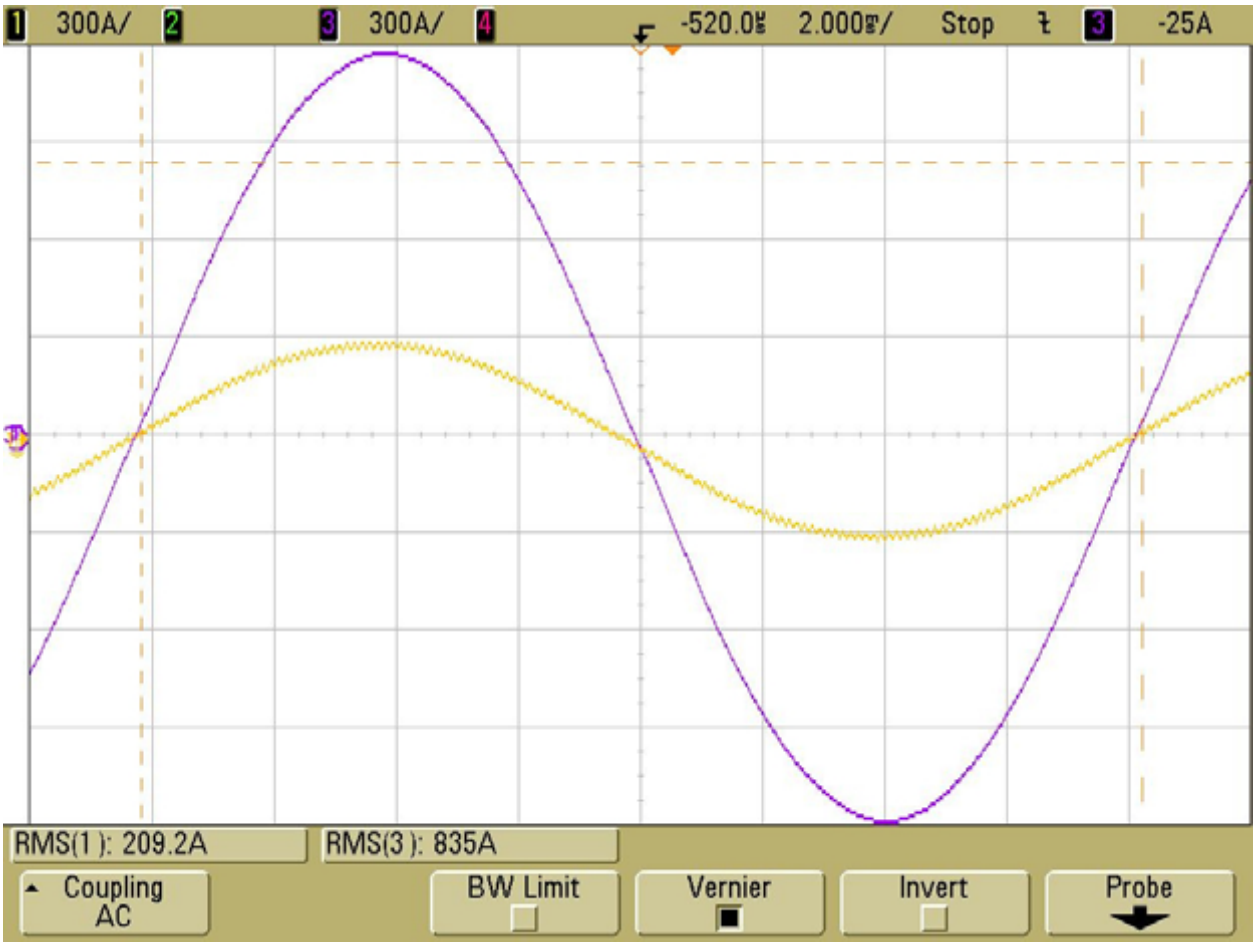



**Figure 18 - Full Current Operation at Maximum DC Voltage**

The 500kW inverter is comprised of four 125kW bridge matrix assemblies; Matrix A, Matrix B, Matrix C and Matrix D. Each matrix is a three-phase bridge. A given matrix supplies one fourth of the total line current for each of the of the three utility line phases #1, #2 and #3. Figure 18 is actual test data showing two captured waveforms. The 209Amp, yellow waveform is the line phase #1 current contribution from Matrix A alone. The 835Amp, purple waveform is the sum of all four line phase #1 Matrix currents. The other two line phase currents #2 and #3 are identical to Figure 18.

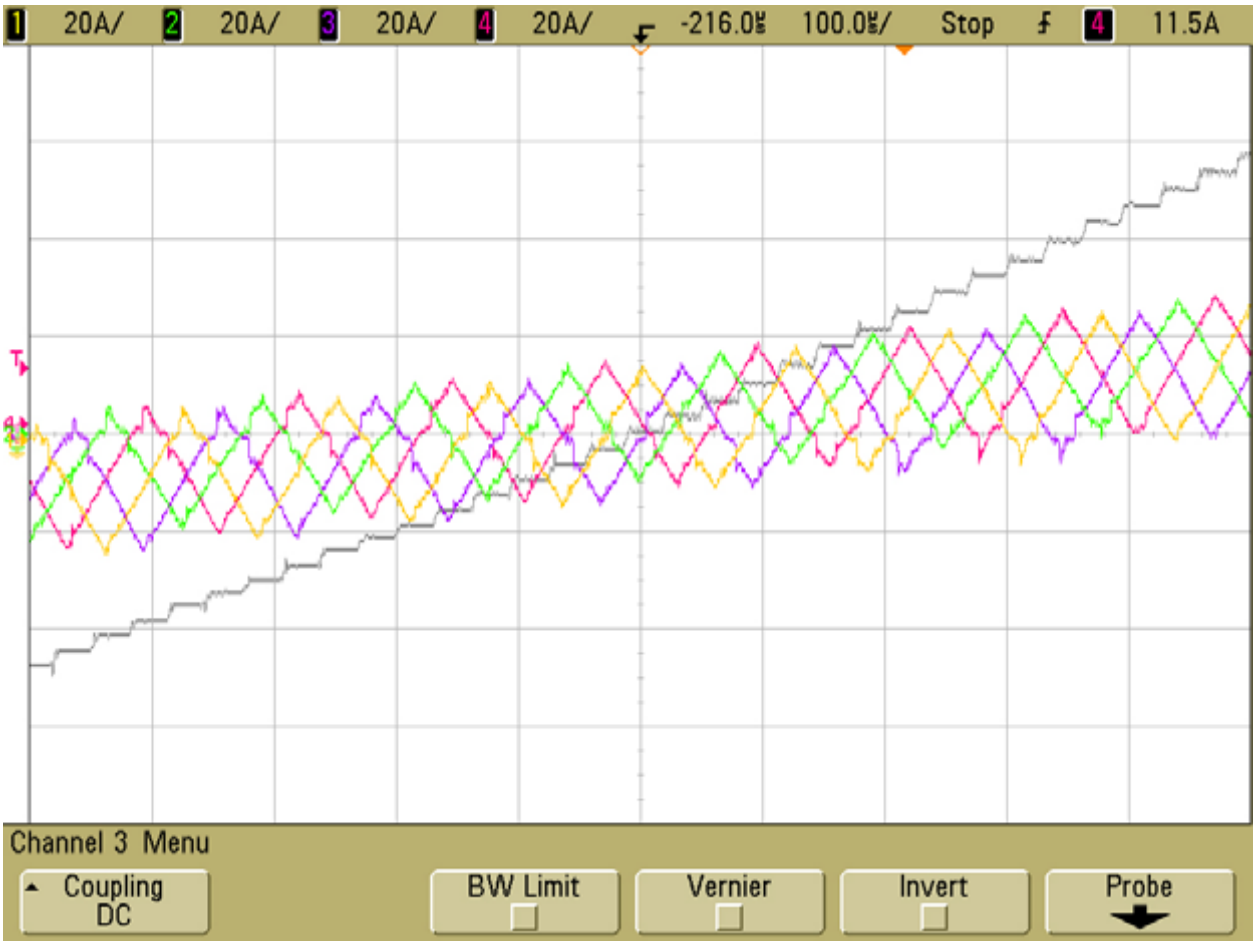



**Figure 19 - Interleaved High Frequency PWM Switching**

In Figure 18, each Y-axis grid space represents 300Amps while in Figure 19 each Y-axis grid space represents 20A. In Figure 18, each X-axis grid space represents 2 milliseconds while in Figure 19 each X-axis grid space represents 100 microseconds. The Figure 19 grid is, in effect, a small portion of the Figure 18 grid, highly magnified in amplitude and in timebase. The yellow trace is still the Matrix A current contribution to line phase #1 but shown only close to the phase current #1 zero-cross region. The green, purple and pink traces are the phase #1 current contributions of Matrices B, C and D respectively. The gray trace is the sum of all four matrix currents.

In any switching mode power supply or power converter, it is advantageous to keep the switching frequency as low as possible to minimize switching losses but and as high as possible to minimize the filtering required to convert the PWM (Pulse Width Modulated) power back to DC or in this case low frequency (60Hz) AC power. This is always the fundamental design tradeoff in this class of PV power conversion equipment. If the four colored waveforms are precisely staggered in time, as shown, the resultant high frequency peak-to-peak current ripple imposed on the gray trace, is much lower than the peak-to-peak current ripple on the colored traces because of the ripple cancellation effect. The cancellation is by simple algebraic addition.

If the colored waveforms had concurrent peaks, the peak-to-peak current ripple imposed on the gray trace would be 80Amps rather than 2Amps. This topology and control method provides switching losses typical of a 10kHz switching frequency but with the filter reduction benefits of a 40kHz switching frequency with none of the associated tradeoff penalties. This technology is protected under US Patent # 7,046,527.

This topology with multiple bridges running with interleaved high frequency switching is a very significant technological achievement and is directly responsible for the cost, weight, and size reductions achieved in this development effort.

The 500kW inverter was proven into a short circuit at full rated output current and input voltage and with interleaved high frequency switching fully operational.

# 4 SUMMARY / CONCLUSIONS

The subcontract goals were to reduce the parts cost, weight and size of the 500kW inverter by 25% when compared to state-of-the art photovoltaic inverters while extending the reliability by 25%. All subcontract goals were exceeded as shown below.

| | |
|---|---|
| **Reduced Cost** | **46% parts cost reduction** |
| **Reduced Weight** | **35% weight reduction** |
| **Reduced Size** | **56% volume reduction** |
| **Improved Reliability** | **32% extension in mean time to failure** |

Although not a specific subcontract goal, inverter conversion losses were reduced by 44%. In a system rated for an AC output of 500kW and assuming an installed PV cost of $5/Watt, this improvement in performance translates to a system cost savings of $39,000+.

| | |
|---|---|
| **Improved Performance** | **44% reduction in power conversion losses** |

In addition, a number of advancements in inverter technology were achieved.

**System Integrated Inverter Design**

**Optimized Inverter for Multi-Megawatt PV Systems**

**Plug-and-Play Manufacturing and Repair**

**High Voltage PV Array Input**

**Advanced Power Conversion Topology**

# 5 ACKNOWLEDGEMENTS

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**14. ABSTRACT** *(Maximum 200 Words)*
This report presents the outcome of this contract, first describing the 500-kW inverter, then describing the accomplishments under each of eleven contract tasks. The subcontract goals were to reduce the parts cost, weight, and size of the 500-kW inverter by 25% when compared to state-of-the-art photovoltaic inverters while extending the reliability by 25%. These goals were exceeded.

**15. SUBJECT TERMS**
PV; inverter; reliability; system integrated; power converters; single-axis tracker; manufacturing; balance-of-systems

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