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# Thin Film Si Bottom Cells for Tandem Device Structures

## Final Subcontract Report
## 15 December 2003 – 15 October 2007

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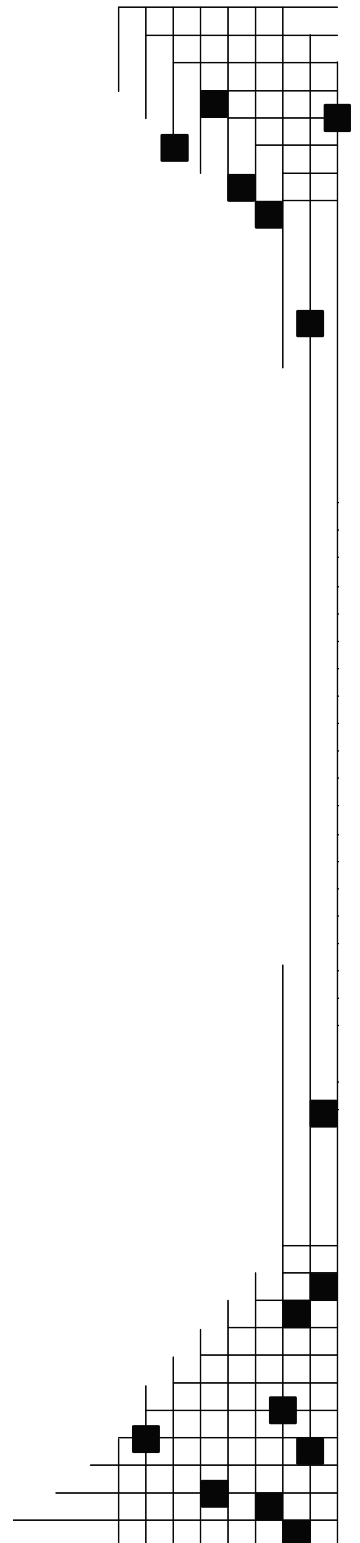*Georgia Institute of Technology*
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**Summary**

During this subcontract, Georgia Tech in conjunction with the Institute of Energy Conversion (IEC) has focused their efforts to develop high-efficiency tandem solar cells using Si bottom cells. This has involved development of the thin film Si bottom cell; and demonstrating that a wide-bandgap top cell can be deposited on a Si cell in a tandem configuration without reducing the bottom cell performance. The objectives of this project are: 1) evaluate the compatibility of Si solar cells to the CuInGaSe2 processing environment and to the subsequent cell fabrication processes; 2) develop approaches to enhance the properties of HWCVD Si films and devices; and 3) develop thin film Si devices that can be used in a tandem device configuration.

In the first phase of this work, we focused on determining compatibility of Si cells with Cu(InGa)Se2 processing and on low temperature deposition of thin film Si emitter and contact layers. Preliminary investigations used mc-Si wafers to represent the eventual polycrystalline thin Si film. Results indicate that the Si solar cell lifetime and junction properties are not impacted by the Cu(InGa)Se2 processing. PECVD deposited low temperature a-Si and μc-Si emitters and contacts have been applied to p-type c-si and mc-Si wafers achieving comparable FF~77% but lower Voc than the standard Si device. The μc-Si is a better n-type emitter but a-Si is a better p-type rear contact. Mc-Si appears more sensitive to the emitter deposition than c-Si but this may be due to lack of a high temperature P gettering step with a deposited emitter.

Next we report on the crystallization of a-Si films deposited at low temperatures on glass substrates for the fabrication of the Si bottom cell. The crystallization was performed in an RTP system after dehydrogenation of hot-wire or PECVD Si films by subjecting samples to a series of short heat pulses each with a peak temperature of 800°C or 850°C. Our results show that crystallization of a-Si films deposited by hot-wire CVD on textured glass begins in as few as two RTP cycles, with complete crystallization occurring by 10 cycles. X-ray diffraction analysis shows that the grain size in the crystallized film deposited by hot-wire CVD is only 869 Å. Crystallization after pulsed RTP was not observed for samples deposited by electron beam evaporation, suggesting that hydrogen in the CVD films or voids left behind after dehydrogenation play a role in initiating crystallization.

In the final year of the project, a shift in the strategy was made to improve the cost-effectiveness of the tandem cell. In the final year, the research focused on an a-Si thin film/crystalline silicon wafer tandem cell using a very low-cost Si wafer. The goal was to exceed the performance of low-cost c-Si solar cells, such as ribbon silicon cells, which have efficiencies in the range of 13-15%. The device fabrication was to be relatively low cost. This device would have four unique features over past efforts: 1) the mc-Si would be very low cost material, including ribbon Si, and low purity wafers; 2) the mc-Si wafer thickness would be reduced to 100-200μm to reduce costs; 3) we would investigate deposited emitter/passivation layers as an alternative to diffused emitters; 4) it would be a 2 terminal design. The mc-Si back contact and wafer passivation would be performed at GT, while the a-Si device, deposited emitter, and cell fabrication would be performed at IEC.

We fabricated an a-Si thin film/crystalline silicon wafer tandem cell using a very low-cost Si wafer and low-cost device fabrication. As part of the development of this device structure, we investigated deposited n-type emitters and found that they give low performance on mc-Si likely due to the lack of phosphorus gettering and hydrogen passivation. Because the a-Si cell in this device structure operates with light entering the n-layer, we have attempted to increase carrier collection by investigating a-Si and a-SiC n-layers. Bifacial cells with an a-Si n-layer have respectable $V_{oc}$ and FF but low $J_{sc}$ because of low i-layer thickness and the lack of a proper back reflector. We also found that the a-SiC n-layer can lead to higher $J_{sc}$, but lower FF and $V_{oc}$. We investigated Si wafers from new feedstock sources for String Ribbon growth to reduce the cost of the bottom cells. FTIR measurements showed that [Cs] and [Oi] in the samples from each of the three new feedstocks are lower than in the standard material. [Cs] in wafers from each new feedstock is quite similar (2 to 3 x 1017 cm-3), and the oxygen concentration in samples from feedstock A was relatively low (3 x 1015 cm-3). After all processing, which included PECVD SiN deposition, Al printing, and co-firing, the carrier lifetime in all wafers increased dramatically to the range of 68 µs (Feedstock A) to 98 µs (standard material). The average cell efficiency for each feedstock was in the range of 13.9 to 14.6%, indicating that the feedstock source did not strongly affect cell performance. Wafers from feedstock D showed the same average cell efficiency (14.6%), suggesting that feedstock D could be used in place of the standard feedstock if there is a cost benefit.

Finally, we investigated two methods to increase Jsc from the top cell of an a-Si/c-Si tandem device. The substrate temperature was increased from 200 to 300°C to increase the bandgap of a-Si. This did increase the short circuit current however, the $V_{oc}$ of tandem devices dropped when the deposition temperature was increased. Therefore, increasing the deposition temperature above 200°C was been dropped from further consideration. In another attempt to increase the current from the top cell, we increased the i-layer thickness from 0.25 µm to 0.35µm to increase absorption in the i-layer. This improved the current from the top cell without reducing Voc. However the fill factor decreased concurrently resulting in a modest improvement in cell efficiency (0.3%) due to the increase in i-layer thickness. The experiments were not able to reproduce the 11.3%-efficeinct tandem device on FZ Si that was achieved in the last section. We believe that contamination limited the efficiency of the best tandem devices to 7.6%.

# 1. Process Compatibility between CuInGaSe2 and c-Si Solar Cells During Tandem Cell Fabrication

## 1.1 Research Objectives

The goal of this project is to develop high efficiency thin Si solar cells as the low band gap bottom cell for high efficiency thin film tandem applications. This work supports the goals of the High Performance Program to achieve a 15% polycrystalline tandem cell by 2006. The objectives of this subcontract over its three-phase duration are: 1) evaluate the compatibility of Si solar cells to the CuInGaSe$_2$ processing environment and to the subsequent cell fabrication processes; 2) develop approaches to enhance the properties of HWCVD Si films and devices; and 3) develop thin film Si devices that can be used in a tandem device configuration.

## 1.2 Technical Approach

There are two approaches to validate the tolerance of Si bottom cells to Cu(InGa)Se2 process conditions. One approach is to deposit Cu(InGa)Se2 layers onto bare wafers, then etch away the Cu(InGa)Se2 and proceed with standard Si solar cell fabrication. A second approach is to deposit Cu(InGa)Se2 on partially or fully completed devices and then test them in novel ways without etching the Cu(InGa)Se2. To meet the objective of developing thin Si devices, we have investigated thin film Si/c-Si heterojunctions using deposited emitters, passivation and contact layers deposited by plasma enhanced CVD (PECVD) as prototypes.

## 1.3 Results and Accomplishments

1.3.1 Impact of Cu(InGa)Se2 Processing on Si solar cells

The possible impact of Cu(InGa)Se2 processing on Si devices has been investigated using several types of structures. One variable is the interlayer or buffer between the Si and Cu(InGa)Se2. This layer must be transparent beyond 700 nm and can act as both a diffusion barrier and as interconnect "tunnel" junction. Since it was known that Cu(InGa)Se2 grows on ITO, a 200 nm ITO layer was sputtered on the Ag grid/SiN surface of the completed c-si solar cells. Cu(InGa)Se2 films with Eg~1.5 eV were deposited at IEC by multisource vacuum evaporation at 550°C for 1 hr on glass and on Si solar cells with ITO.
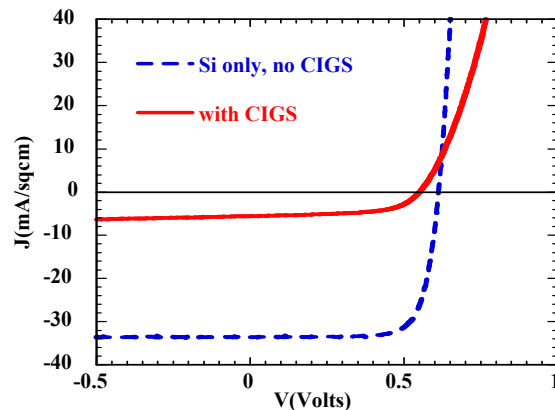


Figure 1-1. Light JV of Si solar cell before and after deposition of Cu(InGa)Se2 layer.

Figure 1-1 shows the JV curves before and after Cu(InGa)Se2 growth.  Clearly the junction remains intact.  Voc decreased from 0.61 t o 0.54, mostly due to the decrease in Jsc from 33 to 5 mA/cm2.  Figure 1-2 shows the QE before and after Cu(InGa)Se2. The dashed line shows that optical transmission normalized by reflection T/(1-R) for the Cu(InGa)Se2 agrees fairly well with the measured QE. Relatively low sub-gap transmission in CIGS is a problem being addressed in other High Performance contracts. Figure 1-2 indicates that the effect of the Cu(InGa)Se2 is primarily optical.  It is not degrading the electronic properties of the Si. This was confirmed by measuring the lifetime of 8 Si wafers with standard diffused junctions before and after deposition and etching of Cu(InGa)Se2.  The wafers had a variety of buffer layers: SiN, ITO, ITO/Mo, and nothing.  There was negligible change in effective Si lifetime with any of these coatings after deposition and etching of the Cu(InGa)Se2.
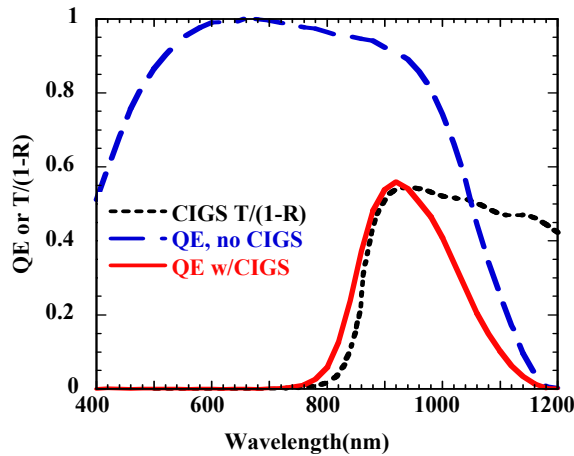


Figure 1-2.  QE of Si solar cell before and after deposition of Cu(InGa)Se2 layer on front.  Also, T/(1-R) of Cu(InGa)Se2 on glass.

1.3.2 Deposited Si layer contacts and emitters to form c-Si solar cells
We used PECVD to deposit a-Si and µc-Si p or n layers on partially processed FZ or mc-Si wafers.  The goal was to not only study their ability to function as parts of the device, but to determine the impact of replacing well-established processes such as eliminating the high temperature gettering associated with the emitter diffusion.

We deposited the p-type a-Si or µc-Si **rear contacts** on p-type wafers having standard diffused front emitters.  Both mc-Si and FZ wafers received the diffused emitter, SiN and Ag screen printed front grids at GT.  Wafers received a 20 nm a-Si p-layer  or µc-Si p-layer deposited by PECVD at IEC  at 175°C followed by a 100 nm Al layer by electron beam evaporation. The device structure was *Ag/SiN/n-diffused/p-Si wafer/p-deposited Si/Al*. We also deposited n-type a-Si or µc-Si **emitters** on p-type FZ or mc-Si wafers having standard Al paste fired rear contacts.  Transparent ITO contacts with Ni grids were deposited on top of the emitter layer giving a *Ni/ITO/n-deposited Si/p Si wafer/Al*

structure.   Table 1-1 lists the cell performance.   There was no effort to optimize the Si layer or the pre-deposition surface treatments.

Considering the first group of 4 devices (deposited rear contact), those with a-Si p-layer contacts had much better FF than devices having µc-Si despite a-Si having a much lower conductivity than µc-Si p-layers ($10^{-4}$ vs 1 S/cm). The a-Si FF's ~77% are comparable to the standard devices with fired Al-paste contacts.  The Voc on FZ wafers was about 10 mV higher than on mc-Si wafers with either a-Si or µc-Si contacts, consistent with the "standard" process.  But Voc's from the standard process are about 30 mV higher.  This suggests that a-Si/Al makes an acceptable low temperature Ohmic contact to Si (comparable FF) but it does not provide sufficient back surface passivation (lower Voc).  It is unclear why there would be such a large difference in Jsc between the deposited p-contacts and the Al fired contacts unless the standard Al processing also increases the lifetime in the bulk for example due to gettering.

The next group of 4 devices in Table 1-1 had the a-Si and mc-Si n-layer emitters.  a-Si emitters give much poorer Voc and FF on mc-Si compared to FZ Si wafers, in contrast to cells with p-type contacts, discussed above. The relatively low performance of the mc-Si base solar cells is likely due to the lack of phosphorus gettering and hydrogen bulk defect passivation step in the process sequence. Conventional mc-Si solar cell processing includes gettering of impurities from the bulk during phosphorus diffusion of the n-emitter. Hydrogenation of bulk defects in mc-Si typically occurs during a rapid anneal of the mc-Si substrates after PECVD SiN film deposition and contact printing. Both phosphorus gettering and hydrogen passivation of mc-Si substrate have been implemented in studies currently underway, which include mc-Si substrates with deposited Si back contact layers and PECVD SiN layers on top of an n-emitter.

Deposition of 10-20 nm intrinsic buffer layers between emitters or contacts as in a HIT cell resulted severe losses in FF demonstrating the sensitivity to interfacial band bending and/or intrinsic layer thickness. Thinner i-layers will be investigated.

Table 1-1. Cell parameters for devices with deposited a-Si or μc-Si p-layer contacts or n-layer emitters on FZ or mc-Si p-type wafers.  Typical results for standard Al paste fired back contact for each type of wafer processed entirely at GT is also shown as "std".

| Starting Substrate | p-type Wafer | Depst'd Si layer | Voc (V) | Jsc mA/cm$^2$ | FF (%) | Eff (%) |
|---|---|---|---|---|---|---|
| Ag/SiN/n/p | FZ | a-Si p | 0.594 | 32.1 | 76.8 | 14.6 |
| " | mc | " | 0.588 | 32.1 | 77.6 | 14.7 |
| " | FZ | μc-Si p | 0.588 | 32.4 | 68.5 | 13.1 |
| " | mc | " | 0.576 | 31.1 | 56.6 | 10.1 |
| p-c-Si/Al | FZ | a-Si n+ | 0.550 | 29.3 | 72.4 | 11.7 |
| " | mc | " | 0.474 | 27.3 | 67.1 | 8.7 |
| " | FZ | μc-Si n | 0.564 | 29.5 | 77.3 | 12.9 |
| " | mc | " | 0.454 | 29.4 | 65.9 | 8.7 |
| Std | FZ | None | 0.635 | 34.7 | 77.4 | 17.1 |
| Std | mc | None | 0.626 | 34.3 | 78.2 | 16.8 |

## 1.4 Conclusions

Preliminary studies of the processing of a Si bottom cell have shown that it is relatively immune to Cu(InGa)Se2 deposition.  Low temperature PECVD deposited rear contacts and emitters are capable of providing low resistance and high quality junctions but with lower passivation and/or lifetime due to lack of certain high temperature process steps.  Future work will focus on developing a low temperature thin Si bottom cell.

## 2. Crystallization of a-Si Films Deposited at Low Temperatures on Glass Substrates

### 2.1 Solid Phase Crystallization of a-Si in RTP

In this section we report on the crystallization of a-Si films deposited at low temperatures on glass substrates to form the bulk of the Si bottom cell. Existing methods of post-deposition crystallization of Si such as zone melt recrystallization (ZMR) and conventional furnace annealing require either high temperature processing that is not compatible with glass substrates or prolonged anneals. The alternative solid phase crystallization method that is investigated in this studied is pulsed rapid thermal annealing (RTP)[1], which involves a series of cycles that consist of a pre-heating the Si sample on glass followed by a fast ramp up to 800 or 850°C for 1 s. In this method crystallization occurs in a matter of minutes and thermal damage to the glass is avoided by the short duration of the high-temperature pulses.

### 2.2 Results – Effect of Pulsed RTP on Crystallization of a-Si Films on Glass

Crystallization of ~1.5 µm a-Si films by pulsed RTP was studied on samples deposited by hot-wire CVD (HWCVD), DC-PECVD, and electron beam (EB) evaporation. Deposition temperatures were 250°C for HWCVD, 300°C for PECVD, and <50°C for EB. Samples deposited by HWCVD and PECVD were annealed in $N_2$ for 1 hour at 400°, 500°C, and 580°C in a tube furnace to drive hydrogen out of the films. Then each sample was subjected to a pulsed RTP treatment that consisted of pre-heating the at 550°C for 60s, followed by a fast ramp up to 800 or 850°C for 1 s and rapid cool down to 550°C. This cycle was repeated for a total of 2, 4 or 10 cycles to enhance grain growth. Crystallization of the a-Si films was observed by Raman spectroscopy (785 nm laser) and crystallite size was determined by X-ray diffraction. Figure 2-1 shows the Raman spectra for ~1.5 µm thick Si films deposited by HWCVD on 1735 glass after deposition, after dehydrogenation, and after two cycles of pulsed RTP with a peak temperature of 800°C. The data shows broad peaks for the as-deposited film and the film after de-hydrogenation alone indicating the presence of an a-Si phase. However, after pulsed RTP a sharp Raman peak centered at about 521 cm$^{-1}$ appears indicating that crystallization has occurred after only 2 cycles of pulsed RTP. Figure 2 shows the Raman spectra for HWCVD Si films on textured 1737 glass annealed in 4 RTP cycles at 800°C and 10

cycles at 850°C, respectively. Analysis of the Raman spectra for the sample annealed in 4 RTP cycles at 800°C showed that the crystalline fraction ($F_C$) was 42%. When the number of cycles was increased to 10 and the peak temperature increased to 850°C, $F_C$ increased to 100% for the HWCVD Si sample on textured 1737 glass. Figure 3 shows the X-ray diffraction pattern of Si films deposited by HWCVD and PECVD after 10 cycles of pulsed RTP. The crystallite size ($D_G$) of each sample in Fig. 3 was determined by measuring the breath of the X-ray diffraction peaks, with a correction for microstrain broadening. The results in Fig. 2-3 show that the crystallite size in the HWCVD film on smooth 1737 glass was greater than that in the PECVD film, and that texturing the 1737 glass leads to a crystallite size of 869 Å after 10 cycles of pulsed RTP. We suspect that hydrogen is playing a role in the pulsed RTP Si crystallization that we have observed. Unlike HWCVD and PECVD Si films, we have not observed crystallization of e-beam Si films on glass after pulsed RTP. This result may be due to the absence of hydrogen in
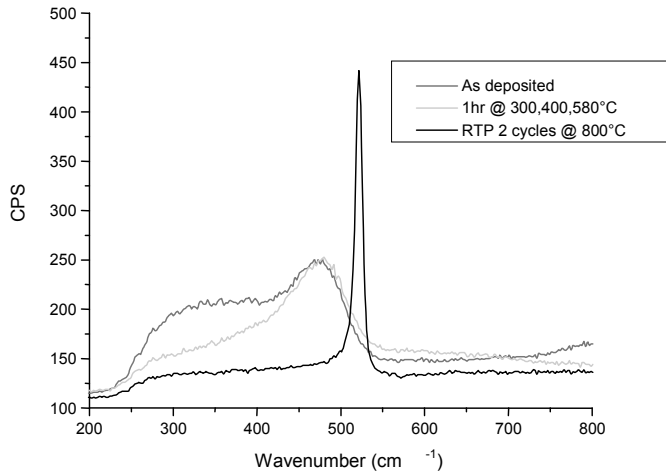


Fig. 2-1 Raman spectra for Si on glass after HWCVD, dehydrogenation, and pulsed RTP.
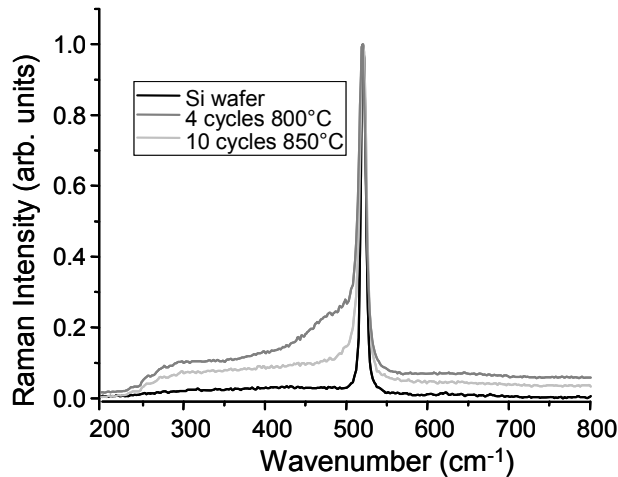


Fig. 2-2 Raman spectra for HWCVD films deposited on textured 1737 glass annealed in 4 cycles at 800°C and 10 RTP cycles.

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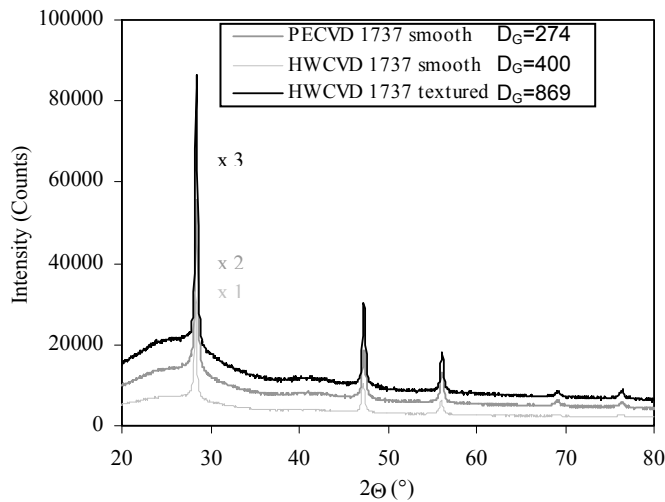
Fig. 2-3 X-ray diffraction patterns for Si films deposited by HWCVD and PECVD on textured and smooth 1737 glass after 10-cycles of pulsed RTP.

the e-beam Si film or voids left in HWCVD and PECVD films after the dehydrogenation anneal, which may initiate crystallization.


## 2.3 Conclusions

We have found that HWCVD and PECVD Si films on glass substrates can be crystallized after deposition during series of short heat pulses in an RTP system. Our preliminary results show that crystallization of a-Si films deposited by hot-wire CVD on textured glass begins in as few as two RTP cycles with a peak temperature of 800°C, with complete crystallization occurring by 10 cycles with a peak temperature of 850°C. X-ray diffraction analysis shows that the crystallite size in the crystallized film deposited by hot-wire CVD and treated in RTP can be as high as 869 Å. Crystallization was not observed after pulsed RTP for samples deposited by electron beam evaporation, suggesting that hydrogen or voids in the CVD films left behind after dehydrogenation may play a role in initiating crystallization. Future will focus on methods to enhance the grain size further by using a low-temperature conventional furnace anneal before or after the pulsed RTP treatment.


## 2.4 References

1. Y. Zhao, et al., "Polycrystalline silicon films prepared by improved pulsed rapid thermal annealing," *Sol. Eng. Mats. Sol. Cells*, **62**, 143-148 (2000).

## 3. Development of a-Si Thin Film/Crystalline Silicon Wafer Tandem Cells

### 3.1 Critical Issues to Develop a-Si/c-Si Tandem Solar Cells

Unlike all other a-Si devices, the a-Si cell in this device structure will operate with light entering the n-layer because we will be using a p-type Si wafer. Therefore, n-type window layers and appropriate buffer (transition) layers will be developed. Another critical issue is to obtain the maximum current from the a-Si top cell since it will limit the two terminal tandem current. Three ways to control the matching and obtain higher tandem currents that will be investigated include increasing the top cell thickness, decreasing its bandgap, or increasing its effective absorption using optical enhancement.

### 3.2 Results and Accomplishments

#### 3.2.1 Performance of deposited Si emitters on mc-Si substrates

We deposited n-type a-Si and µc-Si emitters on p-type mc-Si wafers having standard Al paste fired rear contacts. There was no effort to optimize the Si layer or the pre-deposition surface treatments. Transparent ITO contacts with Ni grids were deposited on top of the emitter layer giving a Ni/ITO/n-deposited Si/p Si wafer/Al structure. Table 3-1 lists the cell performance.

Table 3-1. Cell parameters for devices with deposited a-Si or µc-Si n-layer emitters mc-Si p-type wafers. Typical results for cells with diffused emitters are also shown.

| Deposited Si layer | Wafer | Voc (V) | Jsc (mA/cm$^2$) | FF (%) | Eff (%) |
|---|---|---|---|---|---|
| a-Si n+ | mc-Si | 0.474 | 27.3 | 67.1 | 8.7 |
| µc-Si n | mc-Si | 0.454 | 29.4 | 65.9 | 8.7 |
| None | mc-Si | 0.626 | 34.3 | 78.2 | 16.8 |

The data in Table 3-1 shows that a-Si emitters give much poorer $V_{oc}$ and FF on mc-Si compared cells with diffused emitters. The relatively low performance of the mc-Si base solar cells is likely due to the lack of phosphorus gettering and hydrogen bulk defect
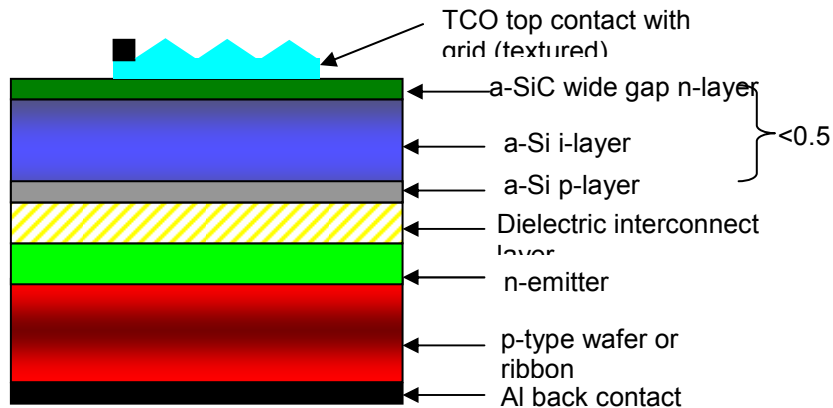


Fig. 3-1. a-Si/c-Si tandem solar cell device schematic

passivation step in the process sequence. Conventional mc-Si solar cell processing includes gettering of impurities from the bulk during phosphorus diffusion of the n-emitter. Hydrogenation of bulk defects in mc-Si typically occurs during a rapid anneal of the mc-Si substrates after PECVD SiN film deposition and contact printing. Since the SiN ARC is replaced by a dielectric interconnect layer between the top and bottom cell, as shown in Fig. 3-1, a new hydrogen defect passivation technique must be developed without depositing SiN on bottom cell's emitter surface. Therefore, future work will focus on hydrogenation techniques such as backside SiN deposition, $NH_3$ plasma exposure, and a forming gas anneal at Georgia Tech, and $H_2$ plasma exposure at IEC.
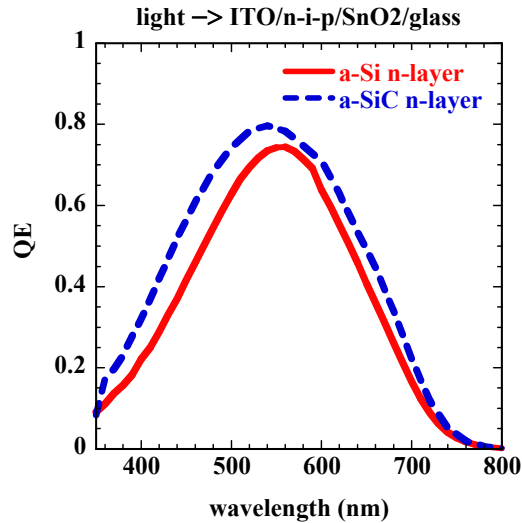


Fig. 3-2. QE at –1V for 2 different a-Si p-I-n devices, with either a-Si or a-SiC n-layer measured for light incident through ITO/n-layer. The integrated photocurrent with a-SiC increases by about 1 mA/cm$^2$ compared to the a-Si n-layer.


### 3.2.2 Increasing collection for light entering through the n-layer

In order to investigate increasing the collection for light through the n-layer, bifacial devices having structure glass/SnO2/p-i-n/ITO/grids were fabricated with a-Si and a-SiC n-layers. Table 3-2 shows JV performance for a-Si devices having a-Si or a-SiC n-layers. For each type, results are shown for standard Al as well as transparent ITO/grid contacts. Results for the ITO/grid devices are shown for light incident through the front (glass/SnO2) or back (ITO/n). Respectable $V_{oc}$ and FF result with the a-Si n-layer, but $J_{sc}$ is low because the i-layer is relatively thin (0.25 µm) and there is not a proper back reflector (ITO/Al, or ZnO/Ag, etc). The FF is comparable for light through p-layer (glass) or n-layer (ITO). However, Table 3-1 shows that the FF decreases with the more resistive a-SiC n-layer. The decrease is greater with the ITO contact compared to Al. The decrease in FF is related to curvature in the JV curve and increased series resistance. We have observed this previously with a-Si solar cells deposited at IEC and solved this problem by using a highly doped µc-Si n-layer.

Table 3-2. JV performance for a-Si devices having a-Si or a-SiC n-layers. For each type, results are shown for standard Al as well as transparent ITO/grid contacts. Results for the ITO/grid devices are shown for light incident through the front (glass/SnO2) or back (ITO/n).

| i-layer | Back Contact | Light Direction | $V_{oc}$ (V) | $J_{sc}$ (mA/cm$^2$) | FF (%) | Eff (%) |
|---------|--------------|-----------------|--------------|----------------------|--------|---------|
| a-Si | Al | **glass** | **0.865** | **10.6** | **73** | **6.7** |
| | **ITO/grid** | **glass** | **0.869** | **11.5** | **66** | **6.6** |
| | | **ITO** | **0.869** | **11.9** | **64** | **6.6** |
| a-SiC | Al | **glass** | 0.820 | 11.4 | 54 | 5.1 |
| | **ITO/grid** | **glass** | 0.808 | 11.4 | 40 | 3.7 |
| | | **ITO** | **0.809** | **12.3** | **46** | **4.6** |

Figure 3-2 shows the QE for devices with a-Si and a-SiC n-layers with light entering through the n-layer. The bandgap of the n-layer increased from 1.7 to 1.85 with the addition of $CH_4$ during the n-layer growth. The integrated AM1.5 photocurrent increased about 1 mA/cm2 with the wider bandgap n-layer. This is greater than the difference in $J_{sc}$ in Table 3-1 because the QE is obtained at –1V where the reverse bias field reduces collection losses.

   Future work will focus on optimizing n-layer properties and the transition buffer layer between each of the doped layers and the i-layer. Recently, we  obtained a $V_{oc}$ of 0.91 V with an unacceptably low FF by incorporating a graded a-SiC buffer at the p-layer, as is commonly practiced.


### 3.2.3 **Transmission of a-Si top cell**
All devices have been fabricated so far on textured SnO2/glass substrates that can have considerable absorption beyond 800 nm due to free carrier absorption in the SnO2, absorption in the glass, and internal light trapping in the textured SnO2.  Since the monolithic tandem will not incorporate a textured SnO2/glass, its optical losses should be removed from the transmission. Fig. 3-3 shows the transmission as-measured from MC0249-08, a p-i-n device on Asahi SnO2/glass with ITO/grids for a back contact. Transmission was measured through the device thus included the 4% loss through the opaque metal grid and the optical loss due to absorption in the SnO2/glass.  The corrected spectra is also shown.  The average value between 800 and 1200 nm is 66%, very close to the milestone goal of 70%.
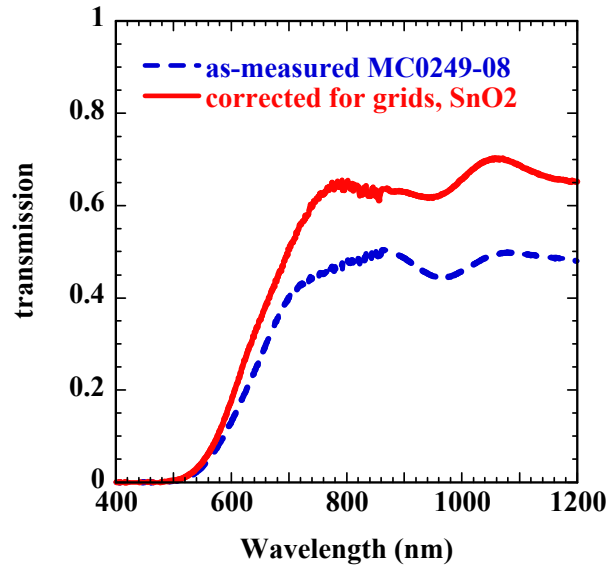
Figure 3-3. Transmission of device on textured SnO2, as measured and after correction for 4% grid shadow and SnO2 absorption.

### 3.2.4 **Modeling to guide device design**

Given that the bottom cell has Jsc>33 mA/cm2 under unfiltered light and the best a-Si cell only has 16-17 mA/cm2, it is clear that the top cell will be current limiting. Thus a major goal is to increase the top cell current. But it must remain transparent which prevents use of a high quality Ag/ZnO back reflector. Without a dielectric buffer layer (giving a favorable index mismatch to reflect light back into the a-Si cell) and without texture (increasing absorption due to light trapping), the a-Si top cell will be limited to about 12-13 mA/cm2.

We applied some optical models developed at IEC under previous NREL contracts for a-Si multijunction analysis. The QE was calculated for various thicknesses, bandgaps and optical enhancement conditions and integrated with AM1.5 spectrum (IQE). The top cell was modeled with the following assumptions:

1. Panchromatic reflection of 2% (assumes an ARC).
2. TCO absorption from a ~0.1um ZnO layer.
3. The top n-layer was 0.01 nm and 2.0 eV using absorption data from our a-SiC p-layers.
4. The i-layer absorption was determined from a 1.8 eV i-layer and also shifted in energy to represent a 1.73 eV a-Si layer.
5. i-layer thickness as variable from 0.08 to 0.5 μm.
6. Optical enhancement was incorporated using the pathlength enhancement factor m which increased from 1 to 5 with wavelength (see Hegedus and Kaplan, Progress in Photovoltaics 10, 2002, pp257-269 for details). But no back reflection was

included ($R_B$=0) since the device must be transparent. This limits the effectiveness of the scattering.

Figure 3-4 shows the effect of i-layer thickness on the Jsc (assumed to be equal to IQE) for two bandgaps and optical enhancements. Our present devices are 0.25 µm thick and have bandgaps of about 1.75 eV, which is in good agreement with the calculation. Clearly it is important to increase the i-layer thickness and lower the bandgap to have
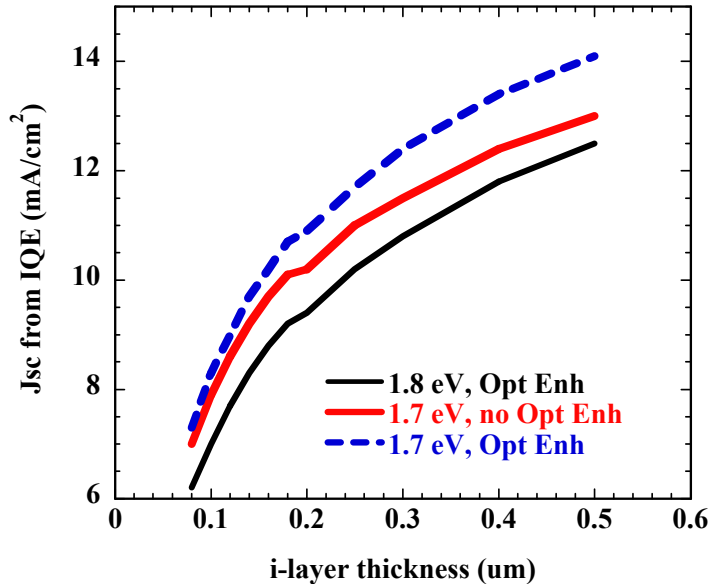


Figure 3-4. Calculated effect of thickness on IQE for two bandgaps, with and without optical enhancement.

substantial increase in IQE. We can reduce the bandgap <1.70 eV by increasing substrate temperature and reducing H2 dilution.  However, the effect on i-layer quality is unknown.  Increasing thickness beyond 0.4 µm increases the effect of light-induced degradation as well.  Figure 3-5 shows the calculated QE for 0.4 µm thick i-layers and the measured QE for the ribbon cell.

To calculate tandem efficiency, we assumed the following:

1. The Voc for the a-Si top cell was 0.88V, which rather conservative since we have already obtained Voc=0.92V but it might decrease with lower bandgaps. Voc was independent of Jsc or thickness, which is consistent with experimental results in this range.
2. The FF for the top cell was 68% independent of bandgap.  This is conservative.
3. The Voc for the Si bottom cell decreased as ln(Jsc) as predicted by the standard equation.  This represented a 20-40 mV loss over the range of top cell Jsc considered here.
4. The FF for bottom Si cell was 76% independent of its Jsc or Voc.

Figure 3-6 shows the calculated tandem cell efficiency as function of top cell Jsc. It increases nearly linearly with current since the top cell is current-limiting.  The best ribbon cells have >15.5% efficiency. Subject to the simplifying assumptions above, the top cell must generate over 15 mA/cm$^2$ to result in a net gain in performance.  While currents of this size are realizable in a-Si, they require rather good optical enhancement and light trapping. This analysis did not consider any optical or electrical losses at the interconnect junction.

Note that United Solar Ovonics produces a very thin (~0.1-0.2 μm) wide gap a-Si top cells for a-Si based triple junctions having ~8 mA/cm2 (no optical enhancement allowed for the top cell), FF=78%, Voc=1.05 V and Eff=6.5%. This is ideal for an a-Si/a-SiGe/a-SiGe triple stack but not acceptable for a c-Si tandem.  Instead we look to the micromorph tandem for guidance in optical design in which the bottom cell is nc-Si. Recently, several groups making micromorph devices have published results showing the benefit of a dielectric layer inserted between the two cells to increase reflection back into the top a-Si device, hence increasing Jsc for the tandem.  This may complicate or may actually assist the formation of the low resistance interconnect junction.
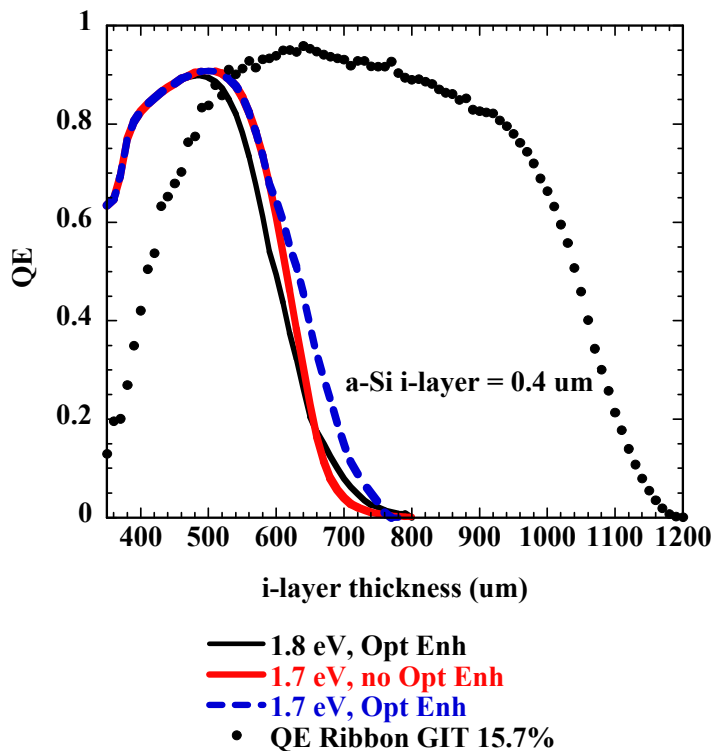


Figure 3-5. Calculated QE for 0.4 μm thickness and 3 combinations of bandgap and enhancement. QE measured at GT on ribbon cell shown for comparison.
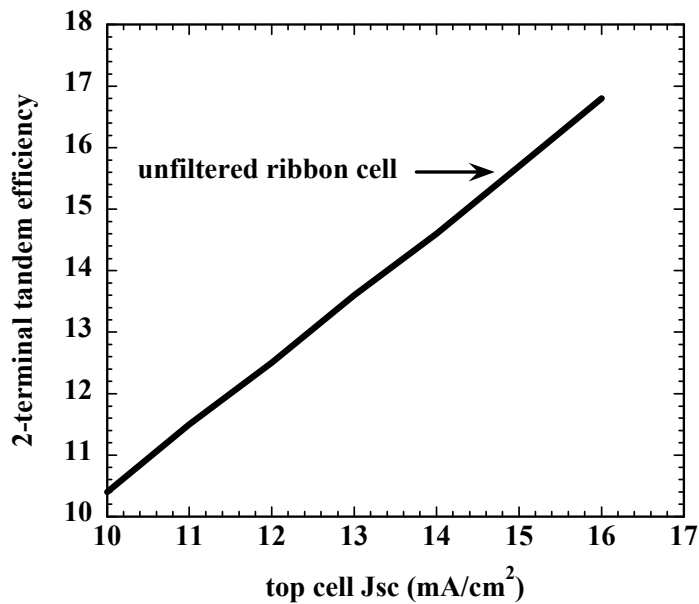
Figure 3-6. Calculated tandem cell efficiency as function of top cell Jsc. The present ribbon cells have 15.7% efficiency.

### 3.2.5 Development of solar cell on ribbon silicon from low-cost Si feedstock

Solar cells were fabricated on wafers from three different feedstocks from Evergreen Solar along with the standard 300 µm thick String Ribbon for comparison. The samples from the three new feedstocks were named A, C and D while the standard String Ribbon sample was named B. For this experiment, two wafers from each feedstock were selected and cut to size for small area (4 cm$^2$) cell fabrication. Wafers from each feedstock were then analyzed using Fourier Transform Infrared (FTIR) Spectroscopy to obtain the oxygen and carbon concentrations in the bulk. FTIR measurements were performed on two wafers from each feedstock.  Carrier lifetime measurements were performed on samples from each feedstock at various stages of cell fabrication as shown in Fig. 3-7.

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┌─────────────────┐              ┌─────────────────┐
│  Wafer Cutting  │ ───────────▶ │  FTIR (Cs, Oi)  │
└─────────────────┘              └─────────────────┘
         │
         ▼
┌─────────────────┐              ┌─────────────────┐
│    Cleaning     │ ───────────▶ │   As-grown τ    │
└─────────────────┘              └─────────────────┘
         │
         ▼
┌─────────────────┐              ┌─────────────────┐
│ POCl₃ 45 Ω/sq   │ ───────────▶ │ Post diffusion τ│
└─────────────────┘              └─────────────────┘
         │
         ▼
┌───────────────────┐
│ Glass Etch /Cleaning │
└───────────────────┘
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│   PECVD SiNₓ     │
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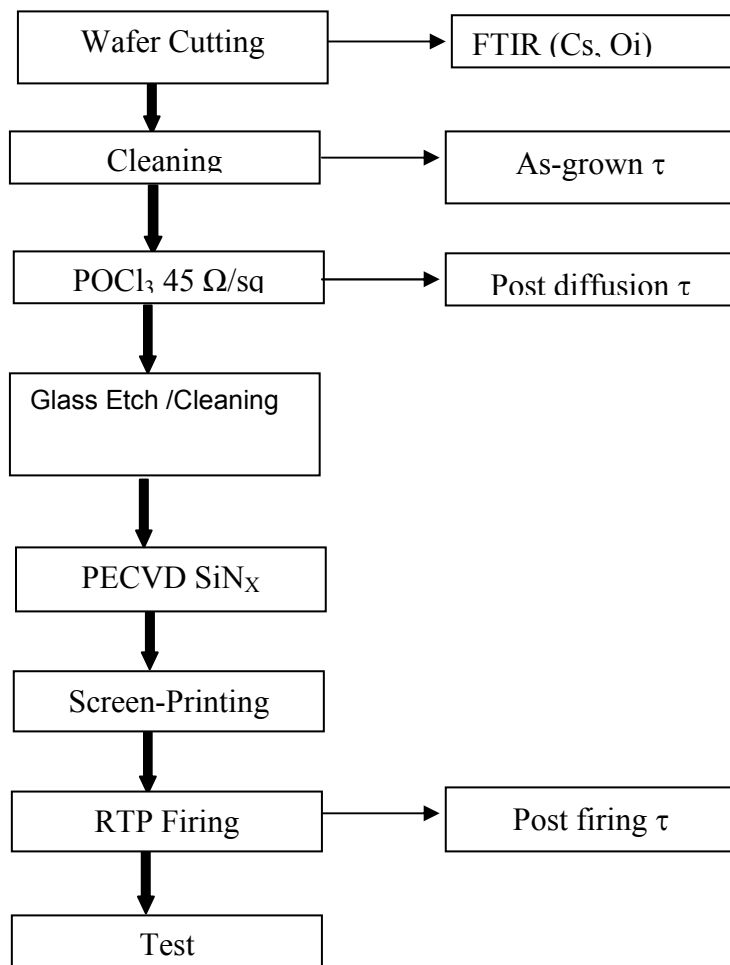
Fig 3-7 Experimental flow chart showing points at which samples
were removed for lifetime and FTIR measurements.

3.2.6 **Measurement of oxygen and carbon concentrations in silicon ribbons**

The results of the FTIR measurement of the susbtitutional carbon (Cs) and interstitial oxygen (Oi) concentrations in each feedstock are as shown in Fig. 3-8, with average values indicated. The results show that the [Cs] and [Oi] in the samples from each of the three new feedstocks are lower than in the standard material. The results also show that [Cs] in wafers from the new feedstocks is quite similar (2 to 3 x $10^{17}$ $cm^{-3}$), and the oxygen concentration in samples from feedstock A was relatively low (3 x $10^{15}$ $cm^{-3}$). It should be noted that Oi levels in all samples was very close to or below the detection limit for Oi for our FTIR system. In most cases, Oi could be determined for only one wafer per feedstock.
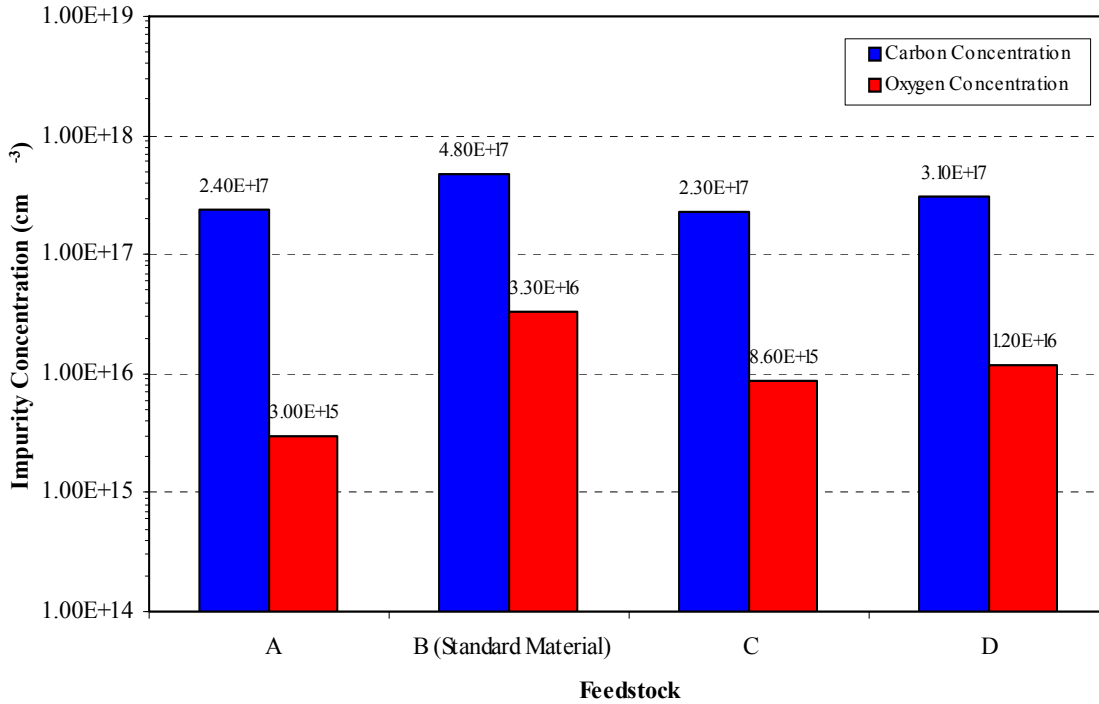
Fig. 3-8 Average interstitial oxygen and susbtitutional carbon concentrations measured on two wafers from each feedstock determined by FTIR.
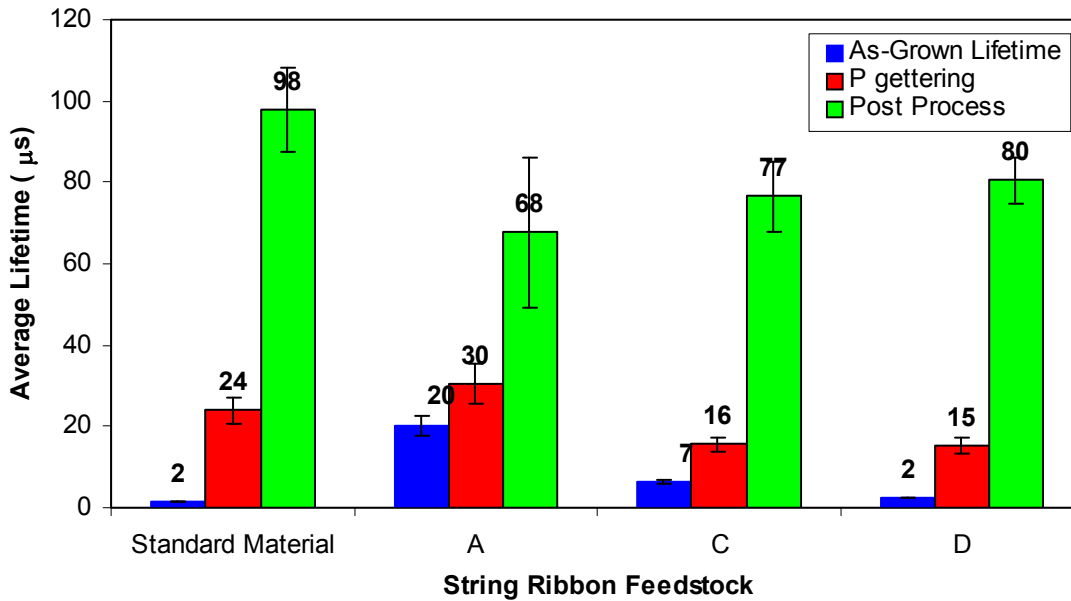


Fig. 3-9 Progress of the lifetime in String Ribbon wafers from three new feedstocks and the standard material during cell processing at Georgia Tech. The excess carrier concentration for each measurement was 1 x $10^{15}$ cm-3.

### 3.2.7 Carrier lifetime enhancement

Fig. 3-9 shows the progress of the carrier lifetime in wafers from the three new feedstocks, and the standard material. The lifetime values shown in Fig. 3-9 are the average of six measurements performed on one wafer per condition. The results show that the carrier lifetime before processing in the wafer from Feedstock A was relatively high (20 µs), while the lifetime in wafers from the other feedstocks was below 10 µs. Note that the carrier lifetime in the standard material was only 2 µs. After phosphorus gettering, the lifetime in wafers from all feedstocks improved significantly. In most cases (except for feedstock C) the same wafer was used for the as-grown and P-gettered lifetime measurements. The wafers from the standard material showed the greatest improvement (2 µs to 24 µs). This suggests that the impurities that limit the lifetime in the standard material can be gettered by phosphorus. The lifetime in the wafer from Feedstock A, which had a high as-grown lifetime of 20 µs, improved to only 30 µs after P-gettering. After all processing, which included PECVD SiN deposition, Al printing, and co-firing, the carrier lifetime in all wafers increased dramatically. The results in Fig. 3-9 show that the lifetime in all wafers after processing was in the range of 68 µs (Feedstock A) to 98 µs (standard material). The appreciable increase in carrier lifetime in wafers from all four feedstocks after SiN deposition and co-firing suggests that hydrogenation of defects in crucial in these materials. It should be noted that the RTP firing cycle used in this study was optimized for wafers from the standard material. Modification of the RTP cycle for wafers from each new feedstock (A, C, and D) may yield even higher lifetime values.

### 3.2.8 Performance of String Ribbon cells on ribbons from low-cost feedstock

The performance of String Ribbon solar cells on wafers from the three new feedstock sources and the standard material is shown in Table 3-3. Note that the average cell performance and the performance of the best cell for each feedstock are shown in Table 3-3. The results show that the average efficiency for each feedstock was in the range of 13.9 to 14.6%, indicating that the feedstock source did not strongly affect cell performance. The results also show that the cells from the standard material had the highest average efficiency (14.6%), the highest cell efficiency (15.5%), and the highest

Table 3-3: Performance of String Ribbon solar cells (4 cm$^2$) on wafers from three new feedstock sources and standard material.

| Feedstock | Details | Voc (mV) | $J_{sc}$ (mA/cm$^2$) | Eff (%) | FF (%) | n- factor | $R_{series}$ ($\Omega$-cm$^2$) | $R_{shunt}$ ($\Omega$-cm$^2$) |
|---|---|---|---|---|---|---|---|---|
| A | Best | 0.597 | 31.4 | 14.4 | 76.6 | 1.30 | 0.51 | 2680 |
| A | Average | 0.594 | 32.1 | 13.9 | 73.1 | 1.40 | 0.90 | 2342 |
| B (Standard Material) | Best | 0.603 | 33.1 | 15.5 | 77.4 | 1.25 | 0.52 | 61920 |
| B (Standard Material) | Average | 0.593 | 32.5 | 14.6 | 75.7 | 1.29 | 0.73 | 82756 |
| C | Best | 0.590 | 32.2 | 14.6 | 76.6 | 1.21 | 0.67 | 3616 |
| C | Average | 0.590 | 32.0 | 14.0 | 74.0 | 1.24 | 1.13 | 4625 |
| D | Best | 0.604 | 32.3 | 15.0 | 77.0 | 1.31 | 0.47 | 40090 |
| D | Average | 0.596 | 32.1 | 14.6 | 76.3 | 1.27 | 0.62 | 14634 |

average lifetime after processing (98 μs). Wafers from feedstock D showed the same average cell efficiency (14.6%), suggesting that feedstock D could be used in place of the standard feedstock if there is a cost benefit.

## 3.3 Conclusions

We have found that deposited emitters on mc-Si give low performance likely due to the lack of phosphorus gettering and hydrogen passivation. To solve this problem, we will focus on hydrogenation techniques that do not rely on SiN on the front surface. Because the a-Si cell in this device structure will operate with light entering the n-layer, we have attempted to increase carrier collection for light entering through the n-layer by investigating a-Si and a-SiC n-layers. Bifacial cells with an a-Si n-layer have respectable $V_{oc}$ and FF but low $J_{sc}$ because of low i-layer thickness and the lack of a proper back reflector. Devices with a-SiC n-layers showed increased $J_{sc}$ values (12.3 mA/cm$^2$), but with lower $V_{oc}$ and FF. The lower FF is due to higher resistivity in the a-SiC n-layer.

Material from three new feedstock sources for String Ribbon growth was characterized in this study. FTIR measurements showed that [Cs] and [Oi] in the samples from each of the three new feedstocks are lower than in the standard material. [Cs] in wafers from each new feedstock is quite similar (2 to 3 x 1017 cm-3), and the oxygen concentration in samples from feedstock A was relatively low (3 x 1015 cm-3). Carrier lifetime measurements with QSS-PC showed that the carrier lifetime before processing in the wafer from Feedstock A was relatively high (20 μs), while the lifetime in wafers from the other feedstocks was below 10 μs. After phosphorus gettering, the lifetime in wafers from all feedstocks improved significantly. The wafers from the standard material showed the greatest improvement (2 μs to 24 μs), suggesting that the impurities that limit the lifetime in the standard material can be gettered by phosphorus. After all processing, which included PECVD SiN deposition, Al printing, and co-firing, the carrier lifetime in all wafers increased dramatically to the range of 68 μs (Feedstock A) to 98 μs (standard material). The appreciable increase in carrier lifetime in wafers from all four feedstocks after SiN deposition and co-firing suggests that hydrogenation of defects in crucial in these materials. The average cell efficiency for each feedstock was in the range of 13.9 to 14.6%, indicating that the feedstock source did not strongly affect cell performance. The cells from the standard material had the highest average efficiency (14.6%), the highest cell efficiency (15.5%), and the highest average lifetime after processing (98 μs). Wafers from feedstock D showed the same average cell efficiency (14.6%), suggesting that feedstock D could be used in place of the standard feedstock if there is a cost benefit.

## 4. The Effect of the Shorting Junction between the Top and Bottom Cells

### 4.1 Introduction

In the previous section, we reported on our attempts to increase carrier collection for light entering through the n-layer by investigating a-Si and a-SiC n-layers. Devices with a-SiC n-layers showed increased $J_{sc}$ values (12.3 mA/cm$^2$), but with lower $V_{oc}$ and FF. The lower FF was due to higher resistivity in the a-SiC n-layer. In this section, we investigated the effect of the shorting junction between the top and bottom cells.

### 4.2 Fabrication of a-Si/c-Si Tandem Cells With Four Unique Si Shorting Junctions

A series of tandem devices on p-type ribbon or FZ were fabricated at IEC and Georgia Tech. The p-type ribbon and FZ Si device processing was performed at Georgia Tech. In selected cases, an n$^+$ layer was formed by POCl$_3$ diffusion in a tube furnace, followed by PECVD SiN deposition on the n$^+$ surface. In some cases, the n$^+$ layer and PECVD SiN layer were omitted. Then the wafers were cut into 1"x1" samples using a dicing saw and the SiN layer, if present, was removed in dilute HF. Then the Si samples were sent to IEC for thin deposition and tandem cell fabrication. IEC used device recipes from run
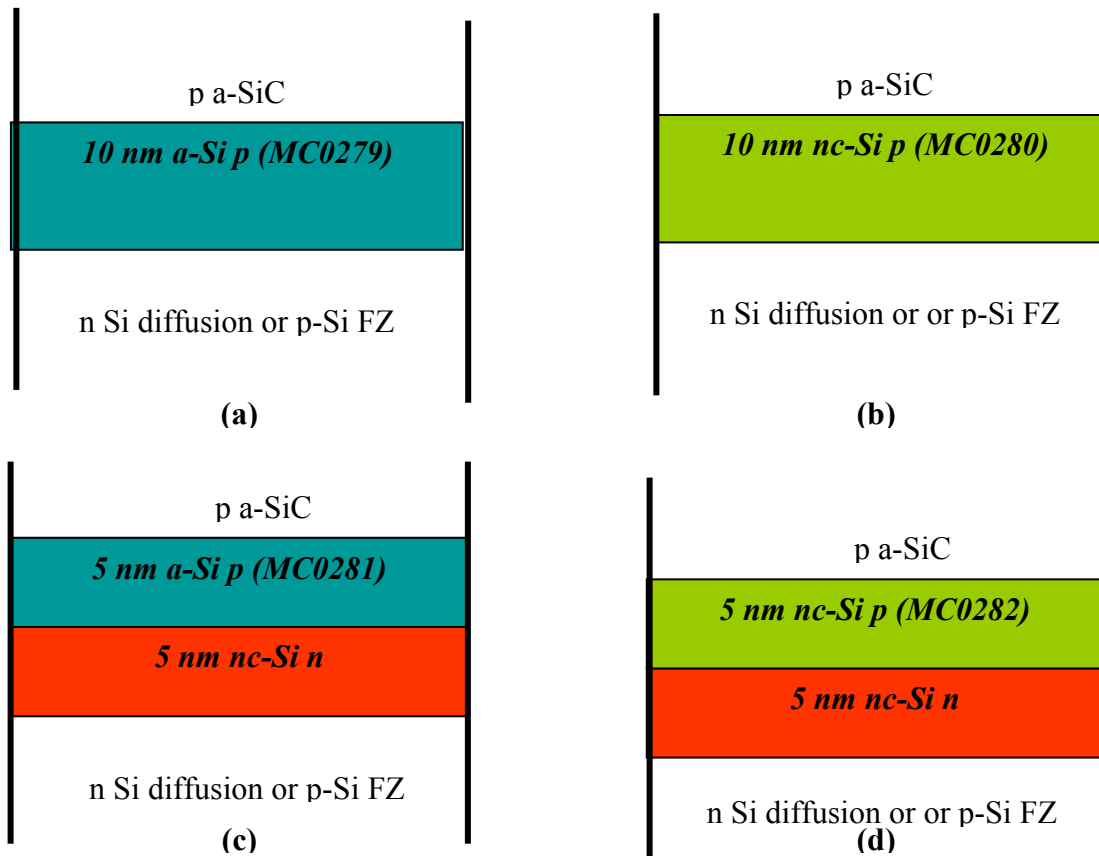


Figure 4-1: Schematic of the four shorting junctions investigated in this study. In all cases the top of the SHJ was contact the a-SiC p-layer of the a-Si solar cell and the bottom of the SHJ was contacting either the diffused emitter or bare FZ p-Si.

MC0256 as the baseline for the top a-Si cell and varied the shorting junction (SHJ), which interconnects the top and bottom cells. Run 256 has a 0.25 μm thick i-layer. The p-layer was a-SiC with a graded H buffer or transition region, and the n-layer was a-SiC terminating with a nc-Si layer. The top nc-Si was needed to give a good ohmic contact with the ITO.

The bottom Si device, if it has a diffused emitter, presents a n-type layer to be contacted by the SHJ. It was not known if a high carrier density nc-Si layer would be needed to provide good contact and high recombination for the holes from the a-Si p-layer. Four different SHJ were investigated as shown in Figure 4-1. The first two (used in runs 0279 and 0280) had a 10 nm thick a-Si (Figure 4-1 (a)) or nc-Si p-layer (Figure 4-1 (b)). The second two (used in runs 0280 and 0282) had a 5 nm nc-Si n-layer followed by 5 nm a-Si (Figure 4-1 (c)) or nc-Si p-layers (Figure 4-1 (d)). Note that this nc-Si n-layer would make an ohmic contact to the n-diffusion, and would act like a deposited emitter on a bare p-Si wafer. Each run had a mixture of p-Si ribbon with diffused emitters and p-Si FZ wafer without any diffusion. Each run also had a piece of textured $SnO_2$ to make a standard a-Si pin cell as a control.

In each run, after the a-Si SHJ and a-Si p-i-n cell was deposited, the wafer was flipped and a 10 nm a-Si p-layer was deposited on the back side of all wafers. Al was deposited on this p a-Si and upon annealing at 200°C for 10 minutes forms an excellent ohmic contact to the Si wafer. Cells were completed with ITO and Ni/Al grids and a cell area of 0.56 cm$^2$ was defined.

## 4.3 Performance of Tandem Cells Using The Four Si Shorting Junctions

Table 4-1 lists the JV performance for the devices on the FZ wafer. Devices from the top two runs (0279 and 0280) have no nc-Si n-layer in the SHJ so they do not form a c-Si bottom cell. They are only top a-Si cells. The bottom two runs (0281 and 0282) have the nc-Si n-layer, which forms a deposited emitter on the p-FZ. From their voltage ($V_{oc}$~1.5V), they are clearly tandem cells. Given that the a-Si top cell has Voc=0.9V, the bottom cell must have Voc=0.6V. The FF is greatly improved with the nc-Si n-layer.

Table 4-1. JV performance for cells on p-FZ silicon.

| Shorting Junction (run) | Voc (V) | Jsc (mA/cm$^2$) | FF (%) | Eff (%) | QE peak |
|---|---|---|---|---|---|
| 10 nm Ar diluted a-Si p (MC0279) | 0.91 | 10.0 | 59.7 | 5.4 | 0.80 |
| 10 nm 'nc-Si' p (MC0280) | 0.90 | 10.0 | 60.1 | 5.4 | 0.78 |
| 5 nm 'nc-Si' n / 5 nm a-Si p (MC0281) | 1.49 | 10.5 | 70.0 | 11.0 | 0.78 |
| 5 nm 'nc-Si' n /5 nm nc-Si p (MC0282) | 1.52 | 10.2 | 72.9 | 11.3 | 0.77 |

The control cells on SnO$_2$ also had Voc=0.9V. Figure 4-2 shows the JV curves for the two devices with SHJ without the nc-Si n-layer. Slight S-shaped curvature was apparent in the power quadrant on 0280. This indicates a blocking contact between the SHJ and wafer since the control piece did not exhibit the S-curvature. Figure 4-3 shows the JV curve for the tandem from 0281 on FZ p-Si having the deposited emitter. Clearly it makes a good junction and good SHJ as well.
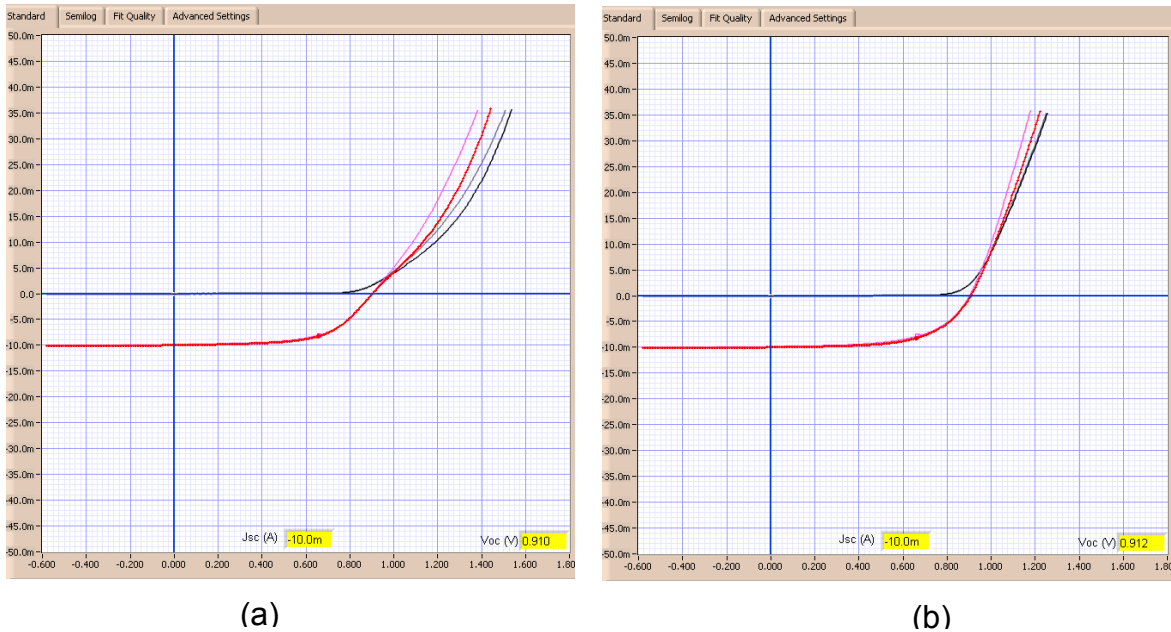


(a)                                    (b)

Figure 4-2. Light and dark JV curves of <u>single junction </u>devices on FZ p-Si wafers with (a) a 10 nm a-Si p SHJ (MC0279) and (b) a 10 nm nc-Si p SHJ (MC0280).

Table 4-2. JV performance on p-Si ribbon with diffused emitter.  These are all tandem devices.

| Shorting Junction (run) | Voc (V) | Jsc (mA/cm$^2$) | FF (%) | Eff (%) | QE peak |
|---|---|---|---|---|---|
| 10 nm Ar diluted a-Si p (MC0279) | 1.42 | 11.1 | 55.8 | 8.8 | 0.81 |
| 10 nm 'nc-Si' p (MC0280) | 1.41 | 10.9 | 53.1 | 8.3 | 0.80 |
| 5 nm 'nc-Si' n / 5 nm a-Si p (MC0281) | 1.45 | 10.4 | 64.5 | 9.8 | x |
| 5 nm 'nc-Si' n /5 nm nc-Si p (MC0282) | 1.43 | 10.0 | 67.6 | 9.7 | x |

Table 4-2 shows the JV performance for the four different SHJ on the p-Si ribbon with the diffused emitter. Compared to the deposited emitters on FZ Si in Table 1, the $V_{oc}$ for the cells on ribbon Si is about 0.1V lower and FF is 5-10% lower as well.  Figure 4-3 shows the JV curves for the two devices without the nc-Si n-layer in the SHJ. Note that 0280 has slight S-curve inflection in the power quadrant just like on the FZ piece in Figure 4-2. This behavior must be within the SHJ itself not the contact between the SHJ and Si since they were so different. Figure 4-5 shows the JV curves for the tandem from 0281. We note the large difference between light and dark JV but have no explanation.

It is well established that the top and bottom cell QE for series connected tandem cells can be measured using colored bias light. Blue bias light is absorbed in the top cell.  If the total bias is 0V, then the top cell is at +Voc and the bottom cell is –Voc so the bottom QE is measured with blue bias. Similarly, with red bias the top cell QE is measured. With full bias light the current limiting cell is measured.  In the dark (no bias
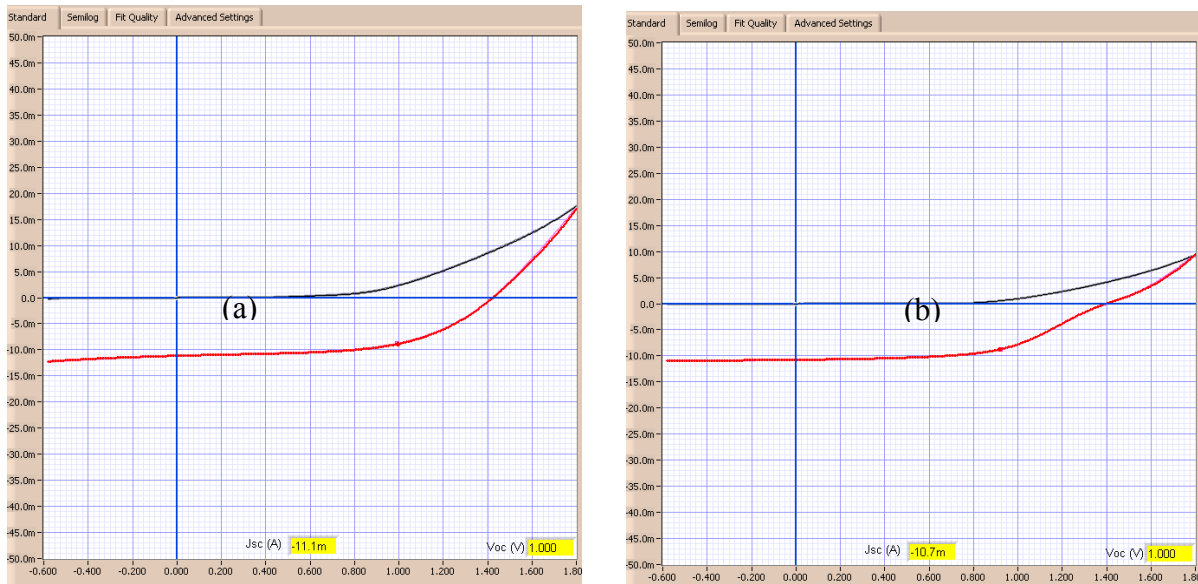


Figure 4-3. Light and Dark JV curves of MC0279 (a) and 0280 b) on ribbon p-Si wafers. These are tandem junction device due to the diffused nc-Si emitter.  Note the S-curve for 0280 just as in Figure 4-2(a).

light) the only response should be from wavelengths that can be absorbed by both devices, ie. in the overlap region. IEC has done these measurements many times on tandem a-Si/nc-Si or a-Si/a-SiGe devices. Figure 4-6 (a) shows the QE under four different bias light conditions at 0V. Note that in all four conditions the top cell QE is obtained. Figure 4-6 (b) shows the same cell measured at +0.9V, which is near the maximum power point. Now the bottom cell response is visible. At +1.2V, the response of the bottom cell is much larger, though this effect is not yet understood. LBIC measurements indicated considerable collection from outside the cell from the Si wafer independent of whether it was diffused emitter or not. Measuring the JV curve with a
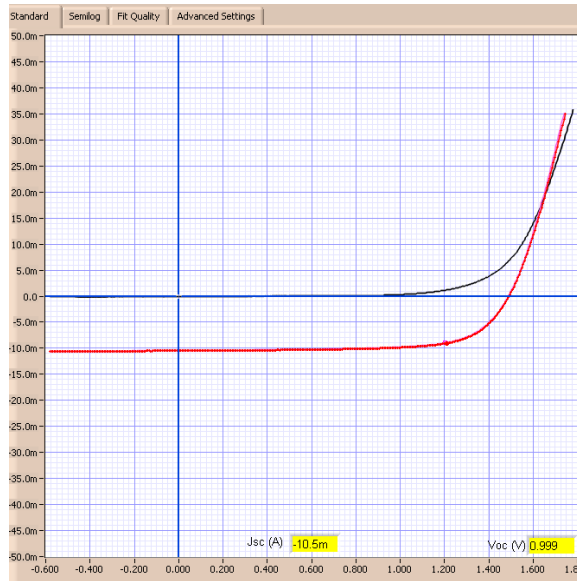


Figure 4-4. Light and Dark JV curves of MC0281 on FZ p-Si wafers.  This is a tandem junction device due to the deposited nc-Si emitter.
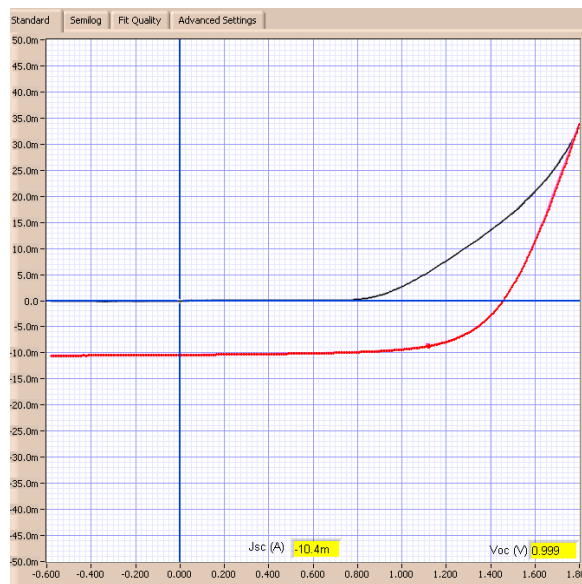


Figure 4-5. Light and Dark JV curve of 0281 on ribbon p-Si wafers. This is a tandem junction device due to the diffused nc-Si emitter.

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mask reduced the Jsc but also Voc and FF. This is not what we have seen before on other Si devices with small area cells. We also measured the JV curves with mask and with narrow band pass blue (450 nm) and red (850 nm) filters. We measured $J_{sc}$ of about 1 mA/cm2 with the blue filters and negligible current with the red filter. This indicates the bottom cell is passing (generating) current when it should not. The top cell is blocking bottom cell generated current as it should. All these results point to the bottom Si cell either passing or generating current when it should be turned off. This will be looked into further.

## 4.4 Conclusions

Given that we have found acceptable $V_{oc}$ and FF, the main goal for the remainder of the project is to increase $J_{sc}$ from the top a-Si device. Lowering the bandgap with Ar dilution during growth, raising temperature during growth, and applying textured ITO on top are all being actively investigated.
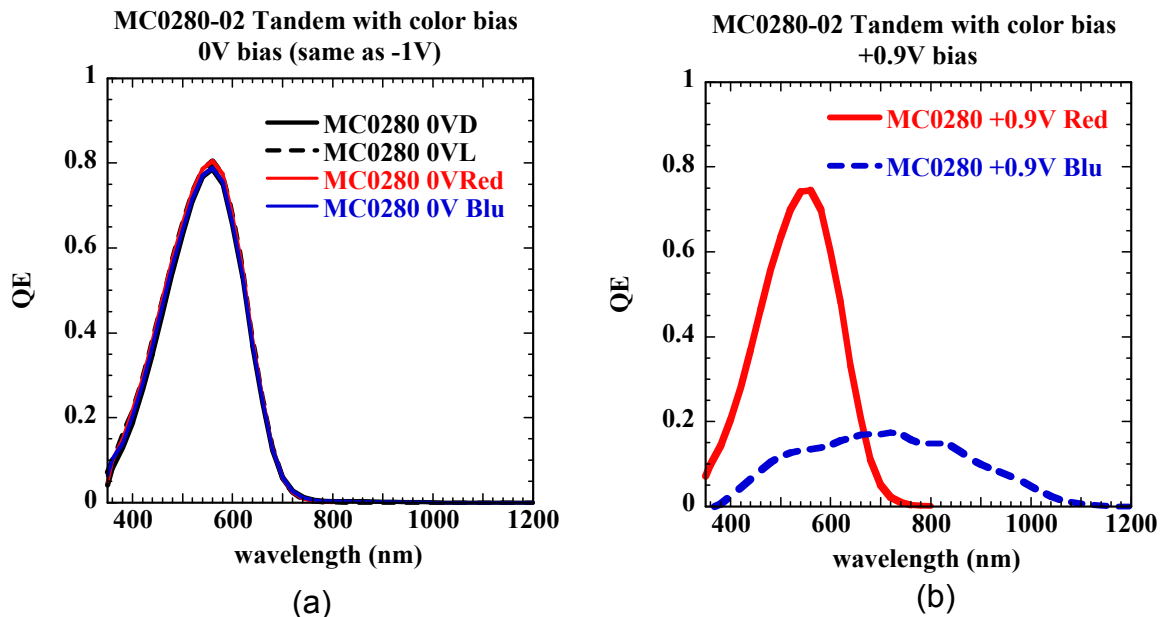


Figure 4-6. QE of 0280 on p-si ribbon with diffused emitter measured with (a) full (L) red, blue, dark (none) bias light at 0V bias; (b) red and blue bias light at V=+0.9V bias

## 5. Methods to Increase the Short Cicuit Current from the Top Cell

In the previous section, we investigated the effect of the shorting junction between the top and bottom cells. We found that the best shorting junction was a stack composed of 5 nm of p+ nc-Si and 5 nm of n+ nc-Si. This produced an a-Si/c-Si tandem solar cell with an efficiency of 11.3% on a float zone Si wafer. We found acceptable $V_{oc}$ (1.52 V) and FF (72.9%), the main goal for the remainder of the project is to increase $J_{sc}$ from the top a-Si device. In this section, we investigated two methods to increase Jsc from the top cell: i) increasing the substrate temperature from 200 to 300°C to increase the

bandgap of a-Si, and ii) increasing the i-layer thickness to increase absorption in the i-layer.

## 5.1 Tandem Cell Device Fabrication

A series of tandem devices on p-type ribbon or FZ were fabricated at IEC and Georgia Tech. The p-type ribbon and FZ Si device processing was performed at Georgia Tech. In selected cases, an $n^+$ layer was formed by $POCl_3$ diffusion in a tube furnace, followed by PECVD SiN deposition on the $n^+$ surface. In some cases, the $n^+$ layer and PECVD SiN layer were omitted. The emitter layer for these cells is subsequently formed by deposition of the shorting junction at IEC. Then the wafers were cut into 1"x1" samples using a dicing saw and the SiN layer, if present, was removed in dilute HF. Then the Si samples were sent to IEC for thin film deposition and tandem cell fabrication. IEC used device recipes developed in run MC0256 as the baseline for the top a-Si cell and a shorting junction (SHJ). The SHJ was composed of 5 nm of p+ nc-Si and 5 nm of n+ nc-Si, and connects the top and bottom cells. The p-layer was a-SiC with a graded H buffer or transition region, and the n-layer was a-SiC terminating with a nc-Si layer. The top nc-Si was needed to give a good ohmic contact with the ITO.

## 5.2 Performance of Tandem Cells With Increased i-Layer Thickness and Deposition Temperature

First attempts (Run 0295 and 0296) to increase the i-layer thickness to 0.35 $\mu$m and increase the deposition temperature to 300°C were not successful. Some flaking in chambers was seen and very low FF were measured even on control samples. Therefore each chamber was cleaned before further device fabrication. Despite these problems, quantum efficiency (QE) measurements of the devices from 0295 and 0296 can be used to evaluate the effect of the i-layer.  Figure 5-1 shows the QE for three tandem cells with i-layers deposited using different deposition conditions. Increasing the
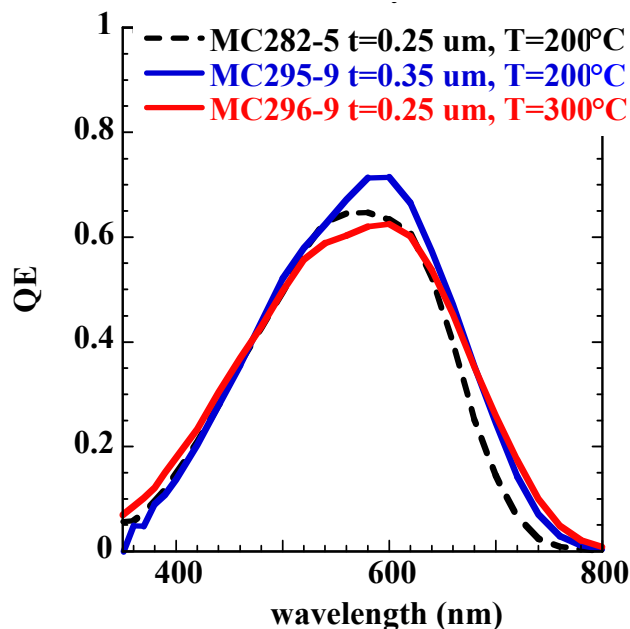


Figure 5-1: QE at –1V through $SnO_2$/p for different i-layer deposition conditions.

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deposition temperature from 200 to 300°C increased the QE for wavelengths greater than 640 nm. To quantify changes in the QE, Jsc for each cell in Figure 5-1 was calculated from integration of the QE. The increase in QE with deposition temperature increased $J_{sc}$ from 9.1 to 9.6 mA/cm$^2$ (Table 5-1). However, the $V_{oc}$ of single junction devices dropped from 0.89 V to 0.62 V when the deposition temperature was increased. Therefore, increasing the deposition temperature above 200°C has been dropped from further consideration.

Table 5-1: $J_{sc}$ from integration of QE for tandem cells with i-layers deposited under different conditions.

| Cell ID | Voc (V) | Jsc (mA/cm2) | FF (%) | Efficiency (%) |
|---|---|---|---|---|
| FZ (MC0307-05) t=0.25 um | 1.5 | 7.4 | 66.1 | 7.3 |
| FZ (MC0306-05) t=0.35 um | 1.5 | 8.1 | 62.2 | 7.6 |
| Ribbon (MC0307-03) t=0.25 um | 1.42 | 7.8 | 6.7 | 7.0 |
| Ribbon (MC0306-03) t=0.35 um | 1.41 | 8.4 | 60.6 | 7.2 |

Figure 5-2 shows that the QE improved significantly from 520 nm to 800 nm when the i-layer thickness was increased from 0.25 $\mu$m (MC282-5) to 0.35 $\mu$m (MC295-9). Table 5-1 shows that the increase in i-layer thickness leads to an increase in $J_{sc}$ from 9.1 to 10.0 mA/cm$^2$ for the tandem cell.

Table 5-2: Effect of i-layer thickness on the performance of tandem cells with FZ and ribbon c-Si bottom cells. A deposited n-type nc-Si emitter was used in the bottom cell in all cases.

| Tandem cell | i-layer thickness (µm) | Deposition temperature | $J_{sc}$ from QE (mA/cm$^2$) |
|---|---|---|---|
| MC282-5 | 0.25 | 200 | 9.1 |
| MC296-9 | 0.25 | 300 | 9.6 |
| MC295-9 | 0.35 | 200 | 10.0 |

Next an attempt was made to apply the thick i-layer to tandem cells on FZ and ribbon silicon wafers. Table 5-2 shows the results for run MC0307 in which tandem cells with ribbon and FZ wafers were used as the bottom cell. For both c-Si materials, deposited n+ emitters were investigated. Best results (7.0%-efficient) were achieved on the tandem cell with a 0.35 µm thick i-layer and a deposited emitter on FZ Si. Increasing the i-layer thickness to 0.35 µm improved the efficiency of the FZ based tandem cell by

0.3% and the efficiency of the ribbon based tandem cell by 0.2%. For both c-Si materials, increasing the i-layer thickness resulted in significant improvement in Jsc. However, Voc and FF decreased at the same time resulting in a modest improvement in the tandem cell efficiency.

## 5.3 Conclusions

Two methods to increase Jsc from the top cell of an a-Si/c-Si tandem device were investigated. The substrate temperature was increased from 200 to 300°C to increase the bandgap of a-Si. This did increase the short circuit current however, the $V_{oc}$ of tandem devices dropped when the deposition temperature was increased. Therefore, increasing the deposition temperature above 200°C was been dropped from further consideration. In another attempt to increase the current from the top cell, we increased the i-layer thickness from 0.25 μm to 0.35μm to increase absorption in the i-layer. This improved the current from the top cell without reducing Voc. However the fill factor decreased concurrently resulting in a modest improvement in cell efficiency (0.3%) due to the increase in i-layer thickness. The experiments were not able to reproduce the 11.3%-efficeinct tandem device on FZ Si that was achieved in the last section. We believe contamination limited the efficiency of the best tandem devices to 7.6%.

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Georgia Institute of Technology, in conjunction with the Institute of Energy Conversion has focused on developing high-efficiency tandem solar cells using Si bottom cells. This has involved developing the thin-film Si bottom cell and demonstrating that a wide-bandgap top cell can be deposited on a Si cell in a tandem configuration without reducing the bottom-cell performance. The objectives of this project were to: 1) evaluate the compatibility of Si solar cells to the $CuInGaSe_2$ processing environment and to the subsequent cell fabrication processes; 2) develop approaches to enhance the properties of hot-wire chemical vapor deposition Si films and devices; and 3) develop thin film Si devices that can be used in a tandem device configuration.

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