National Renewable Energy Laboratory
A national laboratory of the U.S. Department of Energy
Office of Energy Efficiency & Renewable Energy
Innovation for Our Energy Future

Striving for a Standard Protocol for Preconditioning or Stabilization of Polycrystalline Thin Film Photovoltaic Module

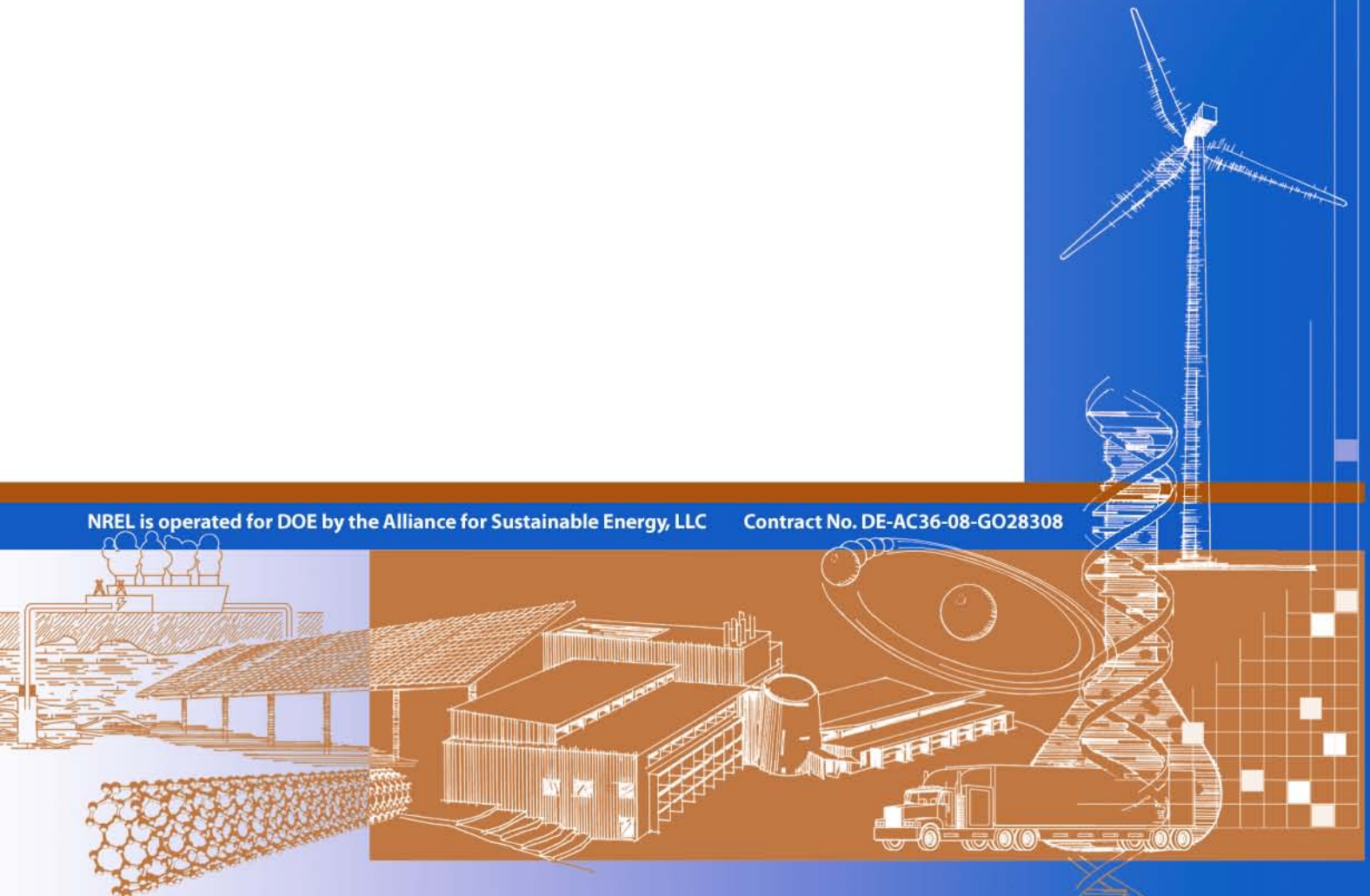
Preprint

J.A. del Cueto, C.A. Deline, D.S. Albin,
S.R. Rummel, and A. Anderberg

To be presented at the Society of Photographic Instrumentation Engineers (SPIE) 2009 Solar Energy + Technology Conference
San Diego, California
August 2-6, 2009

Conference Paper
NREL/CP-520-44935
July 2009

NREL is operated for DOE by the Alliance for Sustainable Energy, LLC Contract No. DE-AC36-08-GO28308



Striving for a standard protocol for preconditioning or stabilization of polycrystalline thin film photovoltaic modules

J.A. del Cueto*, C.A. Deline, D.S. Albin, S.R. Rummel, A. Anderberg
National Renewable Energy Laboratory
1617 Cole Blvd., Golden, CO, USA 80401

ABSTRACT

Polycrystalline photovoltaic (PV) modules containing cadmium telluride (CdTe) or copper indium gallium diselenide (CIGS) thin film materials can exhibit substantial transient or metastable current-voltage (I-V) characteristics depending on prior exposure history. Transient I-V phenomena confound the accurate determination of module performance, their reliability, and their measured temperature coefficients, which can introduce error in energy ratings models or service-lifetime predictions. Indeed, for either of these two technologies, a unique performance metric may be illusory without first specifying recent exposure or state—even at standard test conditions. The current standard preconditioning procedure for thin-film PV modules was designed for amorphous silicon (a-Si), and is likely inadequate for CdTe and CIGS. For a-Si, the Staebler-Wronski effect is known to result from defects, created via breaking of weak silicon bonds or light-activated trapping at the device junction, occurring rapidly upon light-exposure. For CdTe and CIGS devices, there is less agreement on the causes of metastable behavior. The data suggests that either deep-trapping of charge carriers, or the migration and/or electronic activation of copper may be responsible. Because these are quite disparate mechanisms, we suspect that there may be a more practical preconditioning procedure that can be employed prior to accurate performance testing for CdTe and CIGS modules. We devise a test plan to examine and compare the effects of light soaking versus forward-biased dark exposure at elevated temperatures, as parallel strategies to determine a feasible standard protocol for preconditioning and stabilizing these polycrystalline PV technologies, and report on the results of our tests.

Keywords: CdTe, CIGS, preconditioning, stabilization, metastable behavior, I-V, C-V, performance

1. INTRODUCTION

Currently, polycrystalline CdTe and CIGS cells comprise the highest performing thin-film PV devices [1, 2], at least from initial values, while larger-area modules of these technologies also lead in high performance [3]. However, issues of stability or lack thereof including transient and metastable changes in performance of PV modules for both these technologies have come to fore [4–6] and can pose challenging problems, namely: can one truly ascribe a unique PV conversion efficiency and/or performance to polycrystalline thin-film PV devices without specifying prior exposure history? Because it would be advantageous to be able to measure reliable performance data from these devices—especially when determining service lifetimes or conducting round-robin comparisons between different laboratories—an appropriate sequence of preconditioning or stabilization steps for such modules prior to performance testing would lead to reduced ambiguity in determining their long-term energy yield and field reliability. Improved accuracy is imperative because it impacts projections for the levelized cost of electricity produced by systems using these two thin-film technologies. In the current standard for thin-film PV certification (IEC61646), a stabilization sequence is specified, calling for light-soaking until stability of 2% or less change in power is achieved, after consecutive periods of at least 43 kW-h/m^2 of integrated irradiance [7]. However, because it was designed with amorphous silicon (a-Si) devices in mind, and because of the likely different defect mechanisms existing in a-Si—the light-induced Staebler-Wronski [8] effect—versus CIGS or CdTe devices, this procedure may be inadequate or sub-par when applied to CIGS or CdTe modules.

Extensive C-V measurements on CdTe cells have been conduced, with the conclusion that certain aspects of these probes—hysteresis in the C-V profile—may capture changes like ion migration, impacting and/or reflecting upon device stability [6]. With regards to cell stability, the hysteresis in C-V measurements observed when reversing the pre-measurement bias are believed to reflect the presence of mobile ions (intentionally as dopants, unintentionally as impurities) in polycrystalline CdTe [6] and single-crystal CIGS [9]. In CdTe cells, the magnitude of the hysteresis is

* joseph_delcueto@nrel.gov ; 1-303-384-6104 voice, 1-303-384-6790 facsimile, www.nrel.gov

proportional to how much Cu is added as an intentional dopant [10] and has been observed to increase with increasing cell-level stress testing [6]. The increasing hysteresis in the latter case was attributed to continual in-diffusion of Cu from the particular back contact strategy employed. It was also suggested in [6], that the influx of additional impurities not intended for doping purposes was responsible for additional hysteresis observed in particular cells being tested. In these situations, C-V hysteresis studies help to determine the mechanism by which cells degrade. There is an additional benefit offered by this technique towards reliability that can be implied. The large decrease in depletion width observed when adding any Cu to CdTe cells shows the doping 'benefit' Cu provides to CdTe. Another more direct caveat addresses the base question of whether such obvious changes in depletion width (e.g., C-V hysteresis) would manifest in direct changes to cell performance and thus be directly responsible for the various transients observed in thin-film modules based upon their previous storage conditions (e.g., dark storage with V = 0, and light-soak with V = V_{OC}). Due to the series-connected nature of cells in modules, these changes might be additively larger than what might be observed in individual cells. Conversely, we note that a review of the basic literature [11] also suggests that the hysteresis can be explained by the presence of traps in the space charge region that either fill or emit depending on the pre-bias condition; these may also figure into the observed transient behavior.

In CIGS-based devices, metastable and/or transient behavior of the electrical characteristics have been observed in the open-circuit voltage (V_{OC}) after illumination or forward bias [12], as well as reversible changes in fill factor (FF) and V_{OC} after illumination and bias [13]. The causes of these transient phenomena have been ascribed to persistent photoconductivity [13], charging-discharging of donors at the CdS/CIGS interface and deep acceptors in the CIGS [14], copper migration [6, 13], and selenium vacancy, copper vacancy complexes [15]. It is noteworthy in CIGS-based devices, that application of a thermal annealing step, often at open-circuit conditions, appears to put the CIGS into a relaxed state characterized by a low acceptor concentration, whose effect may be countered by subsequent illumination or bias. This conduct generally leads to poor module performance measured after execution of the damp-heat test (85°C/85%RH, 1000 h) in PV module certification tests, if not accounted for. Hence, such transients imply that certain stabilization procedures be enacted upon modules in order to measure a consistent stabilized performance when assessing polycrystalline PV modules, in much the same way that irradiance and temperature are normalized out to reference conditions when comparing outdoor performance.

Some of the goals of our study are: to design a test plan to study the various stabilization and preconditioning steps that feasibly obtain consistent and stable performance measurements for polycrystalline thin-film PV modules; and to investigate alternate measurements with which to categorize or quantify potential metastable and transient behavior in module performance. Measurement of the current-voltage (I-V) characteristics at standard test conditions (STC) for PV modules remains the accepted metric for PV performance. In our study, we incorporate and examine capacitance-voltage (C-V) profiling to potentially identify the likelihood of device stability in either CIGS or CdTe devices. We present our designed experimental test plan in the next section, and examine the results of our test subsequently.

2. EXPERIMENT

2.1 Designed Experimental Sequence to Study Transient and Metastable Phenomena

We present our exploratory study plan that allows us to probe the transitory effects of module performance, schematically in Fig. 1, in flow-chart format: beginning at the left, we performed baseline, reference dark and light I-V measurements at standard test conditions (STC). These baseline measurements, representing 'storage-state' values, all took place between 8 and 12, May 2009; these are the reference values against which all other measurements are expressed as a ratio or percent. The term 'storage state' refers to modules which have lain at low-light levels, at room temperature, and open-circuit (OC) conditions, for at least a few weeks, but in most cases for a few months. After baseline I-V and C-V measurements, all the modules were deployed horizontally outdoors at the Outdoor Test Facility (OTF) at NREL, and light-soaked at open circuit conditions (OC), for 1 kW-h/m^2 (PRECON0) and 26 kW-h/m^2 (PRECON1) exposures under natural sunlight. The integrated irradiance data were measured with a Kipp&Zonen CM-11 pyranometer and recorded with a datalogger; module temperatures were sensed with thermocouples and also recorded continuously. We performed these two preconditioning steps outdoors in order to get all of the modules started in sequence simultaneously—currently, we do not have a light-soaking facility at the OTF large enough to accommodate this many large-area modules. Its purpose was to perform an initial amount of preconditioning before evaluating whether the module efficiency data at STC (η_{STC}) were of sufficient quality (η_{STC} > 7% for CIS; η_{STC} > 5% for CdTe). After the preconditioning steps, all of the modules passed, and went onto the main exposure sequence.

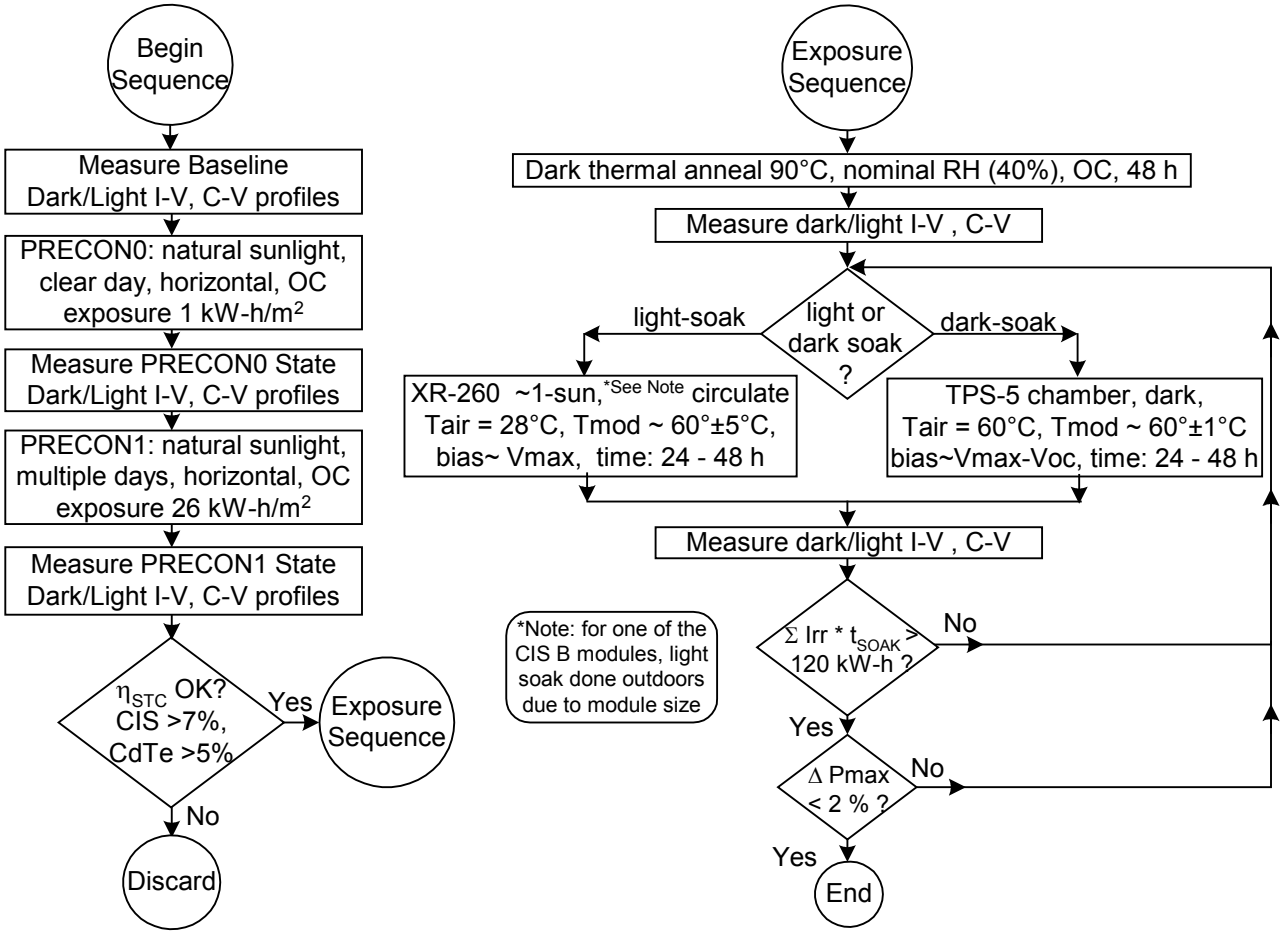


Figure 1. Flow-chart of experimental design plan to study transitory performance.

The main exposure sequence begins with a thermal anneal step conducted in the dark, at OC conditions, in one of the weather chambers (TPS5) at 90°C, and nominal relative humidity (~40% RH) for 48 hours. The rationale for this step is that such thermal exposures are common in PV module qualification tests—albeit for much longer duration—and appear to send at least some modules into a 'relaxed' state where the performance is substantially altered. If such thermal anneals (for shorter durations) result in reversible changes to module performance, we hope to catch some of this behavior with our testing. Subsequently, we performed I-V measurements on all of the modules and C-V profiles on most, except for the CIGS-B types because of size. There are two branches to the stabilization sequence: light-soaking conducted in one of the chambers (XR-260) or forward-current biased exposure in the dark—referred to as biased 'dark-soak'. The light-soak branch emulates the stabilization procedure called for in IEC 61646, except that we specify a higher operating temperature. We are proposing the dark-soak branch because if we can feasibly stabilize module performance without the need for solar light-soak stations, then this should greatly simplify and mitigate the cost of performing such procedures. For both exposure branches, we attempted to maintain the module temperatures as close to 60°C as possible. For one of the CIGS-B modules, exposure was conducted outdoors, again due to size considerations. For each branch of exposure, the initial exposure duration was set at 24 hours (for dark-soak), or ~24 kW-h/m^2 (for light-soak); subsequent exposure increments in the exposure sequence were set at 48 h or 48 kW-h/m^2, respectively, for dark and light. After each exposure, we conducted both light and dark I-V measurements at SRC, as well as C-V profiles.

2.2 Module Set

A diverse set of 11 PV modules comprising CdTe and CIGS technologies from several manufacturers was used to study the effects of our stabilization procedures. Details of this module set are listed in Table 1. The third column labeled exposure denotes the type of stabilization condition imposed: either light soak near 60°C; or forward-bias (voltage controlled) exposure under dark conditions (dark-soak) at 60°C, with bias between V_{OC} and the optimum power point

voltage (V_{MAX}). We note from Table 1, that some of the modules are basically new (nascent), while others were deployed previously outdoors in a hot-humid environment, one was light-soaked indoors, and some were controls that were set aside in house but never exposed. We chose a diverse set of modules to more fully probe pre-existing conditions and transitory effects.

Table 1: CdTe and CIGS modules tested

Module Type	Quantity	Exposure Conditions	Pre-existing exposure conditions
CdTe A	2	One each: light soak, biased dark soak	Yes, hot-humid outdoors 3 years
CdTe B	2	One each: light soak, biased dark soak	No, nascent
CdTe C	1	biased dark soak	Yes, indoor light-soak, 1130 kW-h in 2002
CIGS A	4	Two each: light soak, biased dark soak	Nascent: 3 controls from 2003; 1 pre-exposed in hot-humid outdoors 3 years
CIGS B	2	One each: light soak, biased dark soak	No, nascent

2.3 Capacitance-Voltage (C-V) Profiling

As noted previously and following concurrent parallel research at the cell level [15], C-V measurements were carried out at the module level for most of the modules studied. It may seem unusual to do so, for typically one performs these measurements on cells of limited size due to practical considerations. However, for the thin-film modules tested, all consist of a number (*Nc*) of cells connected in series, each cell comprised of a unit cell area (*Ac*), we point out that as long as the module is sufficiently uniform in thickness and electronic properties—so as to have fairly uniform depletion width thickness in each cell (w_D)— that due to the cancellation of magnitudes of cell numbers and sizes, the C-V profile should measure an average cell property fairly close to that of an equivalent ~ 1–3 cm^2 sized cell. This is shown in Eq. 1 for the capacitance of the module C_M consisting of *Nc* cells connected in series, each with capacitance *Cj* (j=1, 2,…, *Nc*). If the cells are assumed to have uniform capacitance, a simplification may be made to the right hand side of Eq. 1, where: ε and ε_0 are the material dielectric constant and permittivity of free space, respectively. We note that in most of the thin film modules studied, *Nc* varied between 50 and just over 100, and that the area of each cell (based on aperture) ranged from 60 cm^2 to 200 cm^2 in size, so that the ratio *Ac/Nc* ranges between 0.5 and 3; in other words the capacitance of a module consisting of series connected cells as noted, behaves like that of a cell with an area ranging between half to three cm^2; with the proviso that the module cells are uniform and that there are no pathologically unusual cells.

$$\frac{1}{C_M}=\frac{1}{C_1}+\frac{1}{C_2}+\ \ldots+\frac{1}{C_j}\ldots+\frac{1}{C_{Nc-1}}+\frac{1}{C_{Nc}}\quad\Rightarrow\quad C_M\approx\varepsilon\cdot\varepsilon_0\cdot\frac{1}{w_D}\cdot\frac{A_C}{N_C}\qquad(1)$$

To implement the C-V profiles, a precision LCR meter was employed (HP-4284A), with frequency range 20 Hz to 1 MHz; this LCR meter uses measurement components similar to that of Reference [16]. The 4284A supplies both the AC excitation signal and the DC bias voltage (*Vb*) for the sweep. A Keithley 2000 digital multimeter (DMM) was used to accurately measure the applied DC bias, *Vb*, across the module, as it can be appreciably loaded down by either shunt conductance or diode effects. The excitation frequencies were initially varied over a wide spectrum in order to obtain the location where the best (lowest dissipation) capacitance signals resided. Excitation signal voltages were set on the order of 20 millivolts per cell; *Vb* was always cycled to start from zero, then to go negative to maximum reverse bias, then to forward bias, and then back to zero. Both the LCR meter and DMM were interfaced to a laptop PC that carried out the C-V sweeps and measurements, using code developed in Visual Basic. Measurements were made of the circuit capacitance, dissipation, and parallel resistance, at each bias point (*Vb*) with a delay between bias points of about ~ 1.2–1.5 seconds. At the terminus of each reverse or forward bias sweep, the code waited 5 minutes before changing direction, during which time the capacitance, dissipation and parallel resistance were also sampled every 1.2 seconds. After performing the initial C-V (baseline) scans across a broad spectrum of frequencies, subsequent C-V profiles were generally limited to the one or two frequencies where the lowest dissipation levels were obtained.

2.4 Current-Voltage (I-V) Measurements at SRC and in the dark

Module I-V characteristics were measured using the large area continuous (LACSS) solar simulator testbed at the OTF. The LACSS uses a continuous illumination Xe lamp and ramps the module bias using bipolar op-amp power supplies, so that both dark and light I-V measurements are performed. Performed at baseline and after every exposure, the elapsed

times between exposure and I-V measurements were generally less than 12 hours. When possible, the bypass diodes were removed from the modules in order to allow bias into reverse voltage for the dark I-V traces. Typically, the dark I-V traces were measured to voltages beyond the light V_{OC}, sometimes up to 20-30 volts higher—especially for CdTe modules—in order to obtain module forward currents at least the size of the short-circuit current (I_{SC}).

3. RESULTS

3.1 C-V Profiles.

Figure 2 is a multi-pane graph depicting a Mott-Schottky plot on the left, and a plot of theta (the arctangent of the dissipation) vs. frequency plot on the right for one of the CIGS modules. In the left pane, two data sets are shown, one for 50 kHz, and the other at 100 kHz. On the Mott-Schottky plot, the C-V profile begins at Vb=0 where the 'start' is labeled and proceeds into reverse bias; where the scan waits for 5 minutes, during which time the capacitance signal increases (A^2/C^2 decreases). The scan then reverses direction and proceeds into forward bias, crossing *Vb*=0 (Zcros labels on left/right panes), and on up to maximum forward bias; the scan waits for another 5 minutes, before reversing direction and returning to the starting point *Vb*=0, where it again waits for another 5 minutes. The right-hand pane of Fig. 2 shows theta, the angle between the purely reactive portion of the signal and the total complex impedance vector, given as the arctangent of the dissipation. The smaller the value of theta, the closer to purely capacitative the signal is. From the right-hand pane, the C-V scans begin at t=0 (black rhomboid symbols), and then proceed to maximum reverse bias, denoted by the open and filled squares, respectively, showing the values immediately upon reaching reverse bias (RevBias0) and then after holding *Vb* there 5 minutes later (RevBias0 + 5m). On the way up to forward bias, the scan crosses through the point *Vb*=0 (Zcros) which can give a fairly good idea of the size of the hysteresis (offset) from where the scan began. The scan arrives at maximum forward bias (open triangle labels: FwdBias0), and waits for 5 minutes (filled triangle labels: FwdBias0 + 5m) before reversing direction again and returning to its end at *Vb*=0 (open circle labels: End Vb0), after which measurements are sampled for another 5 minutes (filled circle labels: End Vb0 + 5m). The theta-frequency pane to the right of Fig. 2, shows that for this CIGS module, frequencies between 50 kHz and 100 kHz produce the signal with more reliable capacitative component of the impedance as measured by the HP-4284A. Due to time constraints, only a restricted number of frequencies in that range were sampled in subsequent exposure measurements.

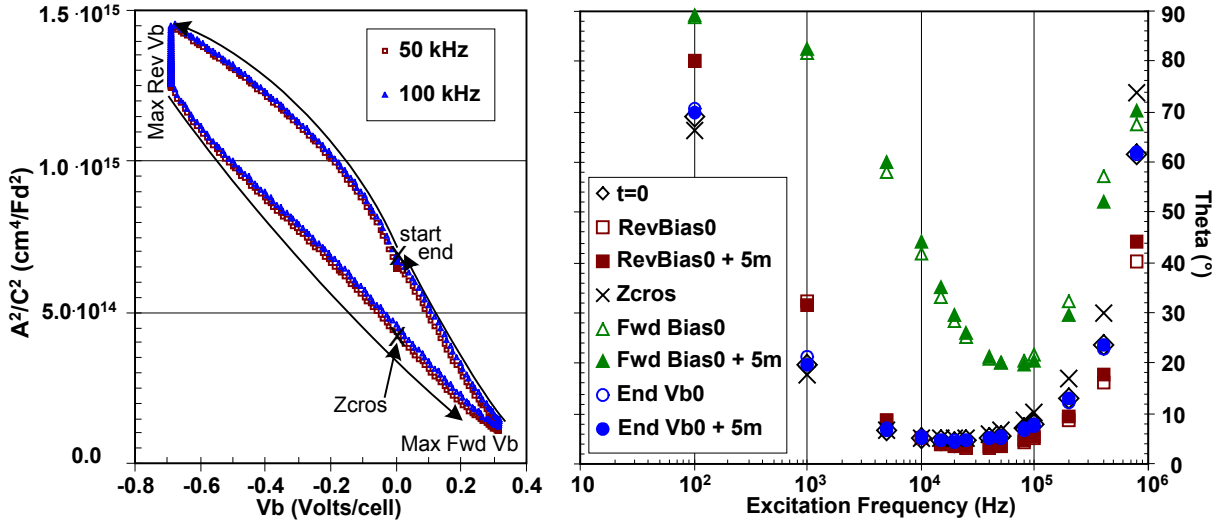


Figure 2. Mott-Schottky plot in the left pane, and theta (arctangent of the dissipation) vs. LCR meter excitation frequency on the right pane, for a CIGS module, measured at baseline.

Figure 3 is a dual pane graph, depicting carrier densities vs. depletion widths in the left pane, and depletion widths vs. cell bias voltages in the right pane, for the same CIGS module, at five different times in the exposure test: 1) baseline, never exposed; 2) after cumulative exposure of ~27 kW-h/m^2 under natural sunlight; 3) after 48 h of dark thermal anneal (90°C) and then respectively, 4) after 24 h, and 5) after cumulative 120 h, of biased dark-soak exposures. From the left-hand pane, we note that at baseline, the carrier densities typically range between $4*10^{15}$ and $2*10^{16}$; and thereafter rise from those levels by about $2*10^{16}$ after the initial outdoor exposure; then collapse down to $(2–5)*10^{15}$ after dark anneal,

and then subsequently rise back up after the biased dark exposure to levels similar to those obtained after the initial outdoor light-exposure. This behavior of the carrier densities in unexposed initial states, after dark anneal, and after subsequent exposure was generally observed for all of the CIGS A modules, both under light-soak in the XR-260 or with the biased dark-soak after dark anneal. Also, for most of the CIGS A modules, the sizes of the hysteresis at *Vb*=0 are about 0.1 microns, which represents about 30% of the size of the overall depletion width, an effect that occurs largely after scanning out to reverse bias and then sweeping forward.

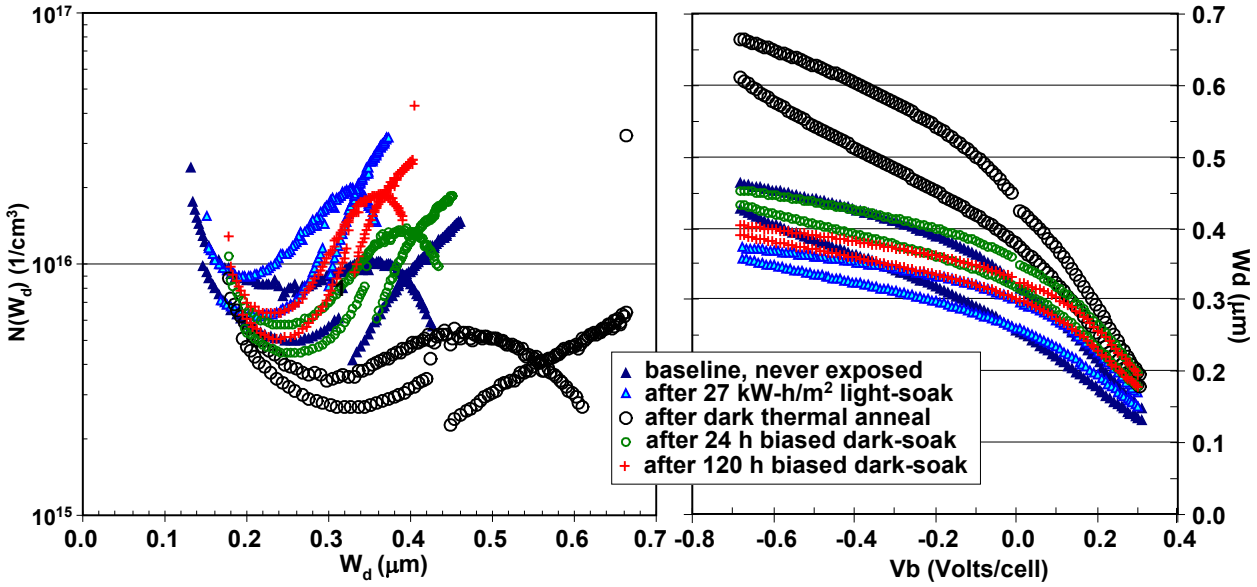


Figure 3. Composite graph showing derived carrier densities along semilog abscissa plotted vs. depletion width along the ordinate in the left pane, depletion width (w_D) along the abscissa vs. bias voltage (Vb) along the ordinate, at right, derived from the C-V data measured at 80 kHz for CIGS A module, at five different times in the exposure test.

From the right-hand pane in Fig. 3, we note that the depletion widths at baseline state, and then after just 24 h of biased dark exposure following the dark anneal, are similar in values especially going into reverse bias. The dark thermal anneal apparently so depletes the area near the junction that it doesn't take much bias voltage to move the depletion layer. After biased dark-soak, the depletion width behaves similarly to its comport after the initial outdoor light-soak, although it seems that after 120 h of the biased dark-soak, the depletion width does not quite reach the level achieved by the outdoor light-soak. The trends and behavior of the carrier densities and depletion widths in this module are nearly identical to those observed for a similar CIGS A module, instead exposed to controlled light-soaking in the XR-260.

Figure 4, is a similar dual pane graph, for a CdTe C module, also at the same five instances of exposure during the test sequence discussed above. As with the previous graph, the carrier densities vs. depletion width are shown at left, and depletion width vs. bias voltage, depicted on the right of Fig. 4. This CdTe C module underwent initial outdoor exposure before the dark thermal anneal, and then underwent the biased dark exposure at 60°C afterwards. We note for this CdTe C module, the minima in carrier density profiles are more than an order of magnitude smaller than for the CIGS A module, just under 10^{14}/cm^3, and the range over which the depletion region is probed spans ~1.7 microns. Also for this module, the size of the hysteresis in the depletion vs. bias pane from Fig. 4 are on the order of half a micron or less, appearing predominantly after scanning up to forward bias and then reversing back to zero bias—which is different than seen in NREL cells. There appears little hysteresis observed as a result of going into reverse bias, and then switching into forward bias. Note that the effects of the dark thermal anneal are also somewhat muted, in comparison to the CIGS module, neither the carrier densities nor the depletion width appear to shift as significantly or abruptly, and that shift in the depletion width vs. bias occurs mostly in forward bias, instead of reverse.

The C-V profiles obtained for CdTe A and B modules were somewhat similar to the C-V profile in Fig. 4 for CdTe module C, with the following exceptions. For the CdTe modules B studied in our tests, somewhat larger changes in the depletion widths and hysteresis of the depletion region were measured especially after the dark 90°C anneal, compared to the CdTe C module. The hysteresis ranged about 0.1–0.15 microns, with reductions in w_D after dark anneal by about 0.3 microns, making the overall sizes of w_D for the CdTe B module very comparable to those shown in the right-hand

pane in Fig. 4. For the CdTe A modules, the hysteresis and shifts in the depletion region were comparable to the CdTe B modules in size, and qualitatively behaved similarly. Namely, the hysteresis and shifts in the depletion region of the CdTe A modules emerge predominantly when going into forward bias and then sweeping back to zero bias, as opposed to sweeping first into reverse bias and then into forward bias. The Mott-Schottky plots for the CdTe A and B modules also bear similarities with the CdTe C behavior, with the depletion width hysteresis appearing largely in the portion of the sweep that goes into forward bias, and then reverses back to zero bias. There was only one substantial difference between the CdTe A and B modules: for one of the A modules, the depletion width was scarcely alterable, it shifted by about 0.1 micron after the dark 90°C anneal, and then exhibited perceptible hysteresis in the depletion width vs. bias, only immediately after the first post-anneal exposure (biased, dark-soak).

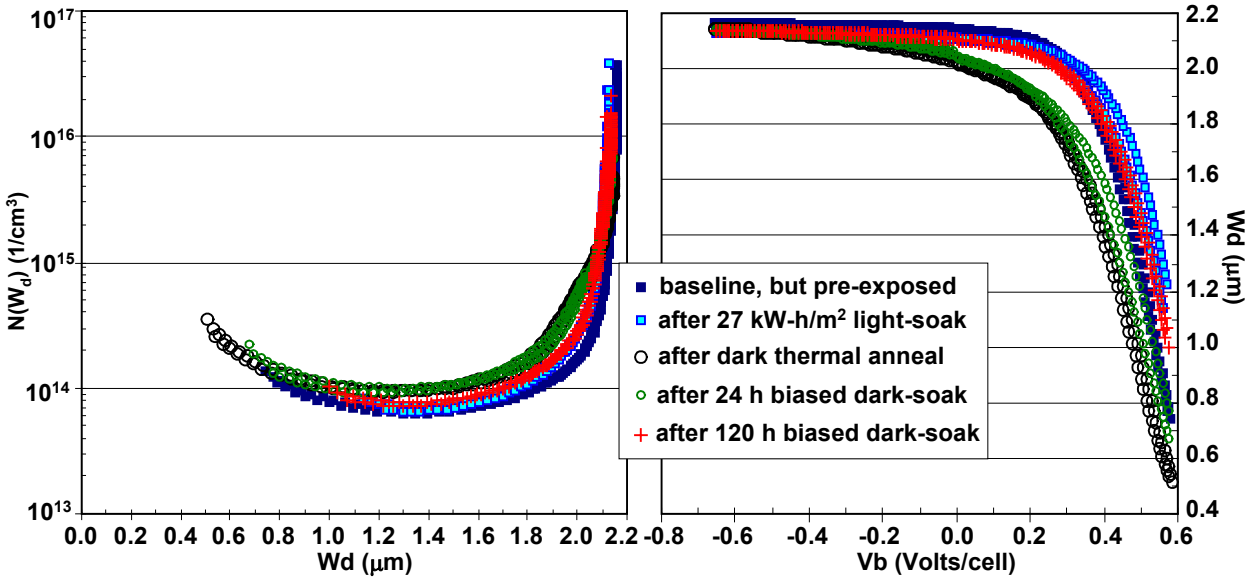


Figure 4. Composite graph showing derived carrier densities along semilog abscissa plotted vs. depletion width along the ordinate in the left pane, and depletion width (w_D) along the abscissa vs. bias voltage (Vb) along the ordinate, at right, derived from the C-V data measured at 80 kHz for CdTe C module, at five different times in the exposure test.

3.2 Performance and I-V Power Parameter Measurement Changes

The performance changes in CIGS modules (A and B) obtained during our exposure study test sequence are depicted in Fig. 5: a multi-pane bar-graph portraying the changes in efficiency (η_{STC}), fill factor (FF), V_{OC} and I_{SC}, respectively, going from top, lower top, upper bottom, and bottom-most panes of the graph. The ordinate axis is a category label denoting the corresponding step in our exposure/stabilization sequence, starting from the left: pre-existing, as measured years before we commenced our study; baseline tests for this study occurring between May 8 and 12, 2009 (all the data are normalized to this baseline); after 1 kW-h/m^2 outdoor exposure; after another 26 kW-h/m^2 outdoor exposure; after 90°C dark anneal; after the first 24 h biased dark-soak or 24 kW-h/m^2 light-soak chamber exposures, and then multiple subsequent 48 h biased dark-soak or 48 kW-h/m^2 light-soak chamber exposures. There are only two 48-h biased dark-exposures, but three 48-h light-soak exposures depicted. Along the baseline category, 2nd from the right, all values are exactly zero, since this is the reference point in time for our study. Note that for the CIGS modules A1, A2 and A3, the pre-existing data in that category exhibit somewhat higher efficiency, indicating that some non-insignificant drop in performance occurred while these modules lay in the dark. CIGS modules A1 and A3, underwent biased dark exposure at 60°C after dark 90°C anneal; module A2 underwent light-soak at nominally 1-sun and 60°C in the XR-260 after dark anneal. CIGS module B1 underwent biased dark-soak; module B2 underwent light-exposure outdoors, due to size limitations, and underwent only one each of the 24 kW-h/m^2 and 48 kW-h/m^2 exposures; monitored module temperatures indicate that during the clear times of outdoor exposures, the module temperatures were near 60°C. We note that one of the CIGS A modules—the one pre-exposed in hot-humid outdoor environment, listed in Table 1—is not depicted in Fig. 5, because after the dark 90°C anneal, its efficiency dropped precipitously, to below 3%.

Starting after the initial outdoor exposures—of ~1 kW-h/m^2 and ~26 kW-h/m^2—all the A modules' performance improved between 1% and 4% relative to the study baseline reference. The CIGS B modules showed ambiguous

behavior after the initial two outdoor exposures: initially one improved by 1% or less, while the other declined by about 1%; then in the second outdoor exposure they had both declined about 1%–2%. A dramatic decline in all CIGS modules' performance is observed after the 90°C dark anneal step: the A modules declined between 7% and 12%, while the B modules declined by 5%–7%, relative to baseline reference values of our study. We note that the source of the degradation in performance after dark anneal for both the A and B modules appears to be composed predominantly of FF losses, ranging 8%–12%, followed in size by V_{OC} declines ranging 1.5% to 3%. The I_{SC} data for the A and B modules appear to improve after 90°C dark anneal. In the first 24 hour exposure period following the dark anneal, each module's performance improves, chiefly as a result of recovering up to half of the FF losses from the previous step. The A1 module, actually exhibits an increase in performance following the first 24-h post-anneal, biased dark-soak, resulting from a 5% improvement in I_{SC}. Most of the other modules (A2, A3, B1 and B2) showed slow and slight improvement during subsequent exposures after the dark anneal step. They still may not have fully stabilized after these exposures.

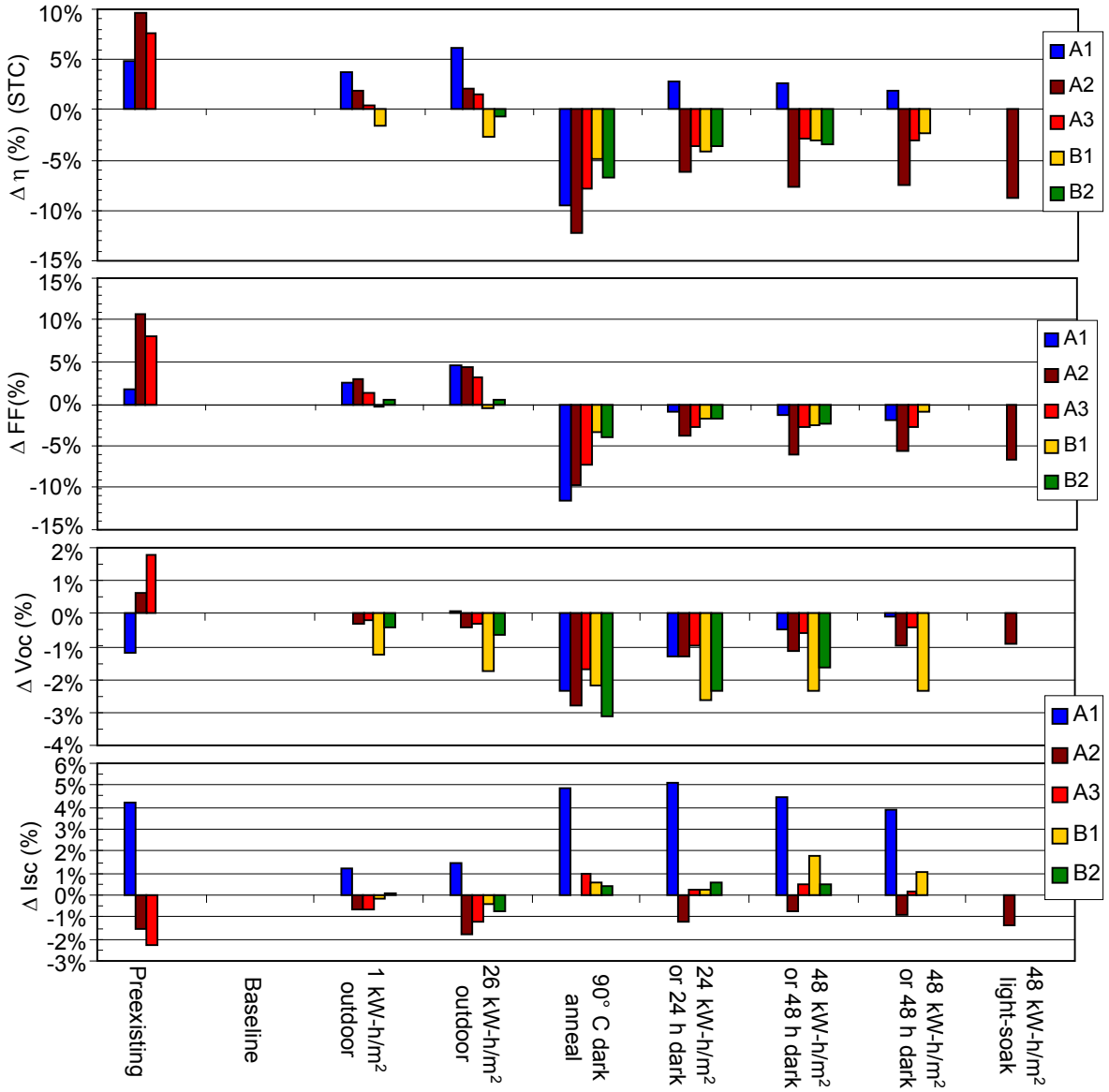


Figure 5. Changes in CIGS module performance, FF, V_{OC} and I_{SC}, respectively at top, second-from-top, second-from-bottom and bottom panes of the graph, occurring as a result of stabilization tests; baseline represents the reference measurements taken in May 2009; hence there are no changes or bars depicted. Note: only data for A2 is depicted for the third 48-h increment of exposure in the right-most category; B2 data are not shown in right two categories.

The changes in CdTe modules' (A, B and C) that we studied in our stabilization test sequence are depicted in Fig. 6, (similar to Fig. 5): a multi-pane bar-graph portraying the changes in efficiency (η_{STC}), FF, V_{OC} and I_{SC}, respectively, going from top, lower top, upper bottom, and bottom-most panes of the graph. Similar to Fig. 5, the ordinate axis is a category label denoting the exposure step in our test sequence, starting from the left: pre-existing, as the modules were at some earlier baseline, years before we commenced our study; baseline,…etc. Just after the baseline reference, all the modules were exposed outside for ~1 kW-h/m^2 and ~26 kW-h/m^2 under natural sunlight. All of the modules then went through the same dark anneal at 90°C for 48 h. Afterwards, the A1, B1 and C1 modules underwent biased dark exposure at 60°C with voltage bias between their respective V_{MAX} and V_{OC}. The A2 and B2 modules were exposed in controlled light-soaking at 60°C in the XR-260 under approximately 1-sun intensity, loaded near their respective V_{MAX}.

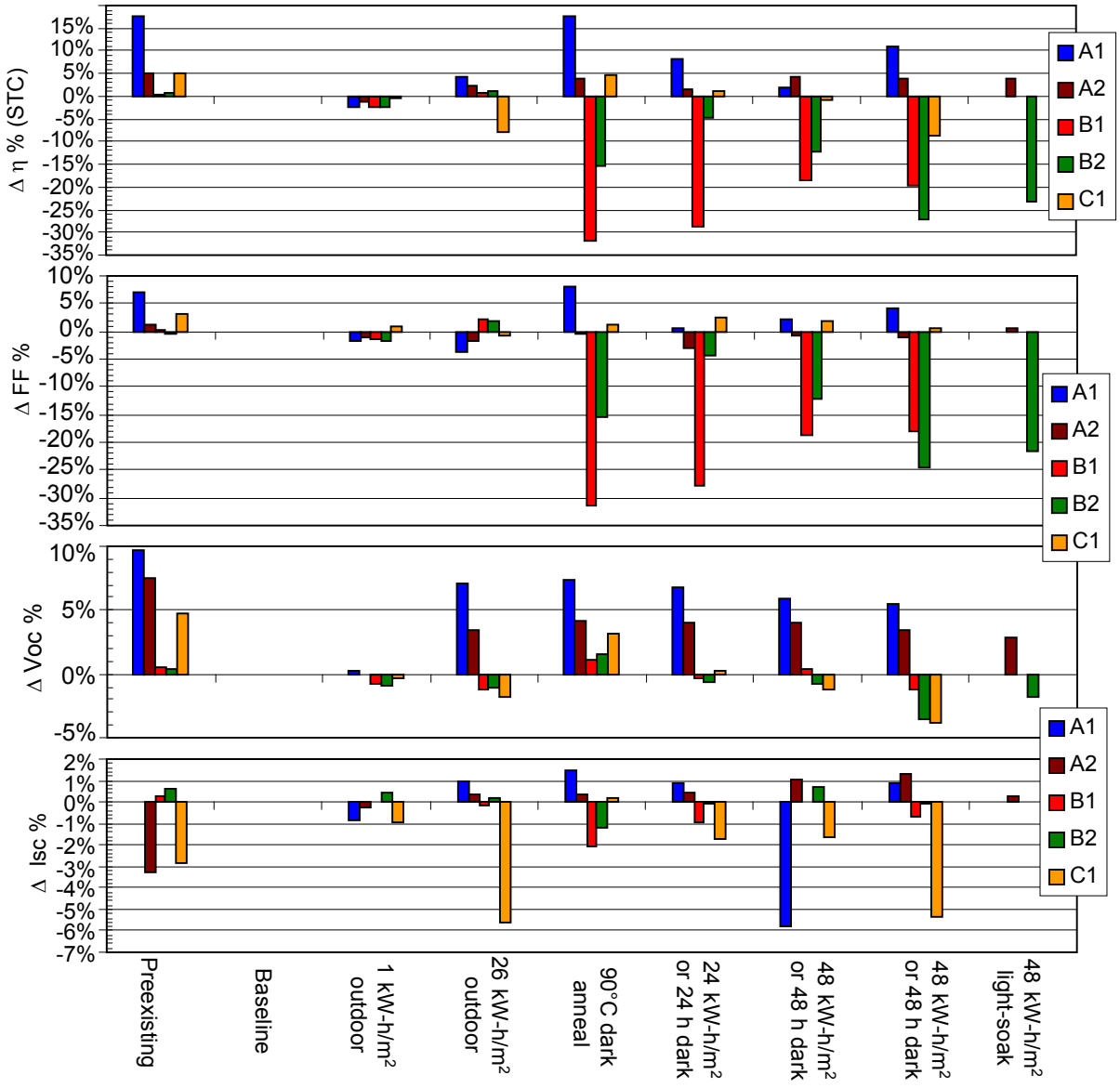


Figure 6. Changes in CdTe module performance, FF, V_{OC} and I_{SC}, respectively at top, second-from-top, second-from-bottom and bottom panes of the graph, occurring as a result of stabilization tests; the baseline category represents reference measurements taken in May 2009, hence there are no changes or bars depicted. Note: only light-soak data for A2, B2 are shown in the third 48-h increment of exposure in the right-most category.

We note from the category for preexisting data in Fig. 6 that, the performance data (top-most pane) for the A1 and A2 modules were 5% to 17% higher than when they were first received at NREL, and declined substantially as a result of

exposure in a hot-humid climate. The B1 and B2 modules lay in storage under low light level conditions at the OTF and correspondingly exhibit little change between their preexisting efficiency and those at baseline. The C1 module had been light-soaked (~ 1130 kW-h/m^2) several years earlier and was stored in the dark since; it too shows that when first received, its performance was about 5% higher than for our reference baseline. After the first set of outdoor exposures (1 kW-h/m^2 and 26 kW-h/m^2), the performance data (η_{STC}) of the CdTe A and B modules exhibit ambiguous changes, first declining by 2%–3%, then improving 1% to 4%. In contrast to the CIGS modules, for the CdTe A and B modules, these changes are driven by a combination of modifications in both FF and V_{OC}, with V_{OC} taking a preeminent role.

Perhaps the most conspicuous difference—in contrast to the CIGS—in the changes observed for the CdTe modules comes about after the dark anneal step: for the pre-exposed CdTe A and C modules, the performance afterwards recovers to the levels posted when the modules were first new and tested at NREL years earlier However, the CdTe B modules appear to suffer substantial degradation in performance—15% to 32%—after dark anneal, comprised largely of FF losses. Moreover, contrary to the behavior of the CIGS modules, all the CdTe modules exhibit modest to significant gains in V_{OC} ranging 1%–7% after the dark anneal.

Subsequent to the dark anneal step, undergoing exposure in either light-soak in the XR-260 or the biased dark-soak at 60°C, both CdTe A modules appear to hold onto their improvements in performance predominantly due to their recovery in V_{OC}. However, the CdTe B modules appear to lose any of the increases in V_{OC} in subsequent exposure steps—both light-soak and dark soak—performed after dark anneal. By the time of the second 48 h exposure step, the A1 and A2 CdTe modules still exhibit a modest gain in performance over baseline, largely as a result of the amelioration in their V_{OC} data, between 3% and 6%; while their FF data exhibit either slight loss (1% for A2) or gain (4% for A1). For the CdTe B modules, following the second 48 h exposure step, the performance losses are more complicated: a) for B1, the FF losses have somewhat reversed, and the performance seems to have stabilized at ~20% lower value than at baseline; b) for B2, the performance degrades after the 90°C dark anneal, shows recovery in the first 24-h exposure after the dark anneal, and then declines again in the two of the 48-h increments afterwards, due to worsening FF and V_{OC}. In contrast, the CdTe C1 module shows an overall reduction in performance of ~9% following the second 48 h biased dark-soak not because of FF changes, but due to a combination of both significant V_{OC} and I_{SC} declines. The right-most ordinate category in Fig. 6, does not depict a third 48-h dark soak, but it does show that we carried out a third 48 kW-h/m^2 light soak for CdTe A2 and B2 modules: after which the A2 module still exhibits a ~4% improvement over baseline, while the B2 module shows a ~20% loss almost entirely due to FF decline.

4. DISCUSSION

After studying the performance changes wrought on polycrystalline CIGS and CdTe PV modules within the limits of our stabilization plan, it appears that we can make the following assertions. First, for CIGS A modules, there appears to be an undeniable decline in performance due to dark thermal annealing at 90°C at OC, even for as little as 48 h of such exposure, comprised largely of FF losses, ranging 3%–12%, and accompanied by declines in V_{OC} ranging from 2%–3%. The degradation observed after dark thermal anneal appears to be markedly correlated to the collapse of the carrier densities within a few tenths of a micron of the junction as measured by C-V profiling, and accompanied by substantial increases in the series resistance derived from both dark and light I-V data—using the canonical derivation of taking the slopes of the I-V curve (dV/dI) and extrapolating to the origin of 1/I or $1/(I+I_{Light}) = 0$, respectively, for dark or light data [17]. The changes obtained in the CIGS A module appear to be at least in part reversible with subsequent light-soak or dark biased exposures, as seen in the amelioration of both the carrier densities—from C-V profiling—and diminishing series resistance. Because it is hard to reconcile the observed series resistance changes—both decline and amelioration—with changes in the conductance of the top transparent conductive oxide (TCO), we've demonstrated that it is likely that the decline in FF and increase in series resistance observed after dark 90°C anneal are in large part due to the collapse of the carrier densities within the CIGS. For the CIGS B modules, we did not perform enough C-V profiles to ascertain changes in carrier densities; however, their failure mode in FF is not so much due to series resistance increase but instead due more from increases in the dark shunt conductance. These failure mechanisms also appear to ameliorate with subsequent exposure, at least for the biased dark exposure. One of the power parameters for CIGS A and B improved after dark 90°C anneal and with either exposure strategies: I_{SC} showed increases ranging from 0.5% to 5%.

For CdTe modules, the C-V profiles reveal that some modules exhibit very little change in either the depletion width after dark anneal, or in hysteresis of the depletion width during the C-V bias sweeps. These low-hysteresis modules appear to be more stable than those exhibiting larger hysteresis in their C-V profile. It is worth noting that the modules with larger hysteresis in the C-V profile are more metastable—CdTe B—but also have higher performance (η_{STC}) than

the more stable CdTe modules (CdTe A or C). However, the dark 90°C anneal negatively impacts these higher performing CdTe modules more so than the lower performing ones, albeit, even at their diminished performance after the dark anneal, the CdTe B module performance data are higher than the performance of either A or C modules. Unlike the CIGS modules, increases in V_{OC} occurred for all of the CdTe modules after dark anneal. These improvements in Voc persisted for the CdTe A modules in subsequent light- or dark-soak exposures following dark anneal.

5. CONCLUSIONS

A stabilization and preconditioning plan was designed for polycrystalline CdTe and CIGS PV modules that allowed us to probe transient and metastable behavior in module performance. It included both short preconditioning steps consisting of outdoor solar exposure, with a cumulative total of 27 kW-h/m^2, a subsequent dark anneal at 90°C at open circuit, with nominal RH ~40%, with 48 hour duration, and a subsequent main exposure sequence consisting of two branches: a biased (between V_{MAX} and V_{OC}) dark soak at 60°C, or light-soak at nominally 1-sun intensity and 60°±5°C, with the modules loaded near their respective V_{MAX}. A set of both CdTe and CIGS modules underwent all of the test sequence steps and exposure branches. The initial outdoor preconditioning exposures revealed that for either unexposed CIGS or CdTe modules, the measured performance may improve following these short natural exposures, with improvements ranging from 1% to 5%. Previously exposed CdTe modules can exhibit either slight improvement or loss after such preconditioning. For previously unexposed CdTe and CIGS modules, the dark 90°C anneal invariably produces substantial degradation in performance, primarily through losses in the FF. For CdTe modules with prior exposures either in the field or indoors, the dark 90°C anneal can actually recover previously lost performance primarily through improvements in V_{OC}. Regardless of preexisting module exposure histories—and there were diverse pasts—it appears that we can bring about a measurable amount of stabilization after dark anneal using either exposure strategies—biased dark soak at 60°C or light soak at 60°C for both CIGS and CdTe modules.

We have yet to accurately quantify the necessary or equivalent exposure times using either light or biased dark exposures branches. More accurately quantifying these should allow for consistent performance assessment, but currently we can say that a minimum amount of time in such exposures appears to be 120 hours. Moreover, it does appear that we may yet be successful in performing either preconditioning or stabilization by applying just the biased, dark exposure procedure, which obviously presents a simplification and cost advantage over indoor light-soaking. Our next steps will entail re-measurement of the same modules after storage for a few weeks, subsequently followed by more light and dark exposures, perhaps even swapping the modules from the biased dark soak branch with those of the light soak branch.

6. ACKNOWLEDGEMENTS

We would like to thank other contributors to this work, specifically Kent Terwilliger, David Trudell, and Ed Gelak with their assistance in operation of the weather chambers at the OTF. We also would like to thank Jose Rodriguez for his assistance in both preparing the equipment for the test and help in setting up the modules in the chambers. This work was supported by the U.S. Department of Energy under Contract No. DOEAC36-08GO28308 with the National Renewable Energy Laboratory..

7. REFERENCES

[1] Repins, I., Contreras, M. A., Egaas, B., DeHart, C., Scharf, J., Perkins, C. L., To, B., Noufi, R., "19.9%-Efficient ZnO/CdS/CuInGaSe2 Solar Cell with 81.2% Fill Factor," Prog. Photovolt: Res. Appl. Vol. 16(3), 235-239 (2008).

[2] Wu, X. "High-efficiency polycrystalline CdTe thin-film solar cells," Solar Energy 77, 803–814 (2004).

[3] Green, M. A., Emery, K., Hishikawa, Y., Warta, W., "Solar Cell Efficiency Tables (Version 33)," Prog. Photovolt: Res. Appl. Vol 17, 85–94 (2009).

[4] del Cueto, J.A., von Roedern, B., "Long-term transient and metastable effects in cadmium telluride photovoltaic modules," Prog. Photovolt: Res. Appl. Vol. 14, 615-628 (2006).

[5] del Cueto, J.A. , Rummel, S., Kroposki, B., Osterwald, C., Anderberg, A., "Stability of CIS/CIGS modules at the outdoor test facility over two decades," Proc. 33rd IEEE PVSC, San Diego, CA, (2008).

[6] Albin, D.S., Dhere, R.G., Glynn, S.C., DelCueto, J., Metzger, W.K., "Degradation and Capacitance-Voltage Hysteresis in CdTe Devices," *ibid*. *these proceedings.*

[7] IEC 61646, "International Standard: Thin-film terrestrial photovoltaic (PV) modules – Design qualification and type approval," Sec. 10.19; International Electrotechnical Commission Central Office 3, rue de Varembé, CH-1211 Geneva 20 Switzerland, 2nd ed. (2008).
[8] Staebler, D.L., Wronski, C.R., "Reversible conductivity changes in discharge-produced amorphous silicon," Appl. Phys. Lett. 31, 292-294 (1977).
[9] Lyubomirsky, I., Rabinal, M.K., Cahen, D., "Room-temperature detection of mobile impurities in compound semiconductors by transient ion drift," J. Appl. Phys. 81 (10) 6684-6691(1997).
[10] Enzenroth, R.A., Barth, K.L., Sampath, W.S., "Transient ion drift measurements of polycrystalline CdTe PV devices," proceedings 4th WCPEC, 449-452, Hawaii (2006).
[11] Schroder, D.K., [Semiconductor Material and Device Characterization], Wiley & Sons, New York, 297-314 (1990).
[12] Sasala, R.A., Sites, J.R., "Time dependent voltage in CuInSe2 and CdTe solar cells," Proc. 23rd IEEE PVSC, 543-548 (1993).
[13] Rau, U., Jasenek, A., Herberholz, R., Schock, H.-W., Guillemoles, J.-F., Lincot, D., Kronink, L., "The inherent stability of Cu(In,Ga)Se2-based Solar cells," Proc. 2nd WCPEC, Vienna, 428-433 (1998).
[14] Zabierowski, P., Rau, U., Igalson, M., "Classification of metastabilities in the electrical characteristics of ZnO/CdS/Cu(In,Ga)Se2 solar cells," Thin Solid Films 387, 147-150 (2001)
[15] Igalson, M., Cwil, M., Edoff, M. "Metastabilities in the electrical characteristics of CIGS devices: Experimental results vs theoretical predictions," Thin Solid Films 515, 6142-6146 (2007).
[16] Schroder, D.K., [Semiconductor Material and Device Characterization], Wiley & Sons, New York, 287 (1990).
[17] Hegedus, S.S., Shafarman, W.N., "Thin-Film Solar Cells: Device Measurements and Analysis," Photovolt: Res. Appl. Vol. 12, 155–176 (2004).

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ORGANIZATION.

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
July 2009	Conference Paper	August 2-6, 2009

4. TITLE AND SUBTITLE
Striving for a Standard Protocol for Preconditioning or Stabilization of Polycrystalline Thin Film Photovoltaic Modules: Preprint

5a. CONTRACT NUMBER
DE-AC36-08-GO28308

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
J.A. del Cueto, C.A. Deline, D.S. Albin, S.R. Rummel, and A. Anderberg

5d. PROJECT NUMBER
NREL/CP-520-44935

5e. TASK NUMBER
PVD91430

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

8. PERFORMING ORGANIZATION REPORT NUMBER
NREL/CP-520-44935

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)
NREL

11. SPONSORING/MONITORING AGENCY REPORT NUMBER

12. DISTRIBUTION AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

13. SUPPLEMENTARY NOTES

14. ABSTRACT *(Maximum 200 Words)*
Polycrystalline photovoltaic (PV) modules containing cadmium telluride (CdTe) or copper indium gallium diselenide (CIGS) thin film materials can exhibit transient or metastable current-voltage (I-V) characteristics depending on prior exposure history. Transient I-V phenomena confound accurate determination of performance, reliability, and measured temperature coefficients, potentially introducing error in energy ratings models or service-lifetime predictions. For either technology, a unique performance metric should first specify recent exposure or state—even at standard test conditions. The current standard preconditioning for thin-film PV modules is for amorphous silicon (a-Si), and is likely inadequate for CdTe and CIGS. For a-Si, the Staebler-Wronski effect results from defects, created via breaking weak silicon bonds or light-activated trapping at the device junction, occurring rapidly upon light-exposure. For CdTe and CIGS devices, the limited data suggest either deep-trapping of charge carriers or the migration and/or electronic activation of copper may be responsible. Because these are disparate mechanisms, we suspect a more practical preconditioning procedure can be used prior to accurate performance testing for CdTe and CIGS modules. A feasible standard protocol was devised for preconditioning the polycrystalline PV technologies under bias eith with light exposure or forward-bias currents at elevated temperatures. The results are reported.

15. SUBJECT TERMS
PV; CdTe; CIGS; preconditioning; stabilization; metastable behavior; I-V, C-V performance; thin film; module;

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			19b. TELEPHONE NUMBER (*Include area code*)
Unclassified	Unclassified	Unclassified	UL		