Thermal Analysis of the Vulnerability of the Spacesuit Battery Design to Short-Circuit Conditions

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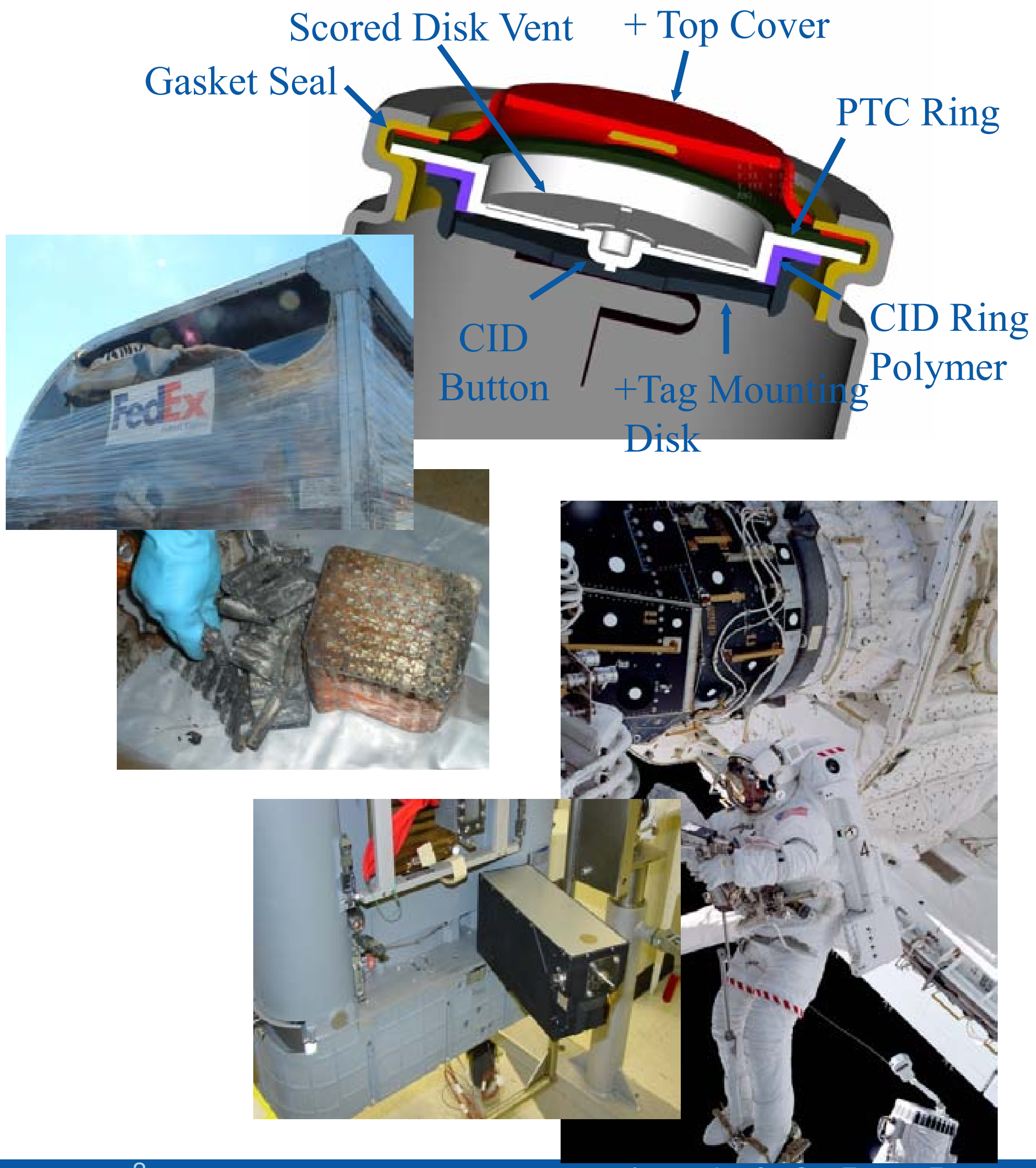
Background and Motivation for Present Work

- **Background**
  - Cell PTC device proven effective control for overcurrent hazards at Li-ion cell and small battery level
  - Proven ineffective in high-voltage battery designs
  - Fire in 2004 Memphis FedEx facility possibly caused by PTC device failures in large-capacity (66p-2s) battery, which shorted while at 50% SOC
- **Motivation**
  - Can NASA's spacesuit battery design (16p-5s) array depend on cell PTC devices to tolerate an external 16p short?
  - What are conditions for safe storage and operation?



Objectives

- Create mathematical model of full 16p-5s spacesuit battery that captures electrical/thermal behavior during electrical shorts
  - Extend PTC, cell, and module models from previous work[1,2,3]

- Assess vulnerability of 16p-5s spacesuit battery to pack-internal (cell-external) shorts between module banks

Photo: ABSL

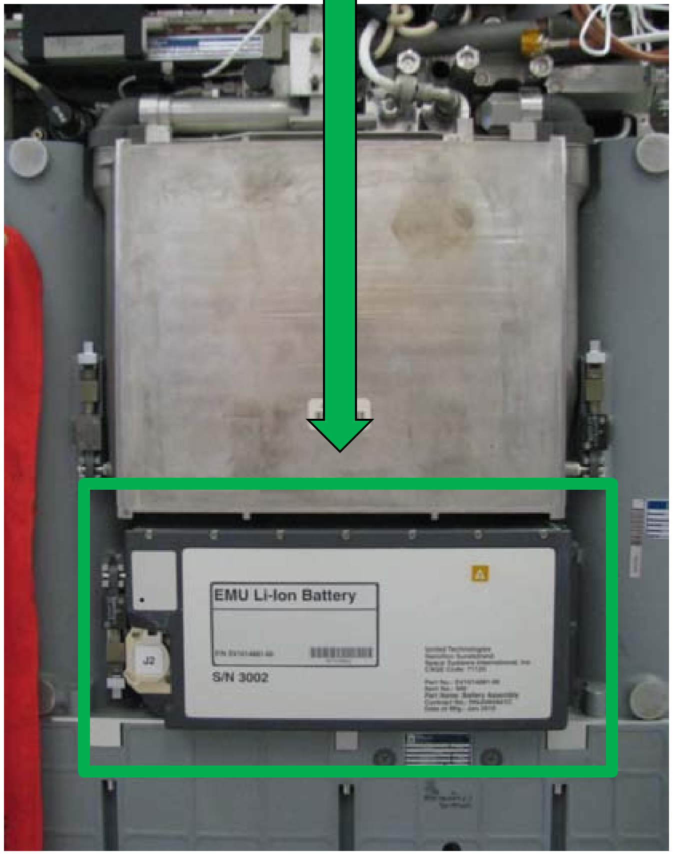
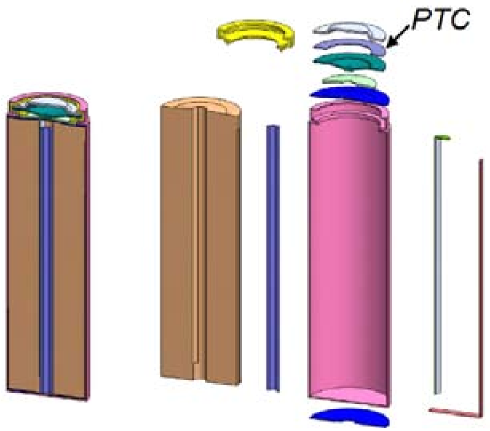


Photo: NASA

1. "Cell PTC Device Characterization," E. Darcy et.al, 2008 NASA Aerospace Battery Workshop
2. "Thermal/Electrical Modeling for Abuse-Tolerant Design of Li-ion Modules," K. Smith et al, 2008 NASA Aerospace Battery Workshop
3. "Thermal/Electrical Modeling for Abuse Tolerant Design of Lithium Ion Modules," K. Smith et al., Int. J. Energy Res., vol. 34, no. 2, pp. 204-215, 2010.

Overview

- Modeling Approach
  - Cell with PTC device
    - Electrical
    - Thermal (5-node)
  - Module
    - Electrical (multinode network)
    - Thermal (multinode network)
  - Pack
    - Electrical (multinode network)
    - Thermal (multinode network)



- Validation with experiments from ABSL
  - Pack-external short of bank 3

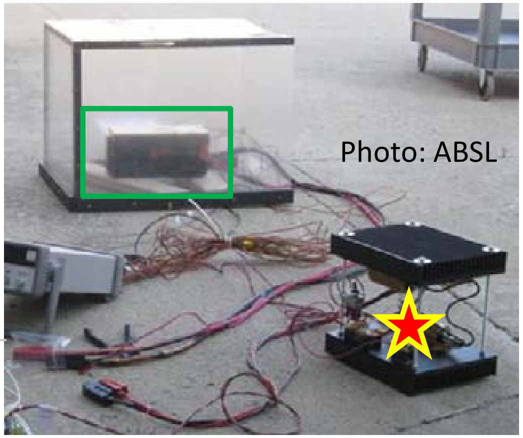
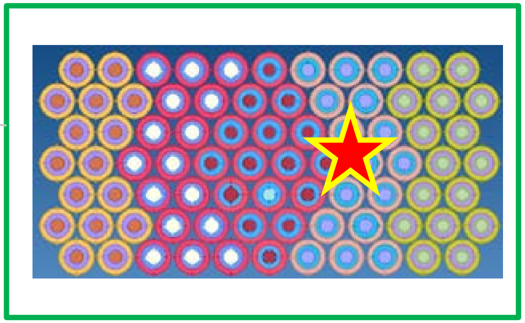


Photo: ABSL

- Modeling analysis
  - Pack-internal short of bank 3
  - Design and storage considerations



- Conclusions

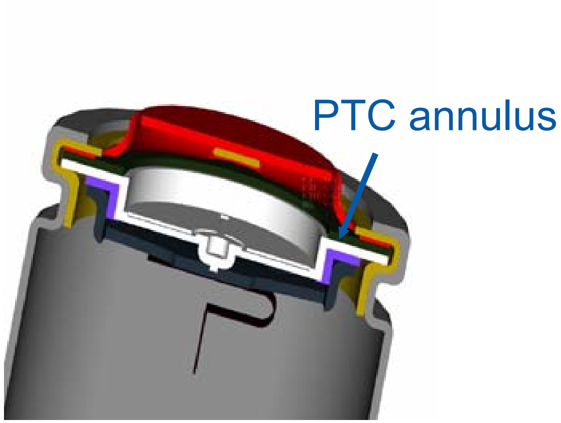
PTC Device – Background

- Commercial lithium ion 18650 cells typically have a current-limiting PTC (positive temperature coefficient) device installed in the cell cap to limit external currents in the event of an external short to the cell.

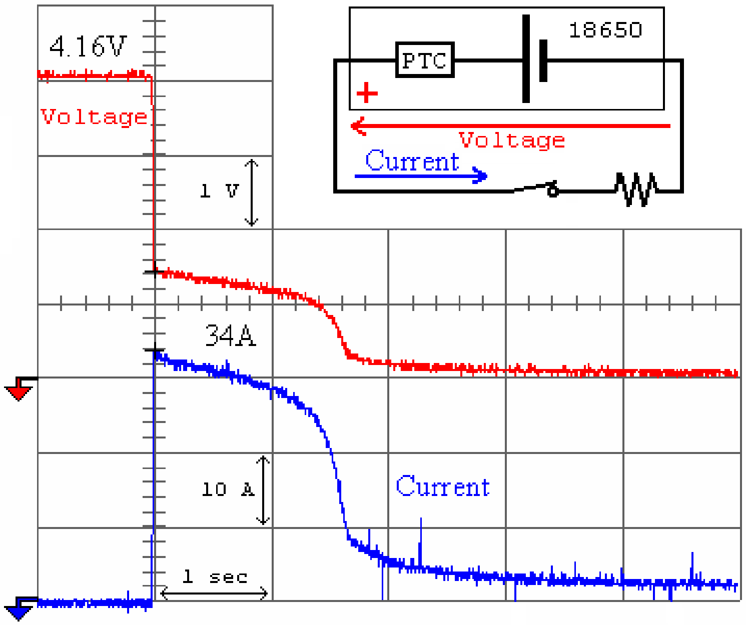
- The PTC device consists of a matrix of crystalline polyethylene containing dispersed conductive particles, usually carbon black.* The resistance of the PTC device increases sharply with temperature.

- When a short is applied to a cell, the elevated currents cause the PTC device to self-heat and move to a high resistance state in which most of the cell voltage is across the PTC device but the current is significantly reduced.

- As long as the short is maintained, the PTC device produces enough heat to keep itself in this tripped state (lower current being offset by greater voltage drop across PTC device).



Single Cell Short:



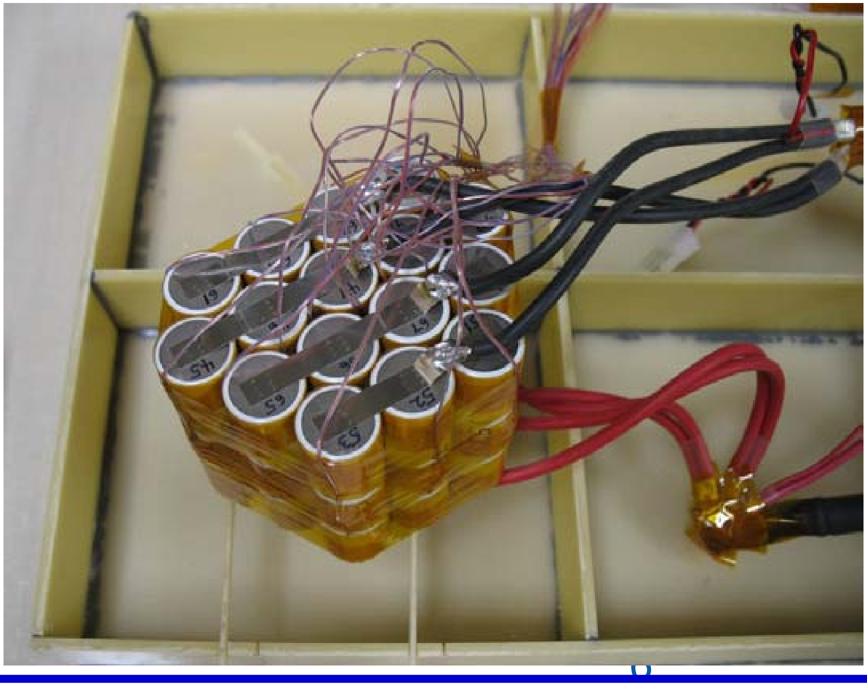
*Doljack, F., IEEE Transactions on Components, Hybrids, and Manufacturing Technology, **4**, 732, 1981

Model has to Capture Key Physics of an Electrical Short

16P Bundle External Short Test

- *Performed by Symmetry Resources, Inc.*
- *Moli ICR18650J cells*
- *16 parallel*
- *10 mΩ external short*

Photos: SRI



- PTC device behavior
  - $R_{PTC}(T)$
  - Thermal connection with the cell
- Cell electrical behavior
  - Current/voltage/temperature relationship
- Cell-to-cell heat transfer
  - Conduction
    - air gaps
    - electrical tabs
  - radiation
- Cell-to-ambient heat transfer
  - Convection to air
  - Conduction through wire leads

Model Development Approach

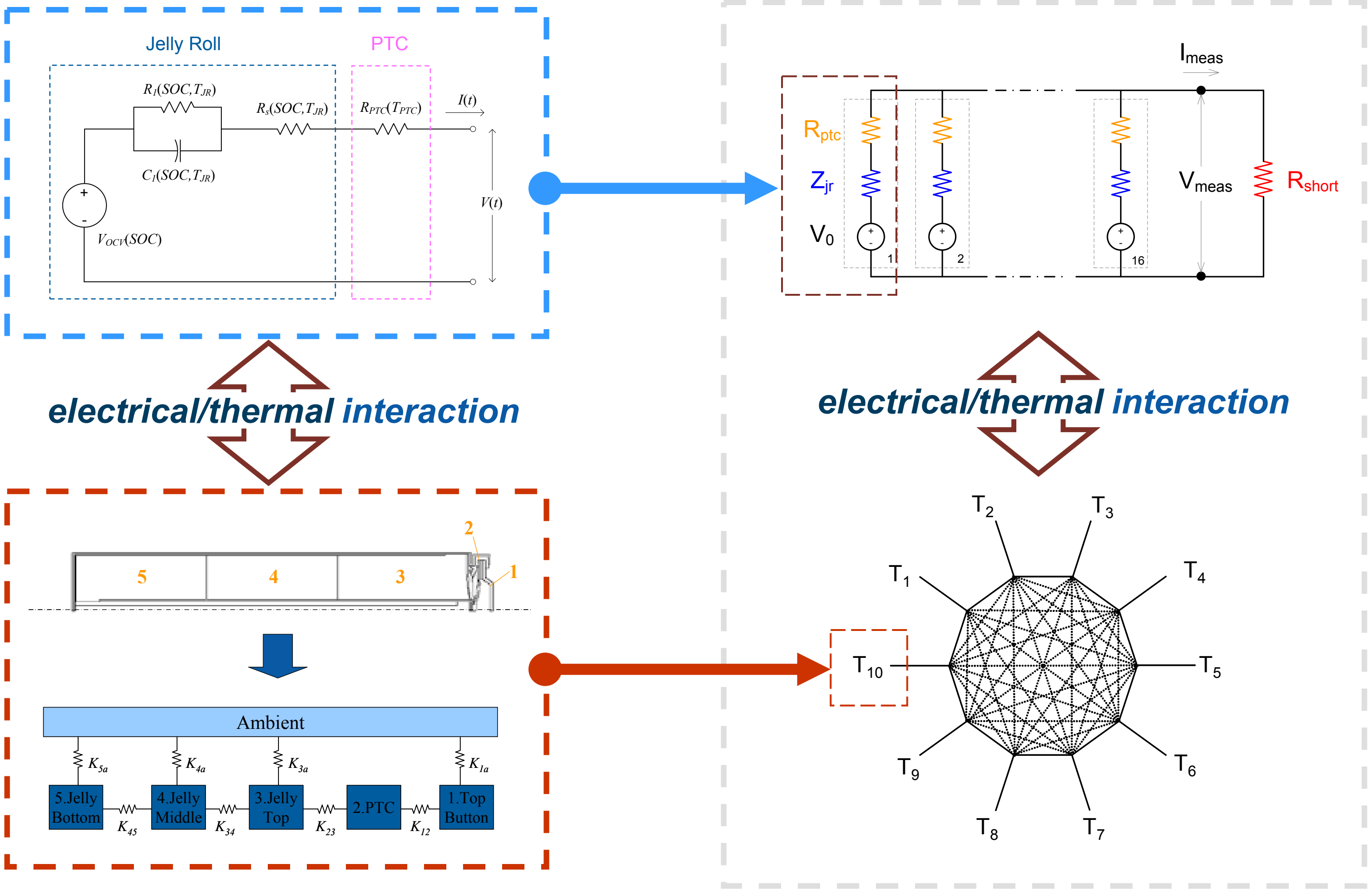
Integrated Thermal and Electrical Network Model *of a Multicell Battery for Safety Evaluation of Module Design with PTC Devices during External Short*

Unit Cell Model

Multicell T&E Network Model

Electrical Model

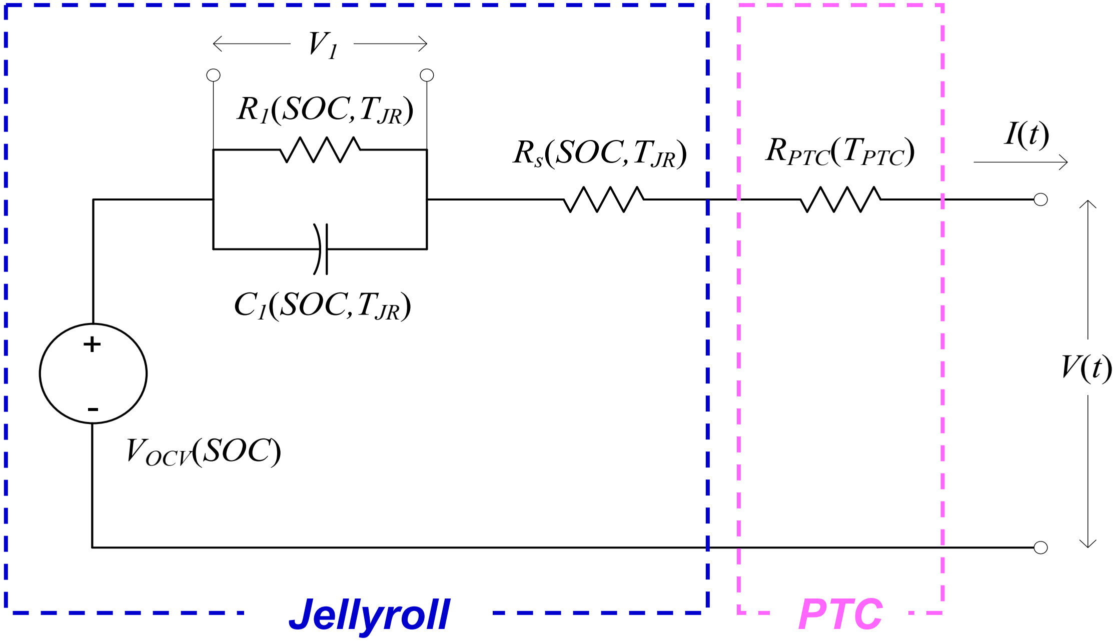
5-Node Thermal Model



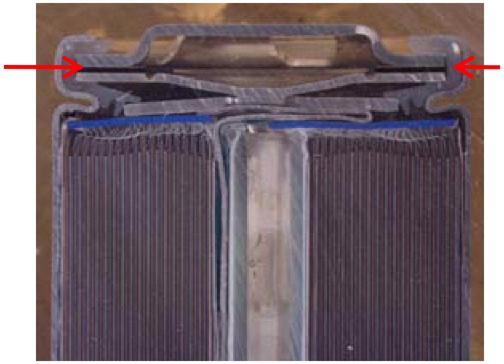
Electrical Network Model

Thermal Network Model

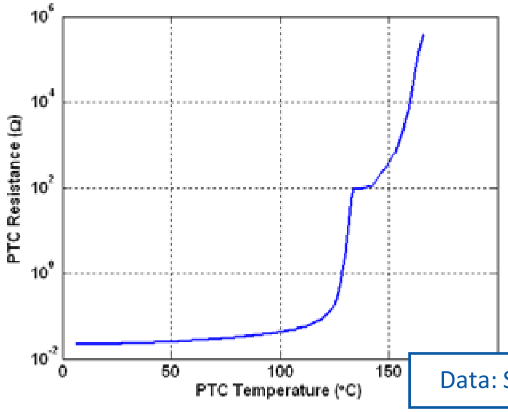
Unit Cell Model – Electrical



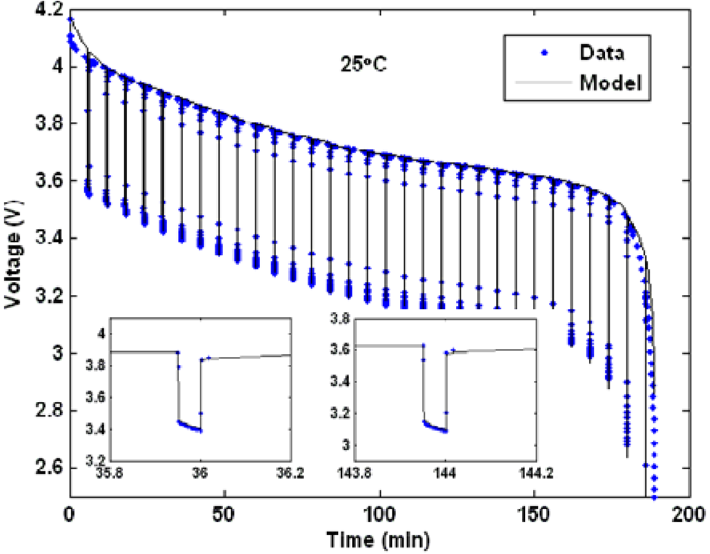
Equivalent circuit model including PTC device



PTC Resistance vs. Temp.



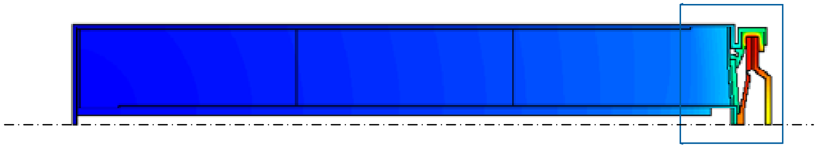
Data: SRI



Unit Cell Model – 5-node Thermal

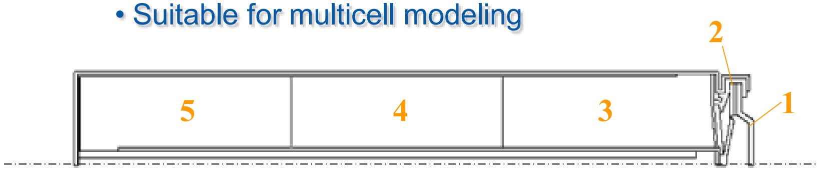
Detailed Cell Thermal Model

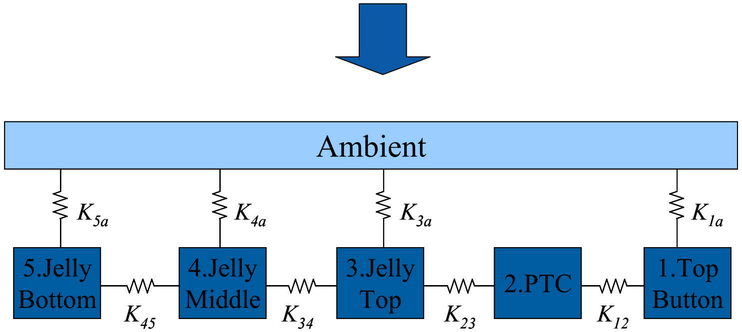
- Large computational requirement
- Not suitable for multicell modeling



5-Node Cell Thermal Model

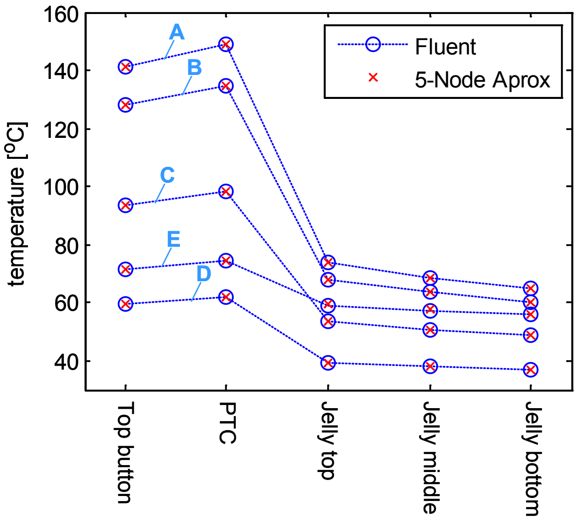
- Low order dynamic model
- Suitable for multicell modeling





Comparison of Detailed and 5-Node Models

for different heat generation conditions



A PTC:3.38W, Jelly:0.0093W
B PTC:3.0W, Jelly:0.0093W
C PTC:2.0W, Jelly:0.0093W
D PTC:1.0W, Jelly:0.0093W
E PTC:1.0W, Jelly:1.0W

Steady Form

$$Q_i = \sum_j K_{ij}\left(T_i - T_j\right)$$

Unsteady Form

$$Q_i = \sum_j K_{ij}\left(T_i - T_j\right) + MCp_i \frac{dT_i}{dt}$$

Multicell Network Model – Thermal

Thermal Network Model

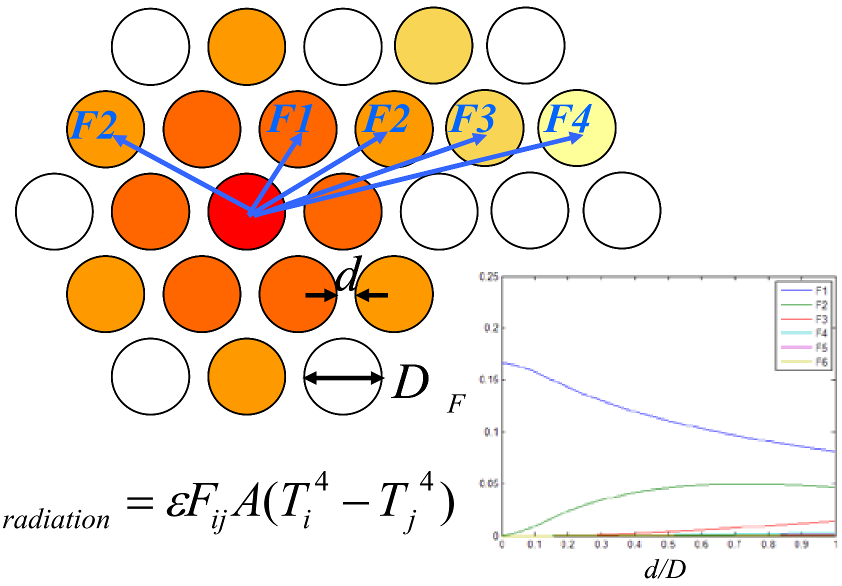
Thermal Mass: Identifying thermal mass at each node

Heat Generation: PTC heat, discharge/charge heat (optional: abuse reaction heat)

Heat Transfer: Quantifying heat exchange among the nodes

$$\Rightarrow \quad Q_{transport,i} = \sum_{j=1,\, j\neq i} -Q_{ij}, \quad Q_{ij} = Q_{ij,radiation} + Q_{ij,connector\_conduction} + Q_{ij,convection} \cdots$$

Cell-to-Cell Irradiative Heat Transfer



$$Q_{ij,radiation} = \varepsilon F_{ij} A (T_i^{\,4} - T_j^{\,4})$$

Staggered Array

Let $X = 1 + \frac{d}{D}$

For $0 \le \frac{d}{D} \le \frac{2}{\sqrt{3}} - 1$, i.e. $1 \le X \le \frac{2}{\sqrt{3}}$

$$F_1 = \frac{1}{\pi}\left[-\sqrt{X^2-1} + \cos^{-1}\left(\frac{1}{X}\right) + \frac{\pi}{6}\right]$$

$$F_2 = \frac{1}{\pi}\left[\sqrt{X^2-1} - \cos^{-1}\left(\frac{1}{X}\right)\right]$$

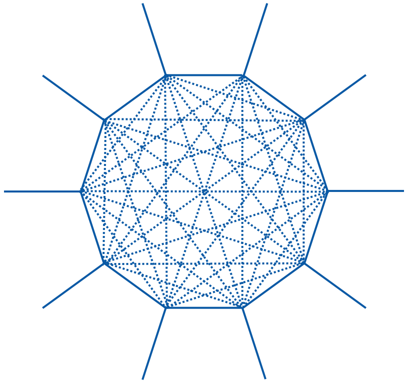
$$F_n = 0$$

For $\frac{2}{\sqrt{3}} - 1 < \frac{d}{D} \le 1$, i.e. $\frac{2}{\sqrt{3}} < X \le 2$

$$F_1 = \frac{1}{\pi}\left[\sqrt{X^2-1} - \cos^{-1}\left(\frac{1}{X}\right) - X + \frac{\pi}{2}\right]$$

$$F_2 = \frac{1}{\pi}\left[\sqrt{3X^2-1} - 2\sqrt{X^2-1} + 2\cos^{-1}\left(\frac{1}{X}\right) - \cos^{-1}\left(\frac{1}{\sqrt{3}X}\right) - \frac{\pi}{6}\right]$$

$$F_n = \frac{1}{2\pi}\left[\begin{array}{l} \sqrt{\{n(n-1)+1\}X^2-1} - 2\sqrt{\{(n-1)(n-2)+1\}X^2-1} + \sqrt{\{(n-2)(n-3)+1\}X^2-1} \\ -\cos^{-1}\left(\frac{1}{\sqrt{n(n-1)+1}X}\right) + 2\cos^{-1}\left(\frac{1}{\sqrt{(n-1)(n-2)+1}X}\right) - \cos^{-1}\left(\frac{1}{\sqrt{(n-2)(n-3)+1}X}\right) \\ +\tan^{-1}\left\{\frac{2}{\sqrt{3}}\left(n-\frac{1}{2}\right)\right\} - 2\tan^{-1}\left\{\frac{2}{\sqrt{3}}\left(n-\frac{3}{2}\right)\right\} + \tan^{-1}\left\{\frac{2}{\sqrt{3}}\left(n-\frac{5}{2}\right)\right\} \end{array}\right]$$



Multicell Network Model – Thermal

Heat Transfer to Ambient

$$Q_{i-a} = h_{\infty} A_i (T_i - T_{\infty}) + \sigma A_i (T_i^4 - T_{\infty}^4)$$

Photo: NASA ISS01E5361

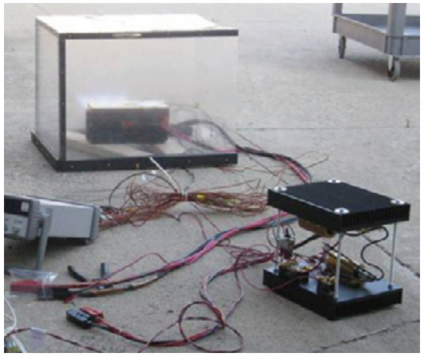
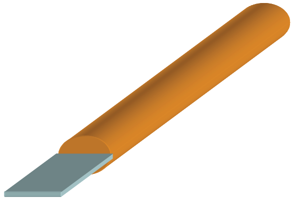
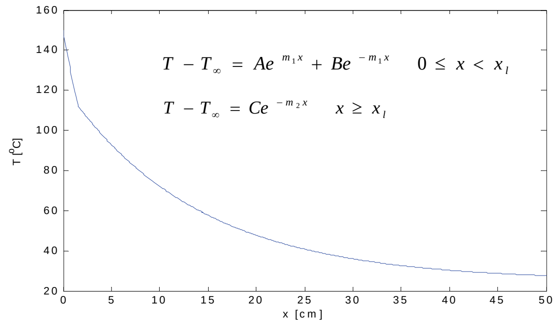


Photo: ABSL

Heat Rejection Through Wires

$$Q_{base} = kA_b \left. \frac{dT}{dx} \right|_{x=0} = hA (T_b - T_{\infty})$$

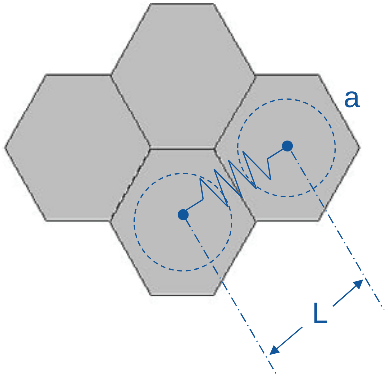




$$T - T_{\infty} = Ae^{m_1 x} + Be^{-m_1 x} \quad 0 \le x < x_l$$

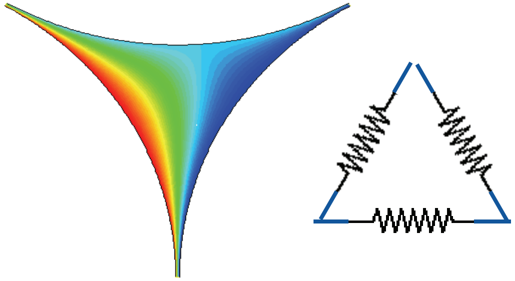
$$T - T_{\infty} = Ce^{-m_2 x} \quad x \ge x_l$$

Transverse Heat Transfer Through Plates



$$\boldsymbol{Q} = \left(\frac{\boldsymbol{k}}{\sqrt{3}} \right) \boldsymbol{H \Delta T}$$

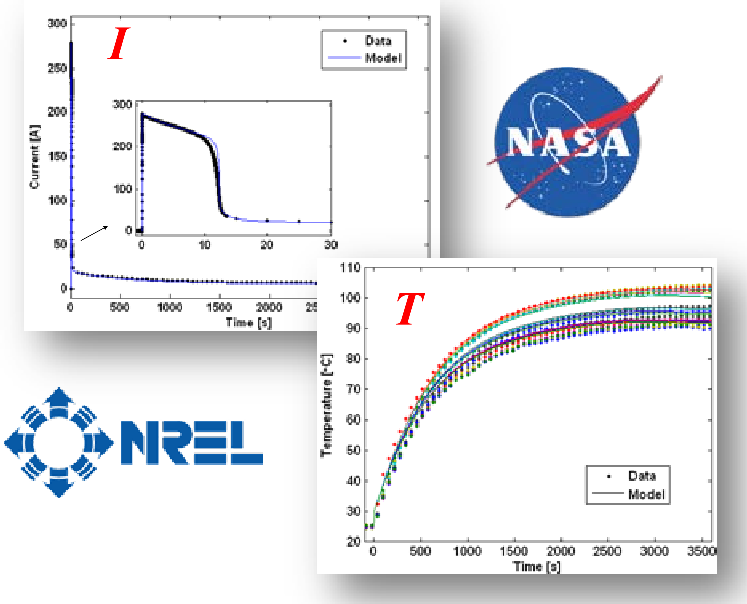
Heat Conduction Through Air Gap



Extend Validated 16P Model for 16P5S Pack

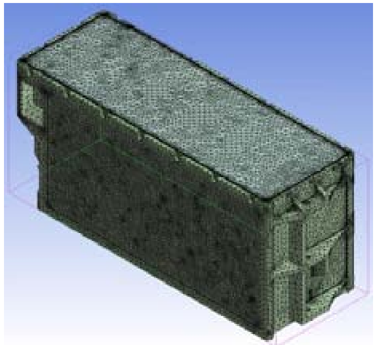
16P model validated against a bank short test

- Created and validated a multicell math model capturing electrical and thermal interactions of cells with PTC devices during abuse
- PTC device is an effective thermal regulator; maximum cell temperature (final state) is very similar for a variety of initial and boundary conditions for tested 16P events

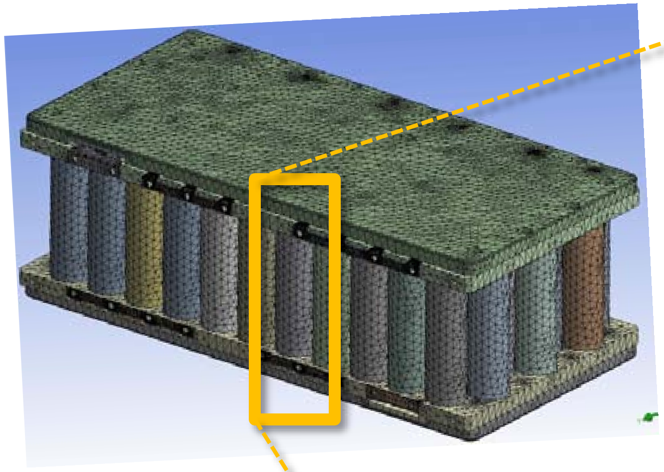


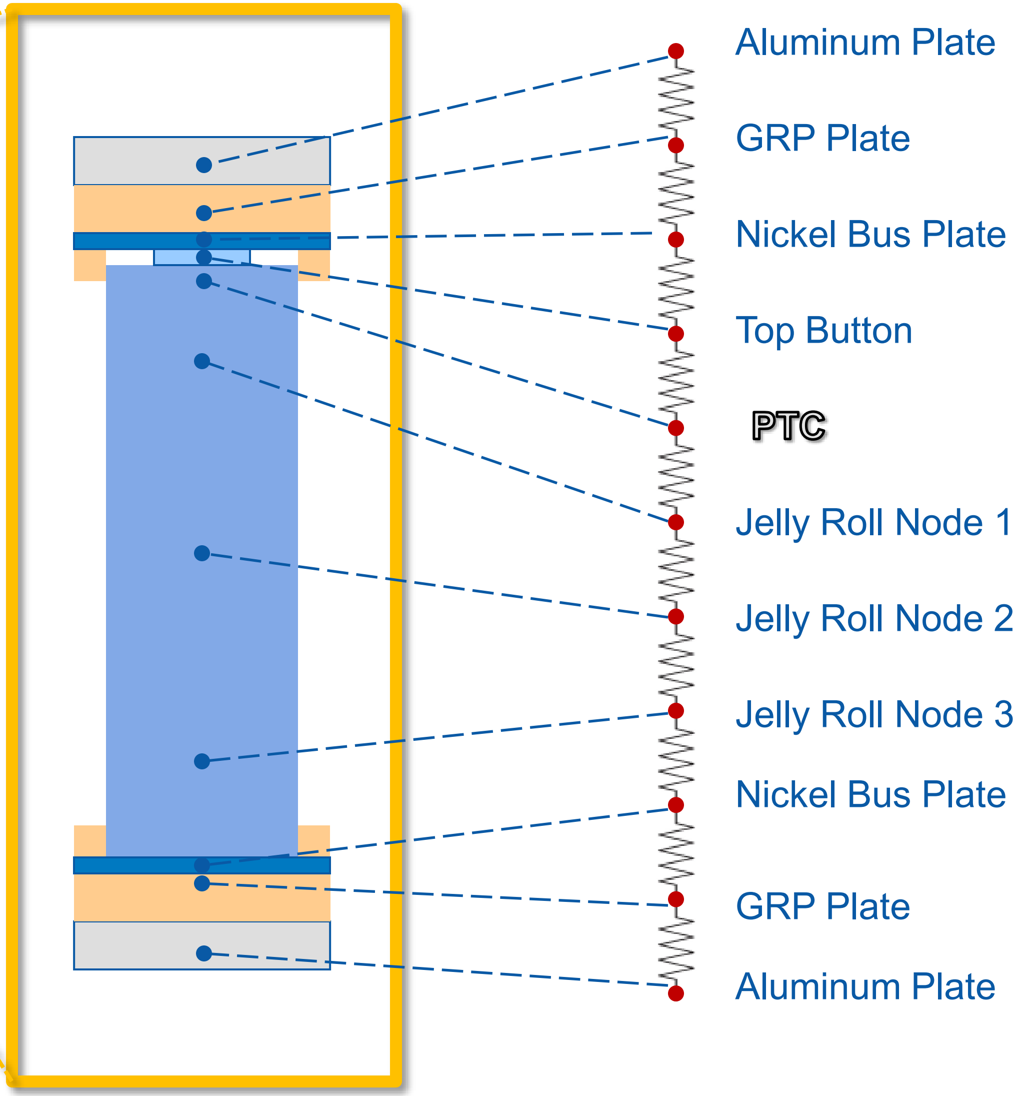
Extend the validated model to 16P5S pack

- Extended the study to identify thermal configuration among the components of the 3d module design
- Expanded the model capability to capture thermal and electrical responses and their interactions in complex geometries
- 881 thermal nodes are used

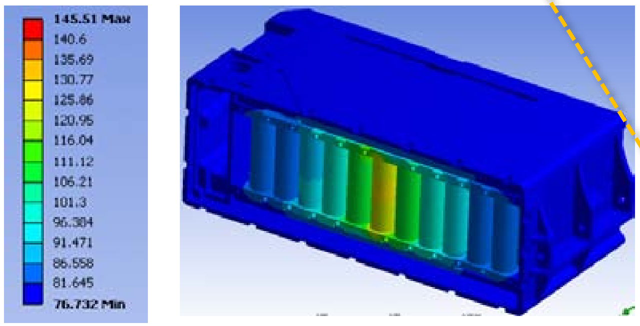


Vertical Arrangement of Thermal Nodes



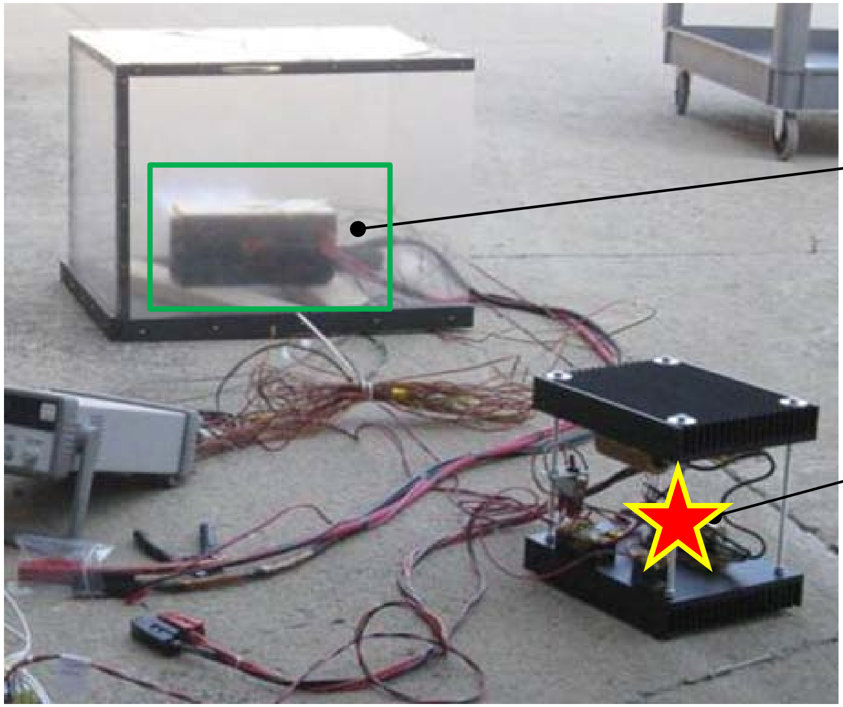


- 11 nodes are vertically placed at 80 cell locations
- Node thermal connections are defined considering various heat transfer modes
- Aluminum enclosure box is considered thermally lumped
- 11 x 80 + 1 = 881 node system



Model Validation for Pack-External Short

ABSL experiment: Bank 3 short through external resistor



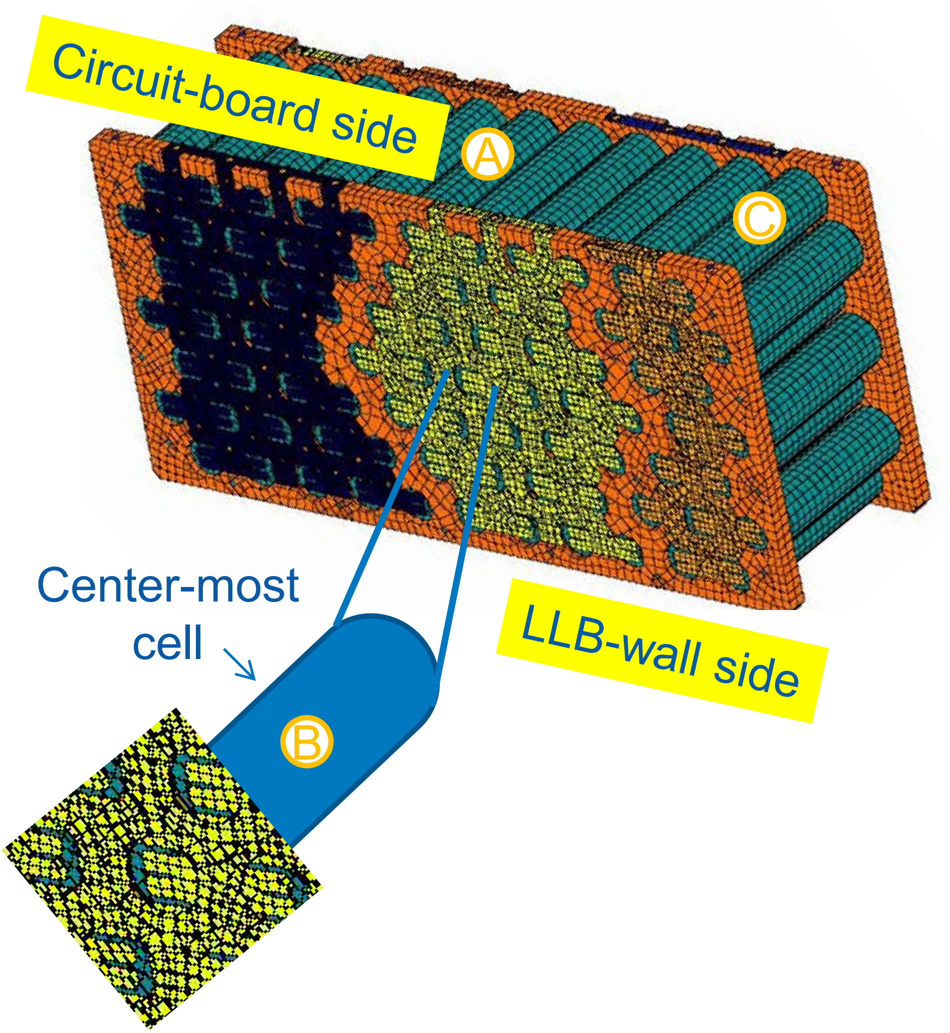
80 cell battery in test enclosure

10 mΩ resistor

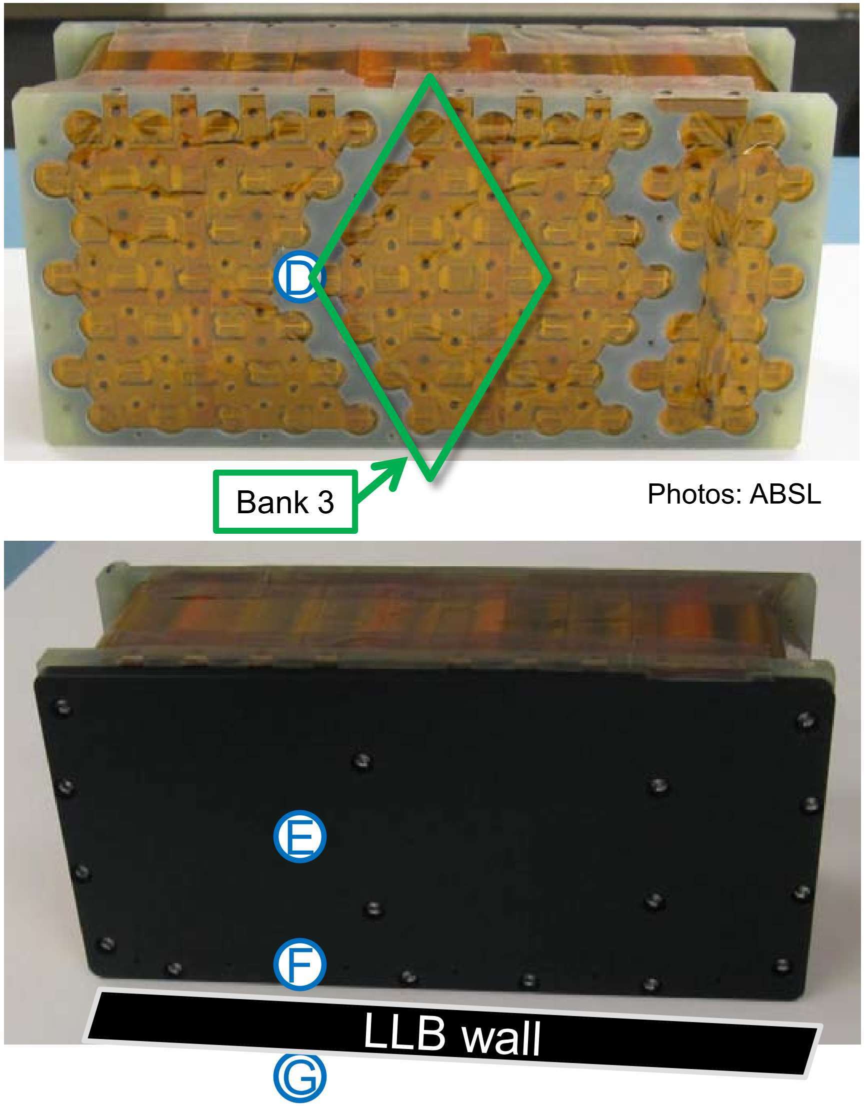
Photo: ABSL

ABSL Instrumentation

Cell Temperature Sensor Locations

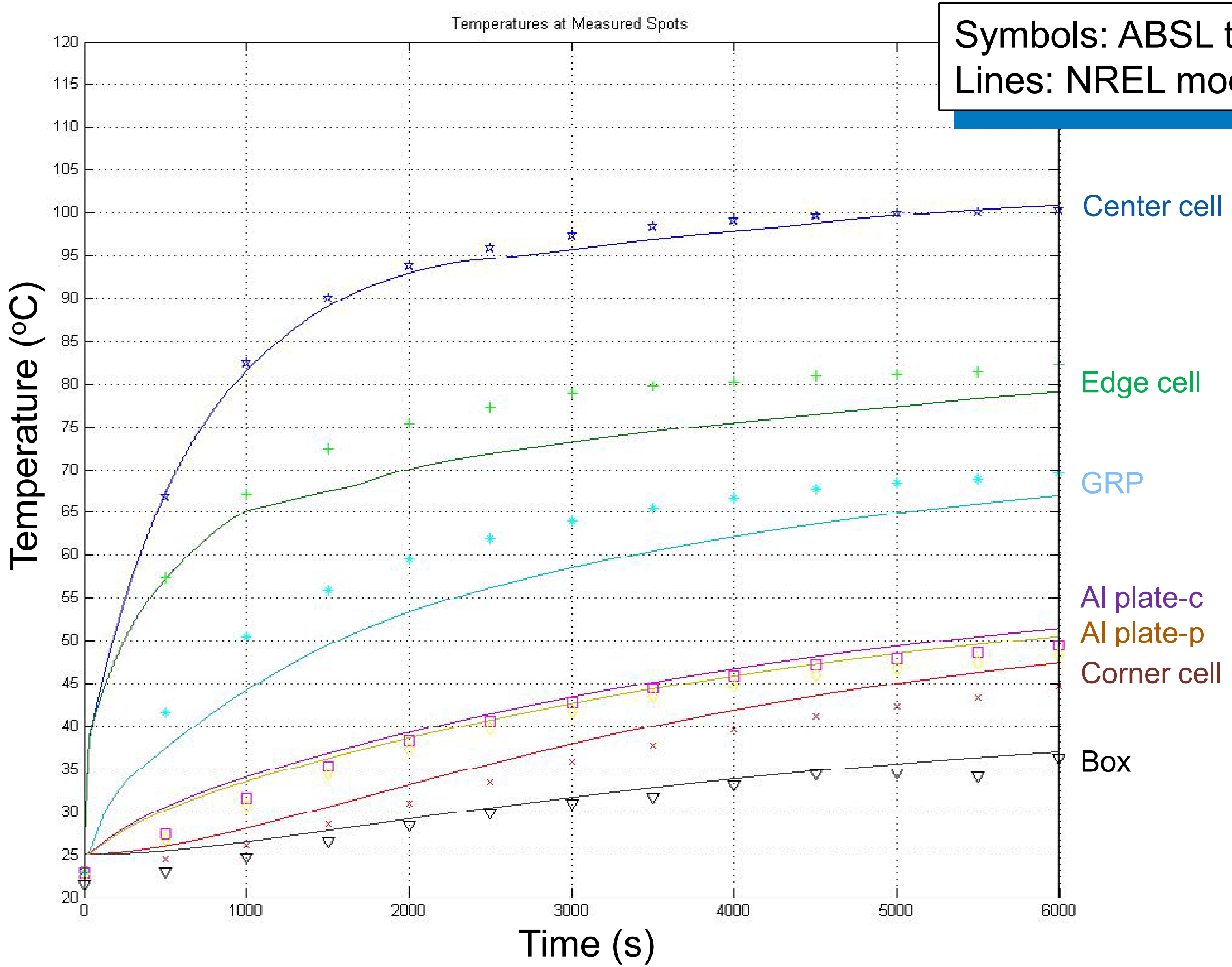


Brick Temperature Sensor Locations



Photos: ABSL

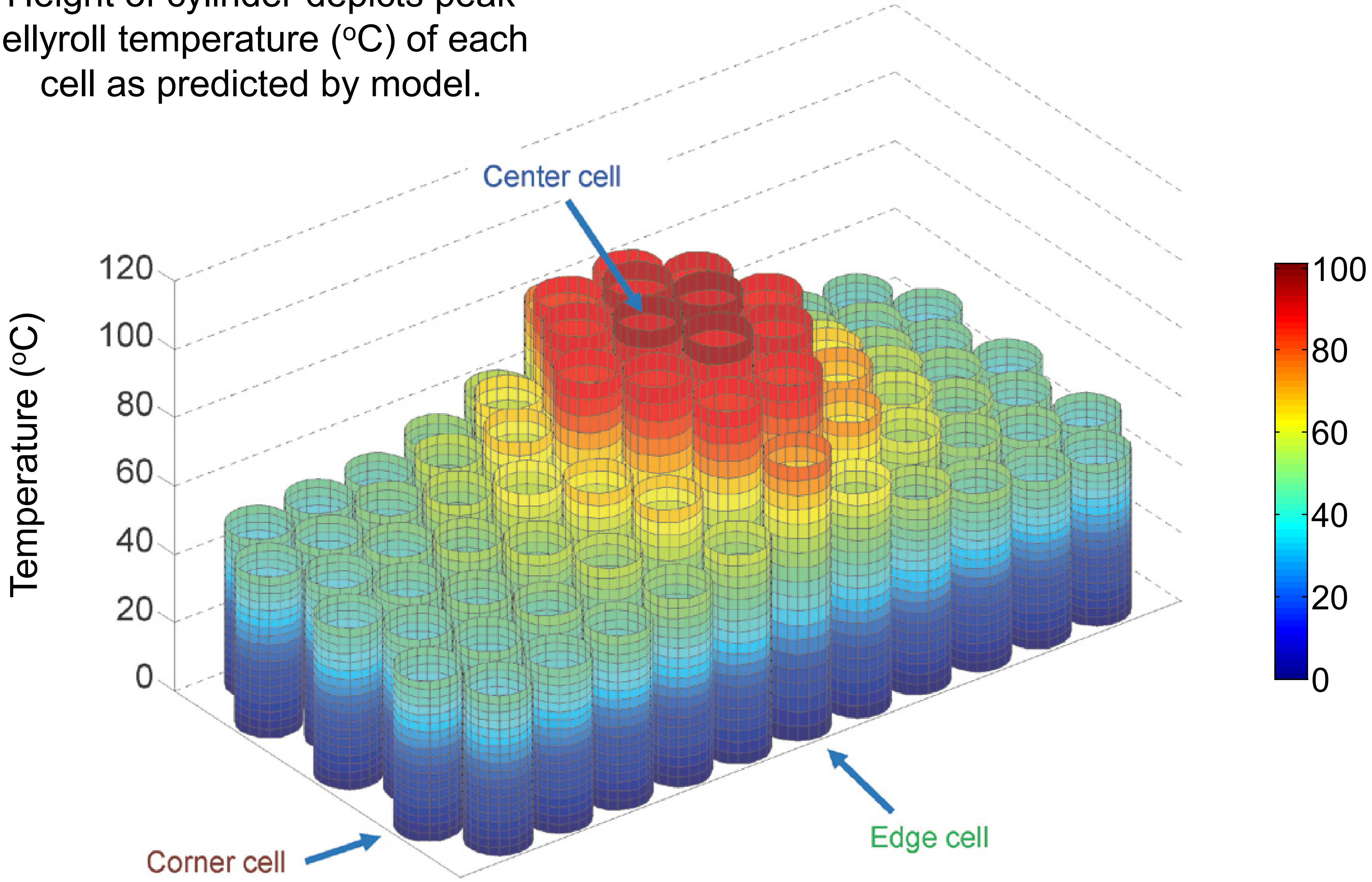
Model Validation – First 6000 seconds



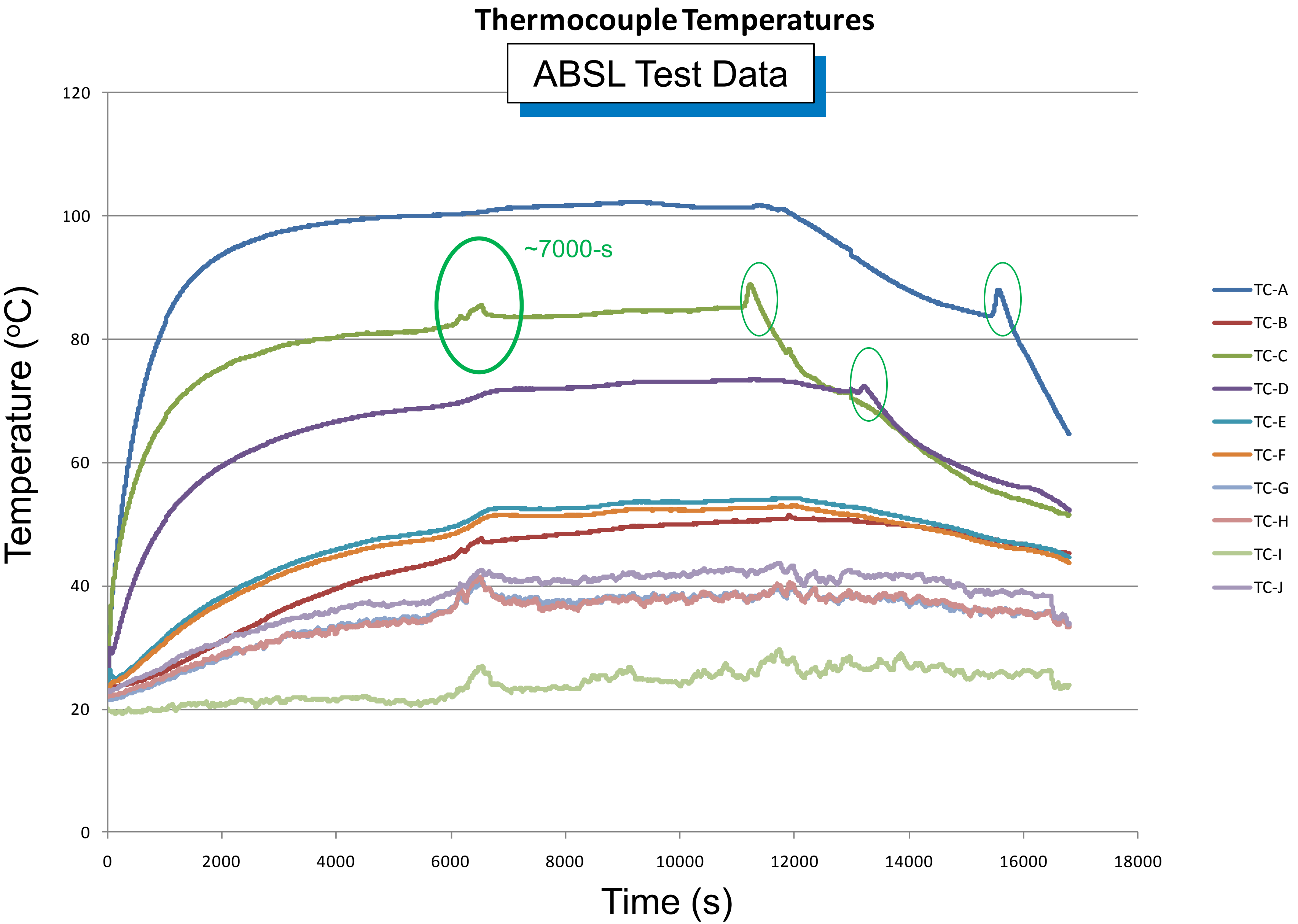
Symbols: ABSL test data
Lines: NREL model output

Cell Temperature Distribution at 6000 seconds

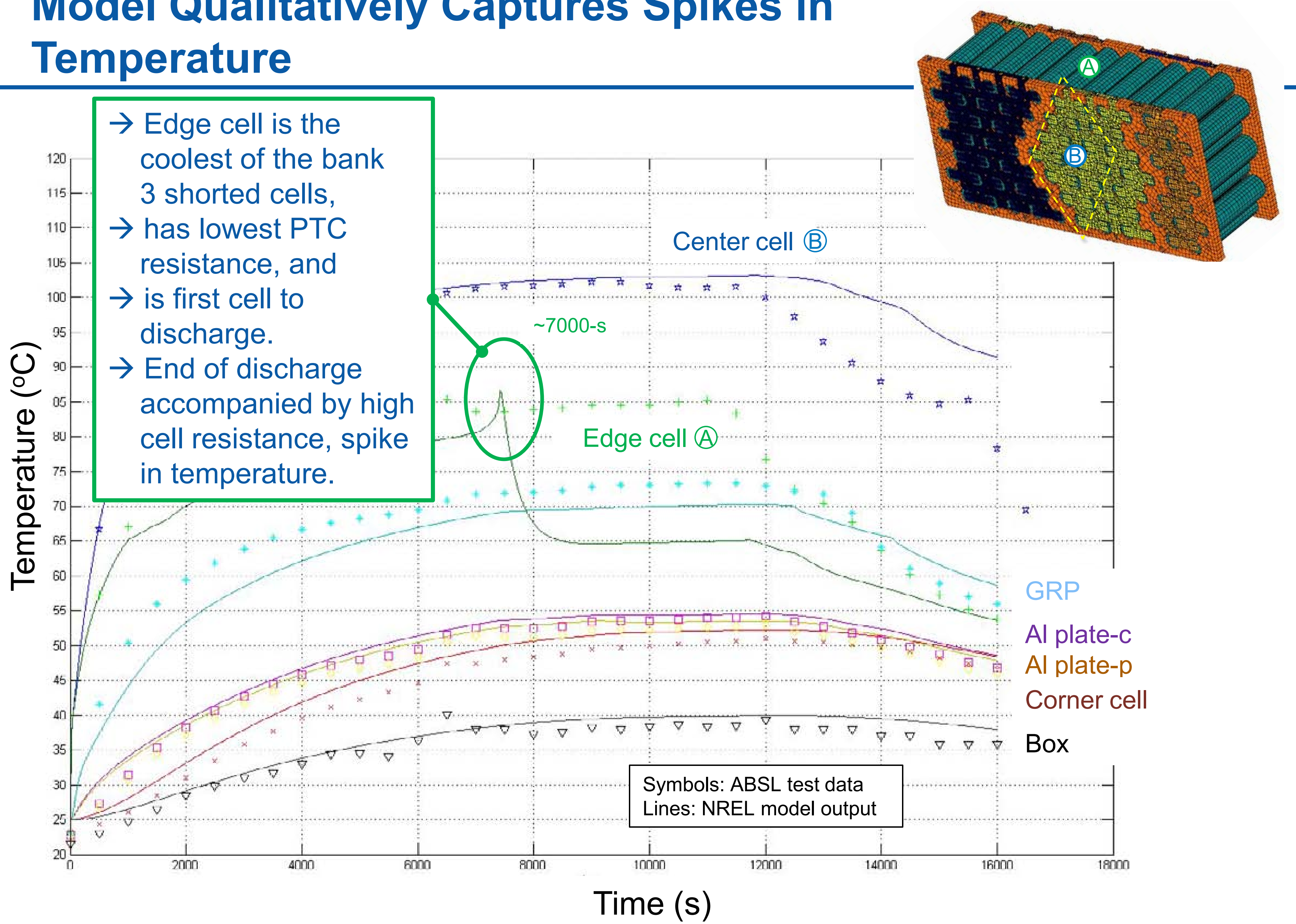
Height of cylinder depicts peak jellyroll temperature (^{o}C) of each cell as predicted by model.



Beyond 6000 Seconds, ABSL Test Data Show Periodic Spikes in Temperature



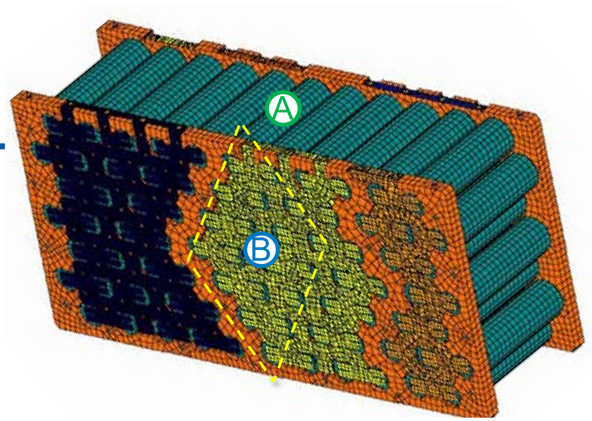
Model Qualitatively Captures Spikes in Temperature



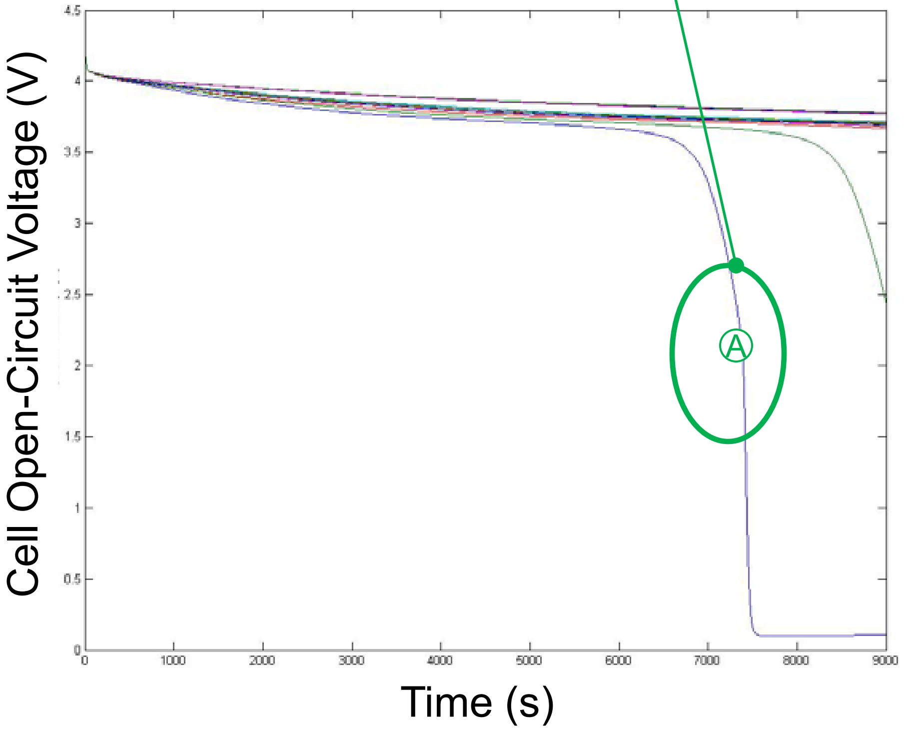
- → Edge cell is the coolest of the bank 3 shorted cells,
- → has lowest PTC resistance, and
- → is first cell to discharge.
- → End of discharge accompanied by high cell resistance, spike in temperature.

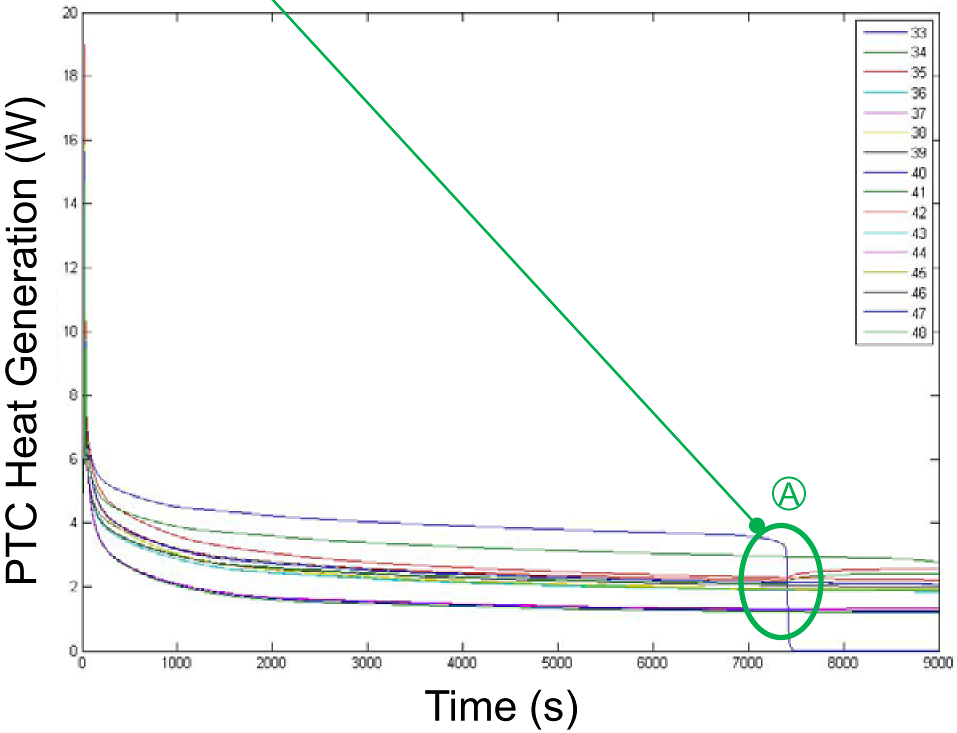
Symbols: ABSL test data
Lines: NREL model output

Model Qualitatively Captures Spikes in Temperature



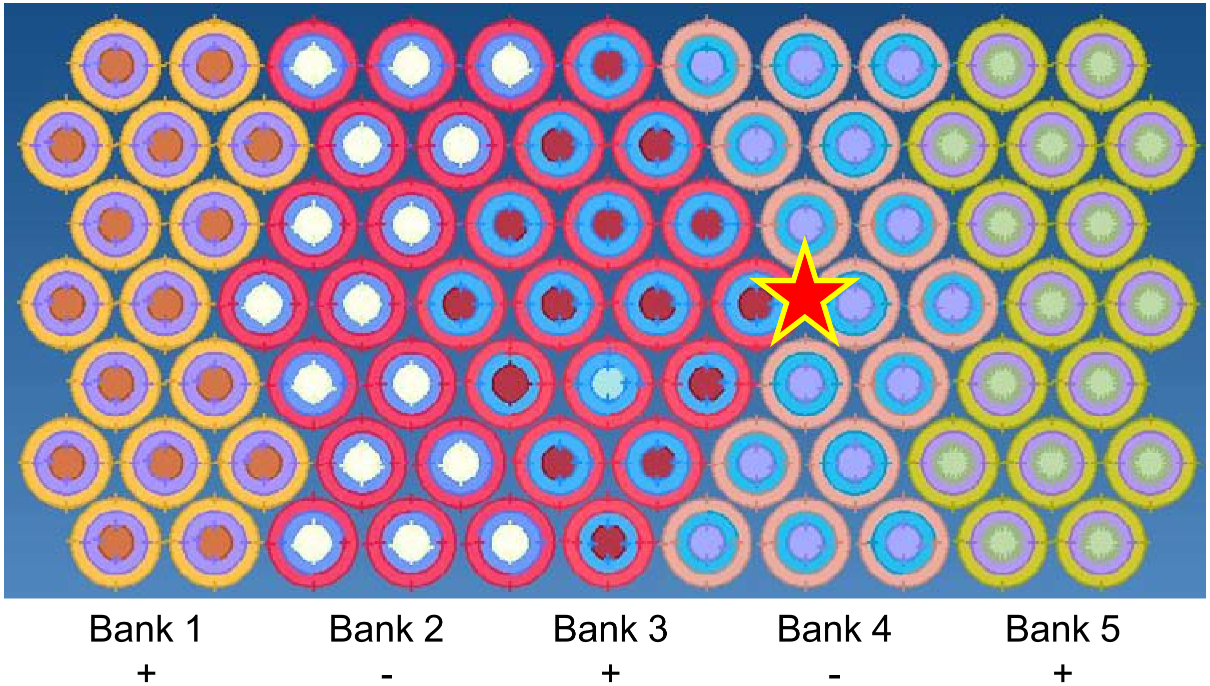
→ Edge cell is the coolest of the bank 3 shorted cells,
→ Has lowest PTC resistance, and
→ Is first cell to completely discharge.





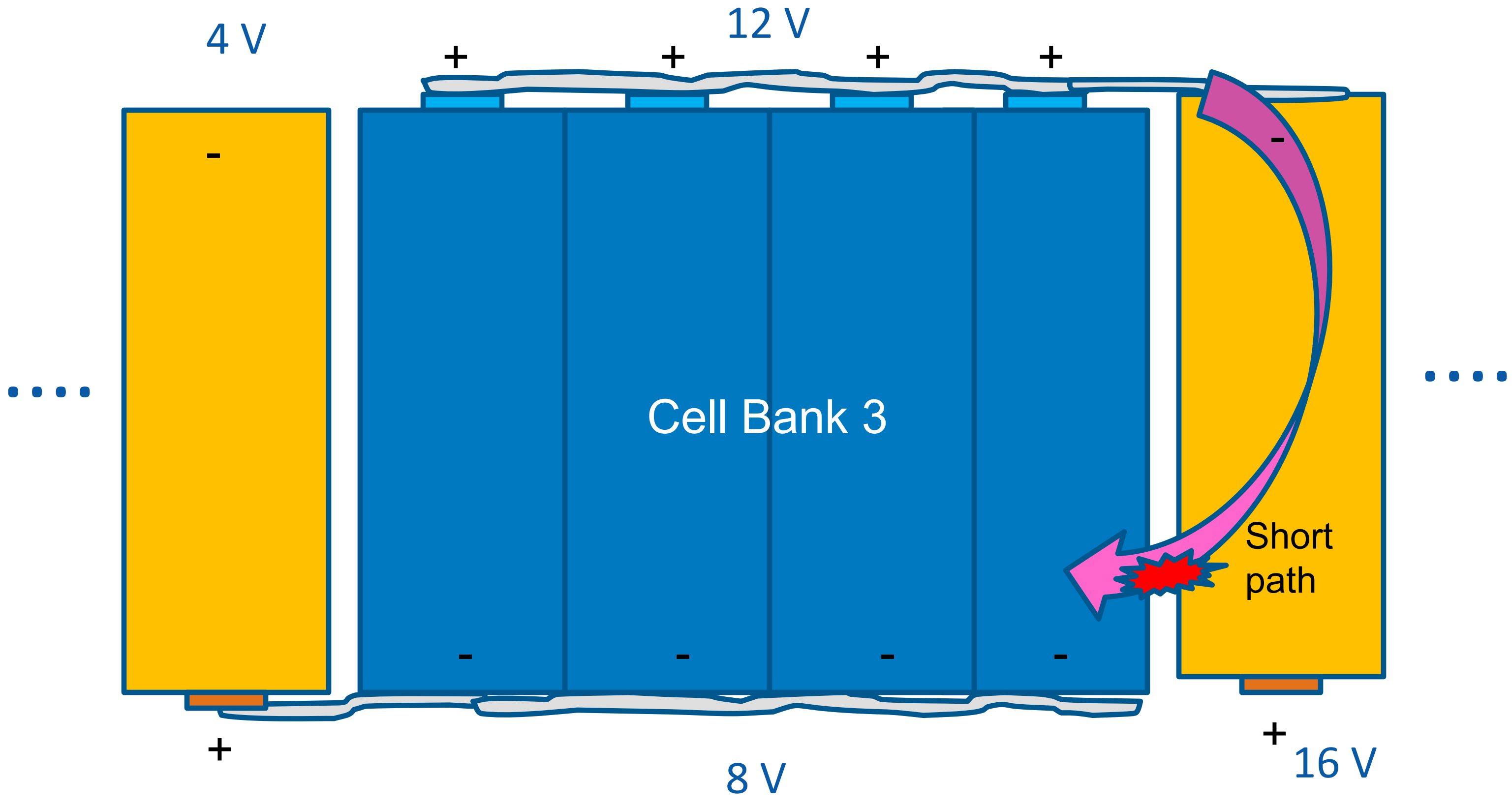
Model Analysis of Pack-Internal Shorts

E.g., bank 3 short is caused by foreign object between banks 3 and 4*



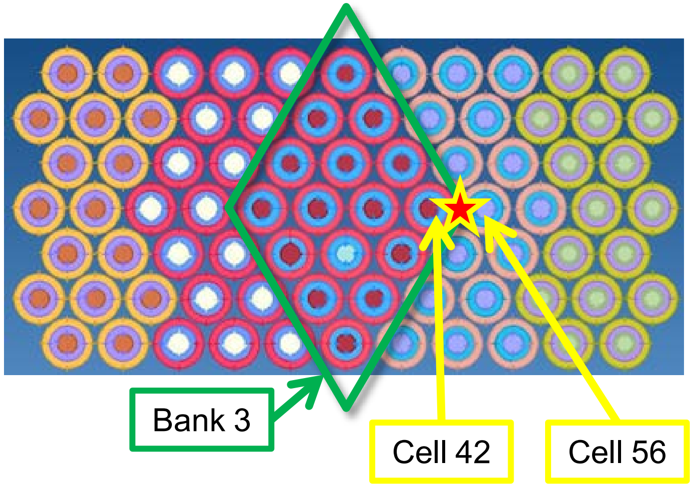
* Requires more than two faults: Introduction of FOD & penetration of Kapton/Nomex/Kapton divider between banks

Schematic of Shorted Middle Cell Bank



- Short runs through cell can of cell from adjacent bank 4
- Bare walls of cells are negatively biased
- Note that 3-layer (Kapton-Nomex-Kapton) bank-to-bank insulator is omitted for clarity

Bank 3 Short from 100% SOC



- Cell 42 (bank 3) participates in electrical discharge
- Cell 56 (bank 4) does not electrically discharge; its external can wall serves as a path for short current
- Model assumes ohmic heat of short shared equally by cells 42 and 56

- Internal-to-pack short more thermally severe than external-to-pack
- Thermal mass dominates – negligible dependence on earth vs. space boundary conditions
- Runaway possibly prevented at 10 mΩ
- Runaway predicted at 20,30 mΩ with collateral damage

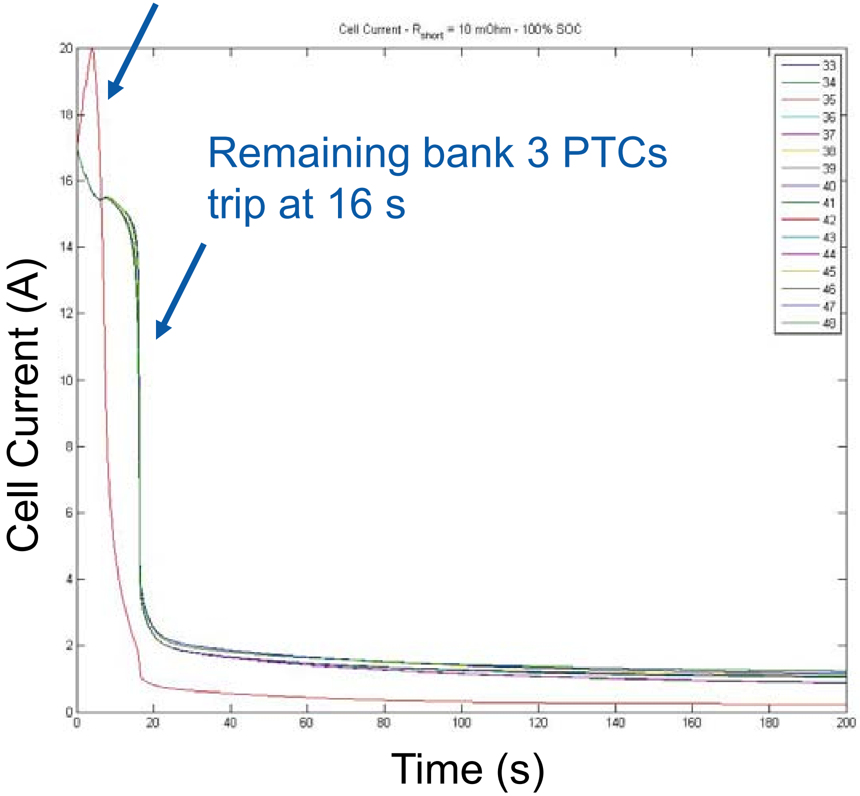
R_{short}	**Short Condition** (SOC_0 = 100%)	**Cell 42 T_{max}** (Bank 3)	**Cell 56 T_{max}** (Bank 4)
10 mΩ	External-to-pack, earth	97°C @ 6000-s	75°C @ 6000-s
	Internal-to-pack, earth	150°C @ 16-s	146°C @ 16-s
	Internal-to-pack, space	153°C @ 16-s	147°C @ 16-s
20 mΩ	Internal-to-pack, space	525°C @ 110-s	522°C @ 110-s
30 mΩ	Internal-to-pack, space	595°C @ 240-s	591°C @ 240-s

Bank 3 Short from 100% SOC: 10 mΩ vs. 20 mΩ

10 mΩ:

Bank 3 PTCs trip quickly and uniformly because high inrush current causes PTC self-heating

Cell 42 PTC trips at 8 s

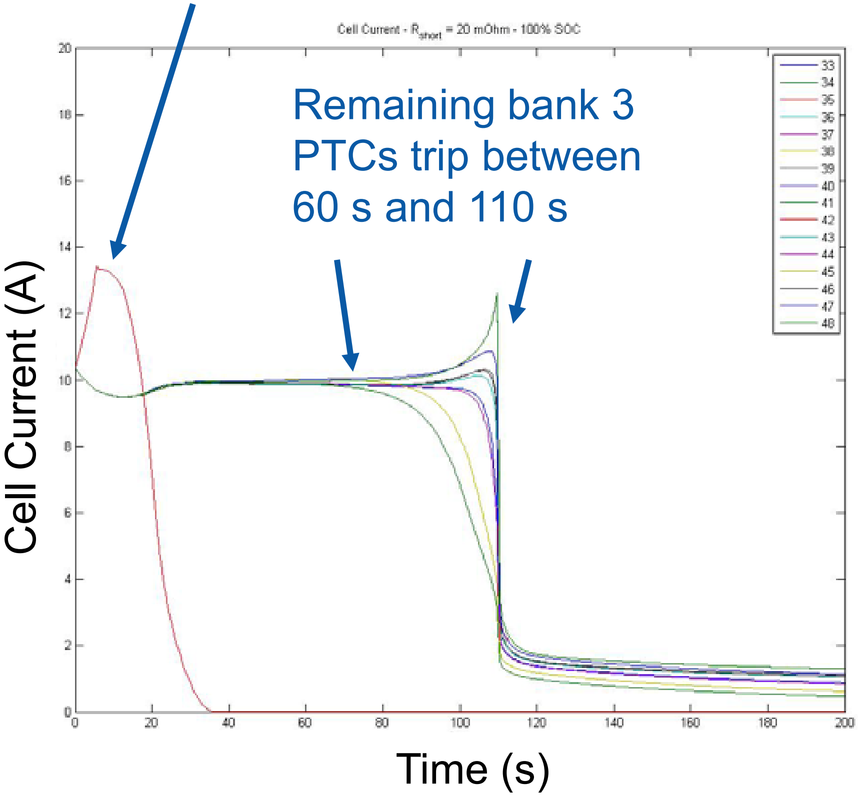


Remaining bank 3 PTCs trip at 16 s

20 mΩ:

Bank 3 PTCs trip slowly at different times, depending upon bank 3 temperature distribution

Cell 42 PTC trips at10 s

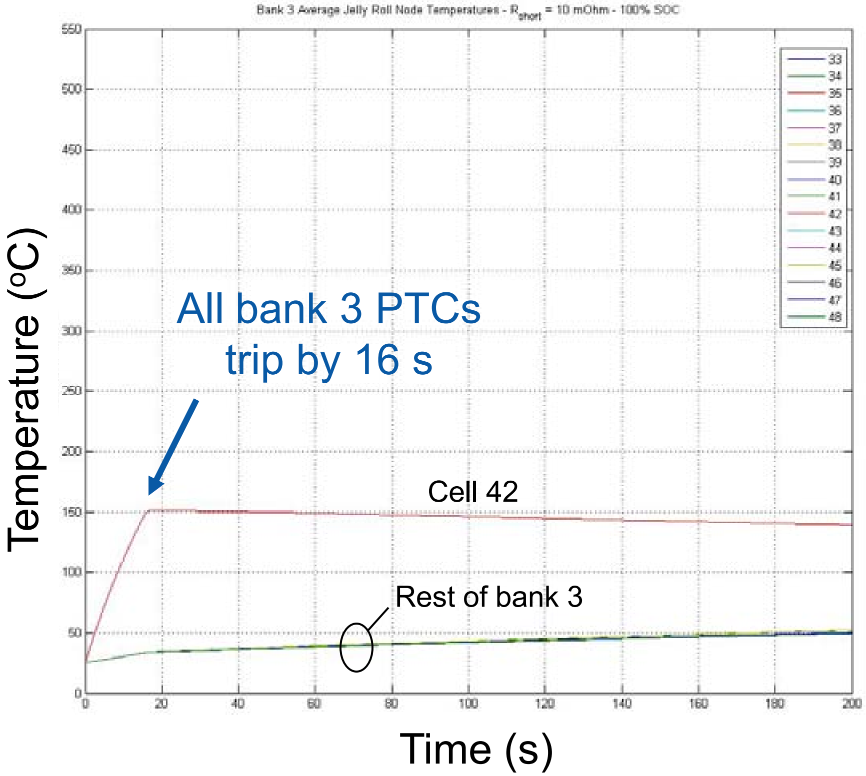


Remaining bank 3 PTCs trip between 60 s and 110 s

Bank 3 short from 100% SOC: 10 mΩ vs. 20 mΩ

10 mΩ:

Bank 3 PTCs trip quickly and uniformly due to high in-rush current causing PTC self-heating



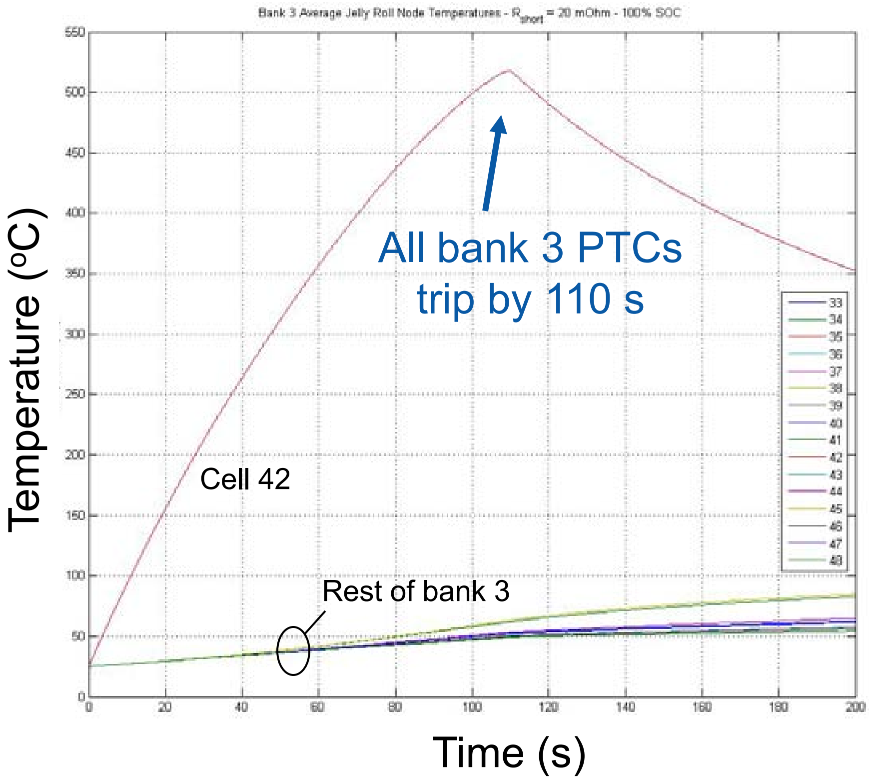
All bank 3 PTCs trip by 16 s

Cell 42

Rest of bank 3

20 mΩ:

Bank 3 PTCs trip slowly, at different times dependent upon bank 3 temperature distribution

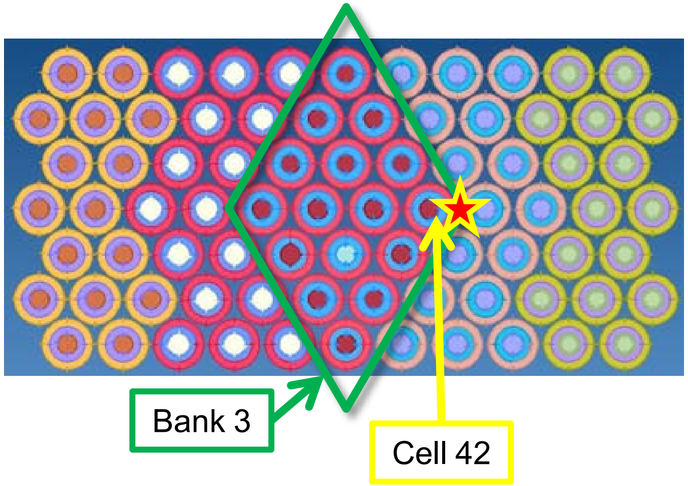


All bank 3 PTCs trip by 110 s

Cell 42

Rest of bank 3

Bank 3 Short from 100% SOC: Cell-to-Cell Radiation



Design question:

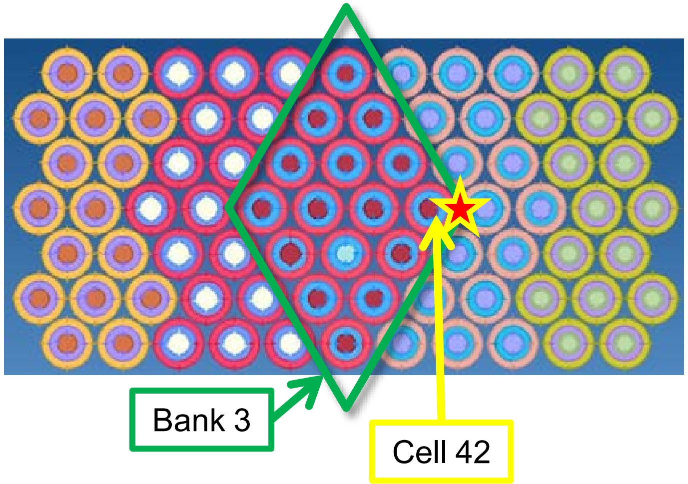
Would a high-emissivity coating applied to bare cell walls help limit thermal excursion?

R_{short}	**Short Condition** (SOC_0 = 100%)	**Cell wall emissivity**	**Cell 42 T_{max}** (Bank 3)
20 mΩ	Internal-to-pack, earth	ε = 0.3 (Nominal)	525°C @ 110 s
		ε = 0.9 (Coating)	410°C @ 102 s

(Minimal change)

Bank 3 Short: SOC Dependence

Is battery design tolerant to pack-internal shorts when stored at low SOCs?



R_{short}	Short Condition	Initial SOC	Initial OCV	Cell 42 T_{max} (Bank 3)
20 mΩ	Internal-to-pack, earth	1.5%	3.428 V	117°C @ 85 s
		0.5%	3.346 V	83°C @ 80 s

No thermal runaway when stored at 0% SOC (3.25 OCV).

What About Cell-Internal Shorts?

- Scenario
  - 20 mΩ short bridging anode and cathode inside a cell jellyroll
  - Defective cell at 100% SOC
  - Battery at room temperature

- Possible projections based on model results
  - Cell bank energy would rapidly dissipate inside the cell and raise its temperature
  - Defective cell's PTC device would trip and choke off current from the 15 cells in parallel, well before their PTC devices trip
  - So, the hazard may be limited to the defective cell only and less collateral damage may result vs. the internal pack short

- Further work is necessary in this area for confirmation

Conclusions

- 80-cell spacesuit battery electrical/thermal model
  - Captures relevant physics for cell-external shorting events, including PTC behavior
  - Agrees well with pack-external bank 3 short experiment run by ABSL
  - Predicts that design will tolerate all pack-external short resistance conditions
- Relocating short from pack-external (experimental validation) to pack-internal (modeling study) causes substantial additional heating of cells that can lead to cell thermal runaway
  - Negligible sensitivity to earth/space BCs (thermal mass dominates)
  - Large sensitivity to R_{short}
    - $R_{short} < 10\ m\Omega$: 16P bank PTCs trip quickly, most likely preventing runaway
    - $10\ m\Omega < R_{short} < 60\ m\Omega$: Thermal runaway appears likely
  - Fortunately, all three layers of bank-to-bank separator must fail for pack-internal short scenario to occur
  - Nevertheless, this finding re-emphasizes the general imperative of battery pack assembly cleanliness
- Design is tolerant to pack-internal short when stored at 0% SOC

Acknowledgments

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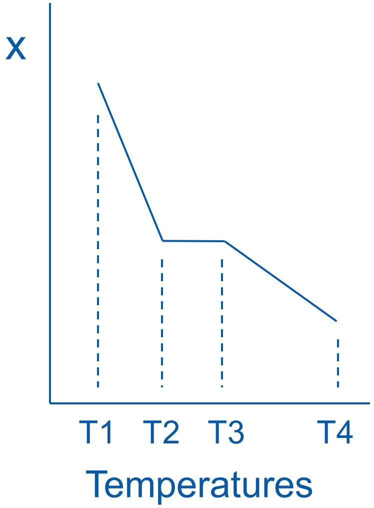
Extra Slides

Contact Resistance Formulation



$$Q = \frac{T_1 - T_2}{\Delta x_{Al} / k_{Al} A} = \frac{T_2 - T_3}{R_i} = \frac{T_3 - T_4}{\Delta x_{Ni} / k_{Ni} A}$$

For uncertainty of quantifying thermal resistance at the contact interface between the parts, a parametric formulation was developed.

Temperature discontinuity at interface, $\Delta T_{interface}$, was set as a fraction of the total temperature difference between the adjacent nodes, ΔT.

$$\Delta T_{interface} = f * \Delta T_{1\text{-}4} \qquad (0 <= f < 1)$$

$$K_{1-4} = \frac{1}{R_{1-4}} = \frac{1-f}{\left(\frac{\Delta x_{Al}}{k_{Al} A} + \frac{\Delta x_{Ni}}{k_{Ni} A}\right)} \quad \left[W/K\right]$$

Δx: half of plate thickness