Polycrystalline Thin Film Solar Cell Durability: Stress Testing, Measurements, and Diagnostics

NREL

David Albin

November 19, 2010
36th ISTFA
Tutorial
Dallas, TX USA

NREL/PR-5200-50569

Speaker Background

1. Experience
   i. B.S. / M.S. University of Illinois (Ceramic Engineering)
   ii. Cathode-Ray Tube Engineer (Tektronix)
   iii. Ph.D. University of Arizona (Materials Science; minor Electrical Engineering)
   iv. 20+ years in Cu(In,Ga)Se_2 (CIGS) and CdTe cell research at NREL

2. CIGS Cell Research (1987 – 1992)
   i. System and Process Development (co-evaporation, selenization) – a ***lot of cells!***
   ii. Film Growth Physics –optical, electrical, microstructural properties of films
   iii. (3) patents associated with high-efficiency CIGS cell fabrication

3. CdTe Cell Research (1993 – present)
   i. System and Process Development (close-spaced sublimation (CSS), chemical-bath deposition (CBD), vapor $CdCl_2$, backcontacts) – ***and still more cells!!***
   ii. Device Physics
   iii. Cell reliability research

4. Cell Reliability (2002 – present)
   i. Leader National Thin Film Cell Reliability Team; NREL Cell Reliability Project Leader
   ii. Data management (performance, processing, reliability)
   iii. Industry interactions – currently 5 years working with PrimeStar Solar, a CdTe start-up (primary owner GE)

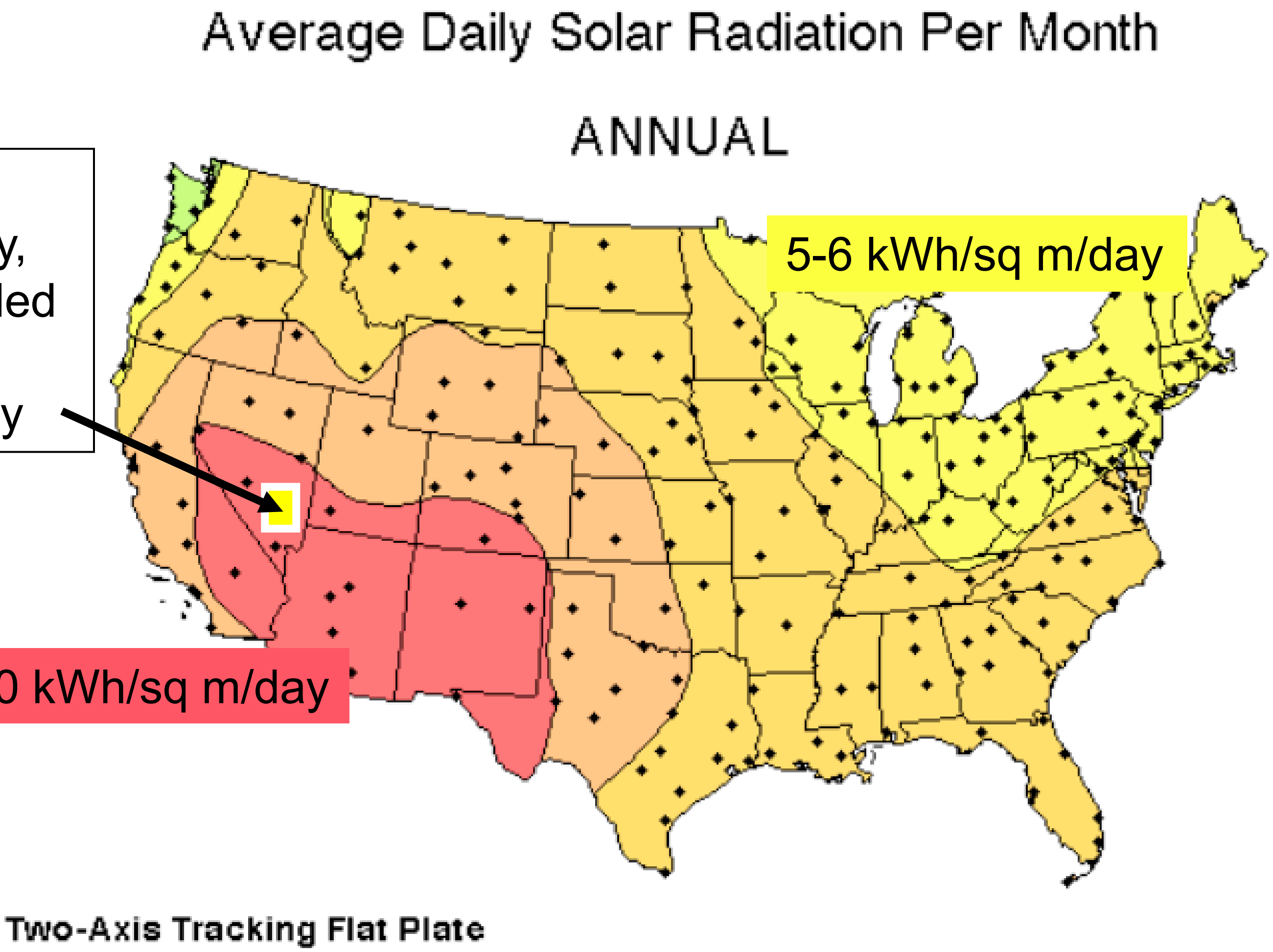
Course Outline

- **The “business” side of thin film photovoltaics**
  - Manufacturing
  - Cost
  - Reliability
- **Measuring “reliability” – Qualification and Testing**
- **Thin Film Solar Cell Physics**
- **Common Failure Analysis Methods**
- **Understanding the non-ideal nature of thin-films vs. crystalline.**
- **Thin film cell processing (CdTe)**
- **The use of DOE and Data Management in Thin Film Development**
- **Thin Film CdTe Durability Case Studies**
  - Backcontact Processing
  - CdTe Processing
  - Degradation Activation Energy Determination
  - The Correlation of C-V transients (hysteresis) with Performance During Stress

The “business” (a.k.a. $$) side of Photovoltaics

Solar as an Energy Source is Viable

Convenient truth: small area can supply our energy needs



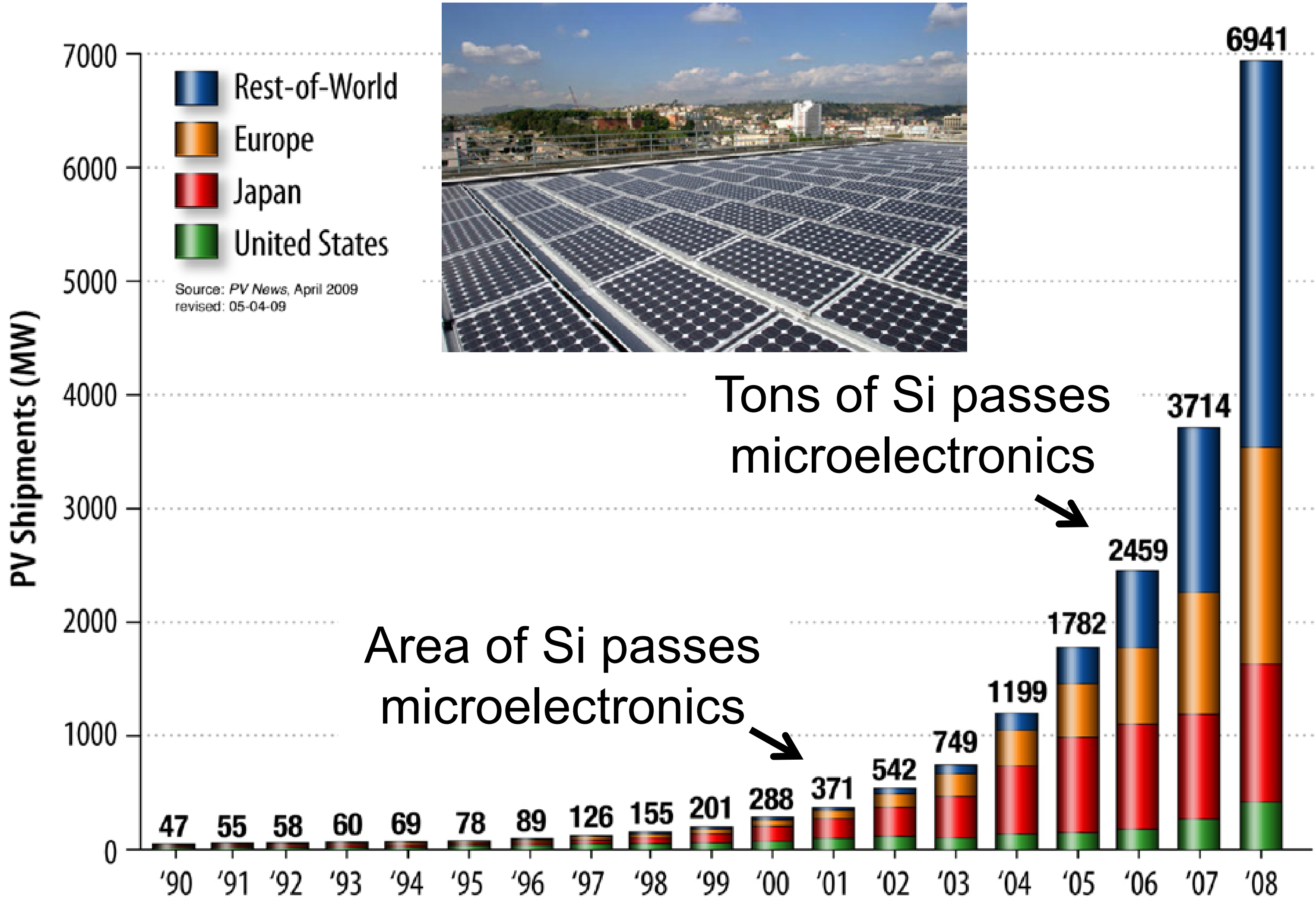
At 10% efficiency, area needed for US electricity

5-6 kWh/sq m/day

>10 kWh/sq m/day

Sunlight reaching earth in 1 hour is enough to power the world for 1 year

Growth of photovoltaic (PV) manufacturing impressive

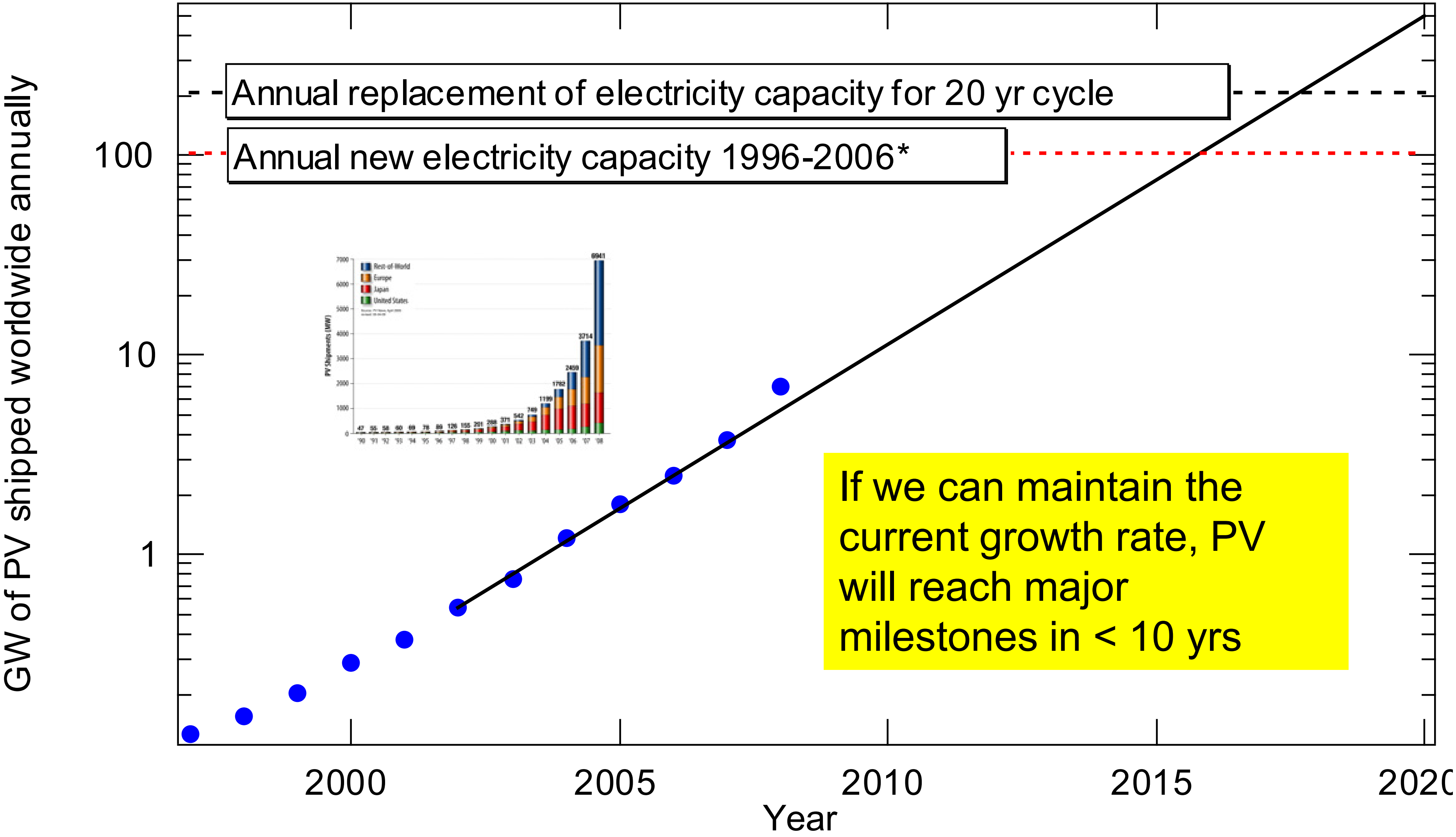


Source: *PV News*, April 2009
revised: 05-04-09

Tons of Si passes microelectronics

Area of Si passes microelectronics

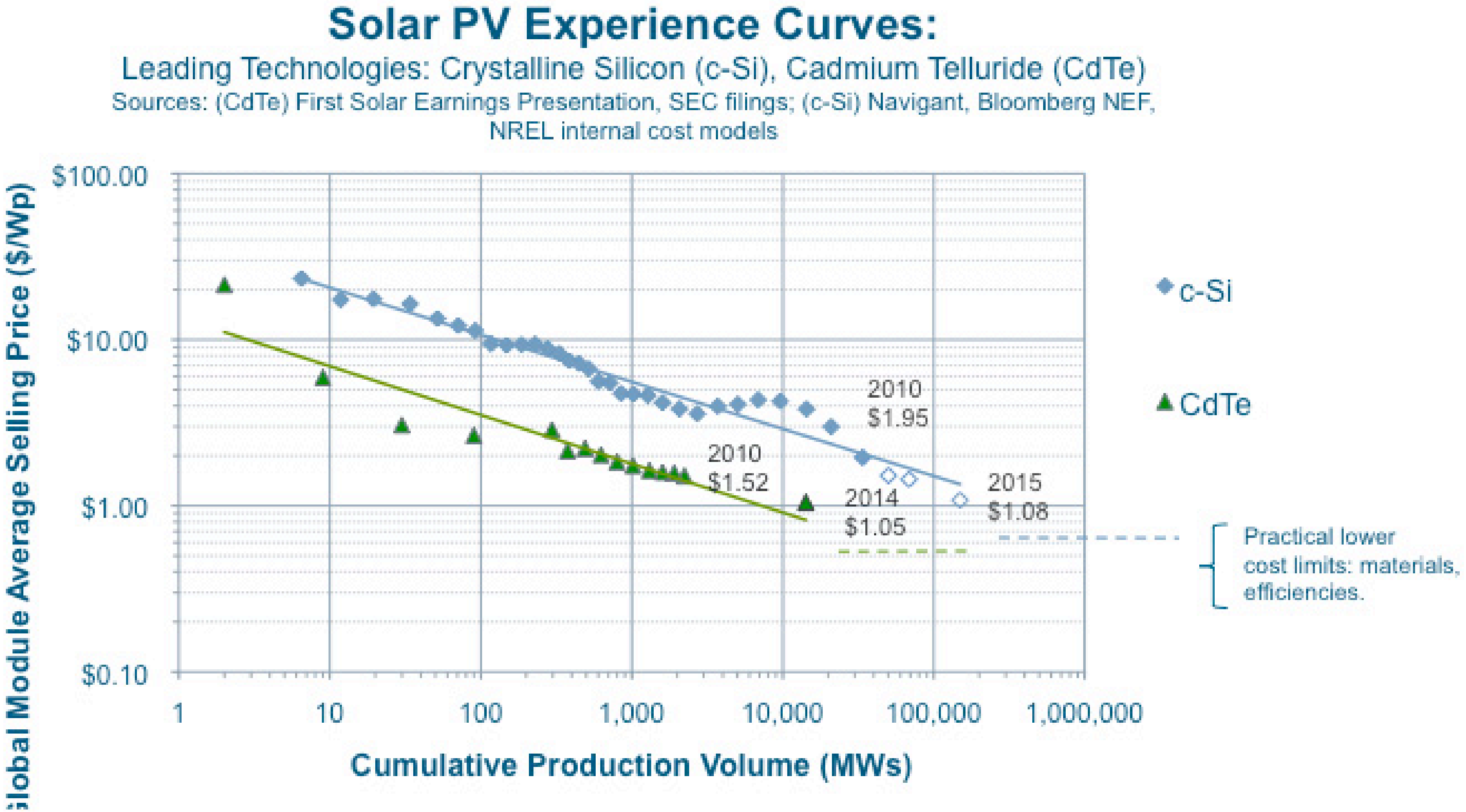
Growth is aligned with projected needs



If we can maintain the current growth rate, PV will reach major milestones in < 10 yrs

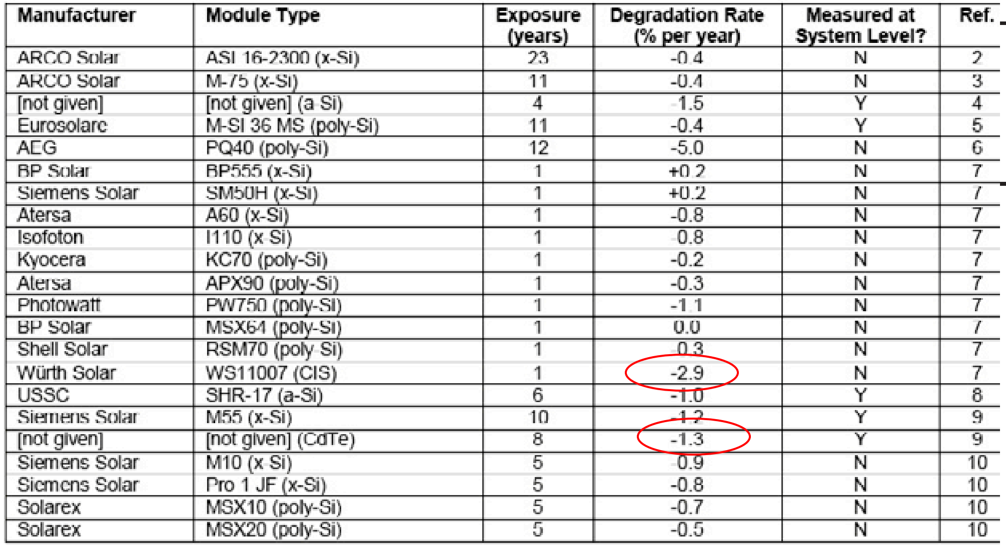
http://www.eia.doe.gov/emeu/international/electricitycapacity.html

PV will soon become competetive



Solar Energy Technology Program (SETP) - DOE

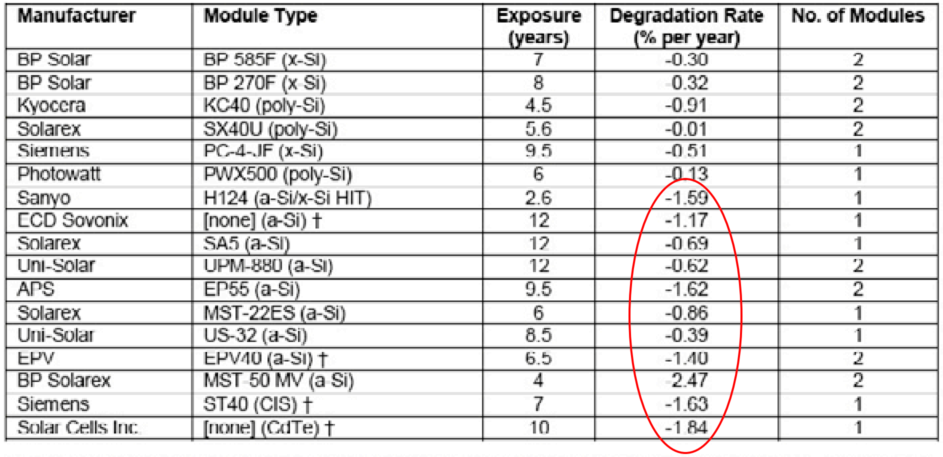
Documented degradation rates are troublesome?



Manufacturer	Module Type	Exposure (years)	Degradation Rate (% per year)	Measured at System Level?	Ref.
ARCO Solar	ASI 16-2300 (x-Si)	23	-0.4	N	2
ARCO Solar	M-75 (x-Si)	11	-0.4	N	3
[not given]	[not given] (a-Si)	4	-1.5	Y	4
Eurosolare	M-SI 36 MS (poly-Si)	11	-0.4	Y	5
AEG	PQ40 (poly-Si)	12	-5.0	N	6
BP Solar	BP555 (x-Si)	1	+0.2	N	7
Siemens Solar	SM50H (x-Si)	1	+0.2	N	7
Atersa	A60 (x-Si)	1	-0.8	N	7
Isofoton	I110 (x-Si)	1	-0.8	N	7
Kyocera	KC70 (poly-Si)	1	-0.2	N	7
Atersa	APX90 (poly-Si)	1	-0.3	N	7
Photowatt	PW750 (poly-Si)	1	-1.1	N	7
BP Solar	MSX64 (poly-Si)	1	0.0	N	7
Shell Solar	RSM70 (poly-Si)	1	-0.3	N	7
Würth Solar	WS11007 (CIS)	1	-2.9	N	7
USSC	SHR-17 (a-Si)	6	-1.0	Y	8
Siemens Solar	M55 (x-Si)	10	-1.2	Y	9
[not given]	[not given] (CdTe)	8	-1.3	Y	9
Siemens Solar	M10 (x-Si)	5	-0.9	N	10
Siemens Solar	Pro 1 JF (x-Si)	5	-0.8	N	10
Solarex	MSX10 (poly-Si)	5	-0.7	N	10
Solarex	MSX20 (poly-Si)	5	-0.5	N	10

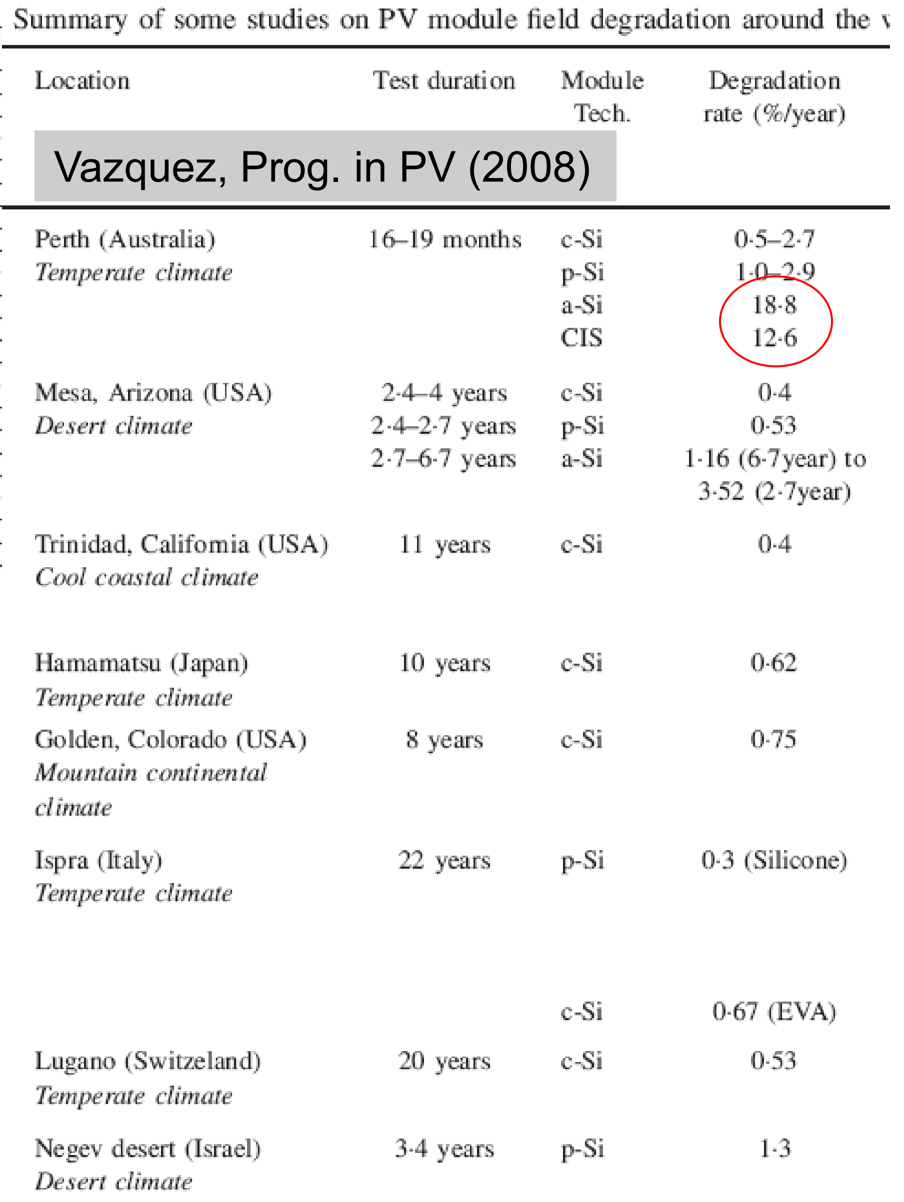
Table 1. PV module degradation rates published within the past five years.

31st IEEE PVSC p.2085 (2006)



Manufacturer	Module Type	Exposure (years)	Degradation Rate (% per year)	No. of Modules
BP Solar	BP 585F (x-Si)	7	-0.30	2
BP Solar	BP 270F (x-Si)	8	-0.32	2
Kyocera	KC40 (poly-Si)	4.5	-0.91	2
Solarex	SX40U (poly-Si)	5.6	-0.01	2
Siemens	PC-4-JF (x-Si)	9.5	-0.51	1
Photowatt	PWX500 (poly-Si)	6	-0.13	1
Sanyo	H124 (a-Si/x-Si HIT)	2.6	-1.59	1
ECD Sovonix	[none] (a-Si) †	12	-1.17	1
Solarex	SA5 (a-Si)	12	-0.69	1
Uni-Solar	UPM-880 (a-Si)	12	-0.62	2
APS	EP55 (a-Si)	9.5	-1.62	2
Solarex	MST-22ES (a-Si)	6	-0.86	1
Uni-Solar	US-32 (a-Si)	8.5	-0.39	1
EPV	EPV40 (a-Si) †	6.5	-1.40	2
BP Solarex	MST-50 MV (a-Si)	4	-2.47	2
Siemens	ST40 (CIS) †	7	-1.63	1
Solar Cells Inc.	[none] (CdTe) †	10	-1.84	1

Table 2. PV module degradation rates obtained from monthly PTC regressions of PERT I-V data. Module types marked with a '†' indicate non-production prototypes that are not indicative of current products.



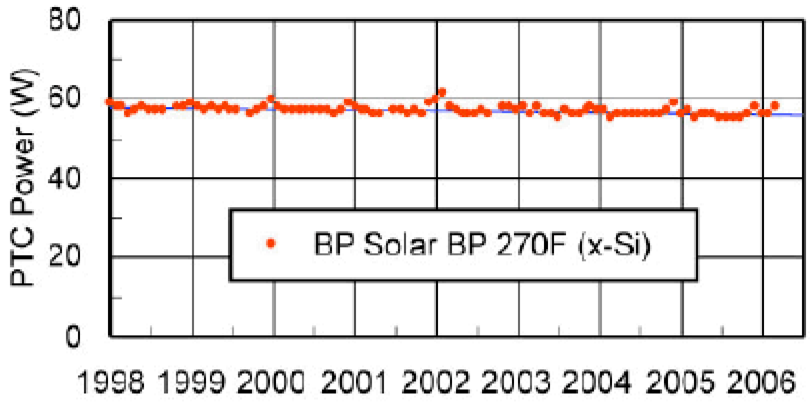
Summary of some studies on PV module field degradation around the

Vazquez, Prog. in PV (2008)

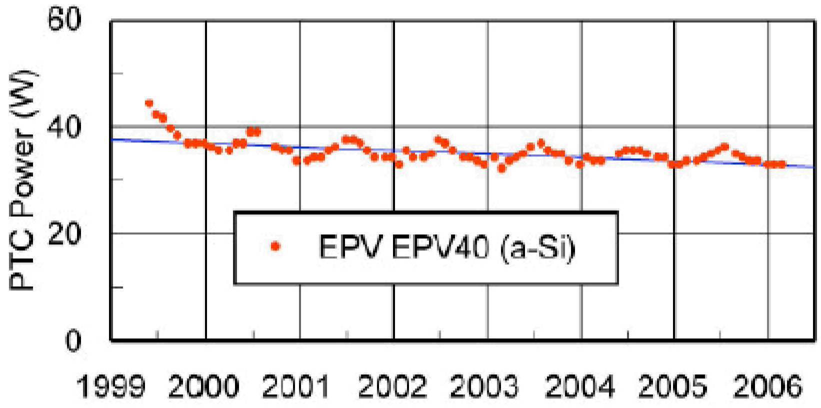
Location	Test duration	Module Tech.	Degradation rate (%/year)
Perth (Australia) *Temperate climate*	16–19 months	c-Si	0·5–2·7
		p-Si	1·0–2·9
		a-Si	18·8
		CIS	12·6
Mesa, Arizona (USA) *Desert climate*	2·4–4 years	c-Si	0·4
	2·4–2·7 years	p-Si	0·53
	2·7–6·7 years	a-Si	1·16 (6·7year) to 3·52 (2·7year)
Trinidad, California (USA) *Cool coastal climate*	11 years	c-Si	0·4
Hamamatsu (Japan) *Temperate climate*	10 years	c-Si	0·62
Golden, Colorado (USA) *Mountain continental climate*	8 years	c-Si	0·75
Ispra (Italy) *Temperate climate*	22 years	p-Si	0·3 (Silicone)
		c-Si	0·67 (EVA)
Lugano (Switzeland) *Temperate climate*	20 years	c-Si	0·53
Negev desert (Israel) *Desert climate*	3·4 years	p-Si	1·3

Documented degradation rates are troublesome?

c-Si and thin film module degradation rates in Golden, CO



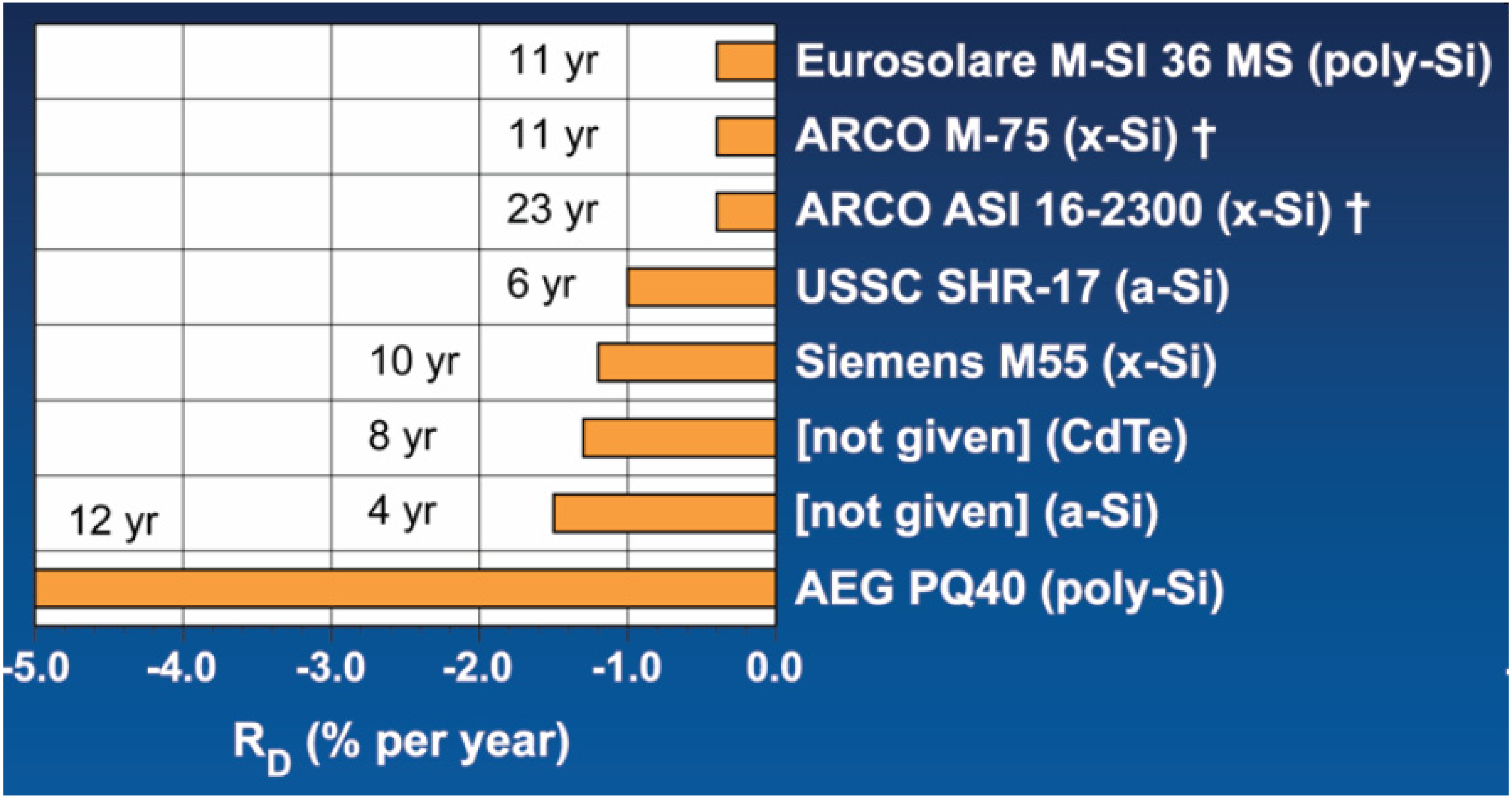
-0.25%/year)



-1.32%/year, after initial stabilization

Osterwald, NREL

Documented degradation rates are troublesome? ☹



Slide provided by J. del Cueto (NREL)

Challenges for PV Reliability

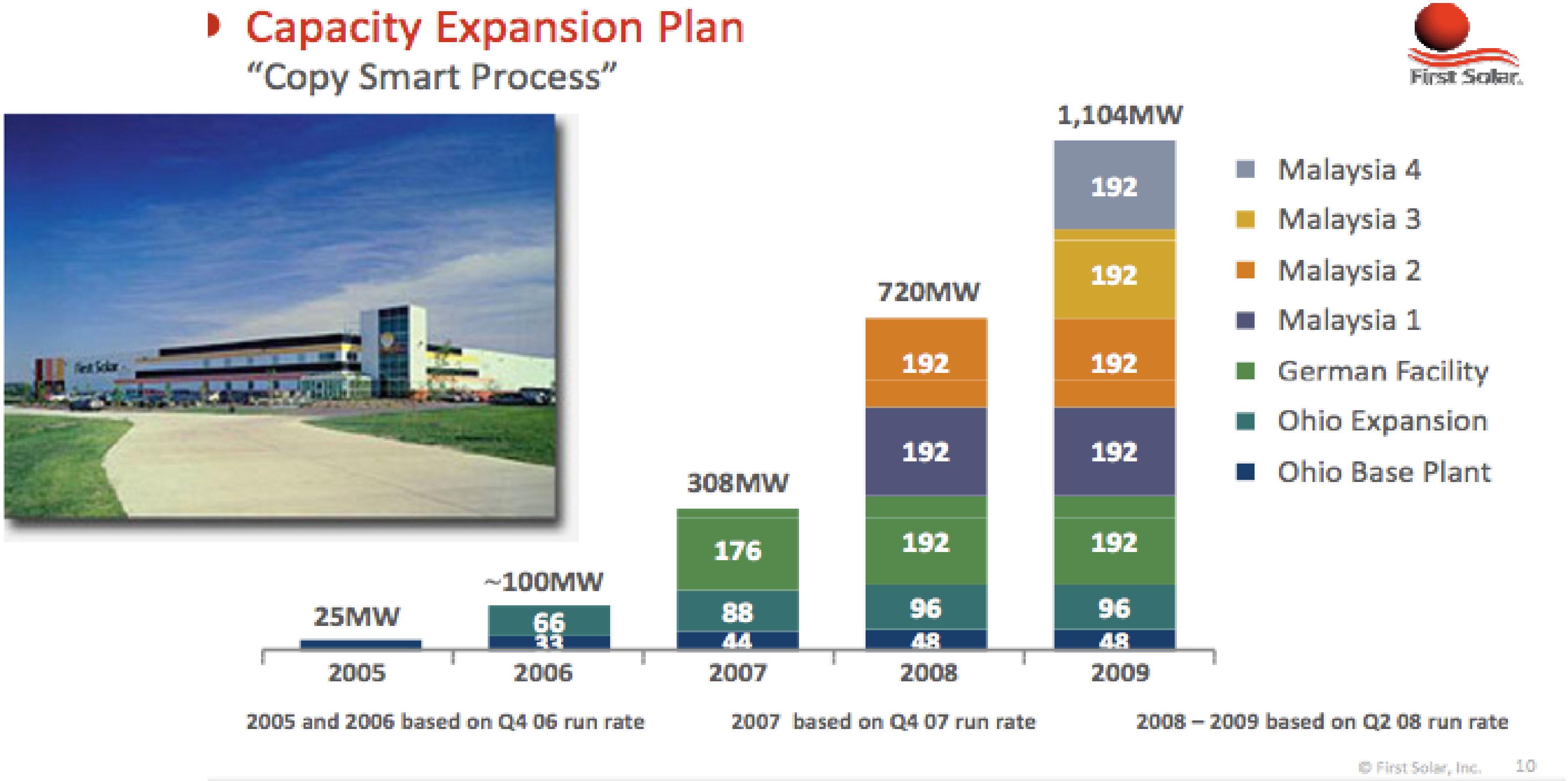
- > 25 year lifetimes desired
- Use environment is highly variable and harsh
- Limited field performance data – the great majority of modules currently under test have not been there long enough to statistically identify failure mechanisms. Thus, no good accelerated lifetime tests (ALTs) available.
- Particularly so for “newer” thin-film technologies
- Existing ALTs primarily optimized for crystalline Silicon products
- Thin-film technologies are constantly evolving – modules under long-term exposure testing no longer representative of current module designs.
- Not just an issue of cost and profit, but also safety. Little known about electrical insulation behavior under 20 years of exposure (fortunately, only real U.S. certification emphasizes safety)

Benefits of improved reliability

- Longer life – lower cost of electricity (each 1% increase in annual degradation increases the levelized cost of electricity (LCOE) ~10%)
- Fewer failures – lower costs associated with system operations & maintenance (O&M)
- Demonstrated reliability – better bankability, lower loan/insurance rates – important since module system installations are expensive
- All of the above will lead to a solar energy (green, sustainable)

Thin-film success – driving the business?

- First Solar – largest thin film company in the world



Capacity Expansion Plan

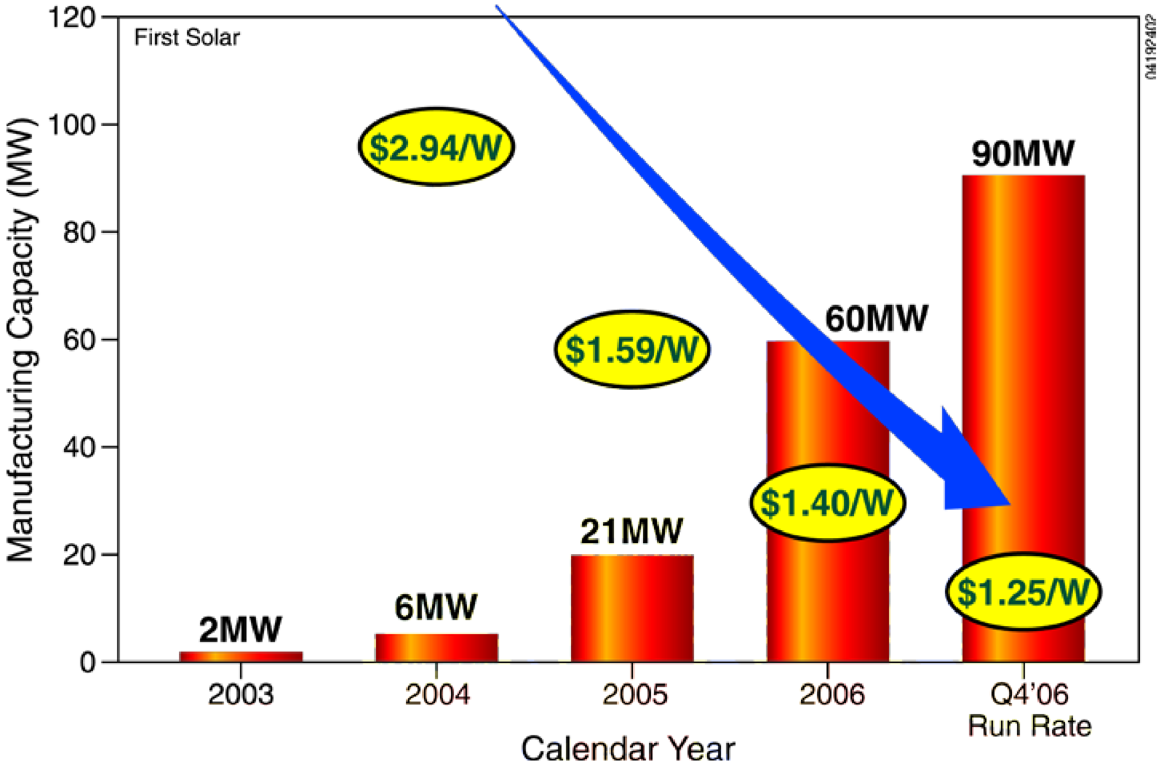
"Copy Smart Process"

2005 and 2006 based on Q4 06 run rate 2007 based on Q4 07 run rate 2008 – 2009 based on Q2 08 run rate

© First Solar, Inc. 10

www.firstsolar.com

Realizing Economies of Scale



Recent data

Year	Capacity (Year End)	Average Mfg Cost
2007	308 MW	$1.23/watt
2008	716 MW	$1.08/watt
2009	1.23 GW	$0.87/watt

www.firstsolar.com

120 MW – Thin Film CdTe Manufacturing–USA

Global Target: 910 MW – 2009

www.firstsolar.com

Similar facility at Abound Solar (formerly AVA Solar) - USA

From Abound Solar brochure

1.8 MW – Thin Film CdTe Solar Roof

First Solar / Juwi Solar

Fast "Large System" Installation – First Solar


Sept 2008

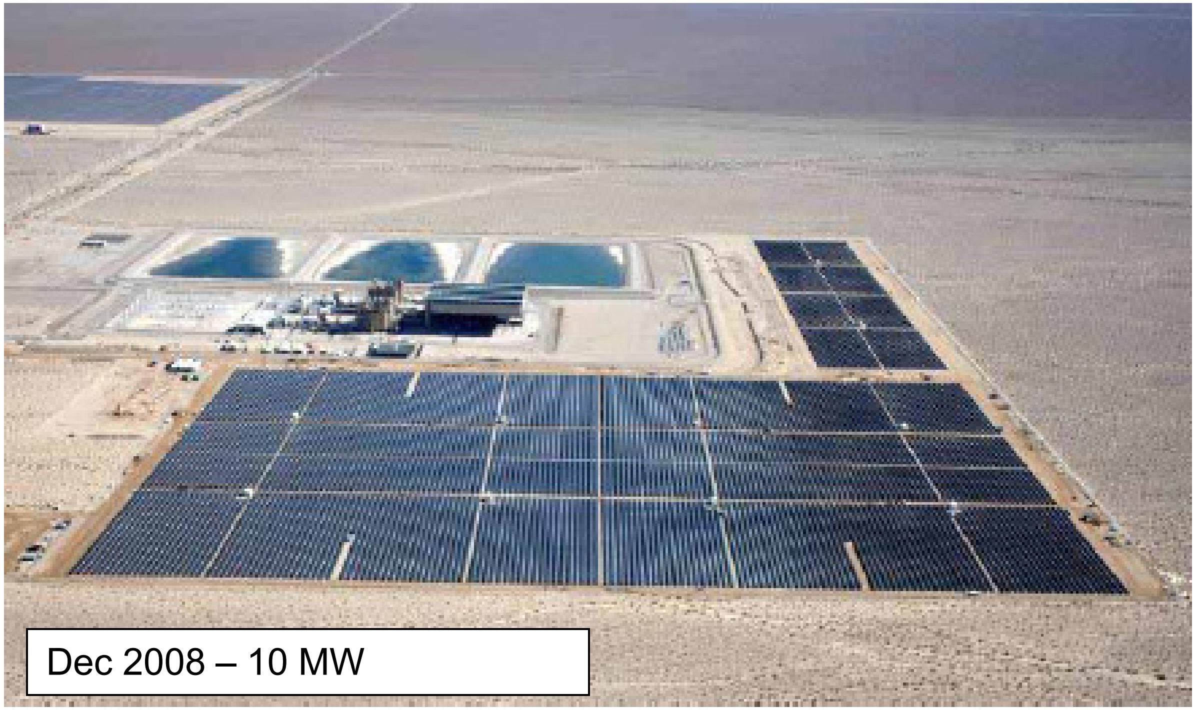

Late Nov 2008

Boulder, NV

10 MW Installed

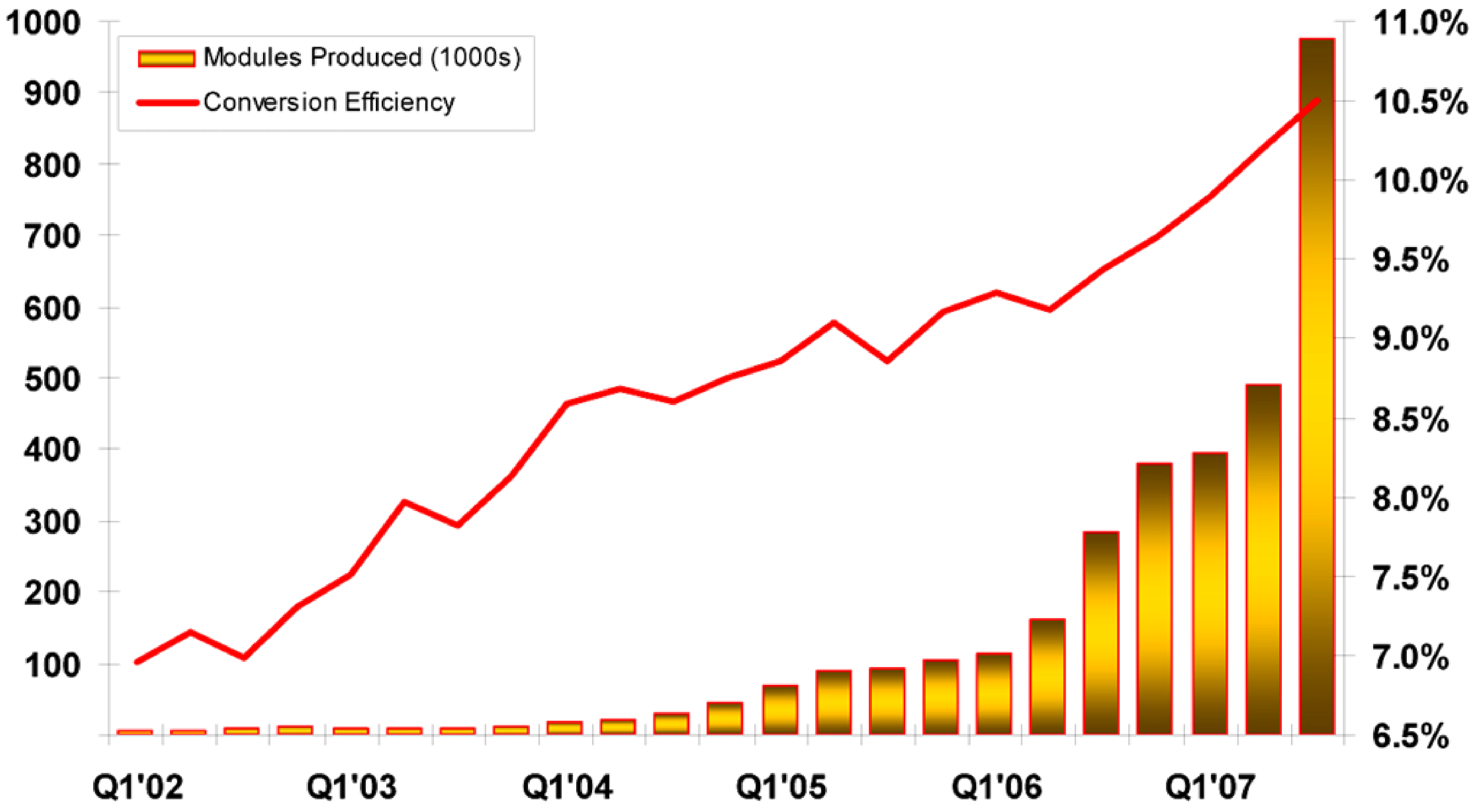

Mid Oct 2008


Early Nov 2008


Dec 2008 – 10 MW

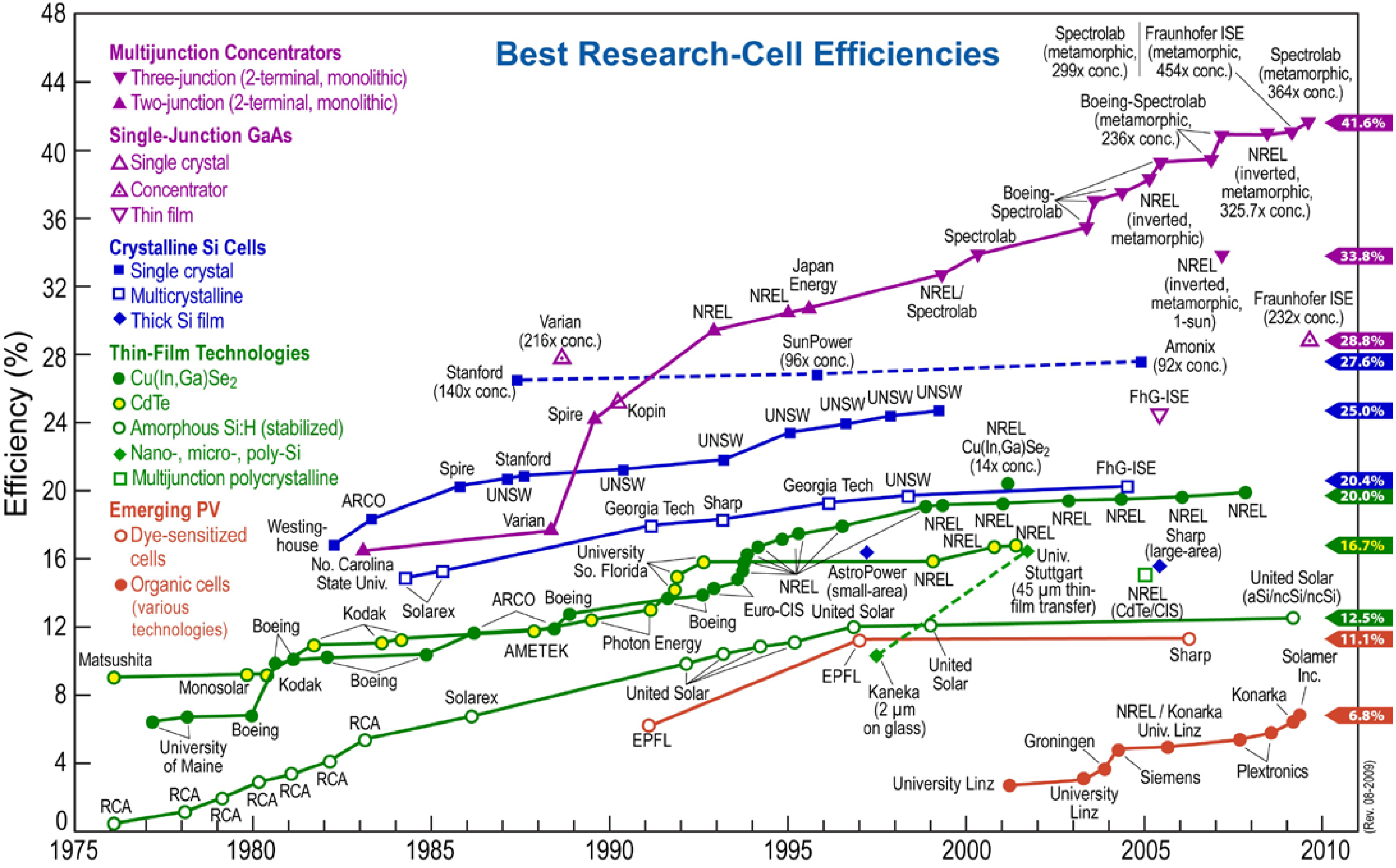
Conversion Efficiencies & Module Shipments

First Solar - Average module efficiency 11.1% (2010/1Q report)

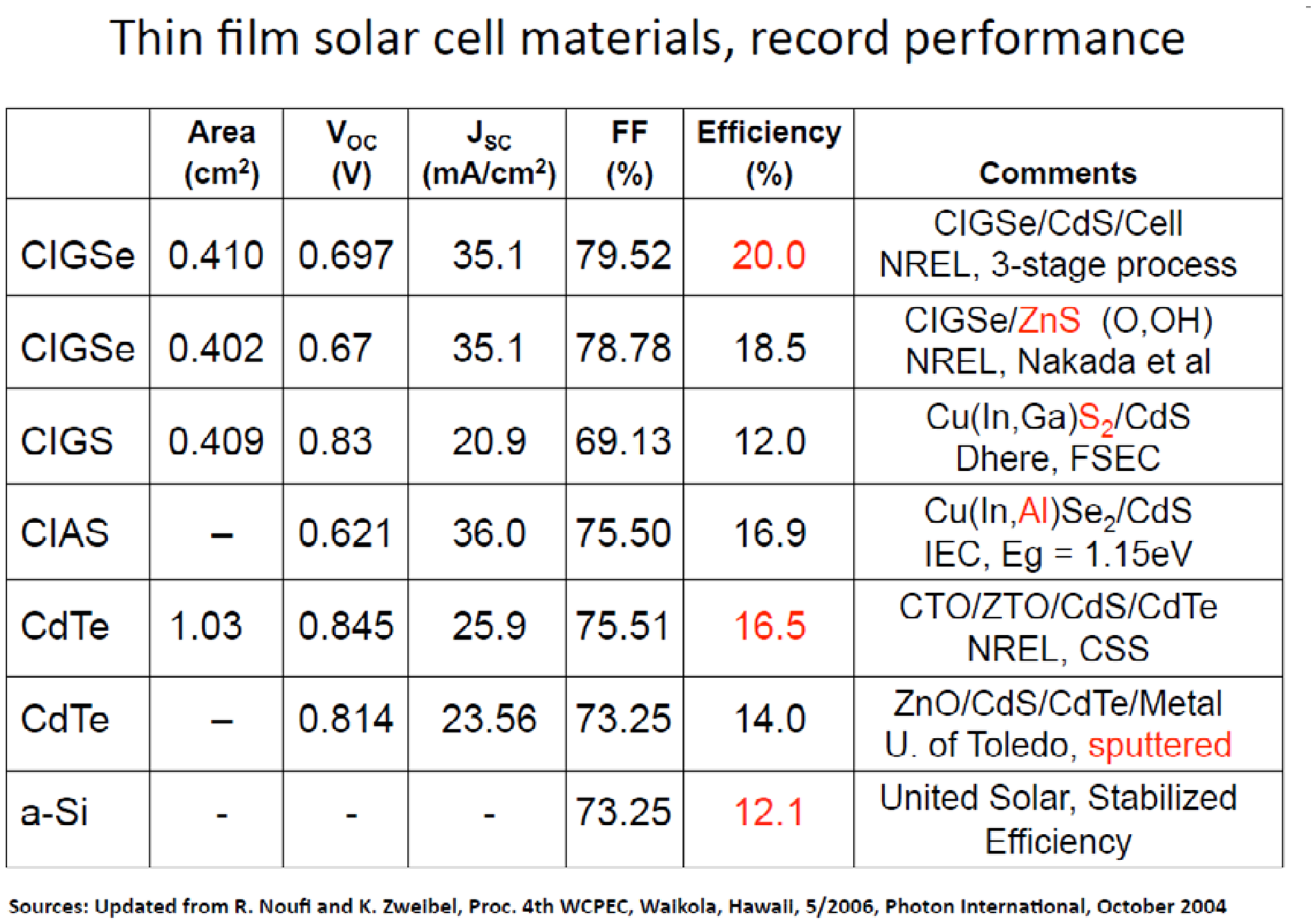


www.firstsolar.com

Many solar energy choices in general – NREL sets upper limit



Thin Film Records

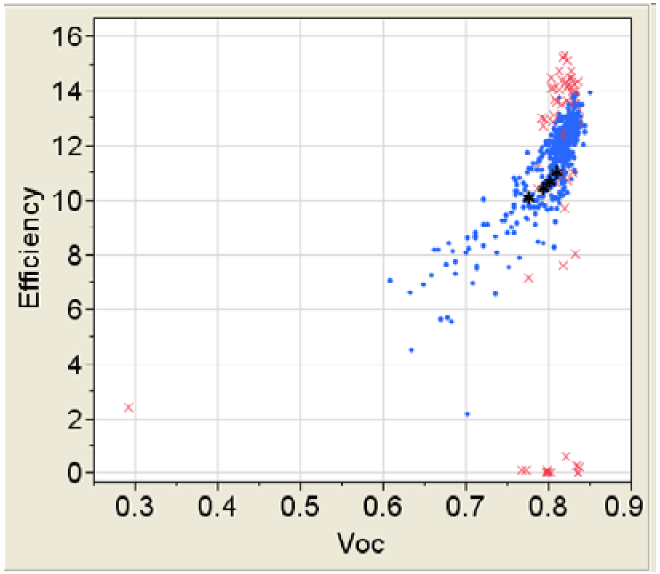


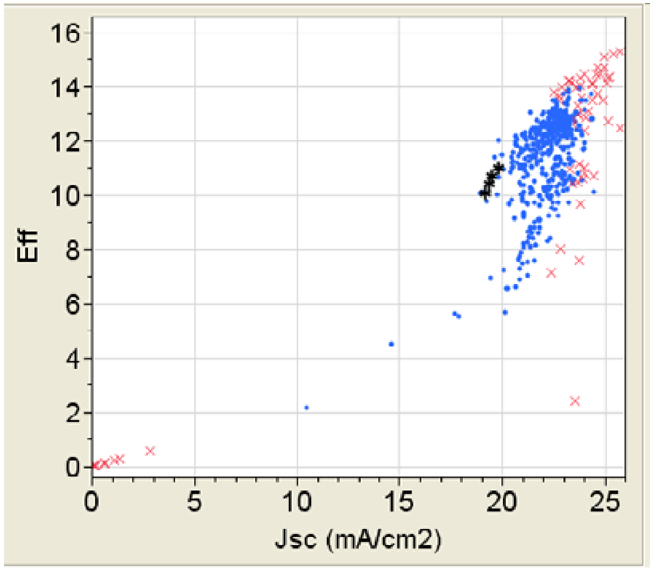
Thin film solar cell materials, record performance

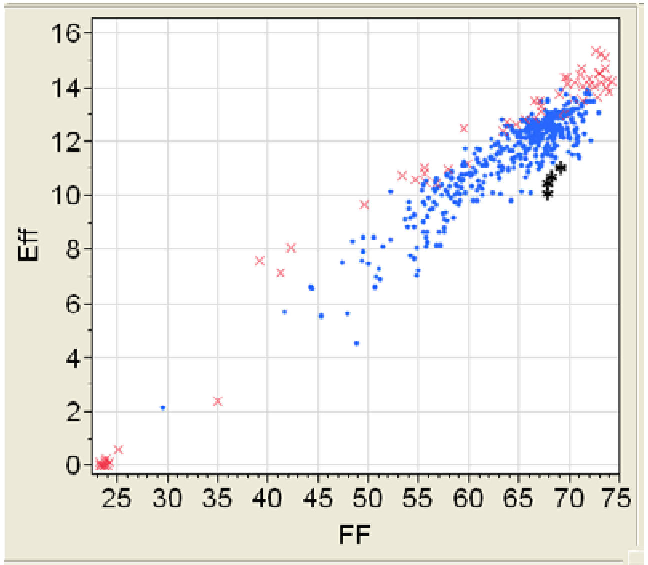
	Area (cm^2)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)	Comments
CIGSe	0.410	0.697	35.1	79.52	20.0	CIGSe/CdS/Cell NREL, 3-stage process
CIGSe	0.402	0.67	35.1	78.78	18.5	CIGSe/ZnS (O,OH) NREL, Nakada et al
CIGS	0.409	0.83	20.9	69.13	12.0	Cu(In,Ga)S_2/CdS Dhere, FSEC
CIAS	–	0.621	36.0	75.50	16.9	Cu(In,Al)Se_2/CdS IEC, Eg = 1.15eV
CdTe	1.03	0.845	25.9	75.51	16.5	CTO/ZTO/CdS/CdTe NREL, CSS
CdTe	–	0.814	23.56	73.25	14.0	ZnO/CdS/CdTe/Metal U. of Toledo, sputtered
a-Si	-	-	-	73.25	12.1	United Solar, Stabilized Efficiency

Sources: Updated from R. Noufi and K. Zweibel, Proc. 4th WCPEC, Waikola, Hawaii, 5/2006, Photon International, October 2004

CdTe still has more top-end potential in manufacturing







● - NREL (Albin) uses TMT SnO_2/7059 glass

X – NREL (Wu/Albin) uses CTO/ZTO advanced window/buffer layers on 7059 glass

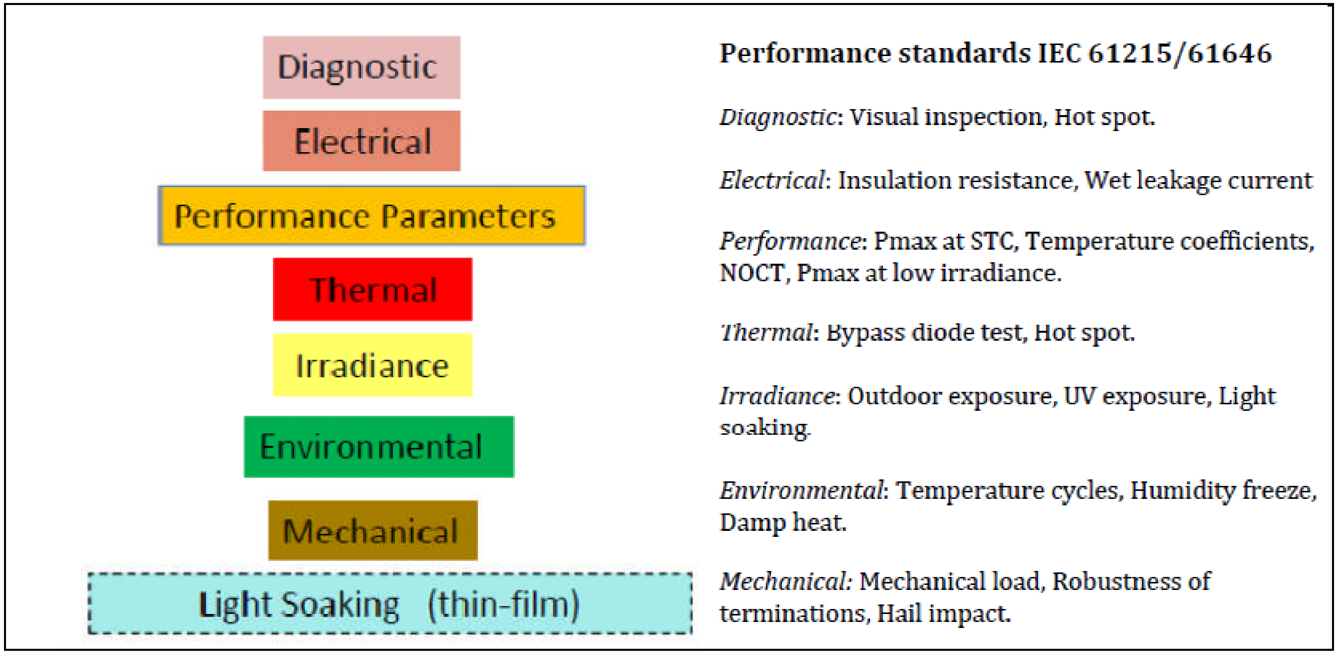
✱ -- based on published First Solar module data (FS 270-273 module data at www.phoenixsolar.com)

World Thin Film PV Capacity (2008-2010)

	Group	Material	Present (MW)	Additional (MW)	Total (MW)	Group	Material	Present (MW)	Additional (MW)	Total (MW)	Totals	Grand Total
USA	**First Solar**	CdTe	135	–	135	AVA Solar	CdTe	–	120	120	1446	6874
	Uni-Solar	a-Si	60	240	300	Nano PV	a-Si	–	4	4		
	MiaSole	CIS	5	50	55	OptiSolar	a-Si	–	40	40		
	Global Solar	CIS	40	100	140	Primestar Solar	CdTe	–	20	50		
	EPV	a-Si	2	25	27	SoloPower	CIS	–	20	20		
	Daystar Technologies	CIS	1	10	11	ISET	CIS	–	3	3		
	Power Film	a-Si	1	10	11	Xunlight	a-Si	3	25	28		
	Ascent Solar	CIS	2	25	27	Heliovolt	CIS	–	20	20		
	Nanosolar	CIS	–	430	430	X Sun X	a-Si	–	25	25		
JAPAN	**Kaneka**	a-Si	20	50	70	**MH1**	a-Si	14	56	70	1312	
	Showa Shell	CIS	20	60	80	**Kanto Sanyo**	a-Si	7	–	7		
	Sharp	a-Si	15	1000	1015	**Honda**	CIS	3	27	30		
	Fuji	a-Si	15	25	40							
EUROPE	**First Solar**	CdTe	160	–	160	Next Solar	a-Si	–	30	30	1206	
	CSG Solar	Thin-Si	10	15	25	AMI	a-Si	–	160	160		
	Wurth Solar	CIS	3	15	18	Johanna Solar Tech	CIS	–	30	30		
	Antec Solar	CdTe	10	–	10	Sonter	a-Si	–	60	60		
	Schott Solar	a-Si	3	27	30	Solisbro	CIS	–	30	30		
	ICP Solar Tech	a-Si	3	–	3	Global Solar	CIS	–	35	35		
	Solar Cells	a-Si	1	–	1	Helio Grid	a-Si	–	50	50		
	Free Energy	a-Si	1	–	1	SunFilm	a-Si	–	60	60		
	Solar Plus	a-Si	–	5	5	T. J. Solar	a-Si	–	40	40		
	Sulfur Cells	CIS	5	–	5	**Signet Solar**	a-Si	–	20	20		
	Aleo Solar	CIS	–	30	30	Clyxo	CdTe	–	60	60		
	Ersol	a-Si	–	40	40	**Avancis**	CIS	–	20	20		
	Inventux	a-Si	–	33	33	Odersun	CIS	–	30	30		
	Solarion	CIS	–	25	25	Scheuten Solar	CIS	–	10	10		
	Pramac	a-Si	–	30	30	EPV	a-Si	–	25	25		
	Corupo Uni Solar	a-Si	–	5	5	Avendi	CdTe	–	15	15		
	Masdar	a-Si	–	110	110							
OTHER	**First Solar**	CdTe	–	704	704	GET	a-Si	–	40	40	2910	
	Bangkok Solar	a-Si	7	–	7	Nanowin Tech	a-Si	–	35	35		
	Sinonar	a-Si	15	35	50	Moser Baer	a-Si	–	20	20		
	T. J. Solar Cell	a-Si	2	–	2	Solar Morph	a-Si	–	20	20		
	Soltech	a-Si	15	–	15	Topray Solar	a-Si	20	–	20		
	Suntech Power	a-Si	–	50	50	Sun Well Tech	a-Si	–	60	60		
	Weihai BTP	a-Si	5	5	10	Sunner Solar	a-Si	–	25	25		
	Nex Power	a-Si	–	50	50	Auria	a-Si	–	60	60		
	CSP	a-Si	–	50	50	HHV	a-Si	–	6	6		
	Aleo Solar	CIGS	–	50	50	Kenmos PV	a-Si	–	5	5		
	Sunvim	CIGS	–	30	30	QS Solar	a-Si	–	25	25		
	BESA	a-Si	–	40	40	Formosun Tech	a-Si	–	15	15		
	C G Solar	a-Si	–	100	100	Mosel Vitelic	a-Si	–	20	20		
	Masdar	a-Si	–	100	100	ASP	CdTe	–	25	25		
	Best Solar	a-Si	–	1000	1000	Baoding Tianwei	a-Si	–	46	46		
	CSF Solar	a-Si	–	150	150							
	China Singyes	a-Si	–	100	100							

Module Qualification and Testing

PV Qualification Testing



Diagnostic

Electrical

Performance Parameters

Thermal

Irradiance

Environmental

Mechanical

Light Soaking (thin-film)

Performance standards IEC 61215/61646

Diagnostic: Visual inspection, Hot spot.

Electrical: Insulation resistance, Wet leakage current

Performance: Pmax at STC, Temperature coefficients, NOCT, Pmax at low irradiance.

Thermal: Bypass diode test, Hot spot.

Irradiance: Outdoor exposure, UV exposure, Light soaking.

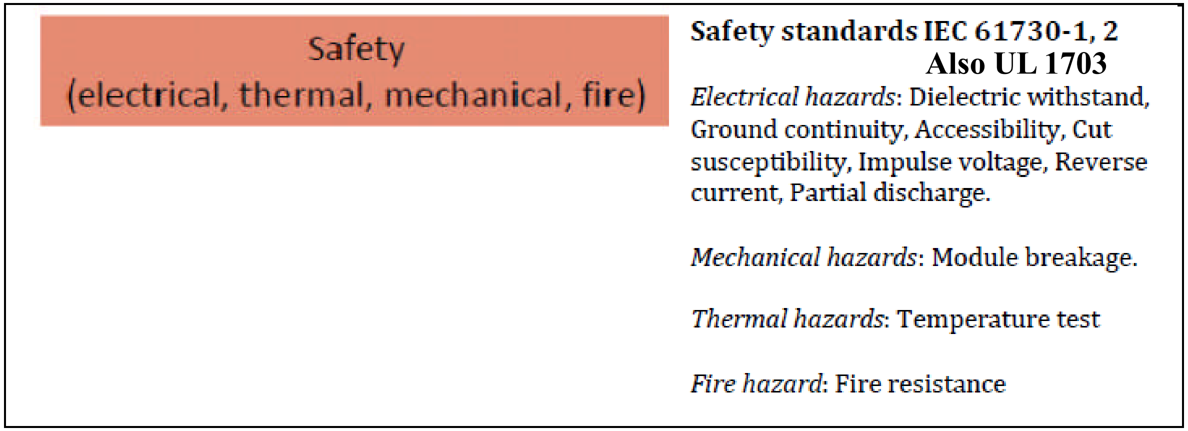
Environmental: Temperature cycles, Humidity freeze, Damp heat.

Mechanical: Mechanical load, Robustness of terminations, Hail impact.

Not Accelerated Lifetime Testing (ALT)!!

(really used to qualify the module design)

http://www.tuvamerica.com/services/photovoltaics/ArticleBasicUnderstandingPV.pdf



Safety
(electrical, thermal, mechanical, fire)

Safety standards IEC 61730-1, 2
Also UL 1703

Electrical hazards: Dielectric withstand, Ground continuity, Accessibility, Cut susceptibility, Impulse voltage, Reverse current, Partial discharge.

Mechanical hazards: Module breakage.

Thermal hazards: Temperature test

Fire hazard: Fire resistance

PV Qualification Testing – qualifies the module *design*

IEC 61215 (crystalline silicon)

Major elements:

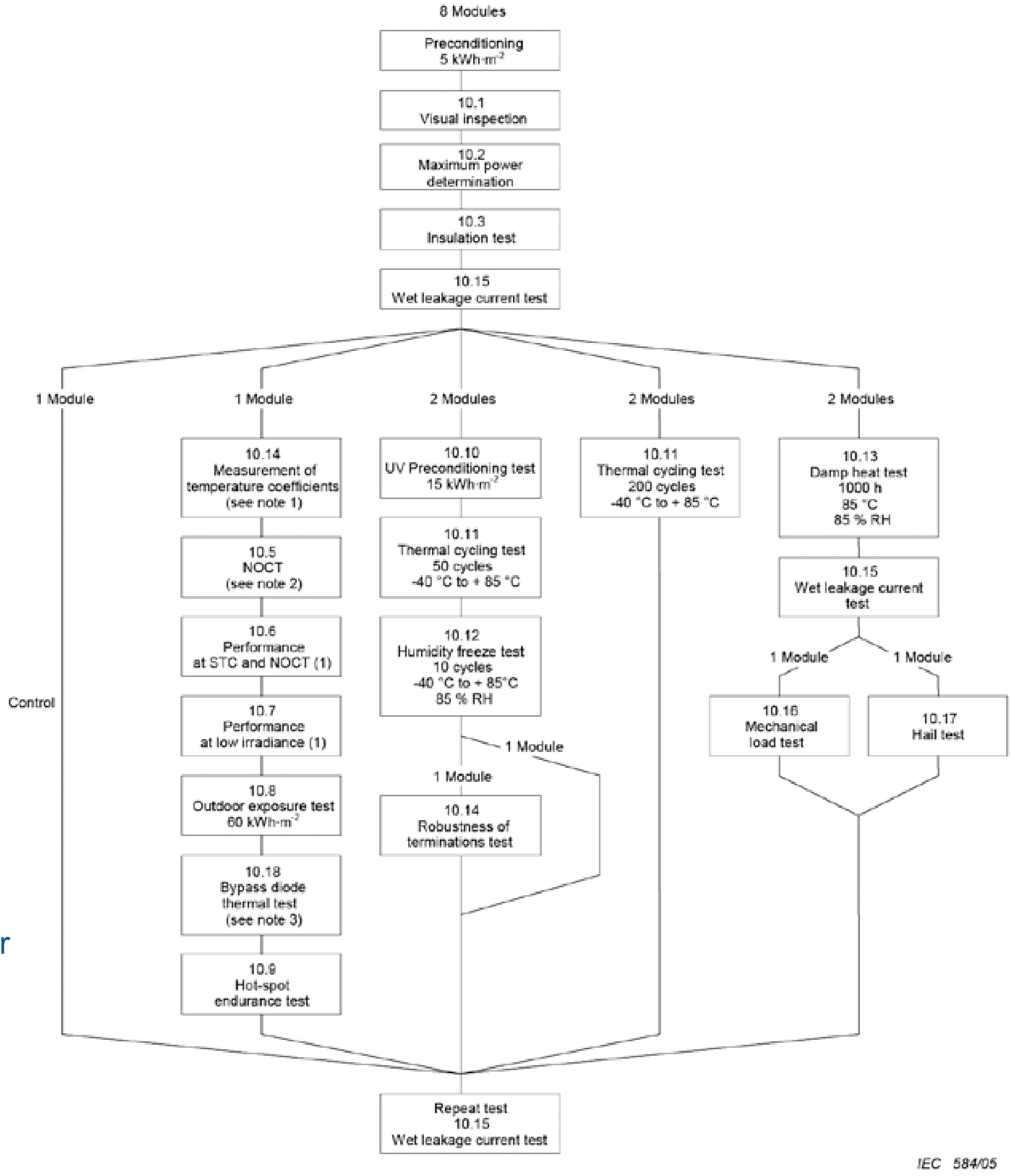
- UV exposure
- Thermal cycling
- Humidity Freeze
- Damp Heat
- Outdoor Exposure
- Wet/dry Hi-potential test

Pass Criteria

- Steps 10.1-10.3 met
- <5%/step or <8%/step sequence

IEC 61646 (thin films)

- Similar legs
- Additional features
  - Removes Pre-conditioning requirement
  - Light-soaking and Annealing to allow for "recovery"
  - Max Power after final light-soak>90% rated value (no 5%/8% step criteria)
  - If ≥ 2 modules fail; design fails

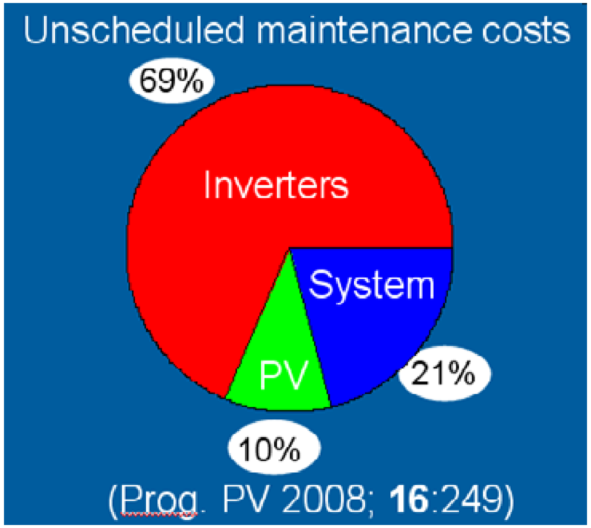


History of Si module qualification test:
JPL (Jet Propulsion Lab) Block buys

Test	I	II	III	IV	V
Year	1975	1976	1977	1978	1981
Thermal Cycle (° C)	100 cycles -40 to +90	50 cycles -40 to +90	50 cycles -40 to +90	50 cycles -40 to +90	200 cycles -40 to +90
Humidity	70 C, 90%RH, 68 hr	5 cycles 40 C, 90%RH to 23 C	5 cycles 40 C, 90%RH to 23 C	5 cycles 54 C, 90%RH to 23 C	10 cycles 85 C, 85%RH to -40 C
Hot spots	-	-	-	-	3 cells, 100 hrs
Mechanical load	-	100 cycles ± 2400 Pa	100 cycles ± 2400 Pa	10000 cyc. ± 2400 P	10000 cyc. ± 2400 Pa
Hail	-	-	-	9 impacts 3/4” - 45 mph	10 impacts 1” - 52 mph
NOCT	-	-	-	Yes	Yes
High pot	-	< 15 µA 1500 V	< 50 µA 1500 V	< 50 µA 1500 V	< 50 µA 2*Vs+1000

JPL Block buys led to dramatic improvements

- One study claimed (Whipple, 1993):
  - Pre-Block V: 45% module failure rate
  - Post-Block V: <0.1% module failure rate
- Studies of c-Si modules show that module failures are small (inverters dominate when cost is low)



Failures from improper installation, lightning strikes, critters, etc., dominate the statistics for many c-Si installations today

Today's qualification standards are similar

IEC 61215 - Crystalline silicon design qualification includes 18 test procedures

- Thermal cycling - 200 cycles -40°C to +85°C
- Humidity freeze - 10 cycles +85°C, 85% RH to -40°C
- Damp heat - 1000 hrs at +85°C, 85% RH
- Wet leakage current - Wet insulation resistance X area > 40 MΩm^2 at 500 V or system voltage
- Requirement is typically to retain 95% of original power production

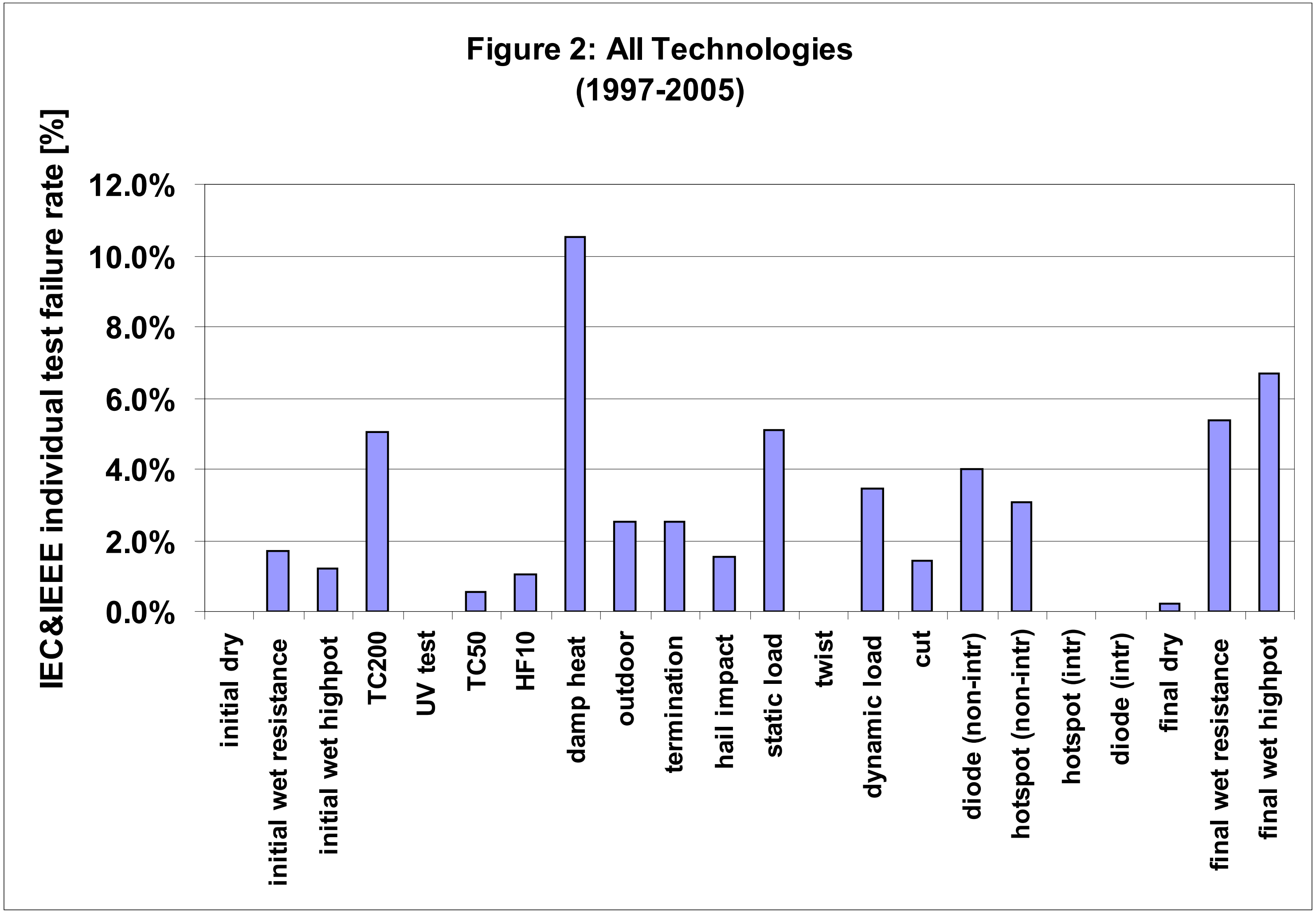
IEC 61646 (thin film) and IEC62108 (CPV) are similar

But again, most of the development of these qualification tests were originally intended for crystalline silicon

Review: Osterwald & McMahon, Progress in PV **17**, p11 (2009)

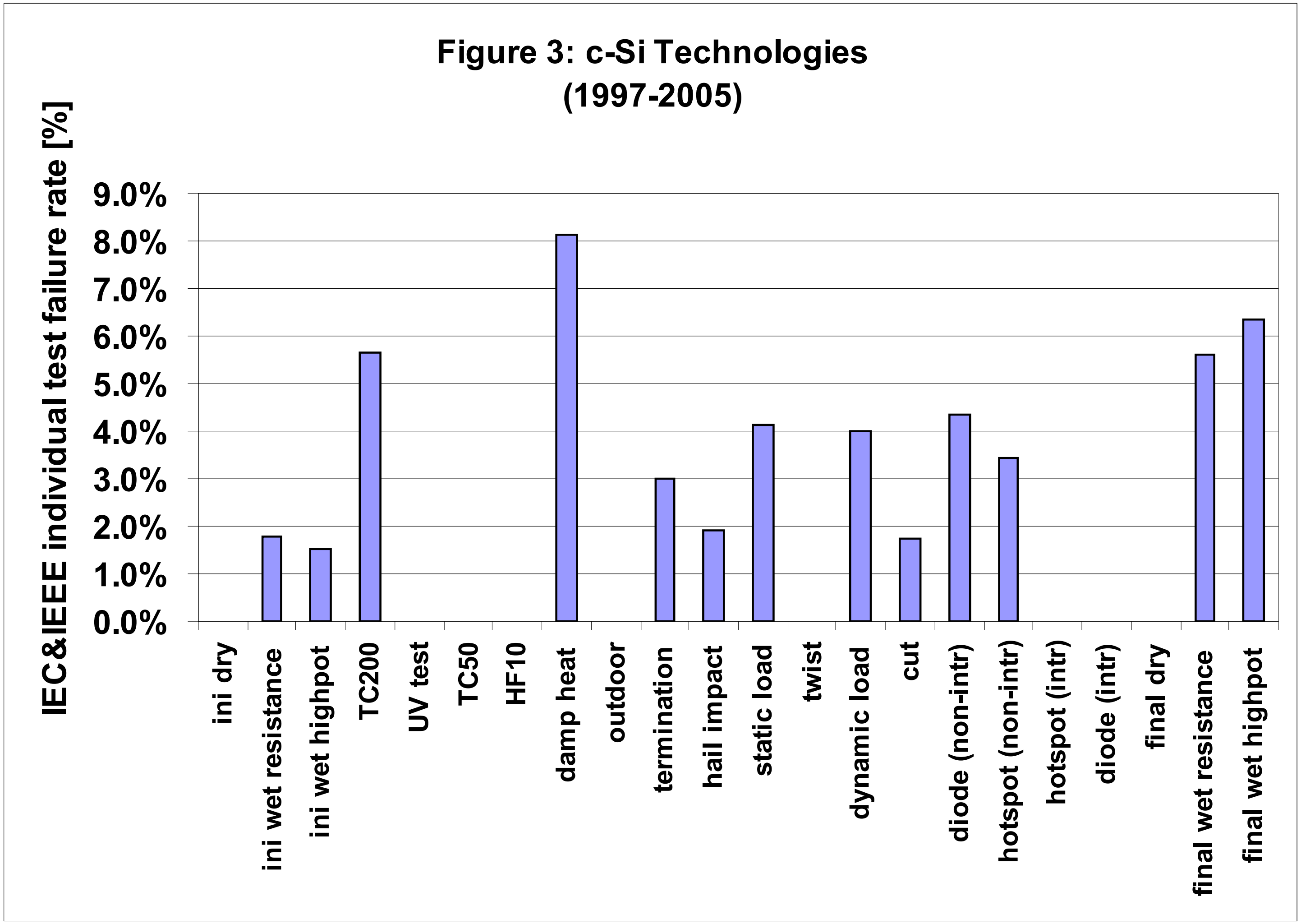
From ASU – TUV Rheinland – Mani G. Tamizh-Mani

All technologies: The stress test with largest failure rate was the damp heat test followed by TC200, static load and diode tests.



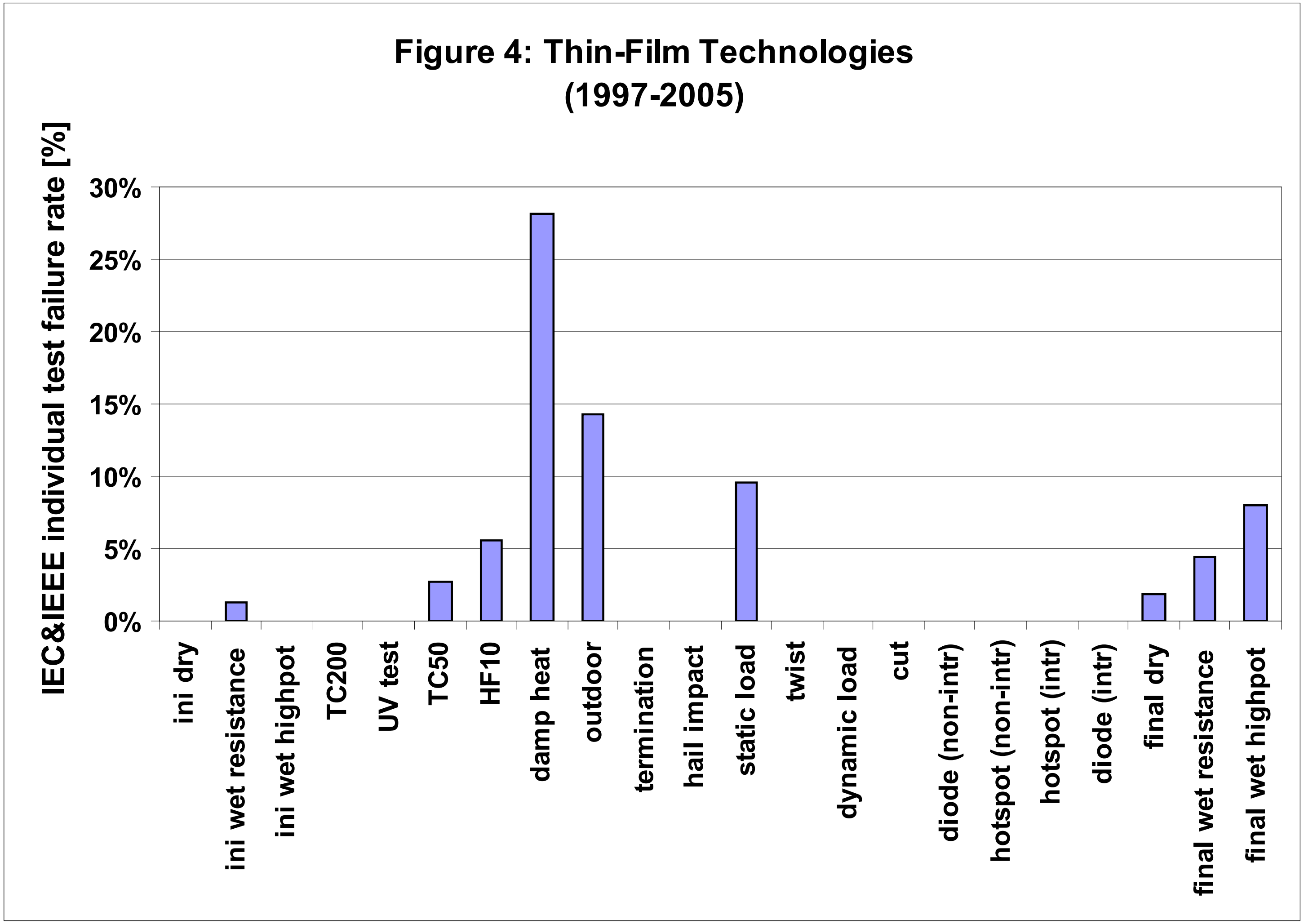
From ASU – TUV Rheinland – Mani G. Tamizh-Mani

c-Si technologies: The stress test with largest failure rate was the damp heat test (8.1%) followed by TC200 (5.6%), diode (4.3%) and static load (4.1%) tests.

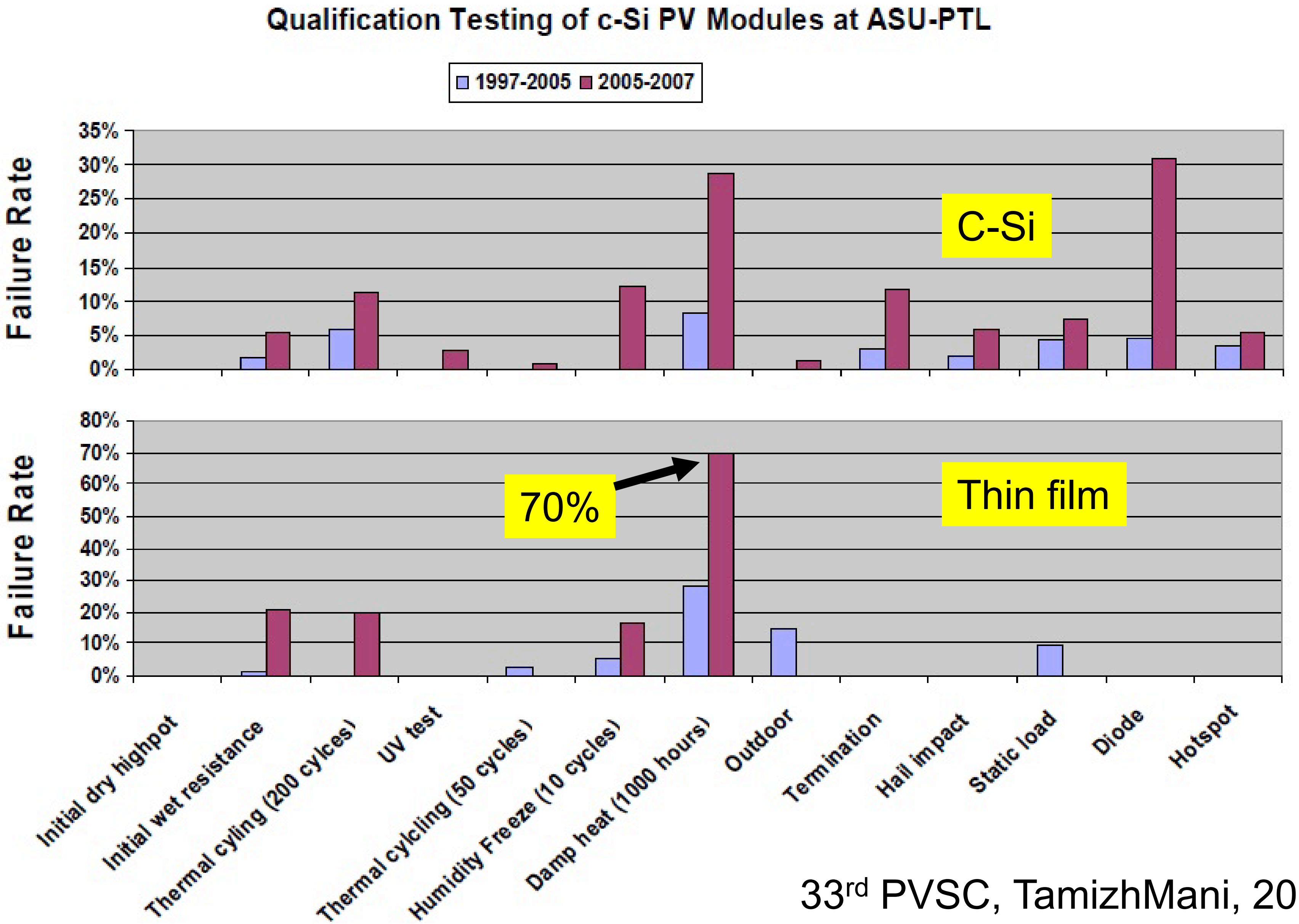


From ASU – TUV Rheinland – Mani G. Tamizh-Mani

Thin-film technologies: The stress test with largest failure rate was the damp heat test (28.1%) followed by outdoor (14.3%), static load (9.5%) and HF10 (5.6%) tests.



Past success does not guarantee future success



33rd PVSC, TamizhMani, 2008

Failure Mechanisms are being identified in Thin-Films

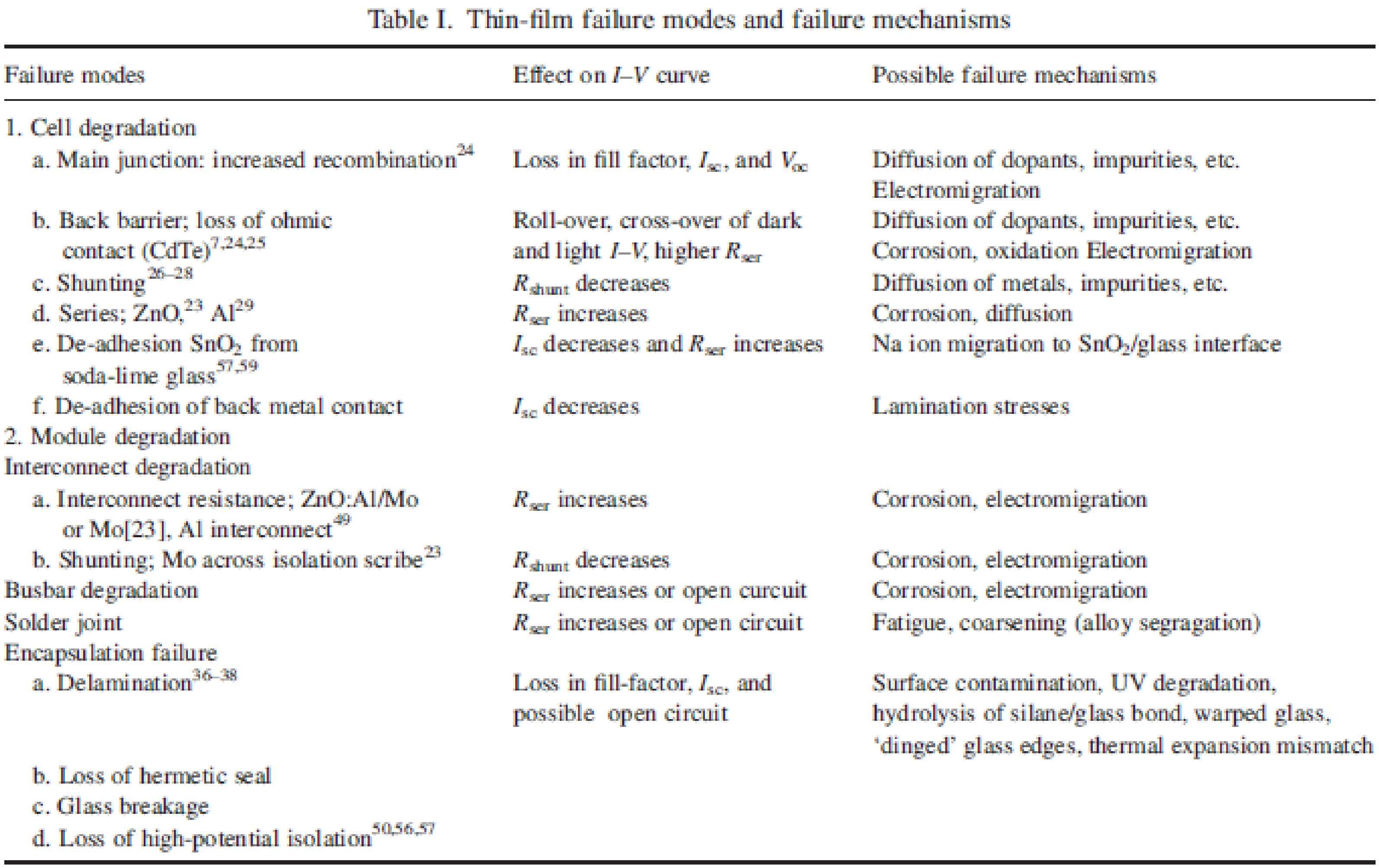
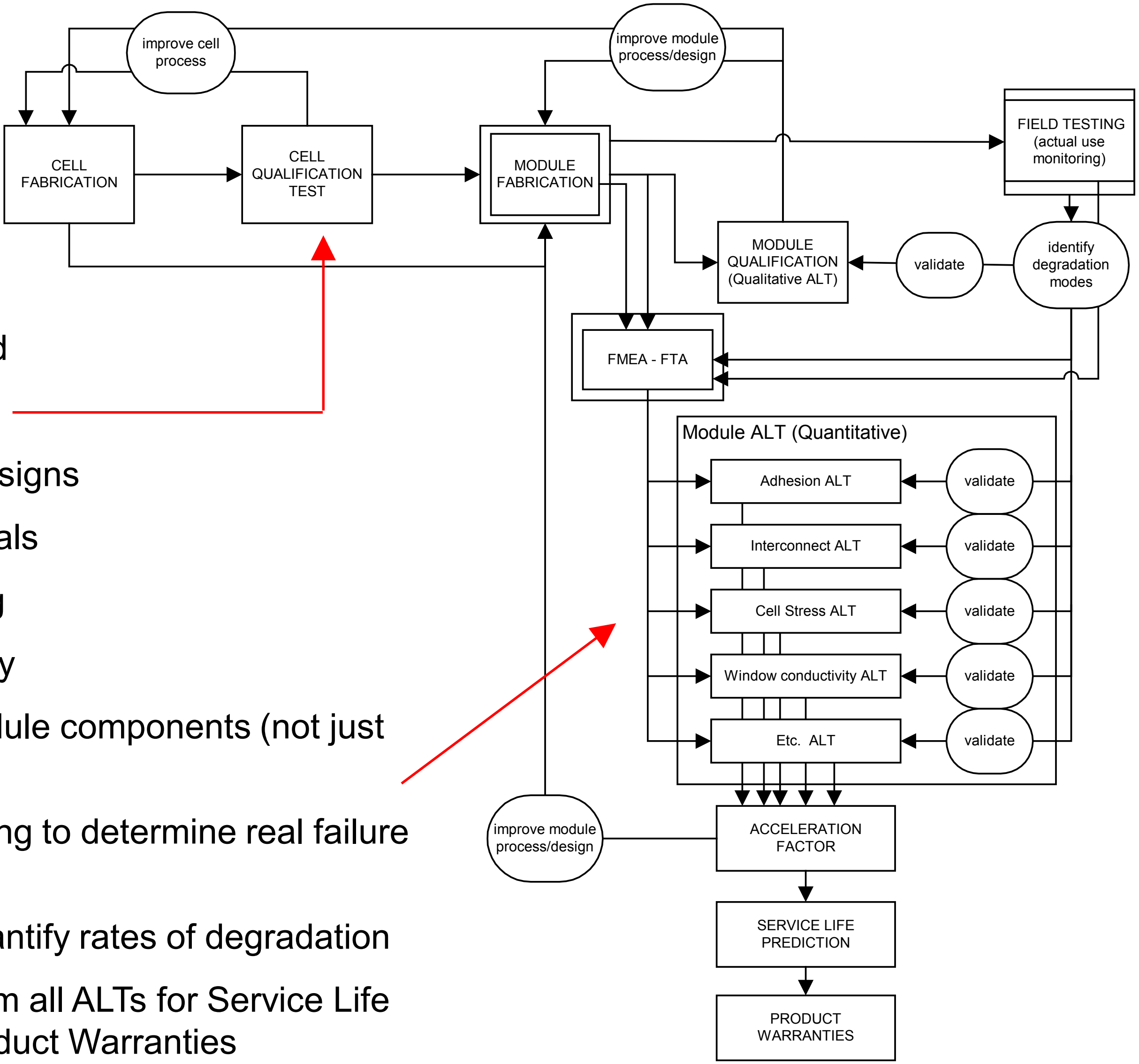


Table I. Thin-film failure modes and failure mechanisms

Failure modes	Effect on I–V curve	Possible failure mechanisms
1. Cell degradation		
a. Main junction: increased recombination[24]	Loss in fill factor, I_{sc}, and V_{oc}	Diffusion of dopants, impurities, etc. Electromigration
b. Back barrier; loss of ohmic contact (CdTe)[7,24,25]	Roll-over, cross-over of dark and light I–V, higher R_{ser}	Diffusion of dopants, impurities, etc. Corrosion, oxidation Electromigration
c. Shunting[26–28]	R_{shunt} decreases	Diffusion of metals, impurities, etc.
d. Series; ZnO,[23] Al[29]	R_{ser} increases	Corrosion, diffusion
e. De-adhesion SnO_2 from soda-lime glass[57,59]	I_{sc} decreases and R_{ser} increases	Na ion migration to SnO_2/glass interface
f. De-adhesion of back metal contact	I_{sc} decreases	Lamination stresses
2. Module degradation		
Interconnect degradation		
a. Interconnect resistance; ZnO:Al/Mo or Mo[23], Al interconnect[49]	R_{ser} increases	Corrosion, electromigration
b. Shunting; Mo across isolation scribe[23]	R_{shunt} decreases	Corrosion, electromigration
Busbar degradation	R_{ser} increases or open curcuit	Corrosion, electromigration
Solder joint	R_{ser} increases or open circuit	Fatigue, coarsening (alloy segragation)
Encapsulation failure		
a. Delamination[36–38]	Loss in fill-factor, I_{sc}, and possible open circuit	Surface contamination, UV degradation, hydrolysis of silane/glass bond, warped glass, 'dinged' glass edges, thermal expansion mismatch
b. Loss of hermetic seal		
c. Glass breakage		
d. Loss of high-potential isolation[50,56,57]		

T.J. McMahon, Prog. Photovolt: Res. Appl., 12:235-248 (2004)

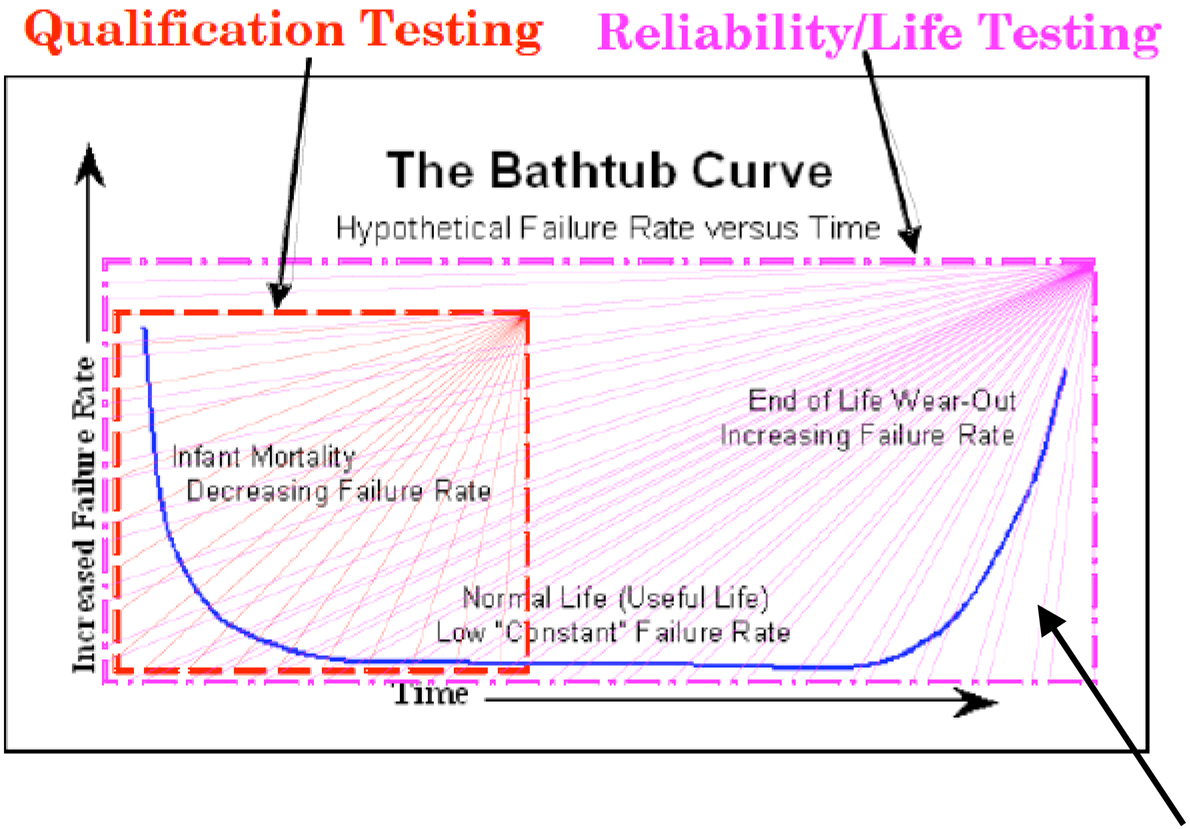
Cell Durability a Key Component in Module Reliability



Cell Testing in a “Module” world

1. Increase Cell Durability
   - Test different cell designs
   - Test different materials
   - Optimize processing
2. Increase Module Reliability
   1. Incorporates all module components (not just cells)
   2. Requires Field Testing to determine real failure mechanisms
   3. Develop ALTs to quantify rates of degradation
   4. Combine results from all ALTs for Service Life Predictions and Product Warranties

A final reminder: Qualification Testing is not Reliability Testing

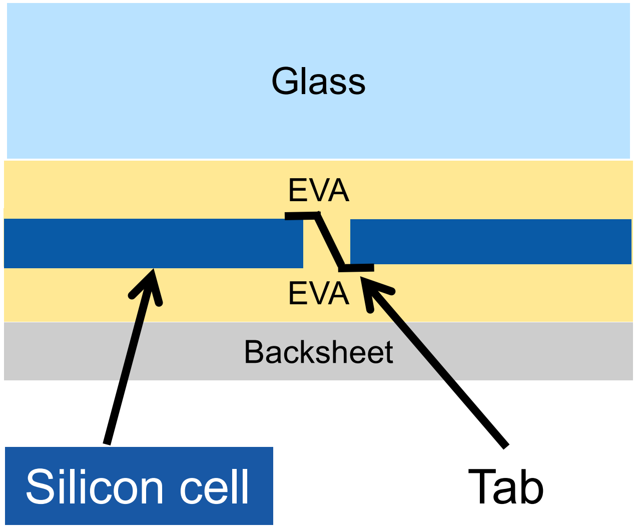


One approach to perform “Reliability Testing” is to use longer times during Qualification Test procedures (i.e., test-to-failure)

Module & Cell Designs

Silicon modules

Si module cross section



Cells are “bulk” materials and less sensitive to cell degradation

Thin-film approaches on the market

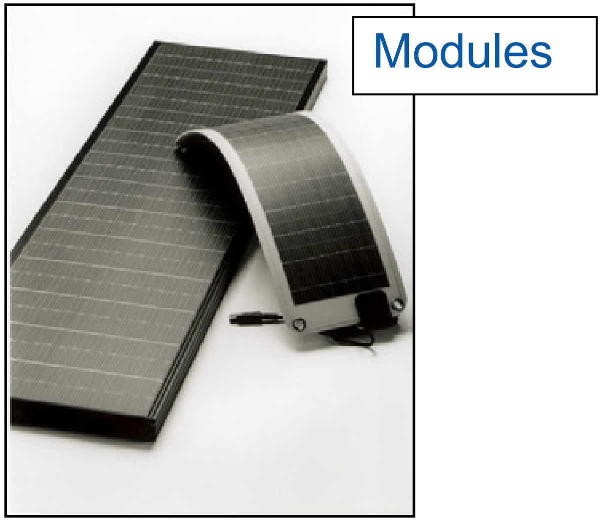
CuIn(Ga)Se

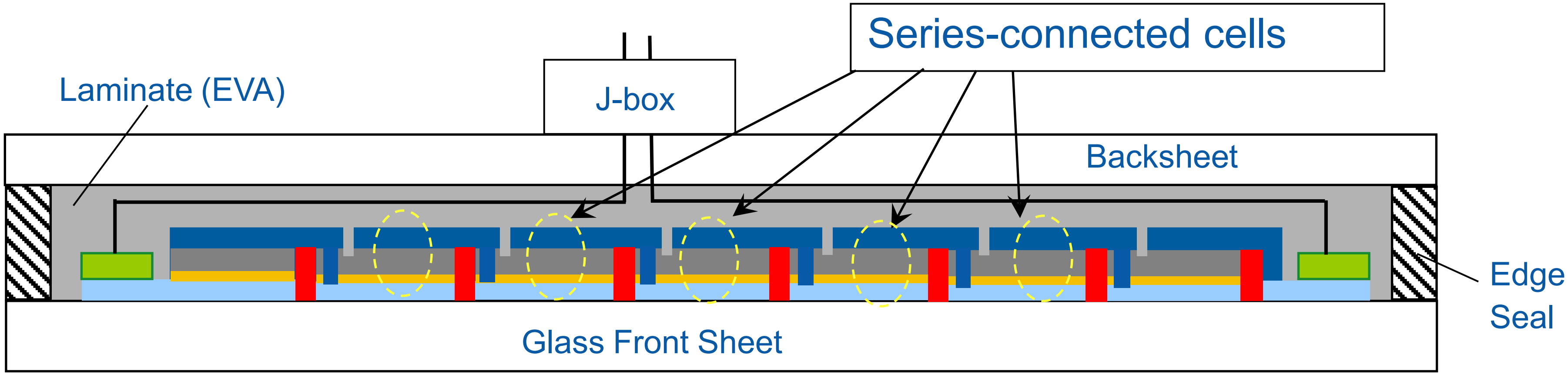
CdTe

Amorphous silicon

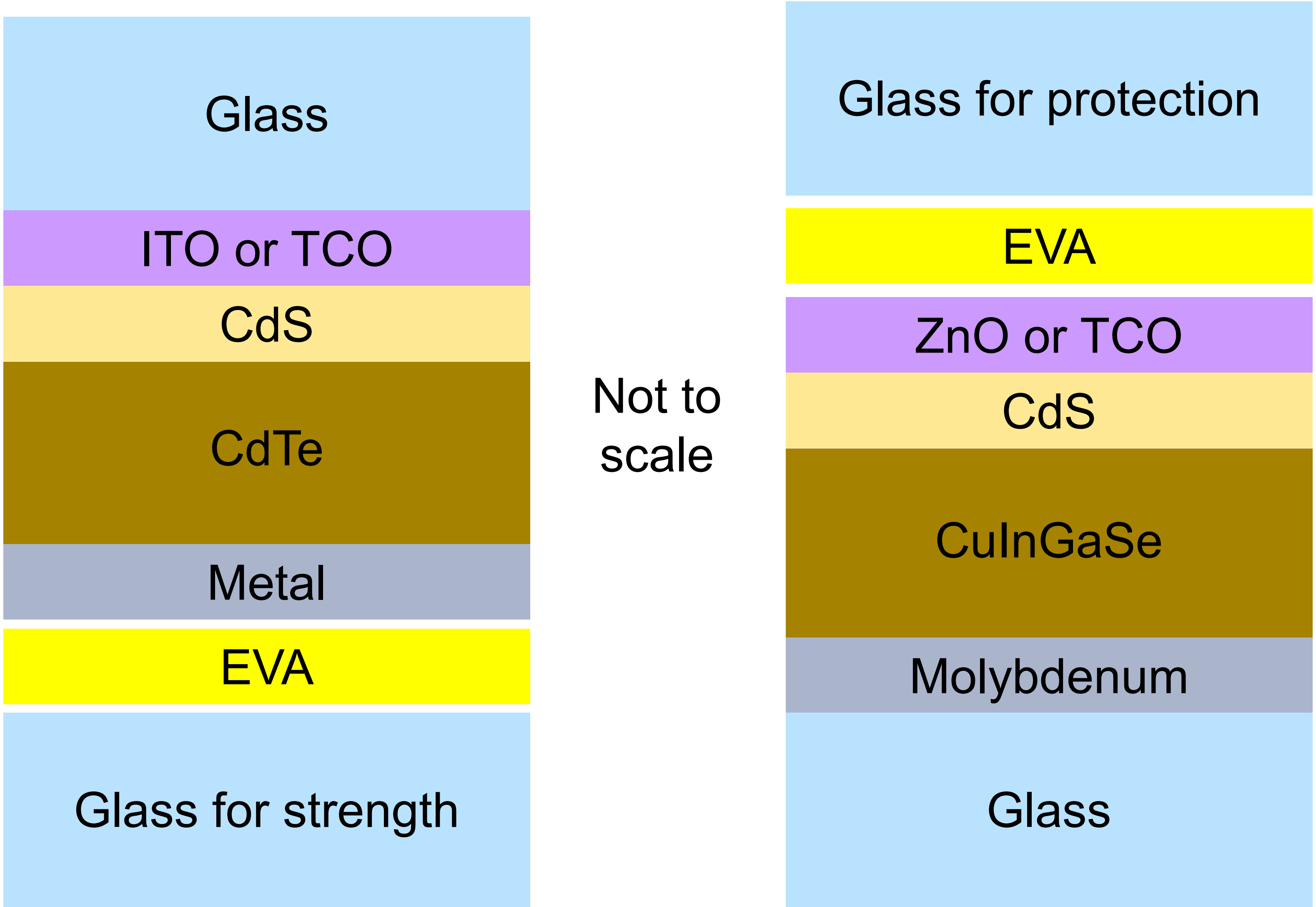
Thin film cells are very thin (< 5 µm) and susceptible to degradation

Cell stability fundamental to module reliability





Typical thin-film structures



CdTe uses superstrate

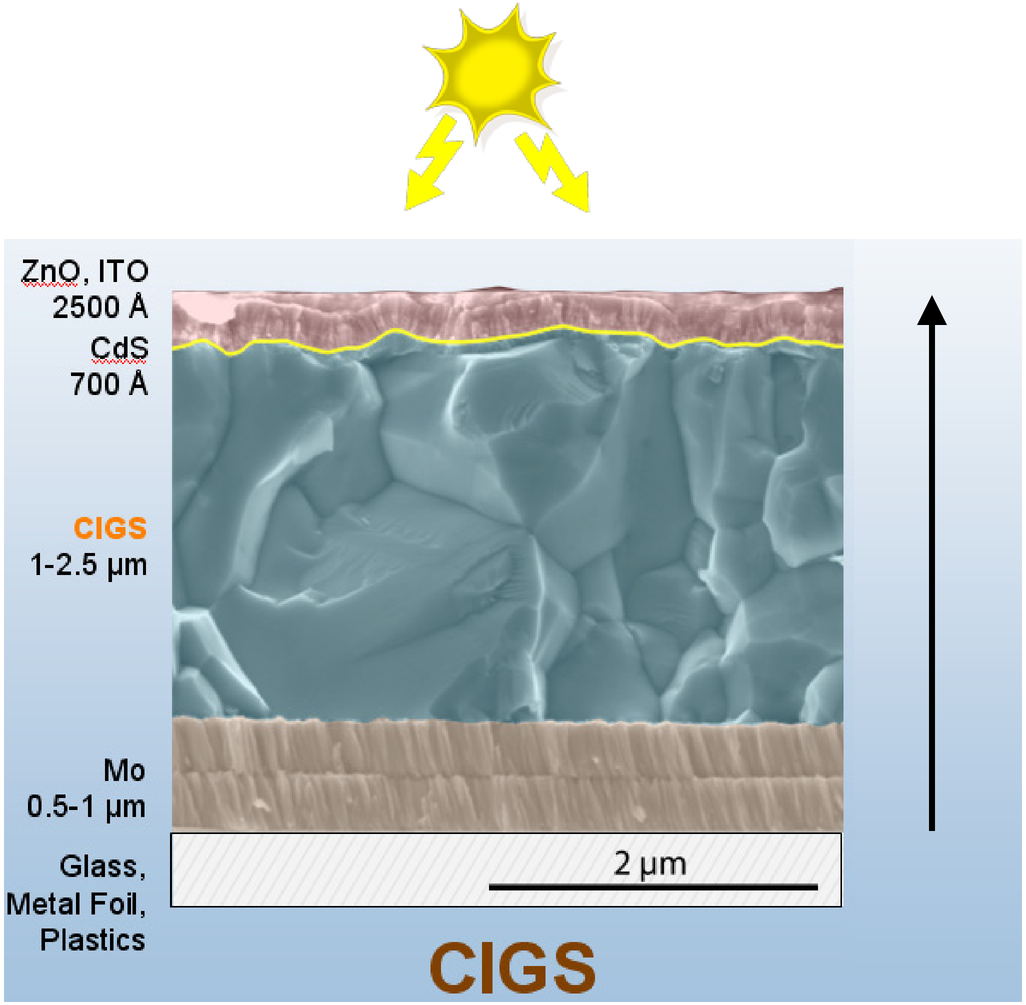
Glass
ITO or TCO
CdS
CdTe
Metal
EVA
Glass for strength

Not to scale

$CuInGaSe_2$ uses substrate

Glass for protection
EVA
ZnO or TCO
CdS
CuInGaSe
Molybdenum
Glass

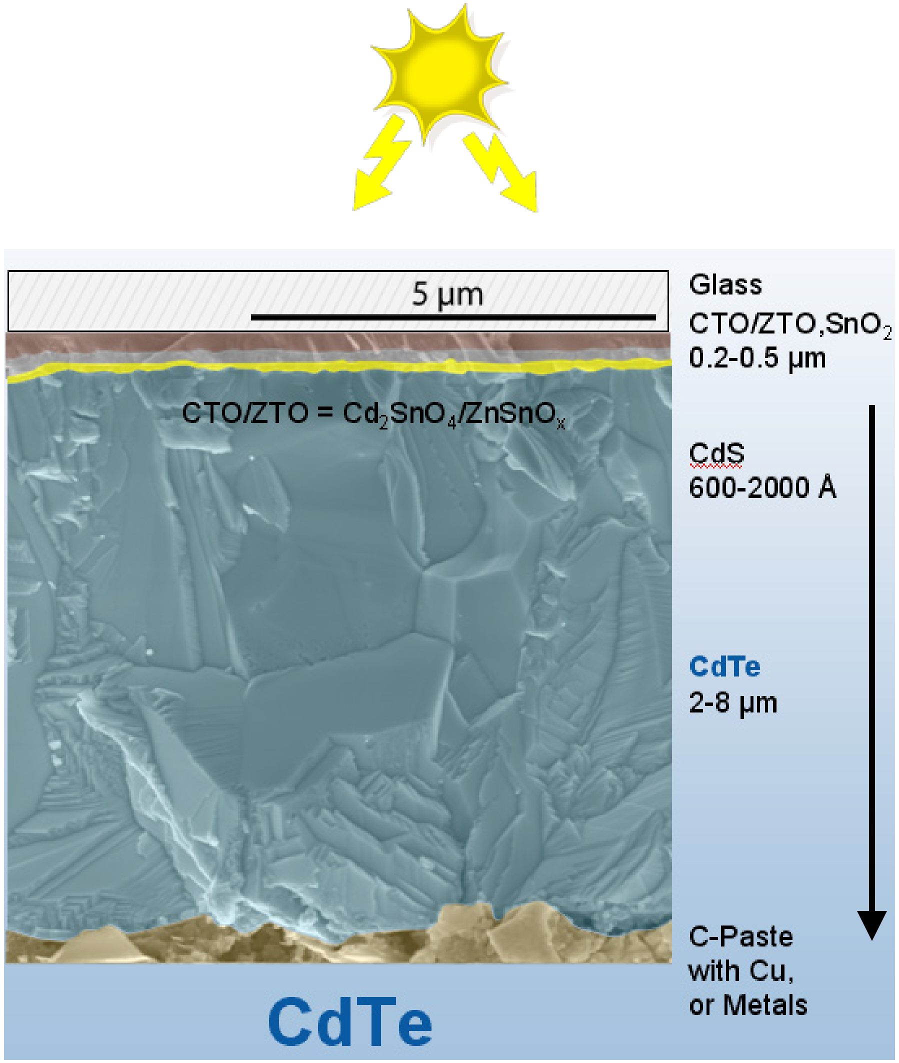
CIGS (substrate) vs CdTe (superstrate)



CIGS is a substrate design

1. Deposit Mo backcontact on substrate (metal foil, glass)
2. Deposit p-type CIGS layer
3. Deposit n-type CdS
4. Deposit TCO (ZnO)

CIGS (substrate) vs CdTe (superstrate)

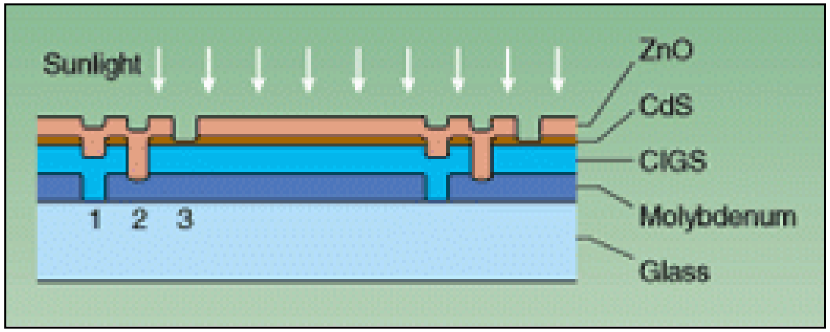


CdTe is a “superstrate” design

1. Deposit TCO on glass substrate
2. Deposit n-CdS
3. Deposit p-CdTe
4. Deposit backcontact

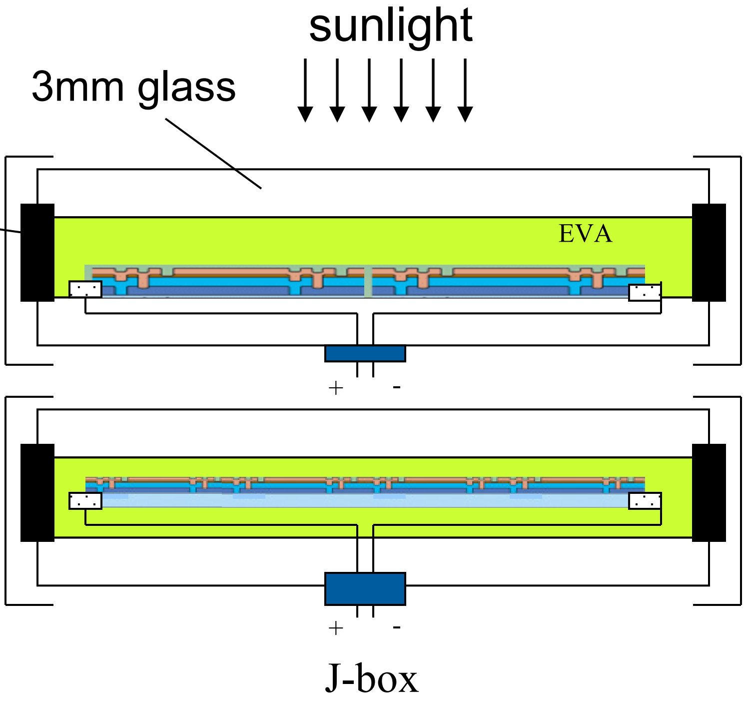
Module – monolithic interconnection

CIGS – substrate (light does not pass through)



Substrate does not have to be optically transparent (i.e., glass)

Substrates can be metal foils



Edge Seal

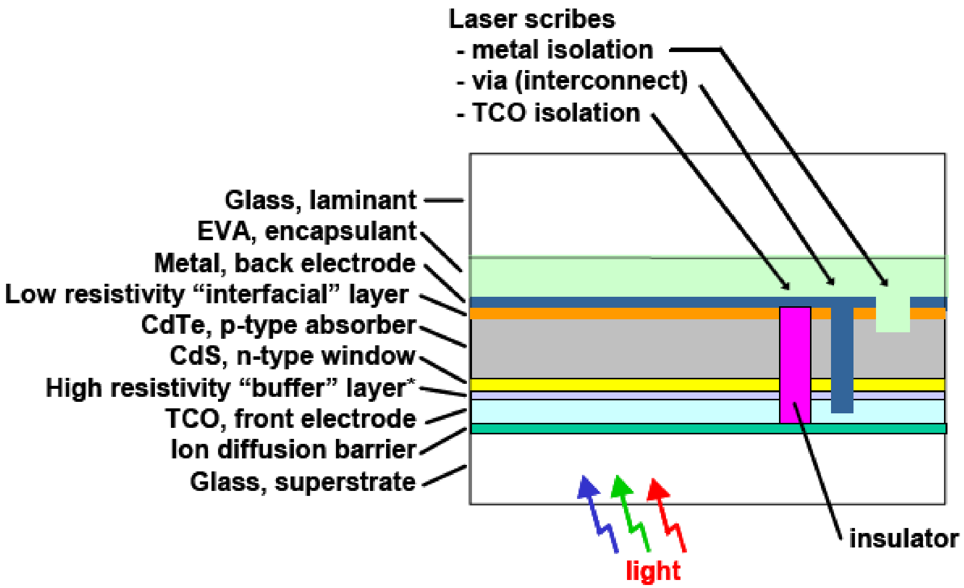
Edge frame (?)

Substrate is backsheet

Substrate not backsheet

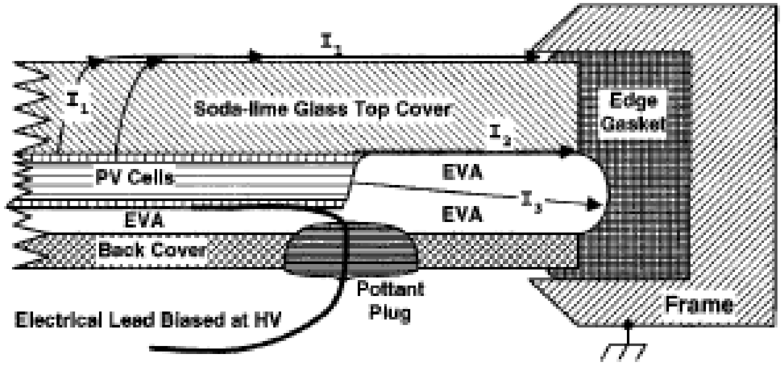
Module – monolithic interconnection

CdTe – superstrate (light passes through glass)



Substrate must be transparent

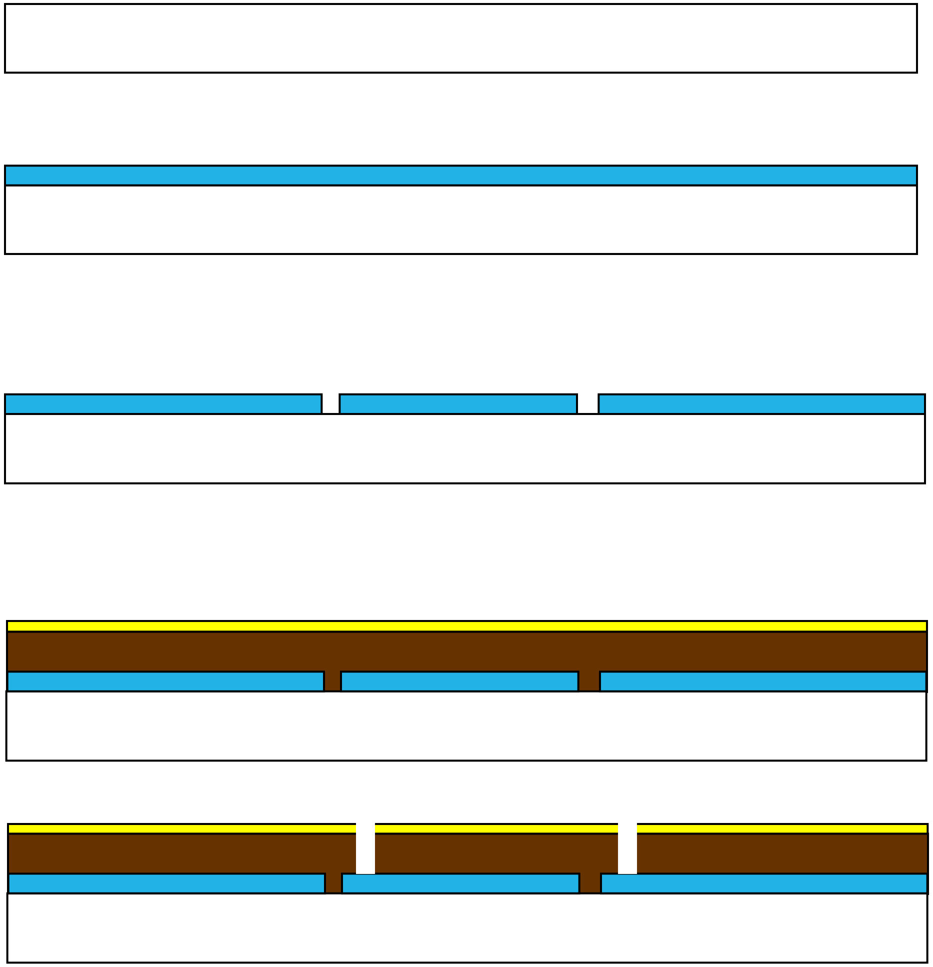
No significant flexible solution exists (but being worked on!)



From ref. below

“Analysis of Leakage Currents in PV Modules under High-Voltage Bias in the Field”, J.A. del Cueto and T.J. McMahon, Thin Solid Films 515 (2006) 2659-2668

Module – monolithic interconnection



glass

Mo sputter

Mo isolation (laser scribe)

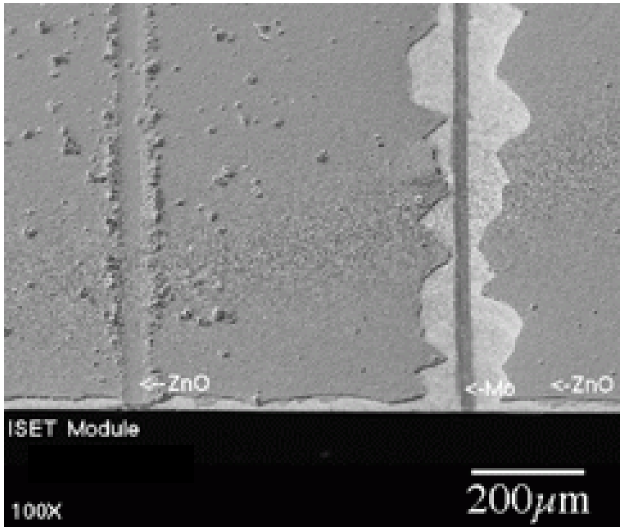
CIS then CdS deposition

CIS/CdS isolation

Interconnection consists of selective scribe lines (laser, mechanical) performed at specific points in thin film fabrication

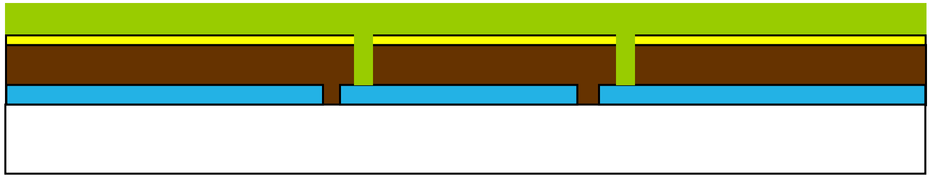
Scribing potentially introduces problems

Susceptible to degradation in modules (weak point)

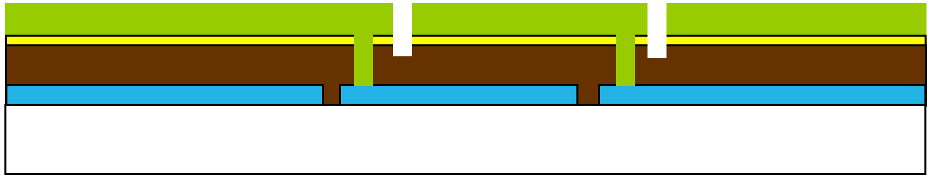


See A. Compann – Laser Focus, 43 (2007)

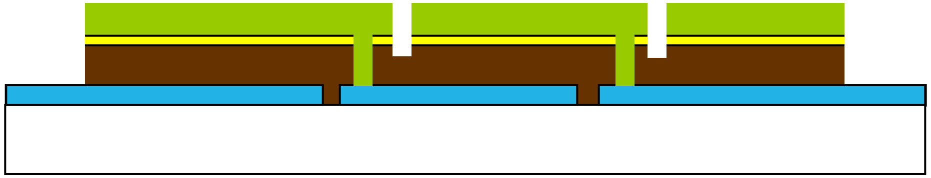
Module – monolithic interconnection



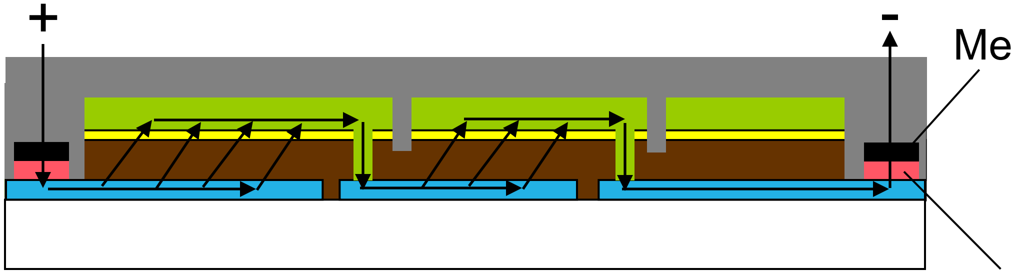
Front TCO (ZnO) deposition



Front TCO isolation



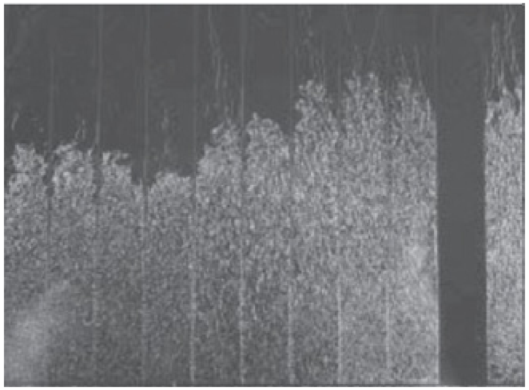
Edge delete



Metal “strip”

Edge busbar and EVA lamination

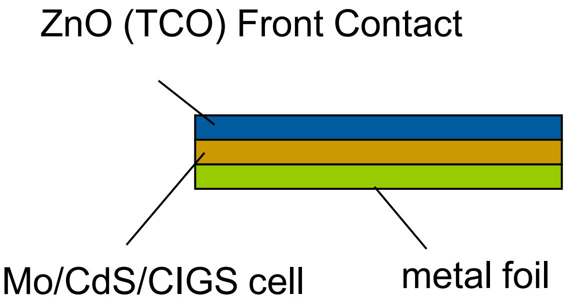
solder



“bar graphing”

Module – Interconnected discrete foil cells

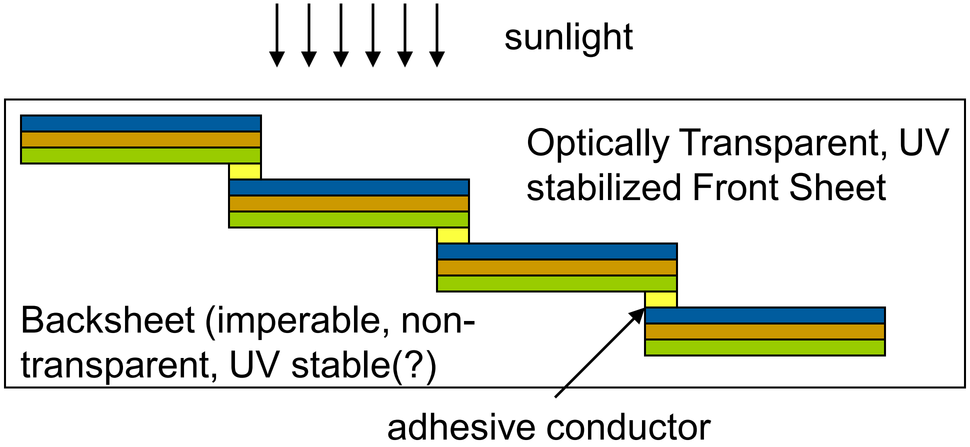
Substrate designs can use metal foils instead of glass. Advantages include faster (roll-to-roll) production and lower balance of system (BOS) costs (weight, installation, shipping)



ZnO (TCO) Front Contact

Mo/CdS/CIGS cell

metal foil



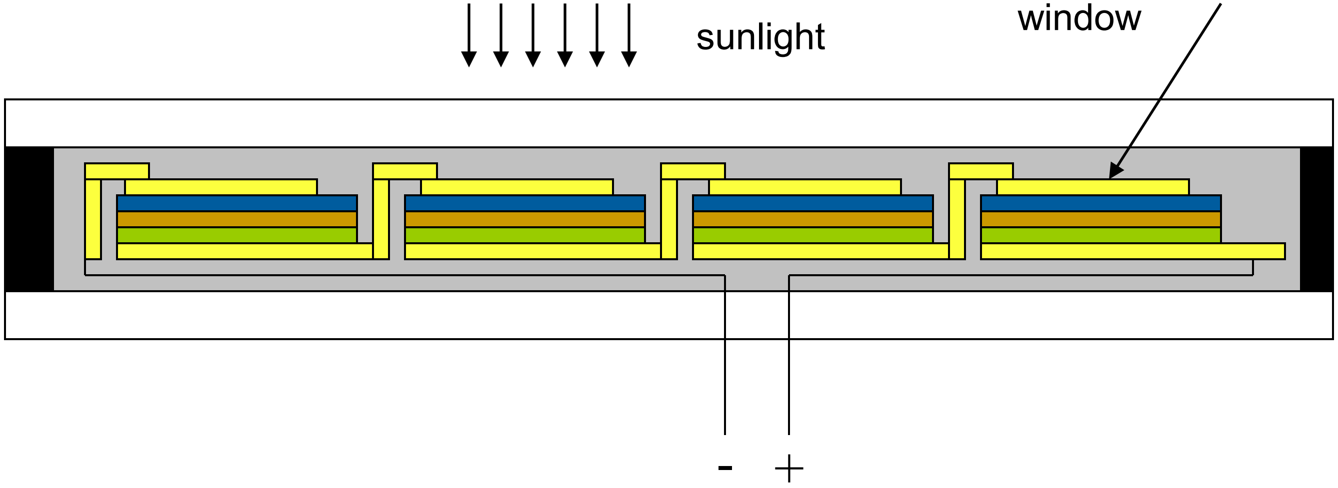
sunlight

Optically Transparent, UV stabilized Front Sheet

Backsheet (imperable, non-transparent, UV stable(?)

adhesive conductor

Flexible CIGS Package



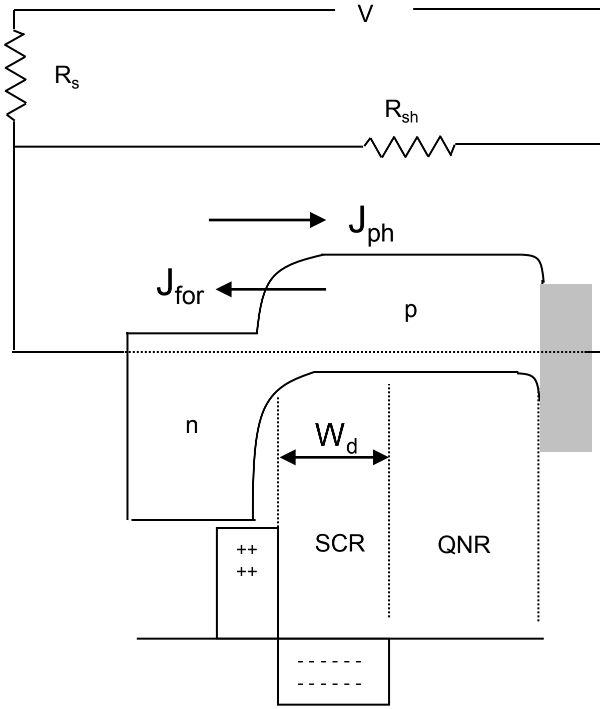
sunlight

metal finger grid over front TCO window

Glass-Glass Package with “hermetic” nature of glass + cheaper roll-to-roll fabrication

Thin Film Solar Cell Physics

Cell Physics – the basic pn junction equations



$$J = \underbrace{J_{SCR} + J_{QNR} + \left(\frac{V - JR_s}{R_{sh}}\right)} - J_{ph}$$

SCR – "space-charge region"

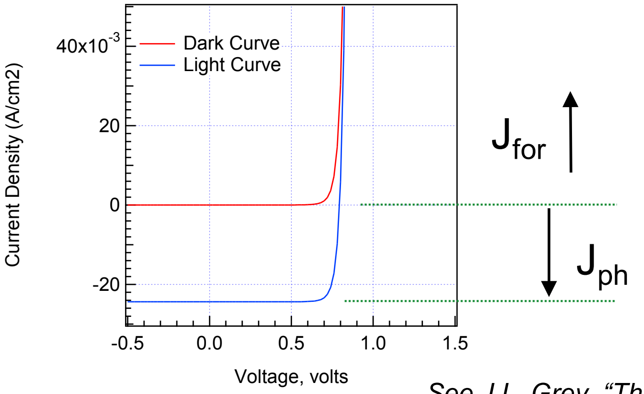
QNR – "quasi-neutral region"

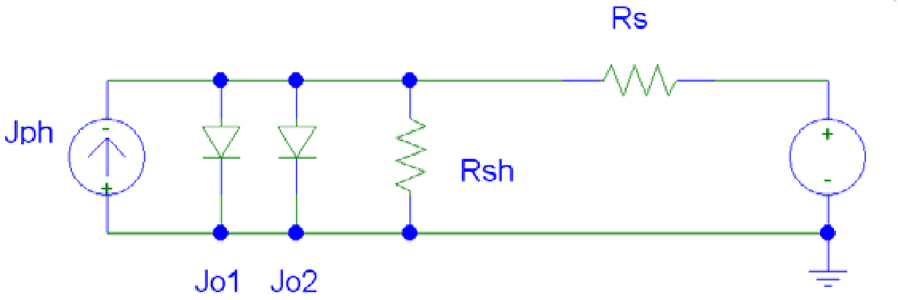
J_{for} (often called "dark current") – loss mechanisms

$$J_{QNR} = J_{01}\left(e^{q(V-JR_s)/kT} - 1\right) \quad \textit{where} \quad J_{01} \sim qD_n n_i^2 / L_n N_A$$

$$J_{SCR} = J_{02}\left(e^{q(V-JR_s)/2kT} - 1\right) \quad \textit{where} \quad J_{02} \sim qn_i W_d D_n / 2L_n^2$$

Note: QNR and SCR often called the "bulk" and "depletion" regions

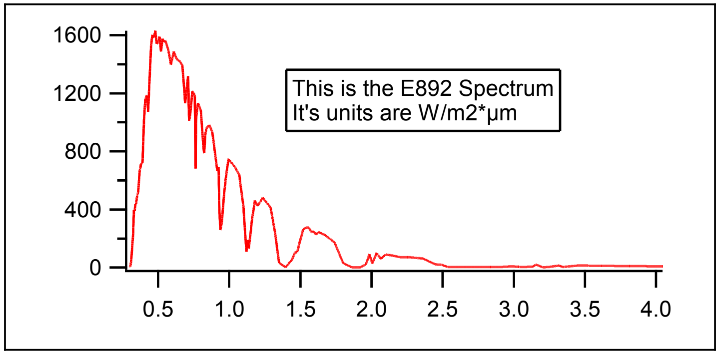


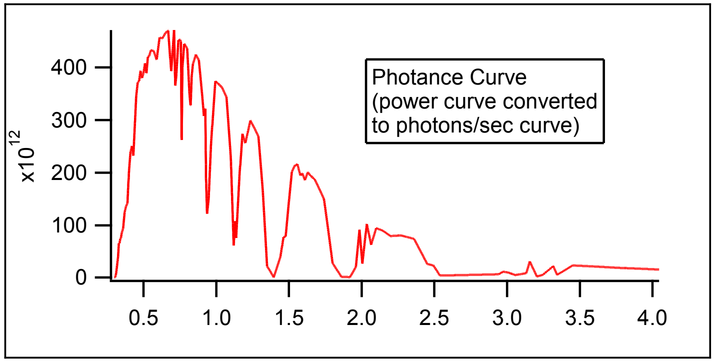


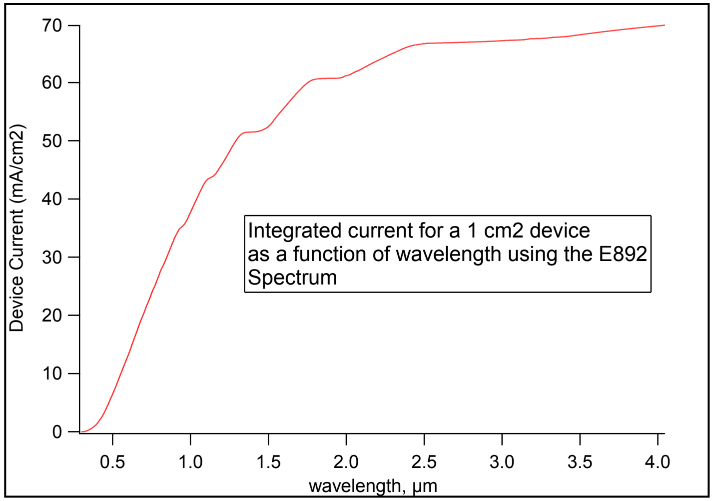
See J.L. Grey, "The Physics of the Solar Cell", Chpt 3, in Handbook of Photovoltaic Science and Engineering, (2003).

Also, "Solar Cells: An Introduction to Crystalline Photovoltaic Technology", by J.A. Mazer, Kluwer Academic Publishers

Cell Physics - Photogenerated Current, J_{ph}


This is the E892 Spectrum
It's units are W/m2*µm


Photance Curve
(power curve converted
to photons/sec curve)


Integrated current for a 1 cm2 device
as a function of wavelength using the E892
Spectrum

E892 Spectrum (AM 1.5 Solar Spectrum normalized to 1000 W/m^2)

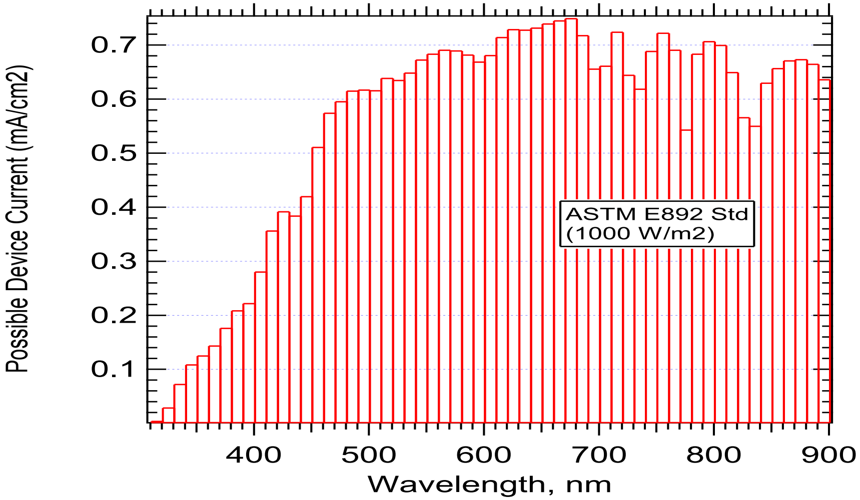
This is an irradiance curve (W/m^2*um)

Integral = 1000 W/m^2

E892 Spectrum converted to Photance curve (photons/sec)

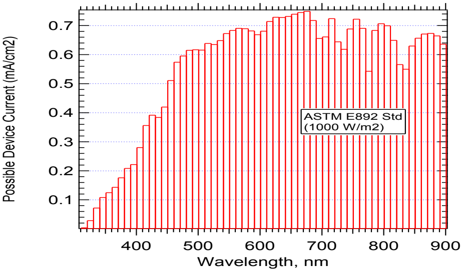
Integral = 4.4e^{+17} photons/sec*cm^2

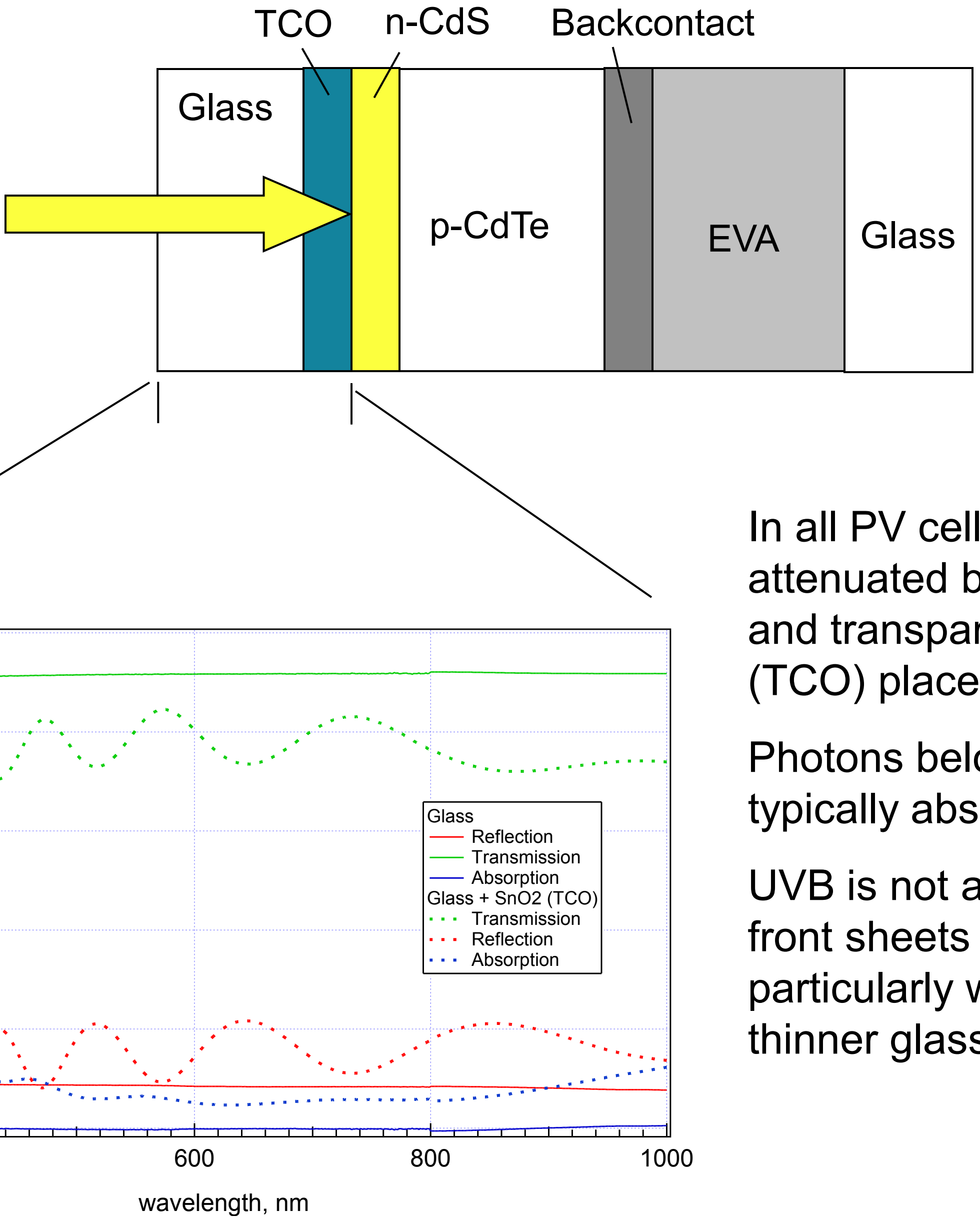
Max Possible current = 69.9 mA/cm^2


ASTM E892 Std
(1000 W/m2)

Cell Physics - Photogenerated Current, J_{ph}

Optical Spectrum





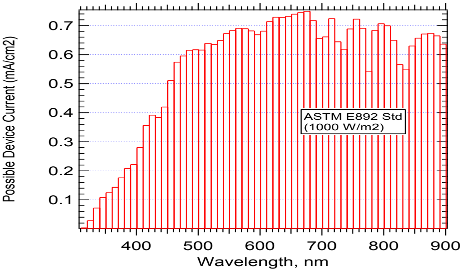
In all PV cells and modules light is attenuated by materials like glass and transparent conducting oxides (TCO) placed before the np layers

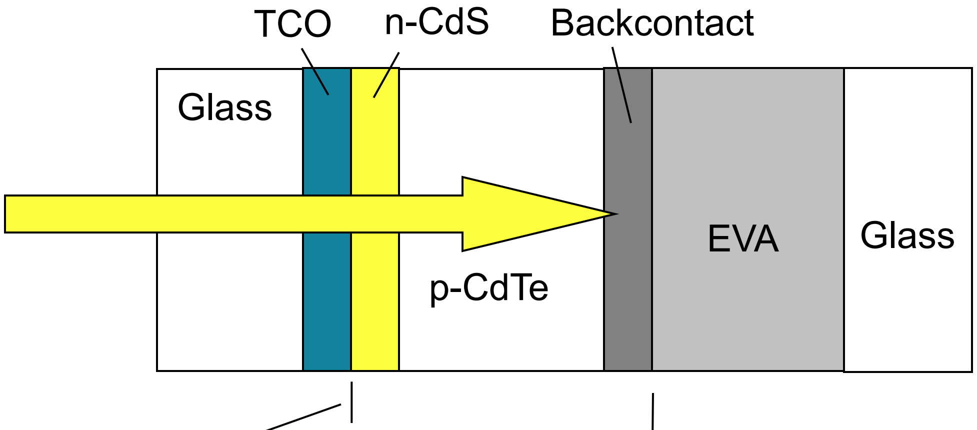
Photons below ~310-350 nm are typically absorbed by glasses

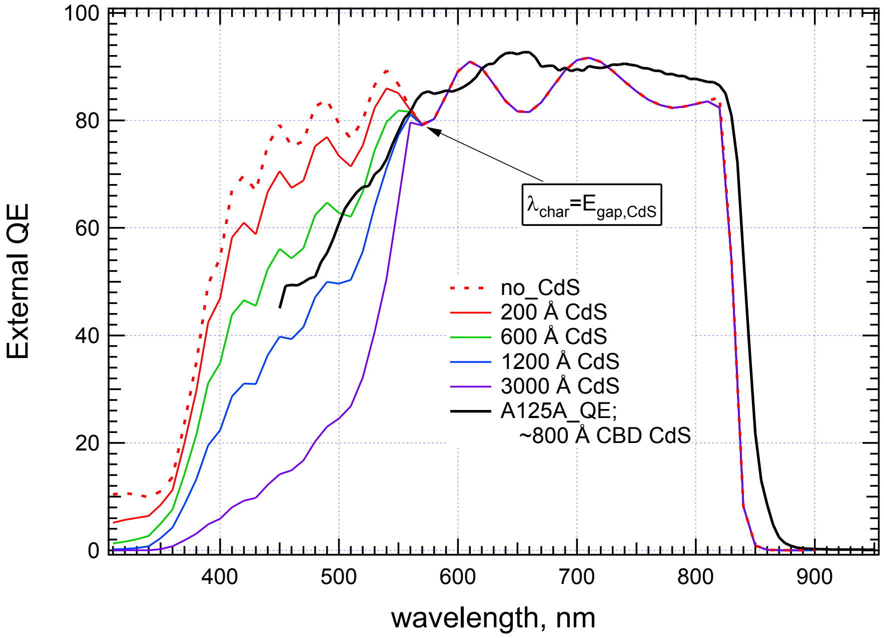
UVB is not a concern with glass front sheets (UVA >315 nm may be particularly with borosilicate and thinner glasses)

Cell Physics - Photogenerated Current, J_{ph}

Optical Spectrum







The n-layer (CdS) behaves like an optical window, i.e., photons absorbed in CdS do not contribute to current.

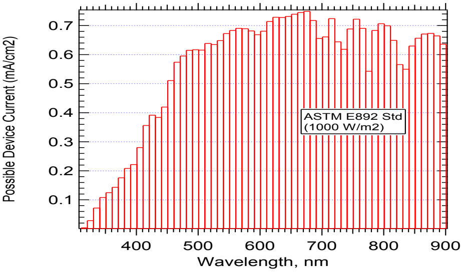
The actual current generation of a device can be modeled in this fashion, i.e., light is attenuated by glass, TCO, and CdS.

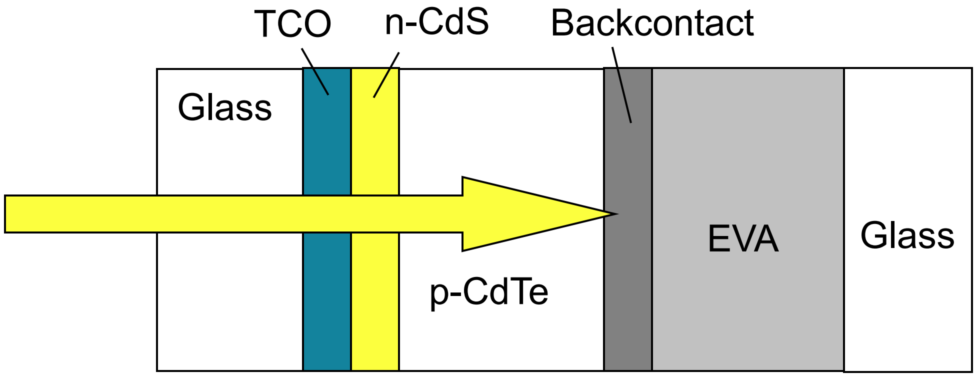
Short wavelength response determined by absorption in the glass/TCO/window layers

Long-wavelength response determined by absorber (CdTe) bandgap

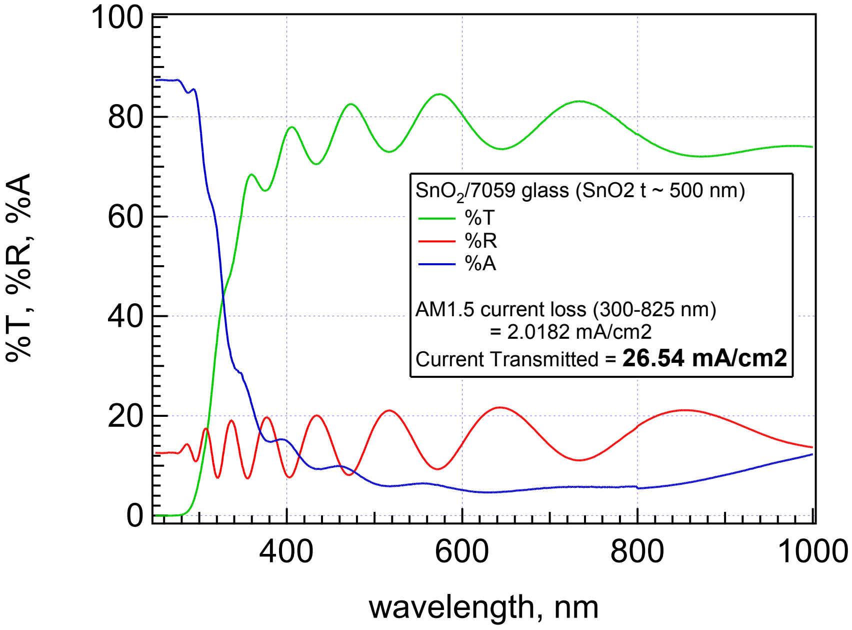
Cell Physics - Photogenerated Current, J_{ph}

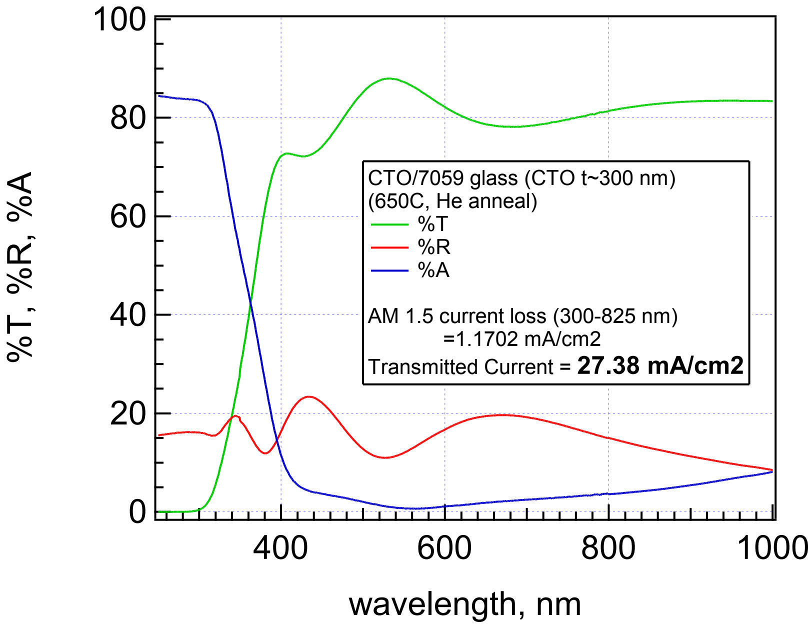
Optical Spectrum





To maximize performance: minimize absorption in TCO; reduce CdS thickness





Cell Physics – Its about Generation and Collection

n-layers in CdTe and CIGS are inactive regarding power generation, they attenuate light.

Generation in cells determined by absorption of “useful light”

Light has to be representative of Sunlight (i.e., Xenon-Arc)

Definitions of “useful light”:

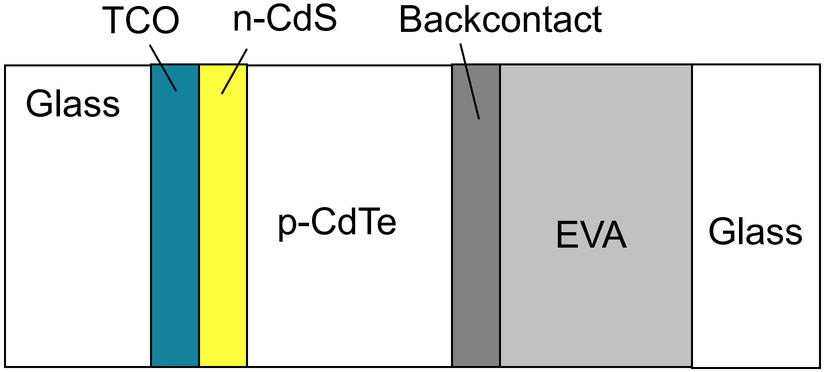
- For CdTe→
  - glass/TCO absorption < λ < $E_{gap,CdTe}$
- For CIGS→
  - glass-glass package→
    - glass/EVA/TCO absorption < λ < E_{gap},CIGS
  - flexible package→
    - tefzel/EVA/TCO absorption < λ < E_{gap},CIGS

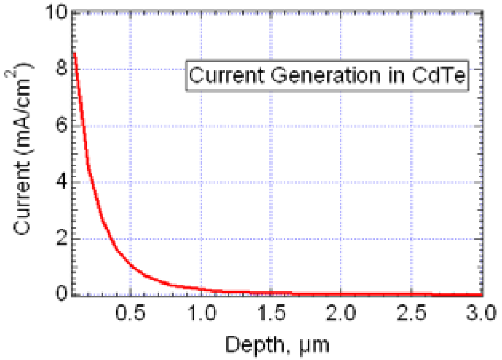
Direct gap semiconductors like CdTe and CIGS have high absorption coefficients

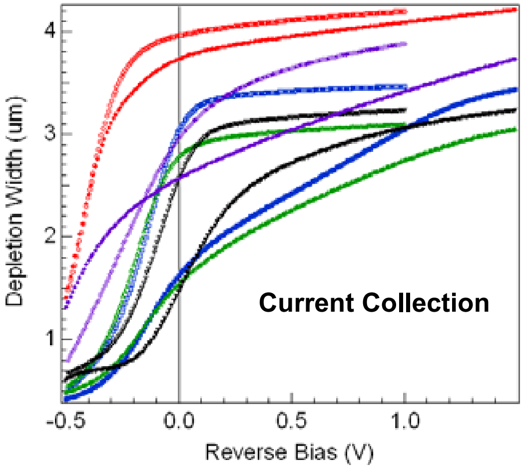
In CdTe, 99% of the absorption occurs in the first 1.5-2 ums.

Capacitance-Voltage measurements help determine the extent of the space-charge (field-limited) as well as quasi-neutral (diffusion-limited) regions.

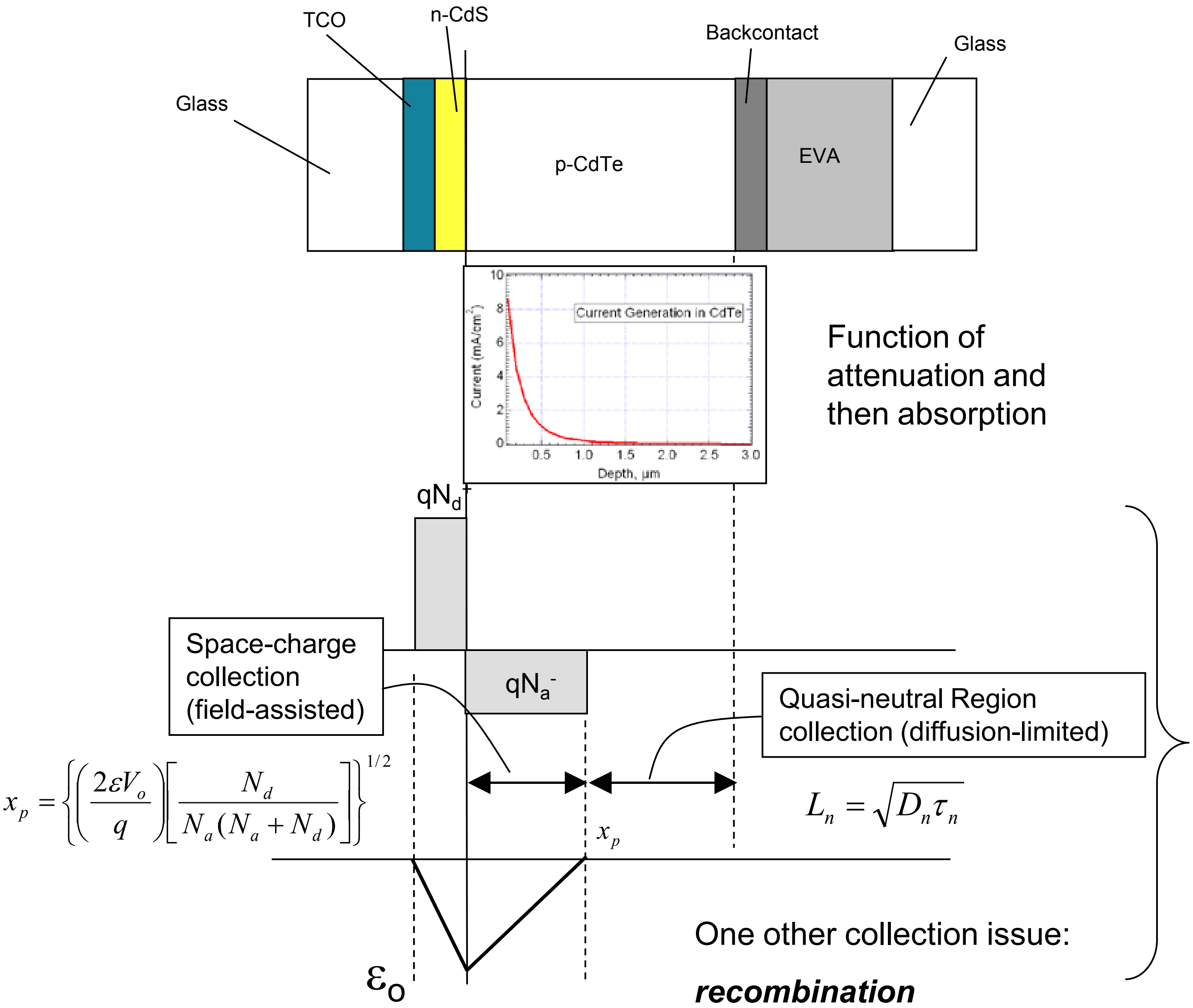
In CdTe, the depletion region (at V=0) ~ 1-2 ums







Cell Physics – Its about Generation and Collection



Function of attenuation and then absorption

Space-charge collection (field-assisted)

Quasi-neutral Region collection (diffusion-limited)

$$x_p = \left\{ \left(\frac{2\varepsilon V_o}{q} \right) \left[\frac{N_d}{N_a (N_a + N_d)} \right] \right\}^{1/2}$$

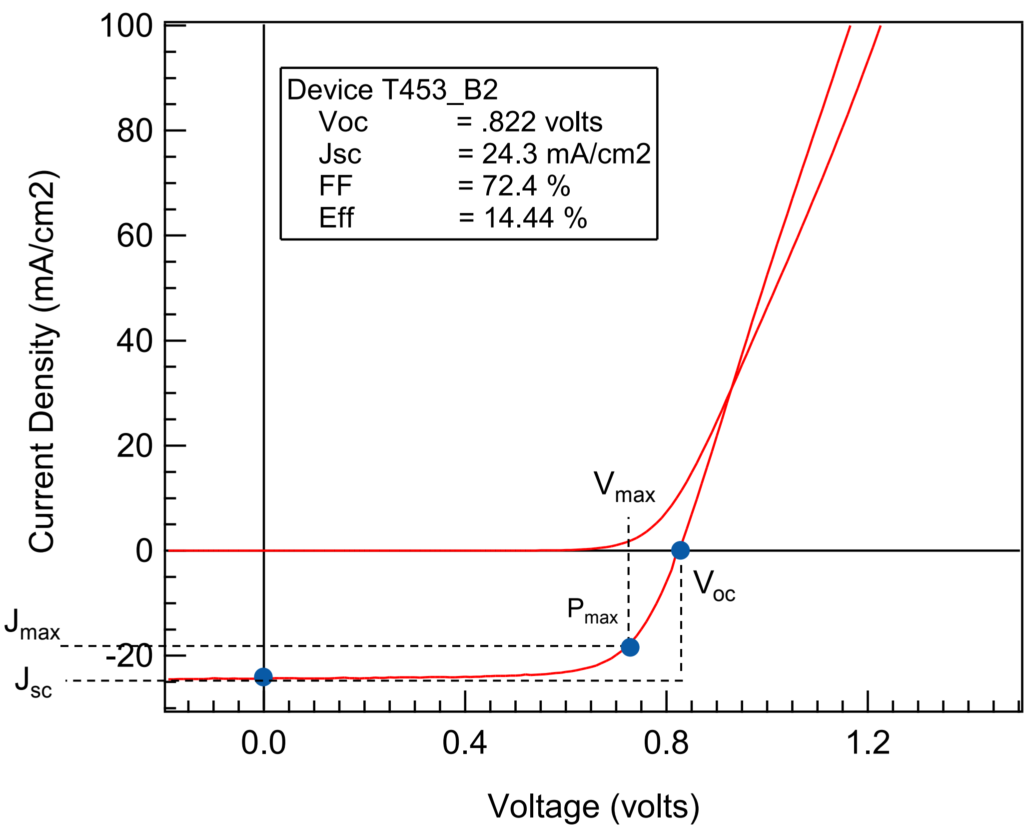
$$L_n = \sqrt{D_n \tau_n}$$

One other collection issue:

recombination

Function of how you make the cell

Cell Physics – J-V Curves



P_{max} *where*

$$\left.\frac{\partial(JV)}{\partial V}\right|_{V=V\max, J=J\max} = 0$$

V_{oc} *where*

$$V\big|_{J=0}$$

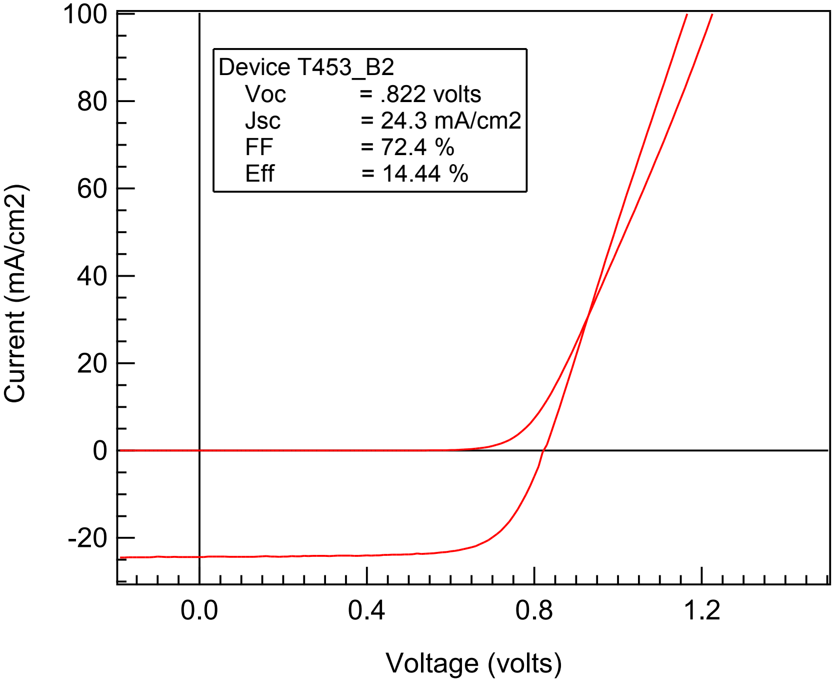
$J_{sc} = J_{ph}$ *where*

$$J\big|_{V=0}$$

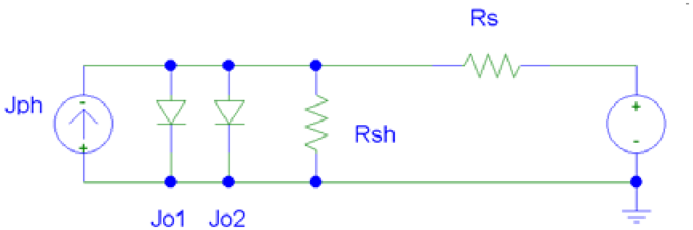
$$FF = {\left(V_{\max}J_{\max}\right)}\Big/{\left(V_{oc}J_{sc}\right)}$$

$$Eff = \eta\% = {P_{\max}}\Big/{P_{in}} = {FF \times V_{oc} \times J_{sc}}\Big/{100\,mW/cm^2}$$

Cell Physics – J-V Curve Modeling



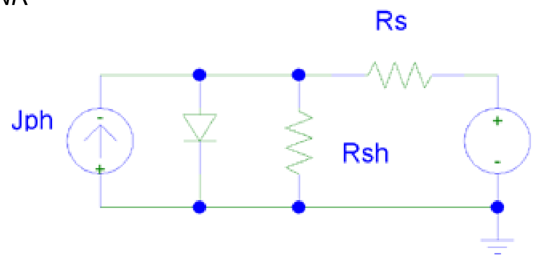
2-diode model



$$J = J_{SCR} + J_{QNR} + \left(\frac{V - JR_s}{R_{sh}} \right) - J_{ph}$$

assumes Shockley-Read-Hall recombination (also 1-trap; near midgap, low injection; similar e-h diffusivities) – fit both J_{SCR} and J_{QNR}

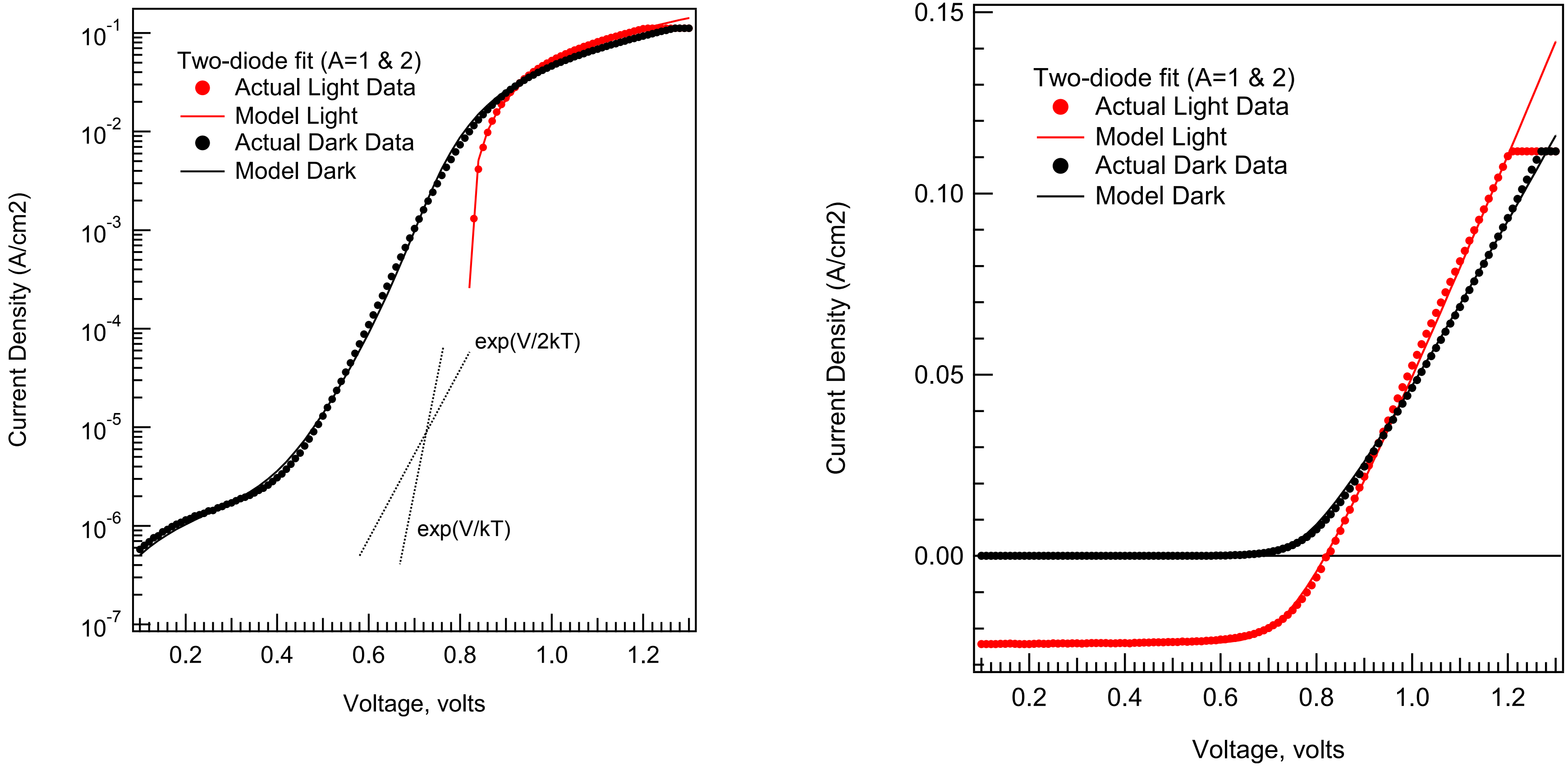
1-diode model



$$J_0 = J_{01} \left(e^{q(V - JR_s)/AkT} - 1 \right)$$

Simpler techniques to curve-fit; can assign A = 1 or A=2 depending on which recombination dominates (for CdTe, use A=2); or determine some value of 1 < A < 2.

Cell Physics – J-V Curve Modeling



2-diode model (A=1 & 2)

Lite Model:

J_{01} (J_{QNR})=3e^{-16}

J_{02} (J_{SCR})=1e^{-09}

R_s=3

R_{sh}=200k

Dark Model:

J_{01} (J_{QNR})=1e^{-15}

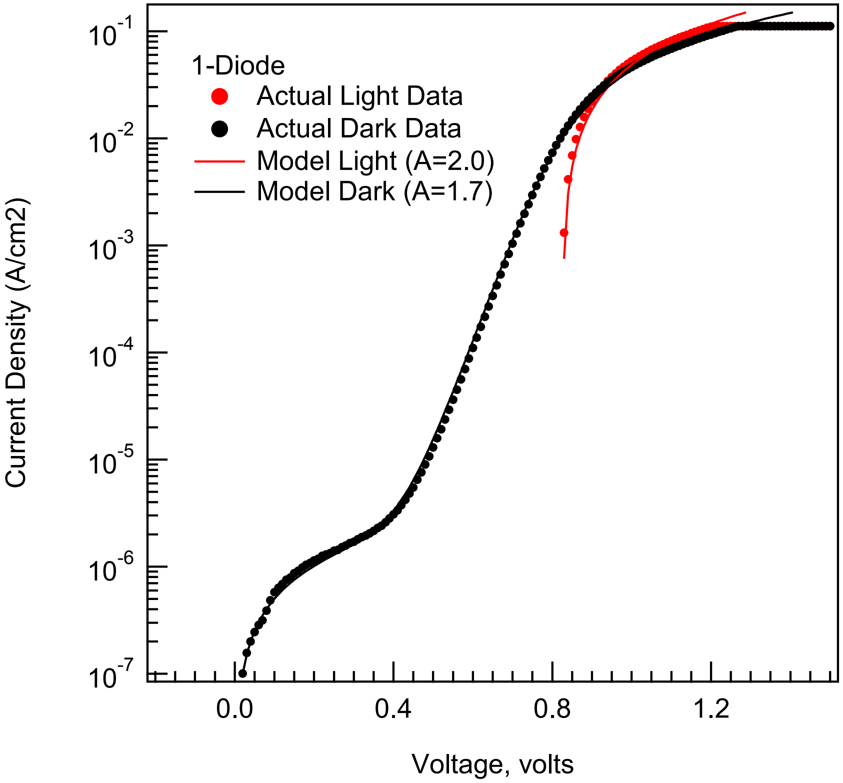
J_{02} (J_{SCR})=7e^{-10}

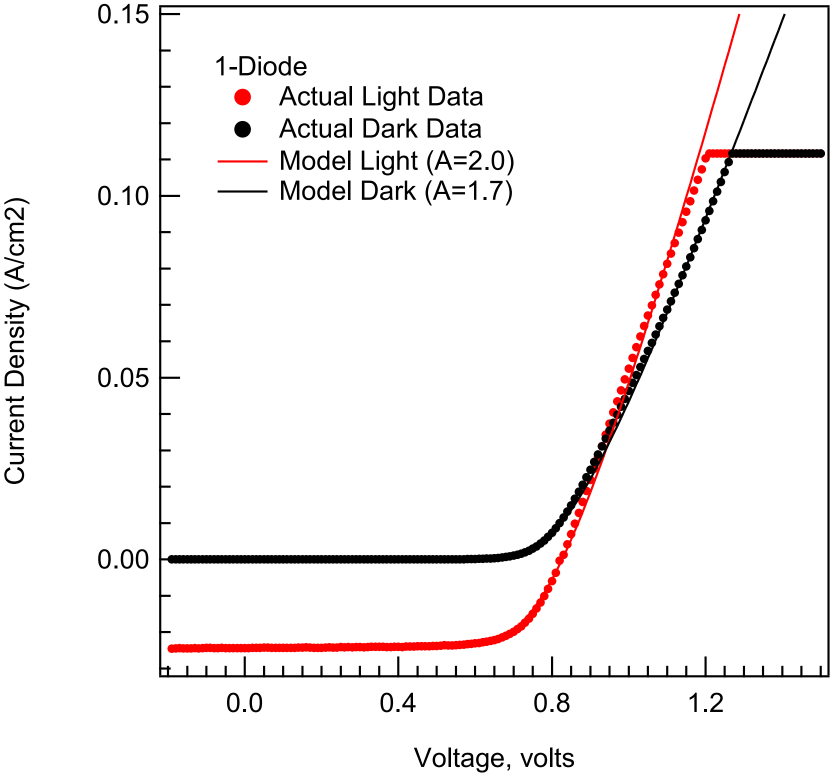
R_s=4

R_{sh}=200k

Recombination in SCR dominates

Cell Physics – J-V Curve Modeling





1-diode model

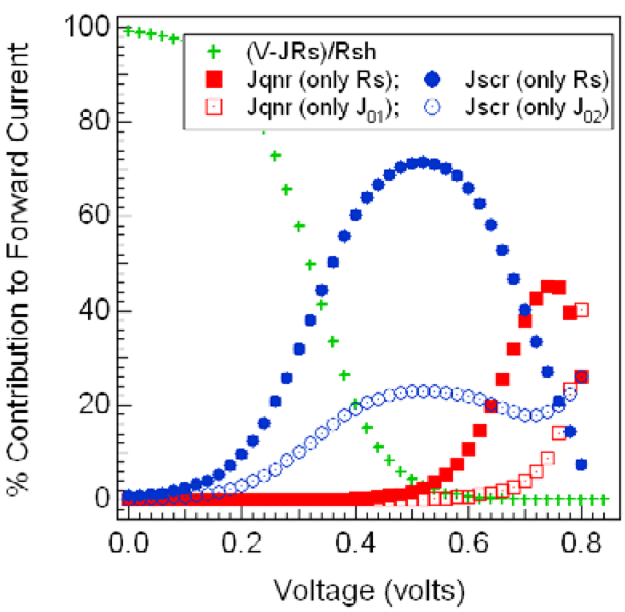
Lite Model (A=2)	Dark Model (A=1.7)
J_{02} (J_{SCR})=2.8e^{-09}	J_0 (J_{QNR}+J_{SCR})=1e^{-15}
R_s=2.4	R_s=3.3
R_{sh}=200k	R_{sh}=200k

1-diode model easier to fit

Here for example, the dark JV curve is fit very nicely with a value of A = 1.7

Values of A between 1 to 2 due to distribution of states in bandgap

Cell Physics – J-V Curve Modeling in 4th (power) quadrant



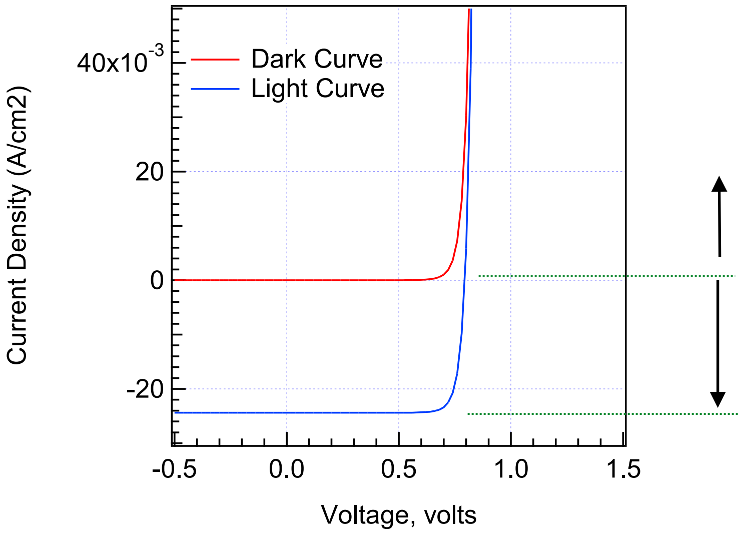
$$J = J_{SCR} + J_{QNR} + \left(\frac{V-JR_s}{R_{sh}}\right) - J_{ph}$$

Minimize these

$$J_{QNR} = J_{01}\left(e^{q(V-JR_s)/kT} - 1\right)$$

$$J_{SCR} = J_{02}\left(e^{q(V-JR_s)/2kT} - 1\right)$$

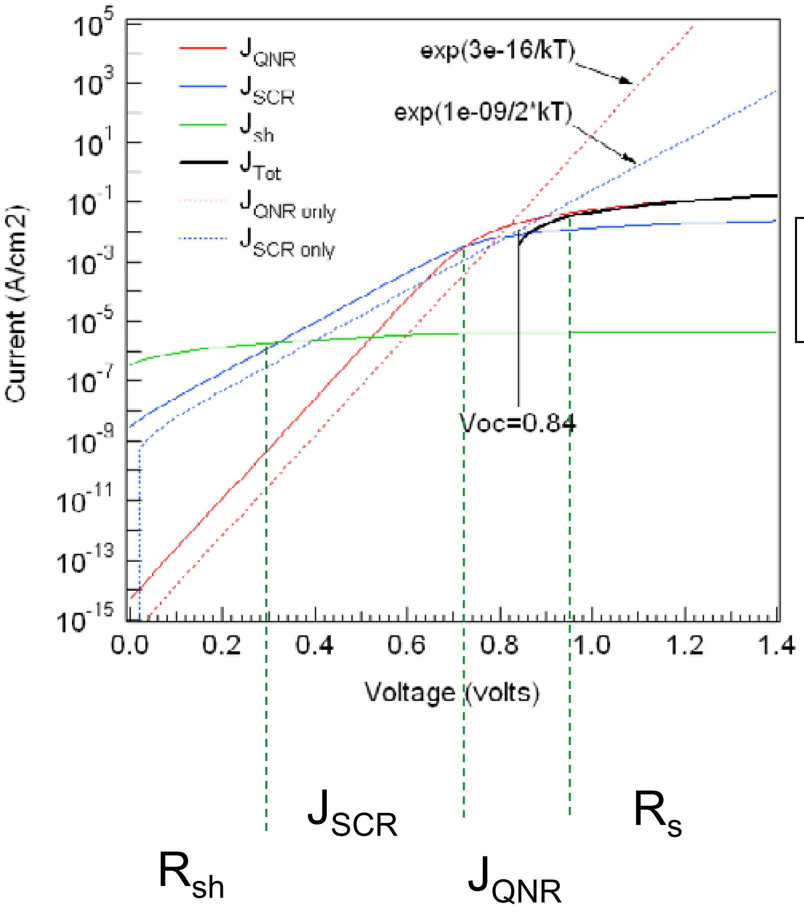
$$J_{sh} = \left(\frac{V-JR_s}{R_{sh}}\right)$$



J_{for} BAD→Minimize this

J_{ph} GOOD→Maximize this

Cell Physics – J-V Curve Modeling in 1st and 4th (power) quadrant



Larger term dominates

$$J_{QNR} = J_{01}\left(e^{q(V-JR_s)/kT} - 1 \right)$$

$$J_{SCR} = J_{02}\left(e^{q(V-JR_s)/2kT} - 1 \right)$$

$$J_{sh} = \left(\frac{V - JR_s}{R_{sh}} \right)$$

If $V_{oc} > V$ where,

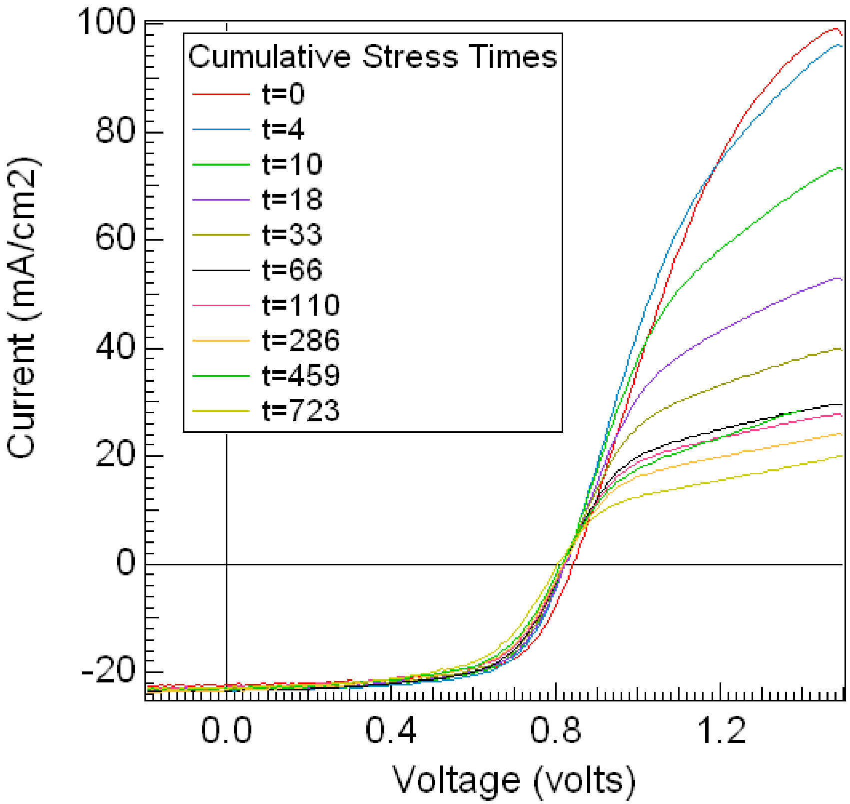
$$V = \frac{2kT}{q} \ln\left(J_{02} / J_{01} \right)$$

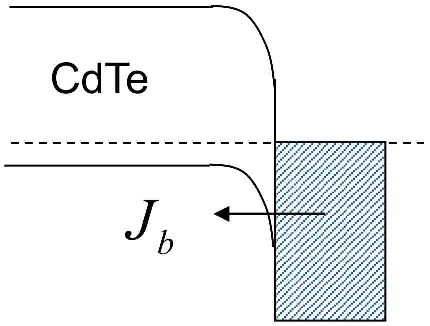
Need to consider effect recombination in the QNR contributes to performance at V_{oc}

Can occur in “high performance cells where J_{02} is smaller

Cell Physics – J-V Curve 1st Quadrant Effects

Thermionic emission model for back contact

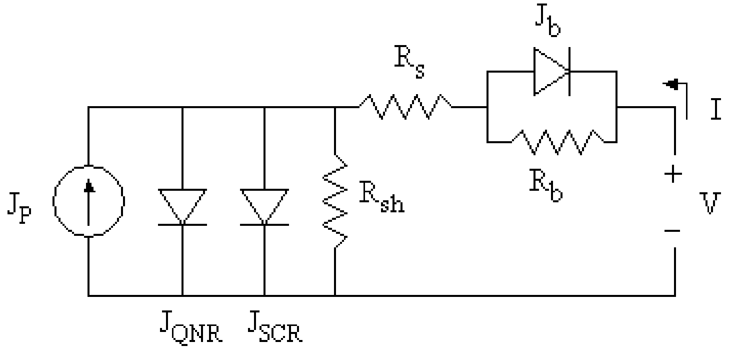




$$J_b = q \cdot v_R \cdot p \cdot e^{-\left(qE_b/kT\right)}$$

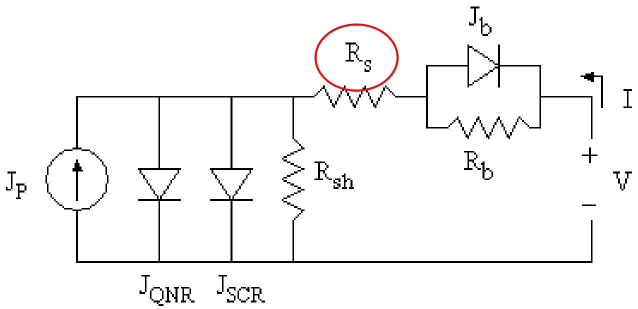
$$v_R = \frac{1}{\sqrt{2\pi}}\sqrt{\frac{kT}{m^*}}$$ ~ 3x10^7 cm/s

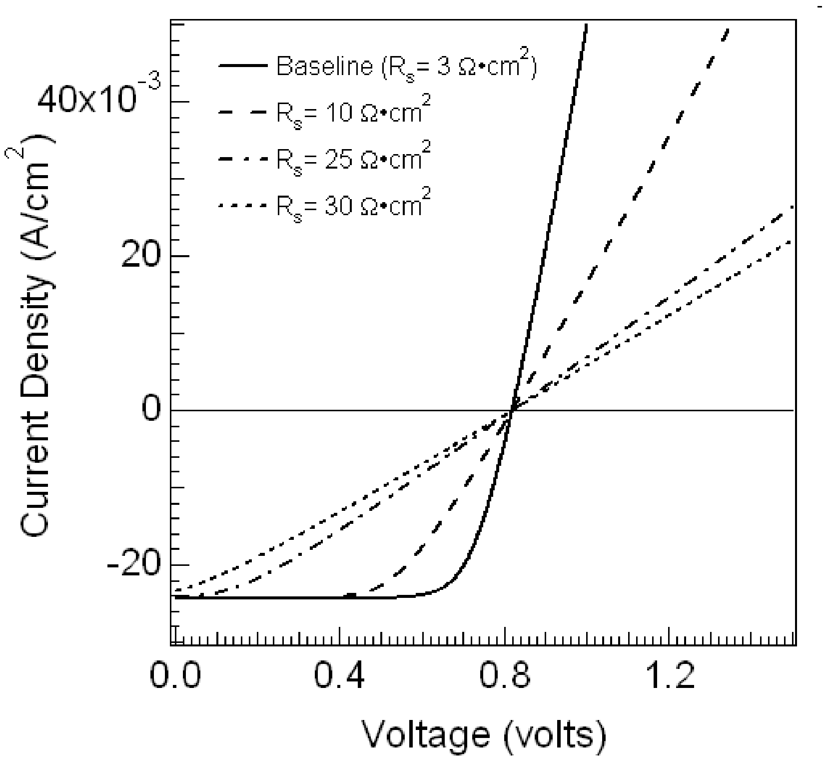
$$p = N_V e^{-(E_f - E_v)/kT}$$ ~ 5x10^{18} cm^{-3}

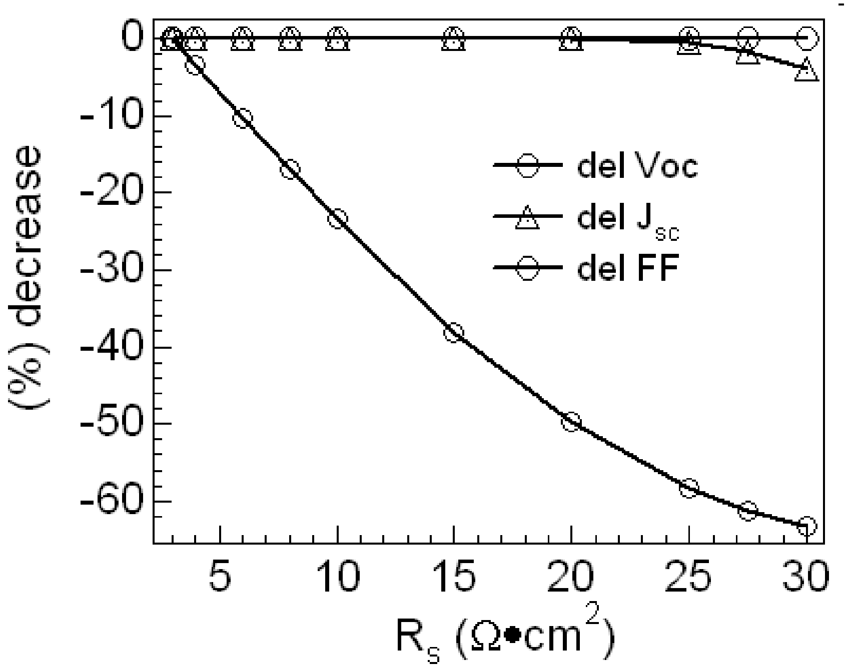


S.H. Demtsu and J.R. Sites, Thin Solid Films 510 (2006) 320-324

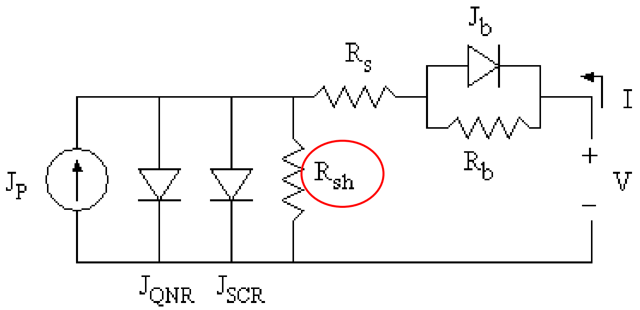
Cell Physics – J-V Curve Modeling (Effect of R_s only)

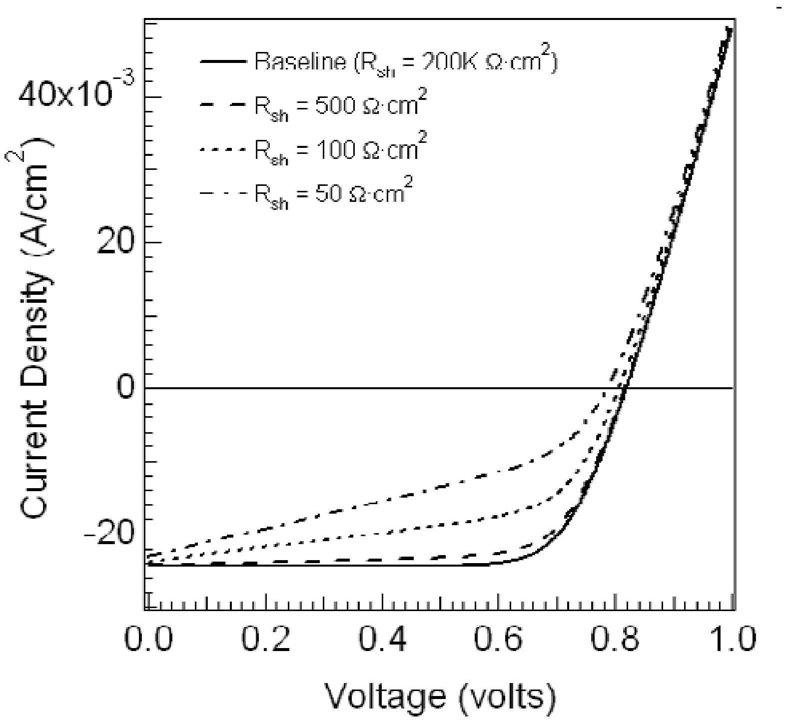


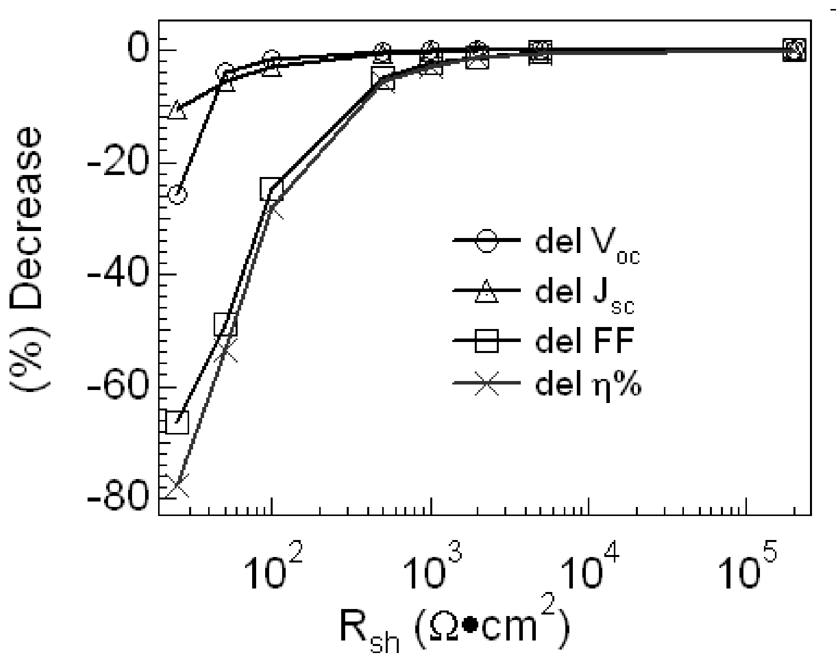




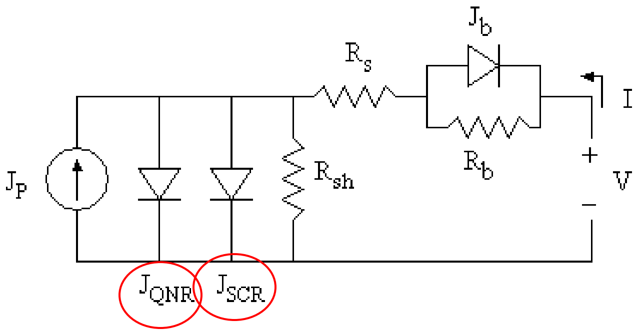
Cell Physics – J-V Curve Modeling (Effect of R_{sh} only)

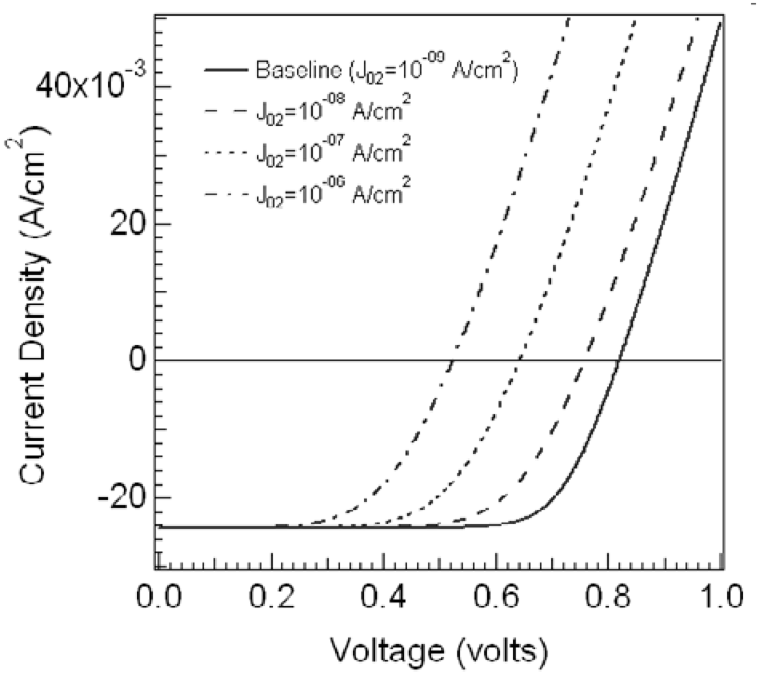


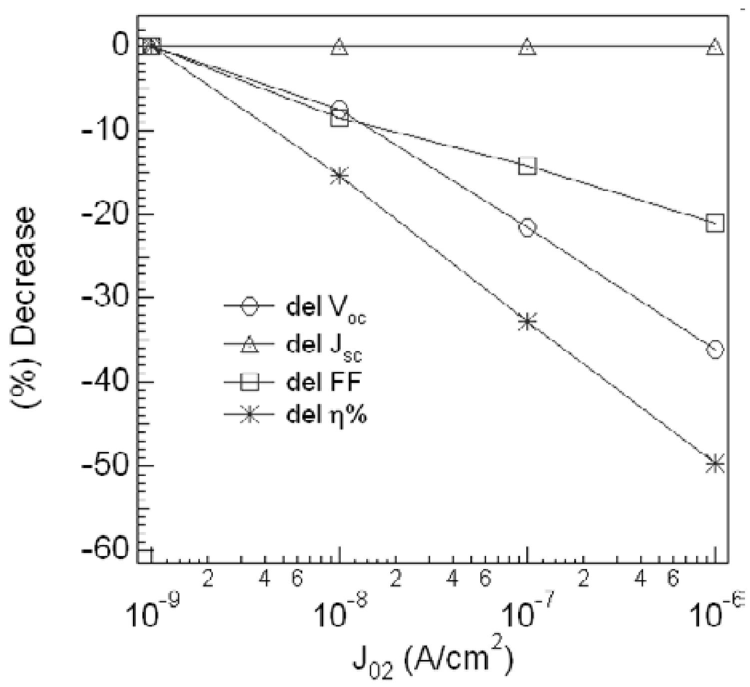




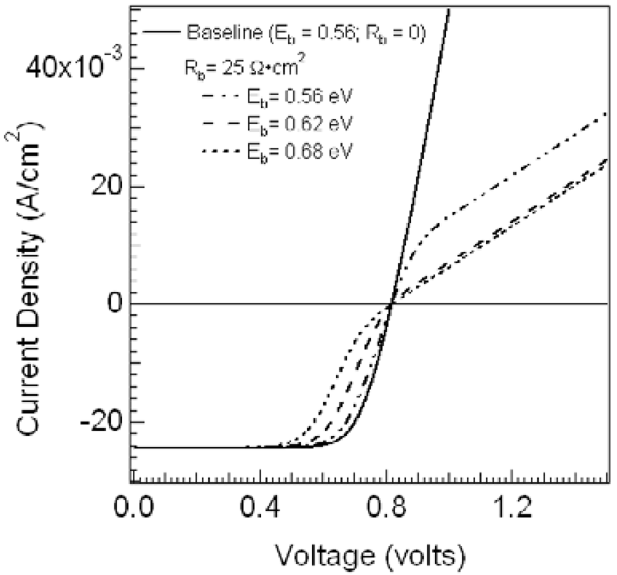
Cell Physics – J-V Curve Modeling (Effect of J_0 only)

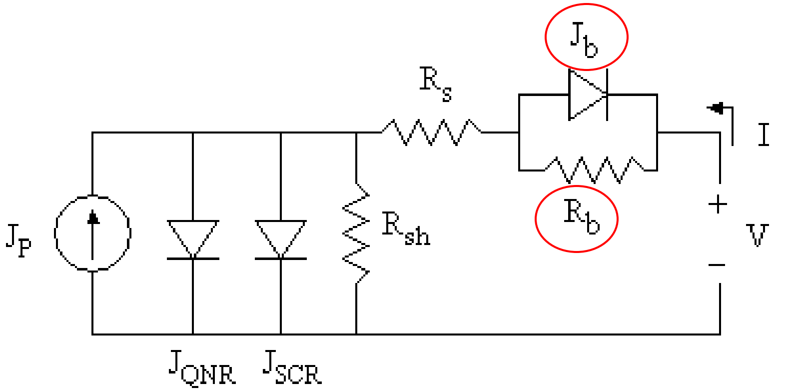


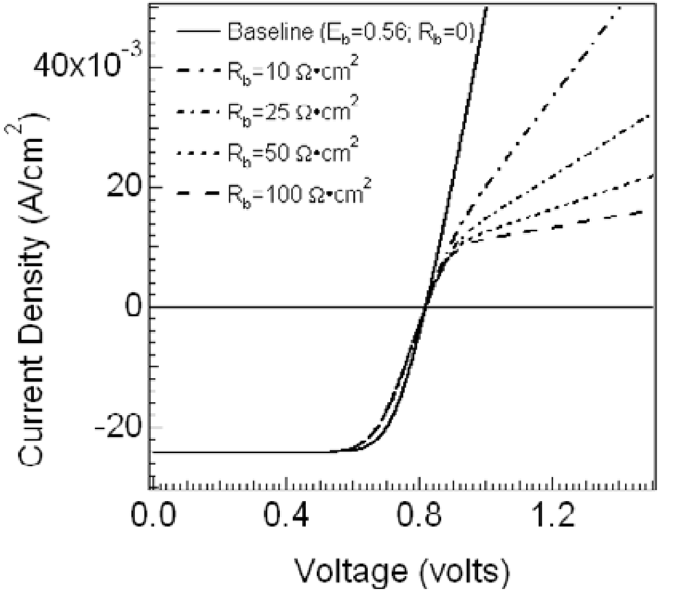


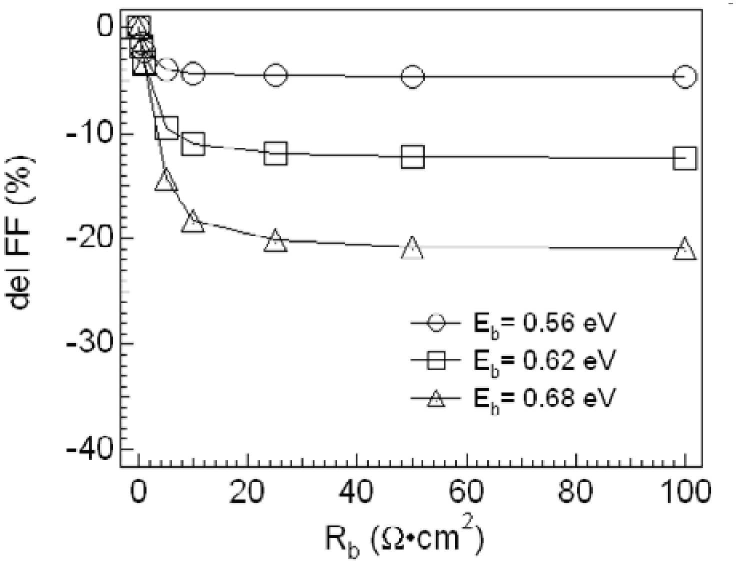


Cell Physics – J-V Curve Modeling (Effect of E_b (J_b) and R_b only)

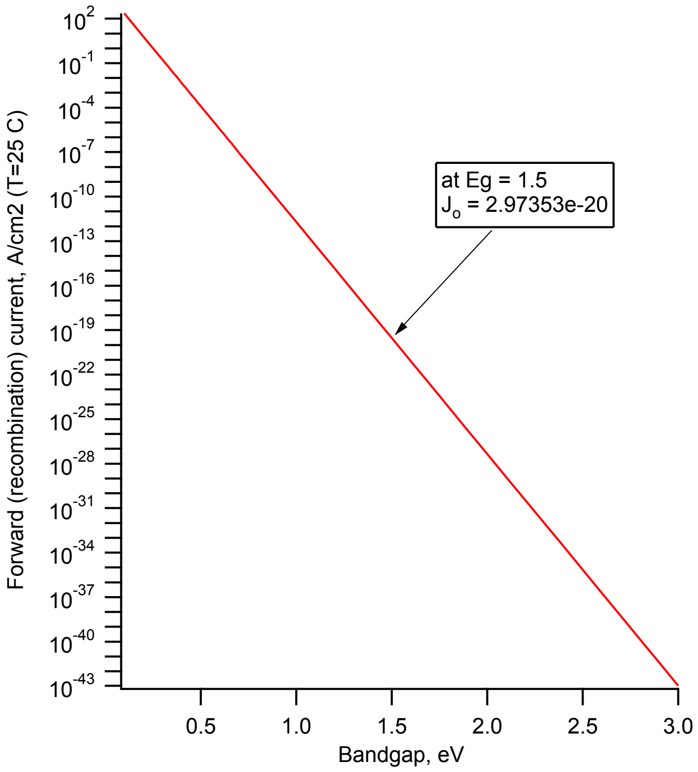








Cell Physics – CdTe cell limitations



at Eg = 1.5
J_o = 2.97353e-20

Regarding CdTe cell performance,

Relative to their single-crystal counterparts, these cells have very high recombination currents

For III-V cells, recombination currents follow this empirical relationship (M. Wanlass)

$$J_0 = \beta\, T^3 e^{\left(-E_g / kT\right)}$$

$$\text{where } \beta = 3.165 \times \mathrm{e}^{\left(2.912 \times E_g\right)}$$

For CdTe (Eg~1.5 eV), we should expect recombination currents on the order of 10^{-20} rather than 10^{-9} to 10^{-10}

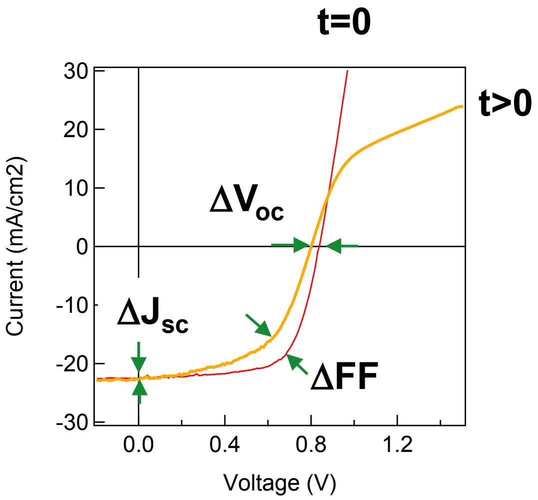
Thus, understanding recombination from the start (for performance) as well as how degradation impacts recombination (durability) is key for CdTe

Improving current will boost module performance in the short-term, but not FF and V_{oc} (world-record CdTe J_{sc} ~ 25.9 mA/cm^2

Cell Performance Changes During Stress

How J-V curves change indicative of Degradation Mechanisms

J-V Degradation Modes - Correlation Analysis

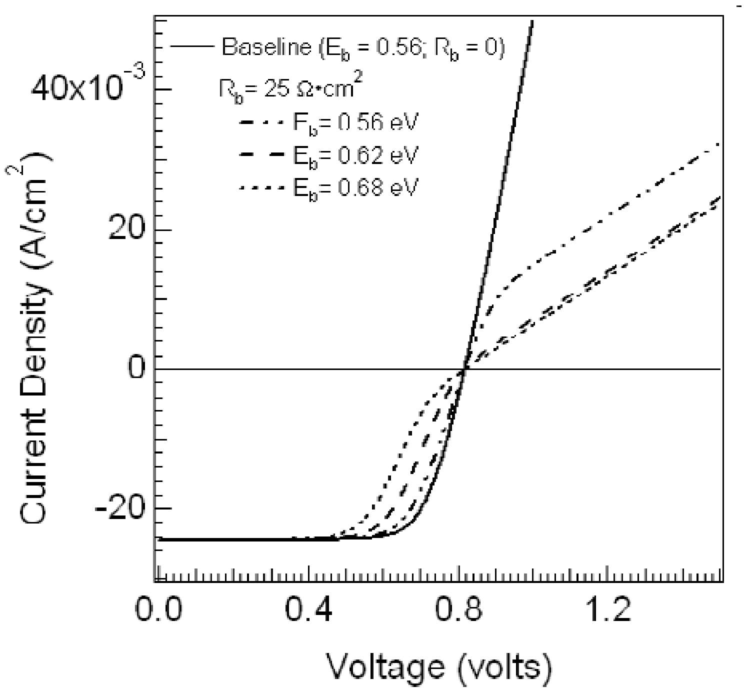


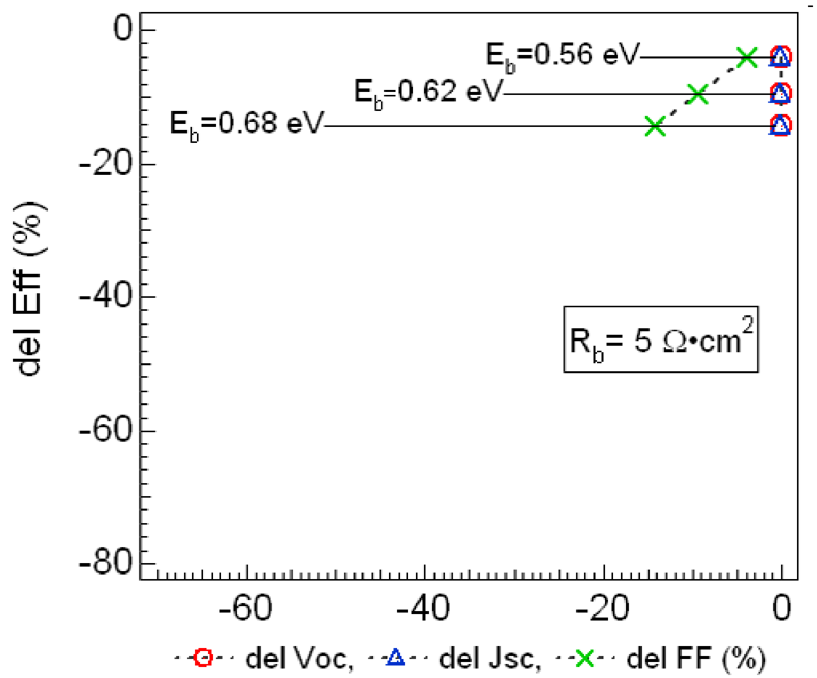
ΔEff vs

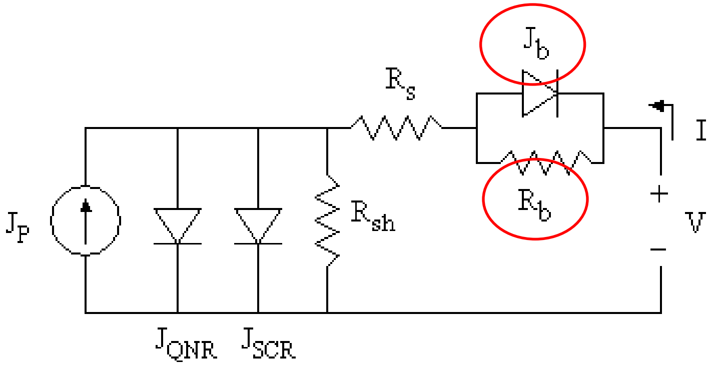
ΔV_{oc}, ΔJ_{sc} and ΔFF

- During test, each JV measurement represents a unique combination of performance parameters
- Plot ΔEff vs. ΔV_{oc}, ΔJ_{sc}, ΔFF.
- Are there statistical correlations?
- Identify “why" performance changes
    - V_{oc}: recombination, shunting
    - J_{sc}: generation and collection, series resistance, voltage-dependent collection
    - FF: everything affects it

Simulating back contact degradation (J_b , R_b)

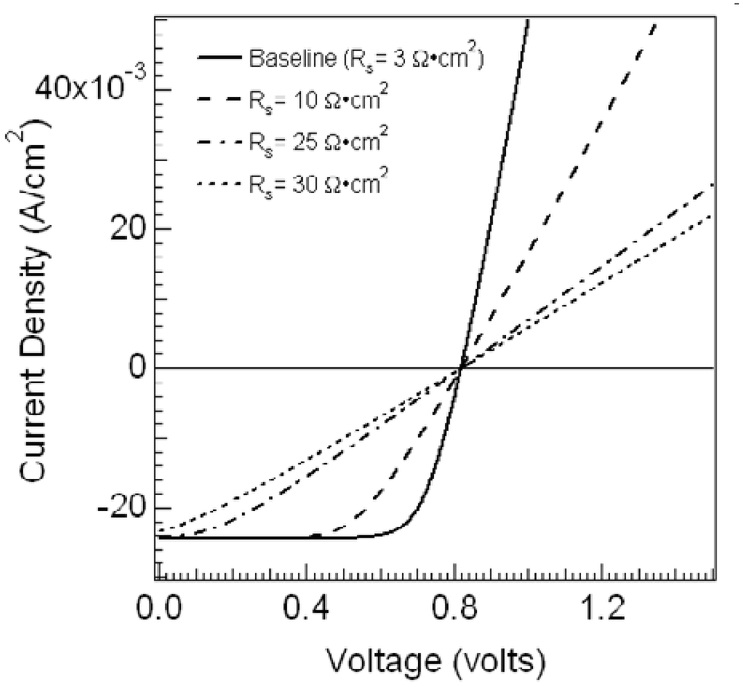


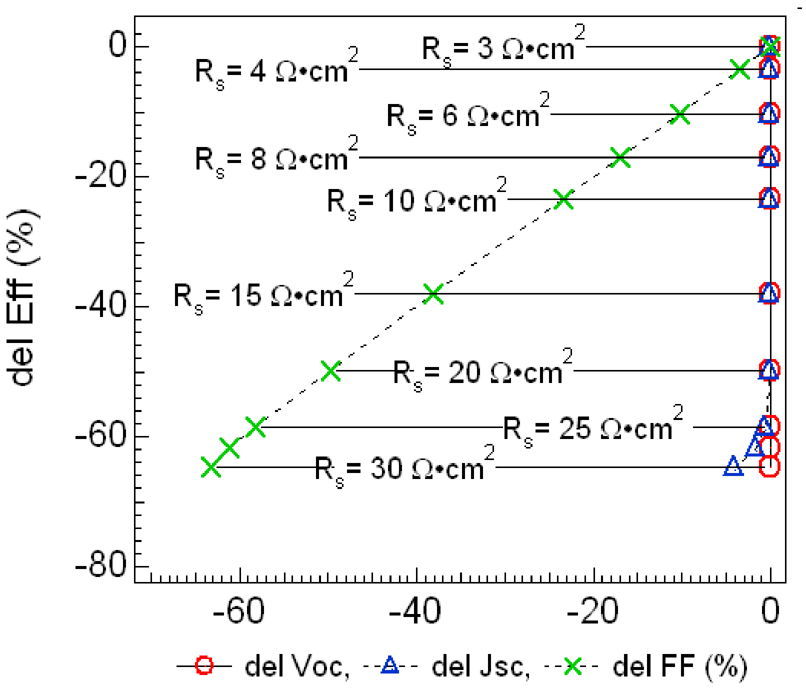


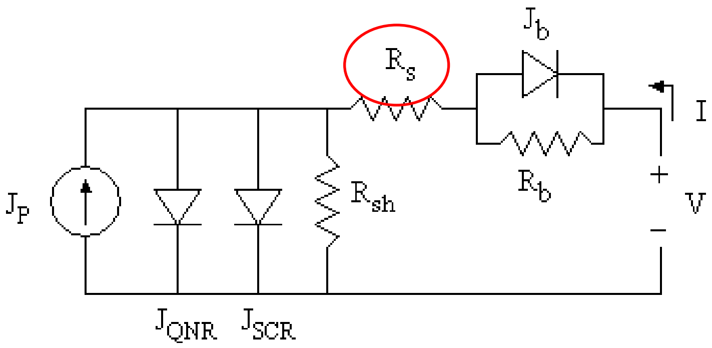


- **Observed changes in J_b, R_b predict only small decreases in performance**
- **No effect on ΔV_{oc}, ΔJ_{sc}**
- **Only affects FF**

Simulating R_s increase

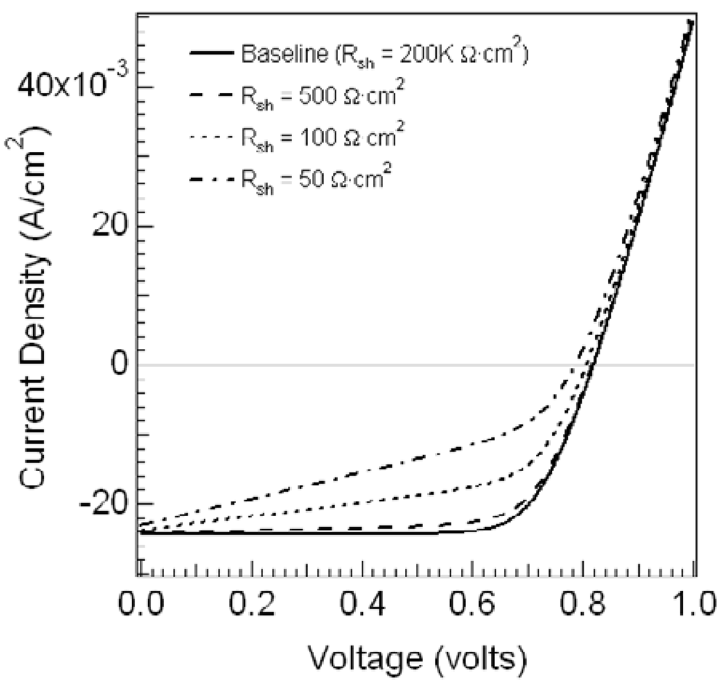


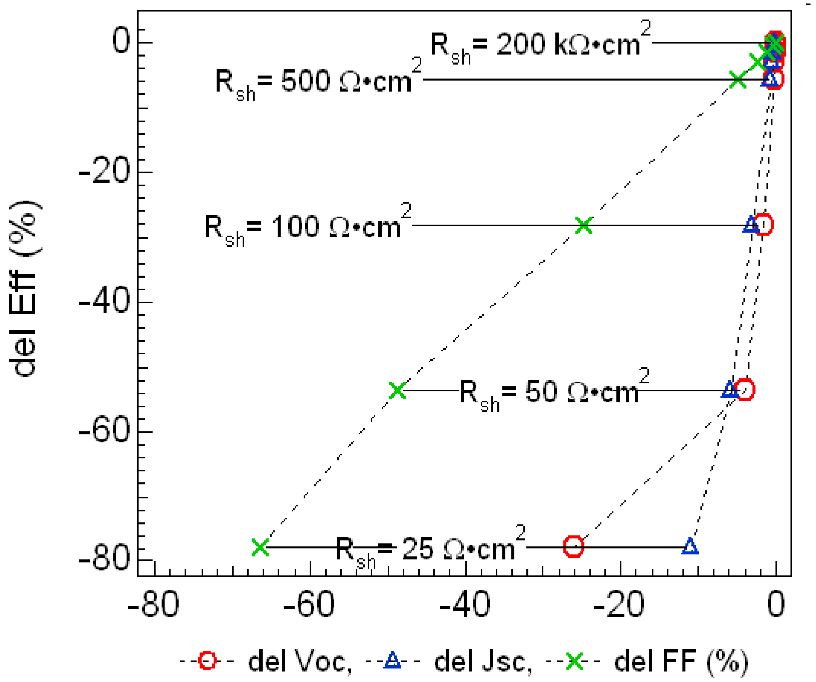


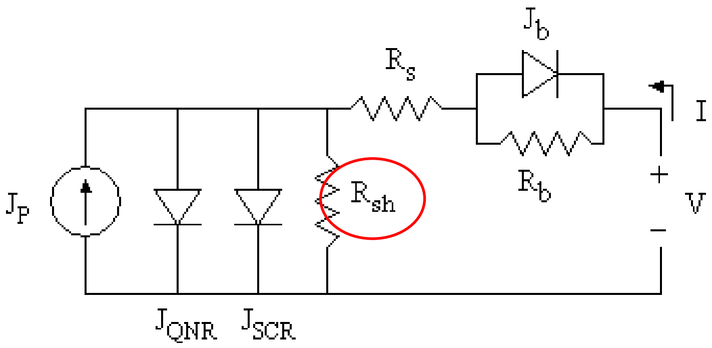


- Unless R_s degrades significantly (catastrophic), no effect on ΔV_{oc} and ΔJ_{sc}
- Generally, only affects FF

Simulating R_{sh} decrease

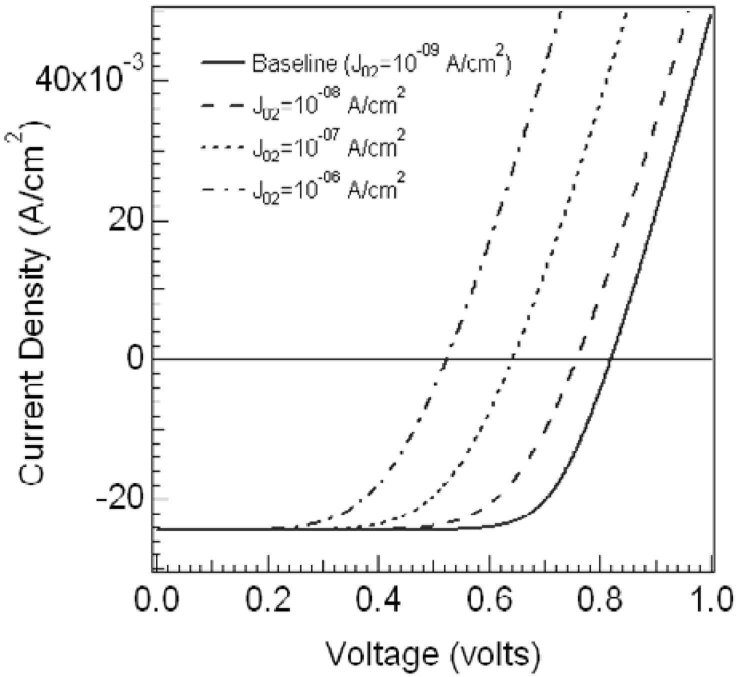


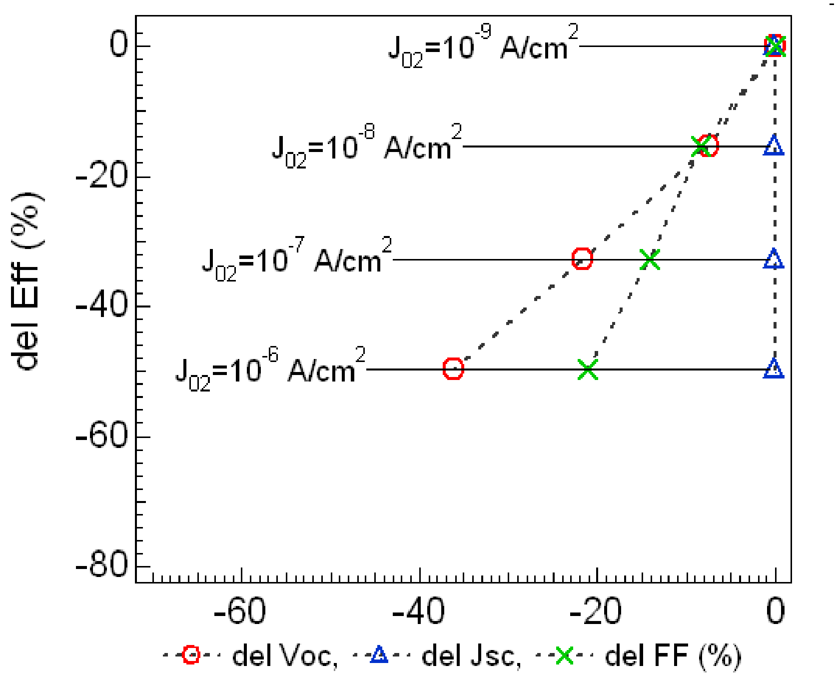


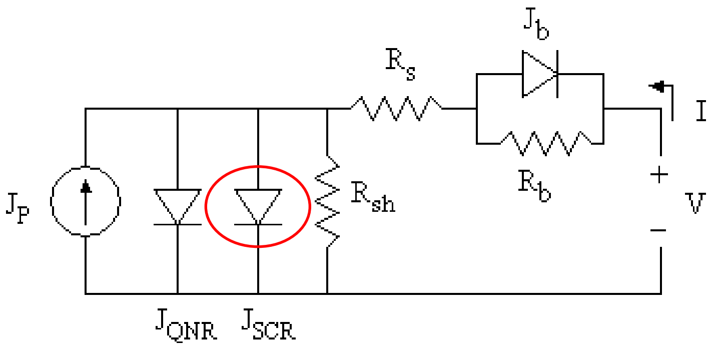


- **Unless catastrophic, effect on ΔV_{oc} and ΔJ_{sc} > - 5 %**
- **Primarily affects FF**

Simulating J_{SCR} increase (increased recombination)

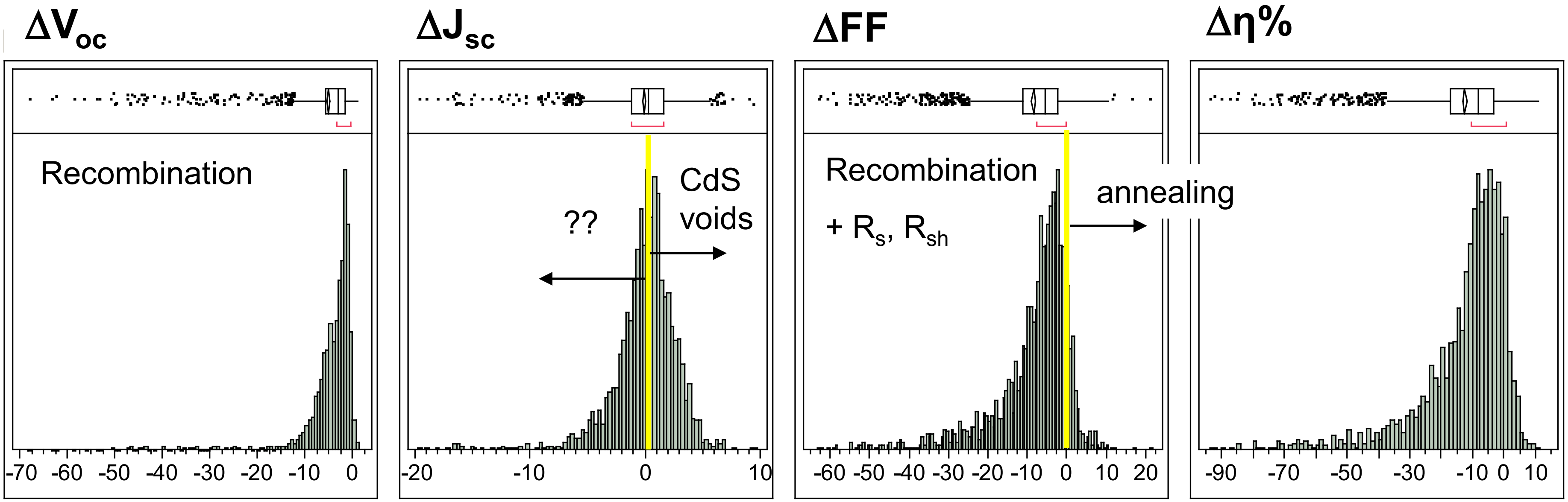






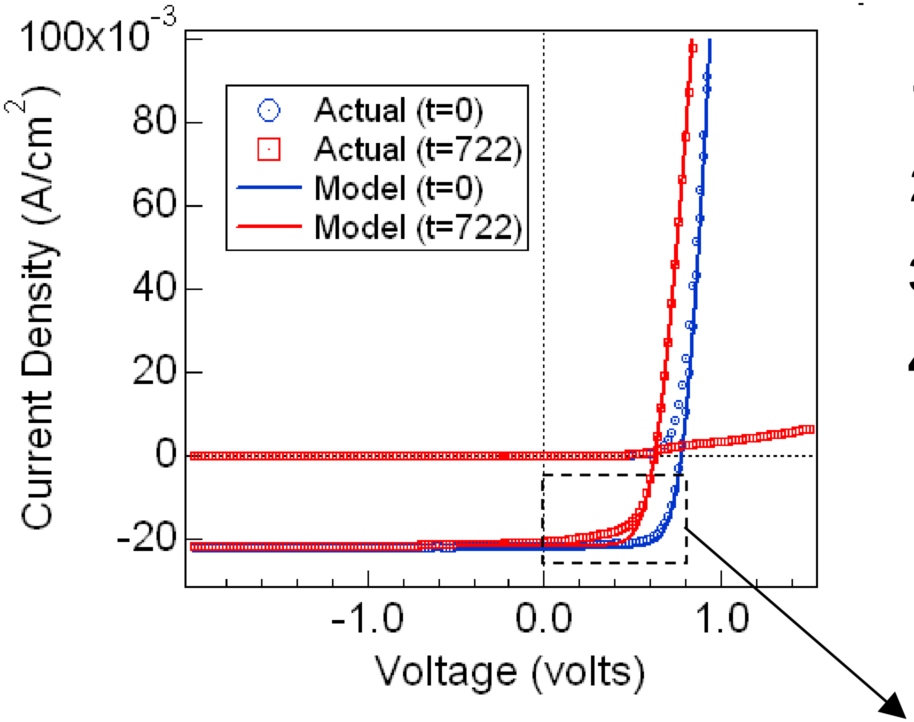
- **Recombination only real way to explain ΔV_{oc} decrease**
- **Again, <u>no effect on ΔJ_{sc}</u>**

Actual observed trends in degradation

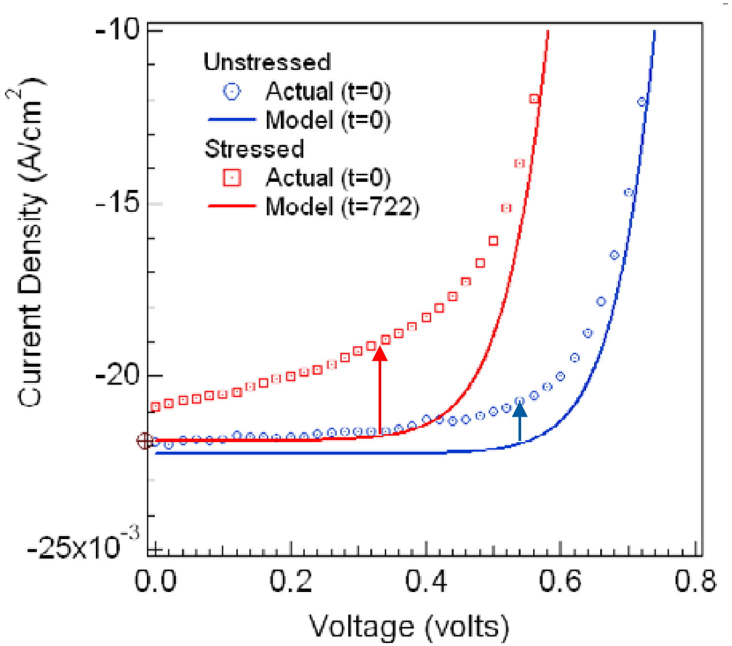


- **Data associated with 2052 measurements performed on "standard" CdS/CdTe devices (CBD CdS)**
- **Behavior in ΔV_{oc}, ΔFF predicted by simulations**
- **$\Delta Jsc > 0\%$ CdS voids – see SPIE (2008)**
- **$\Delta J_{sc} < -5\%$ *not* explained (in absence of *catastrophic* behavior)**

J-V Curve (Actual – Model) = voltage dependent collection



1. Assign J_p at V<<0
2. Assign R_{sh} using dark J-V at V=0
3. Assign R_s using light J-V at V>>0
4. Fit J_{01} J_{02} to fit V_{oc}



Additional Forward Current loss =

voltage-dependent collection

Module Failure Analysis

Current Failure Analysis approach for modules

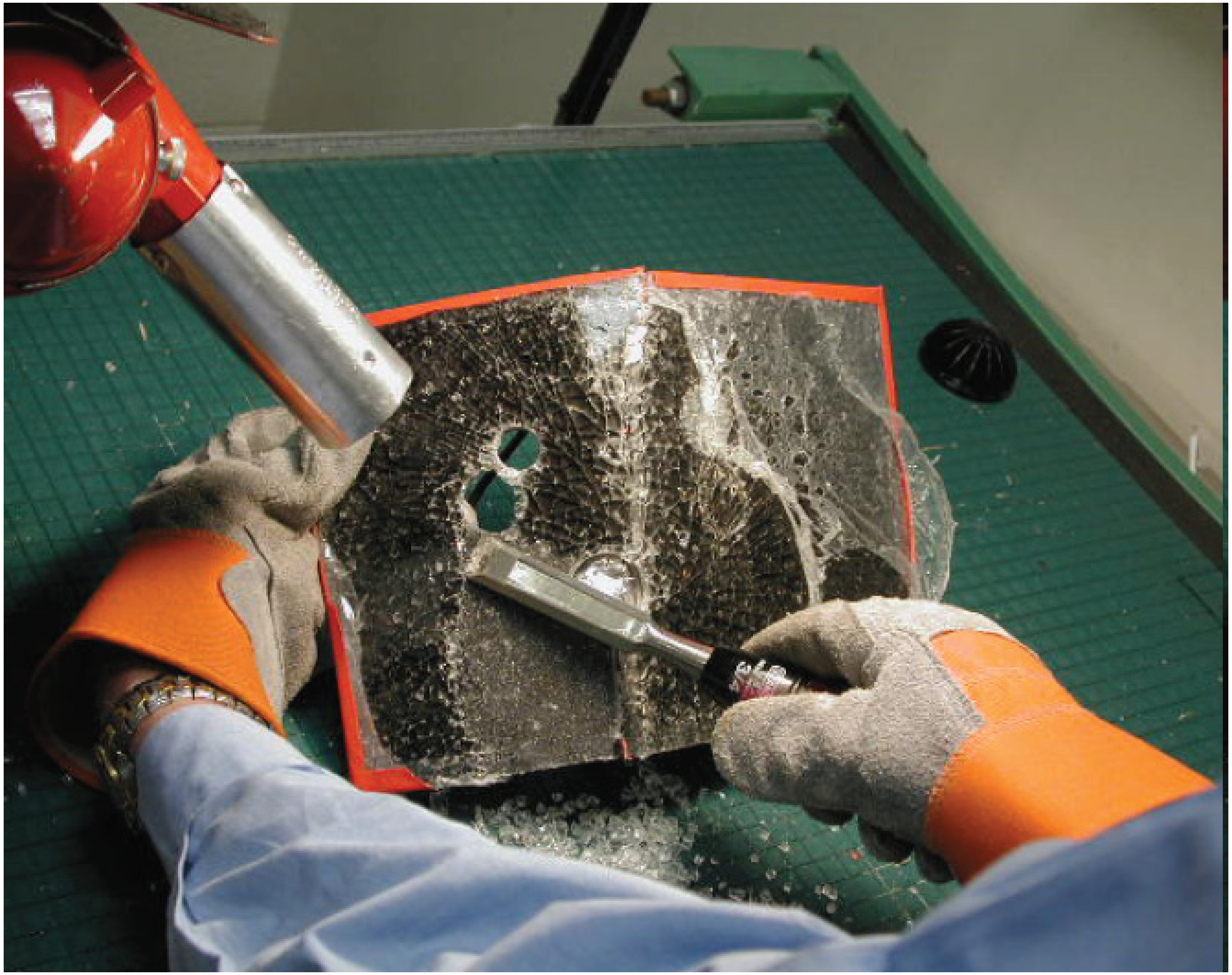
First find defect

- Visual (common)
- Non-invasive techniques (also for analysis)
  1. Emission Spectroscopy
     1. Light-beam induced Current (LBIC)
     2. Electroluminescence (EL)
     3. IR Thermography
  2. Physical Mapping
     1. X-ray Tomography
     2. Ultrasonic Probing, Scanning Acoustic Microscopy (SAM)

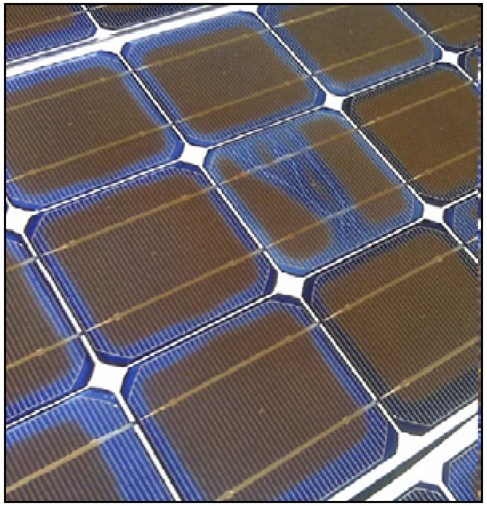
Defect analysis

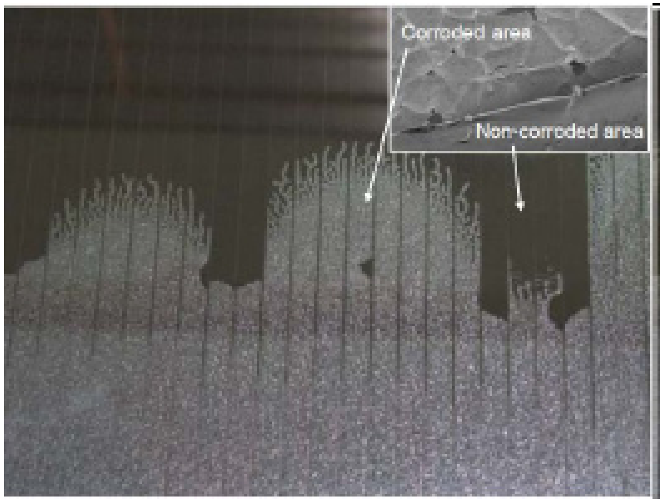
1. Non-invasive techniques (same as above)
2. Invasive techniques
   1. Remove defect for analysis
      1. Heat to loosen encapsulant
      2. Tempered Glass
         1. Coring method – preheated Al ring bonded to glass – localized compressive stress minimizes shatter
      3. Non-tempered glass
         1. “Tape and Break”
   2. Apply conventional micro-analysis and characterization techniques
      1. Compositional and Chemical Analysis (EDX, AES, XPS, SIMS, FTIR)
      2. Structural (microscopy, SEM)

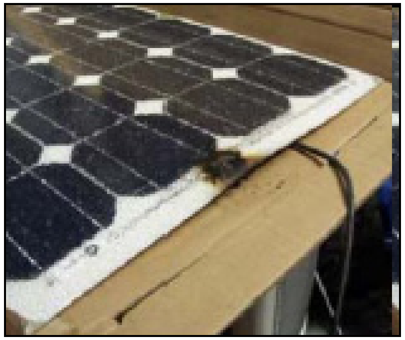
Getting to the defect can be messy

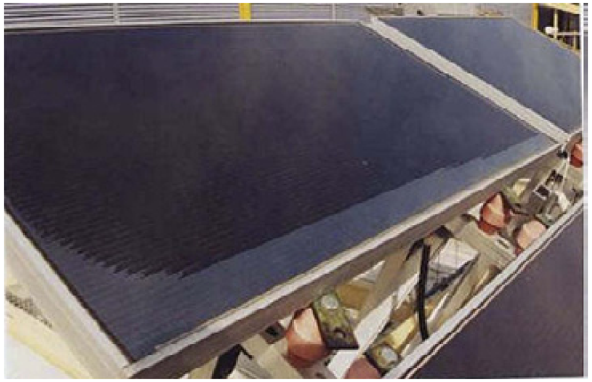


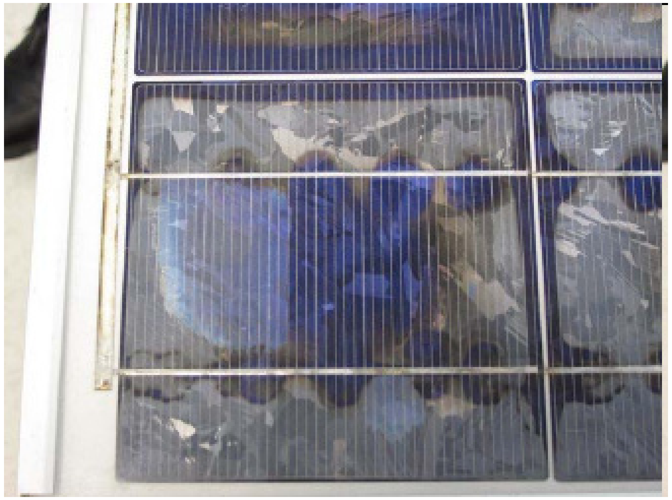
Some failures are visually obvious



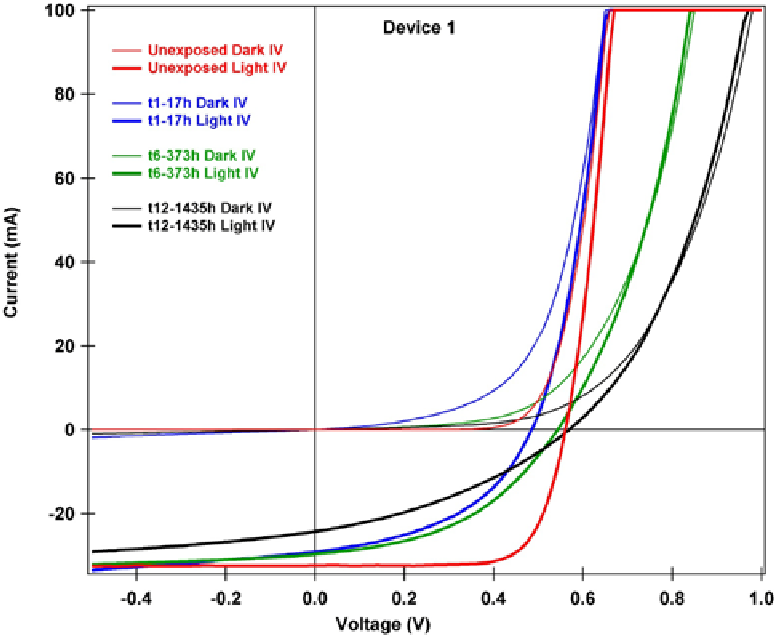








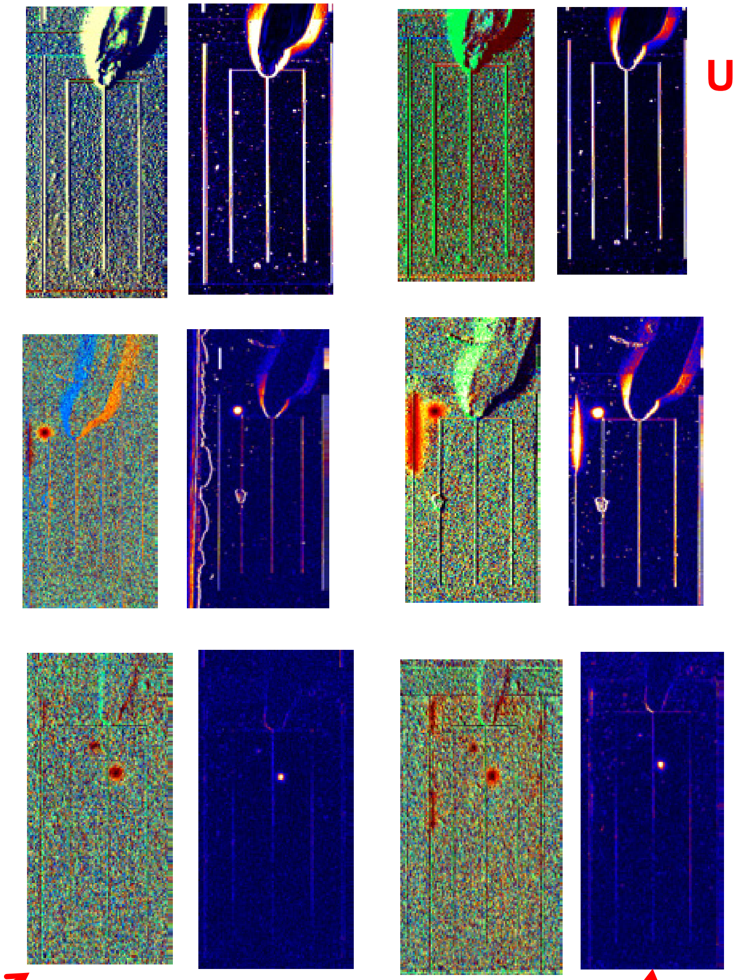
Thermography



Courtesy of R. Sundaramoorthy (NREL)

Reverse Bias

Forward Bias



Unexposed

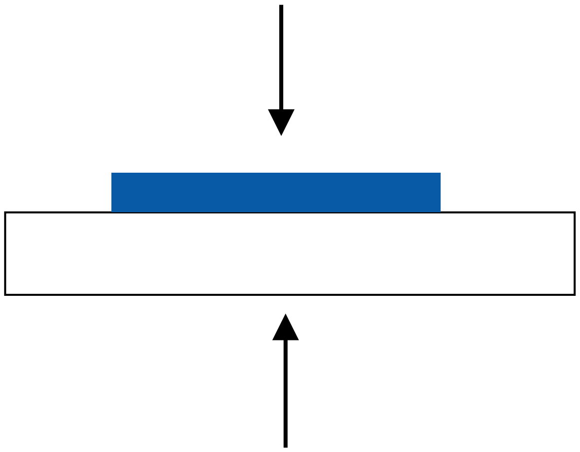
T=17h

T=373h

Thermal-lock-in Phase image

Thermal-lock-in IR image

Thermography (glass reduces resolution)



Cell side

Glass side

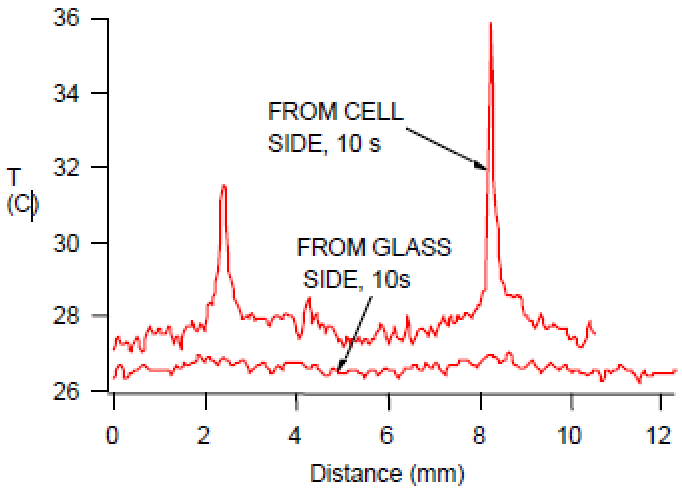
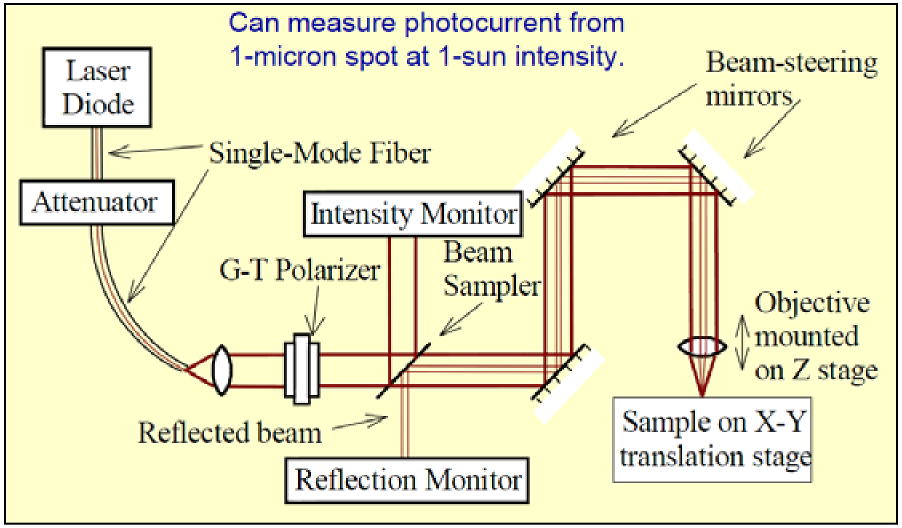


Fig. 4. Temperature profile through point shunts (defects) in CIS cell from IR images recorded of both the cell surface and through the glass substrate, recorded 10 s after -1.1 V reverse bias with 6.9 mA current was applied.

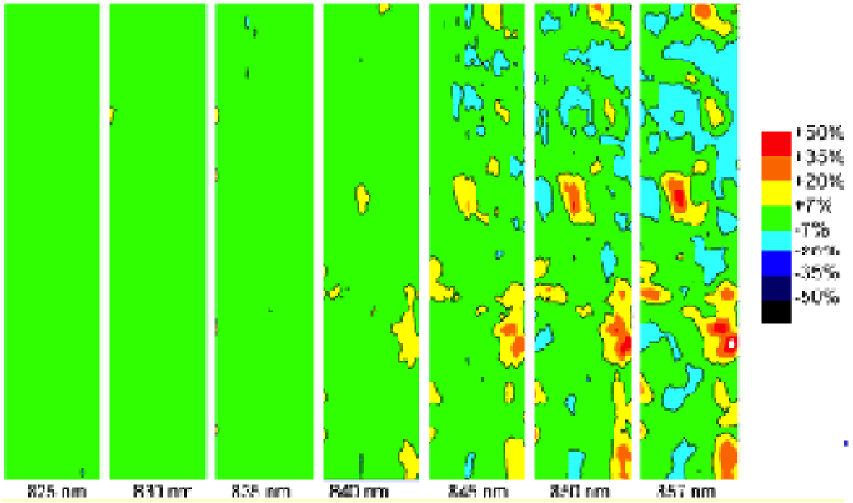
“Applications for Infrared Imaging Equipment in Photovoltaic Cell, Module, and System Testing”, King et al.,

Light beam Induced Current (LBIC)



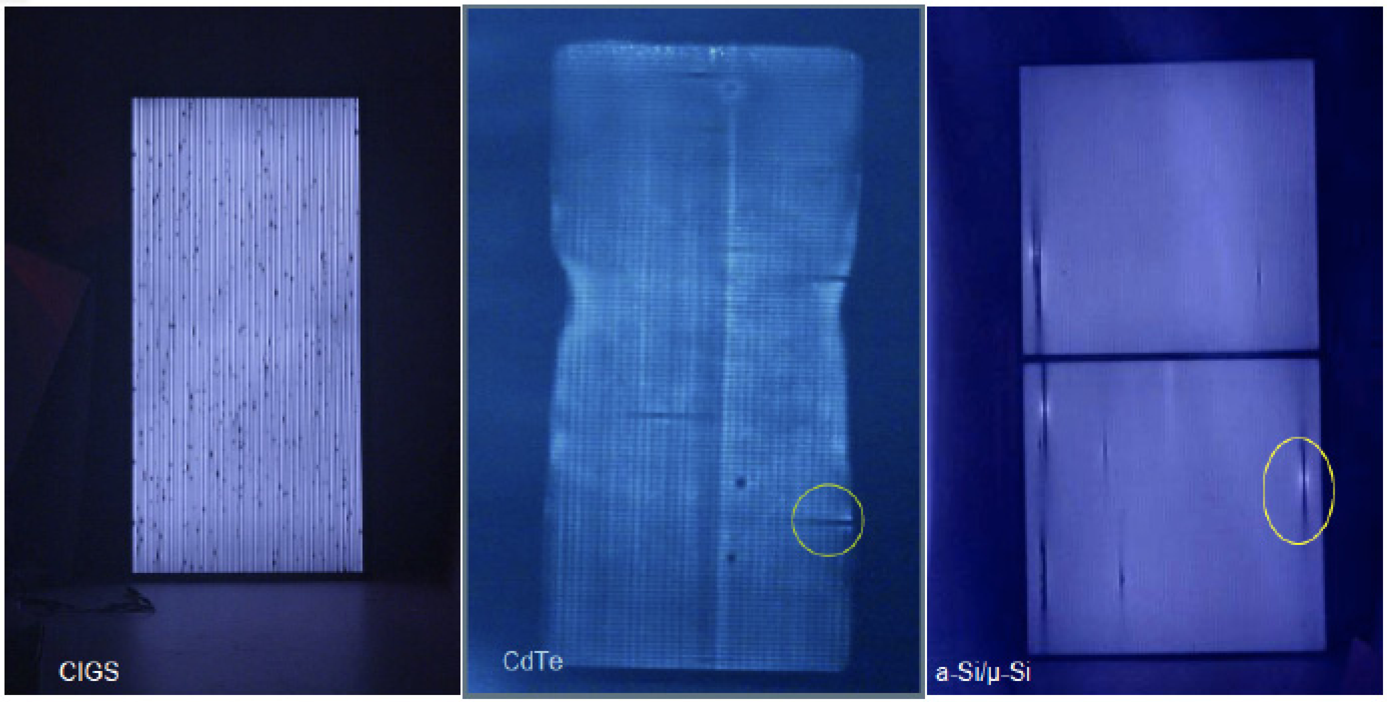
Can measure photocurrent from 1-micron spot at 1-sun intensity.

Sites and Nagle, 31st IEEE - PVSC



Current output across solar cell

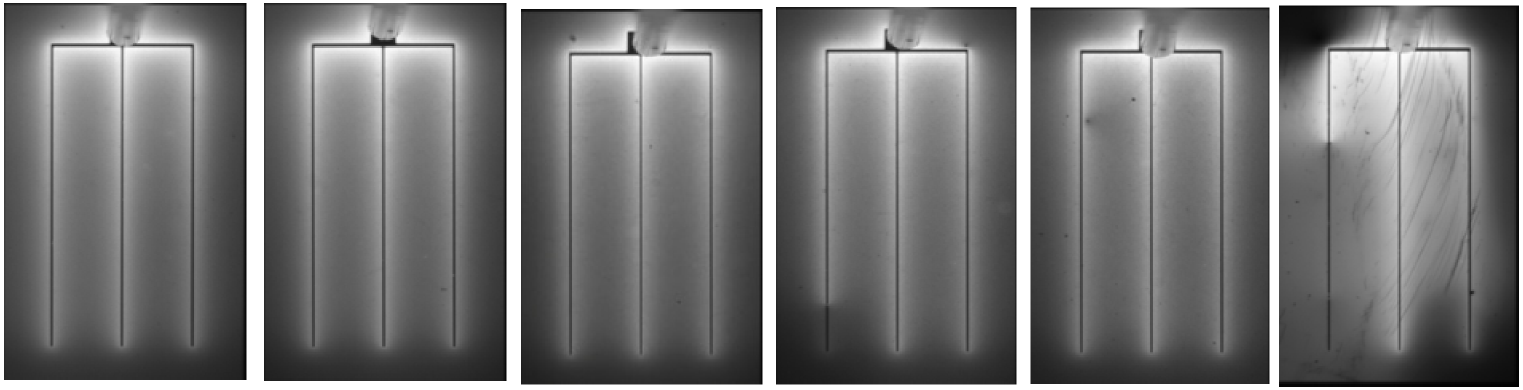
Locating Defects by EL



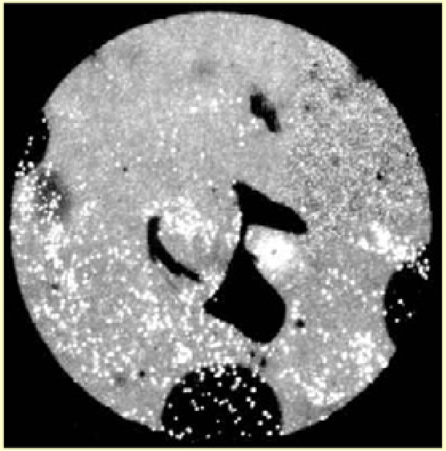
Forward bias electroluminescence NIR imaging

Krauter, PI Photovoltaik-Institut Berlin AG

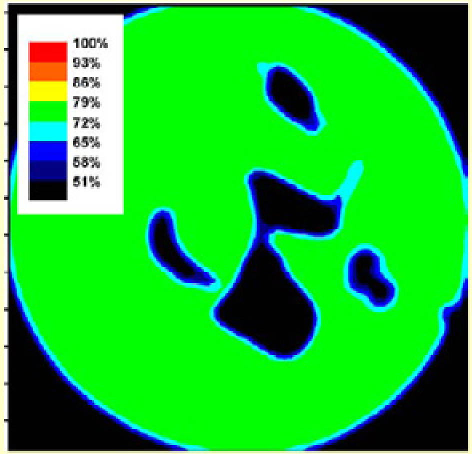
Electroluminescence (EL)



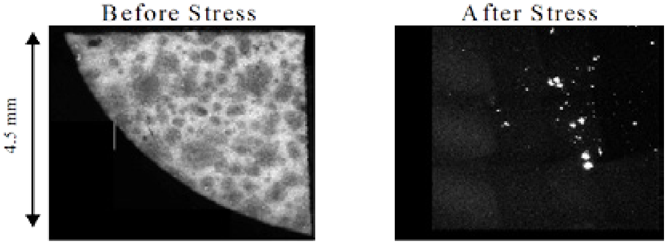
Courtesy of R. Sundaramoorthy (NREL)



Electroluminescence map (Scott Feldman, Colorado School of Mines)



LBIC map of same CdTe cell (Colorado State University)

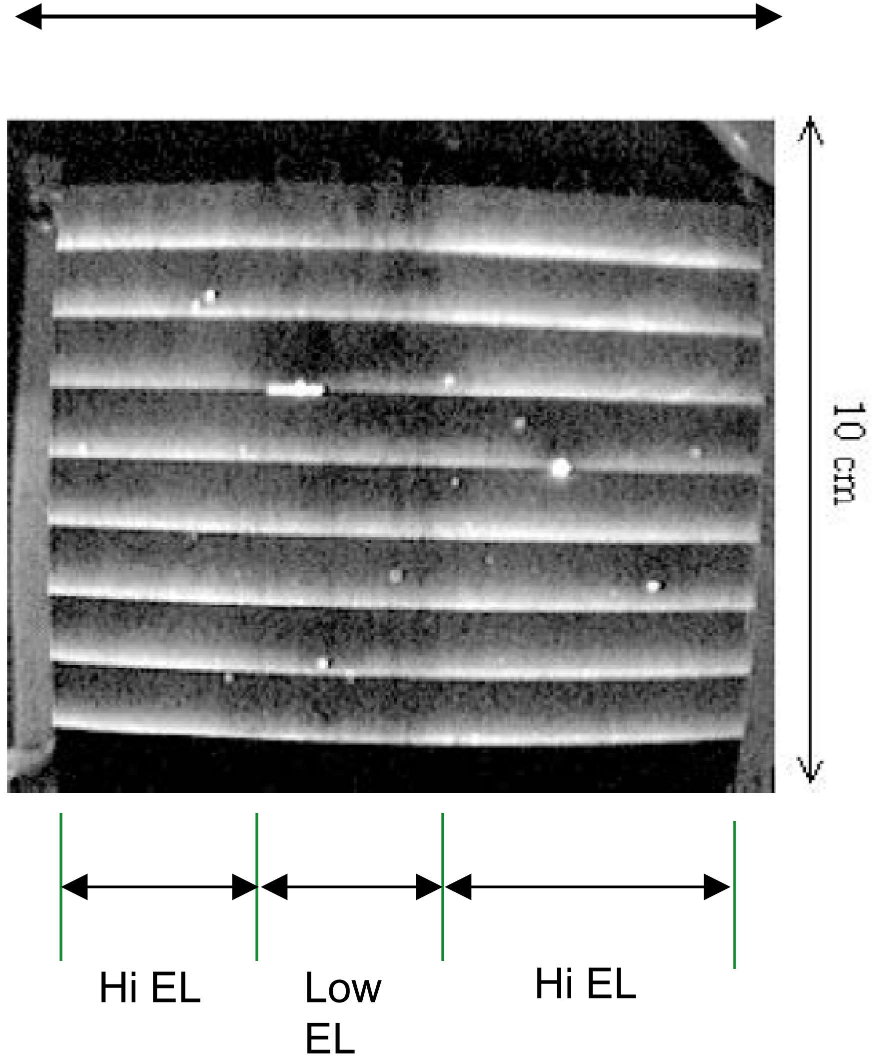


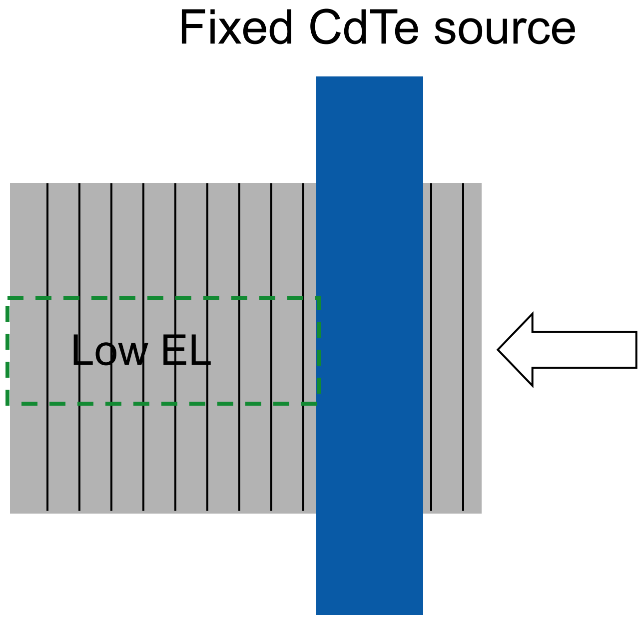
Current density $\gtrsim$ 33 mA/cm^2 for both images.

Bright spots indicate conduction

EL variations related to processing

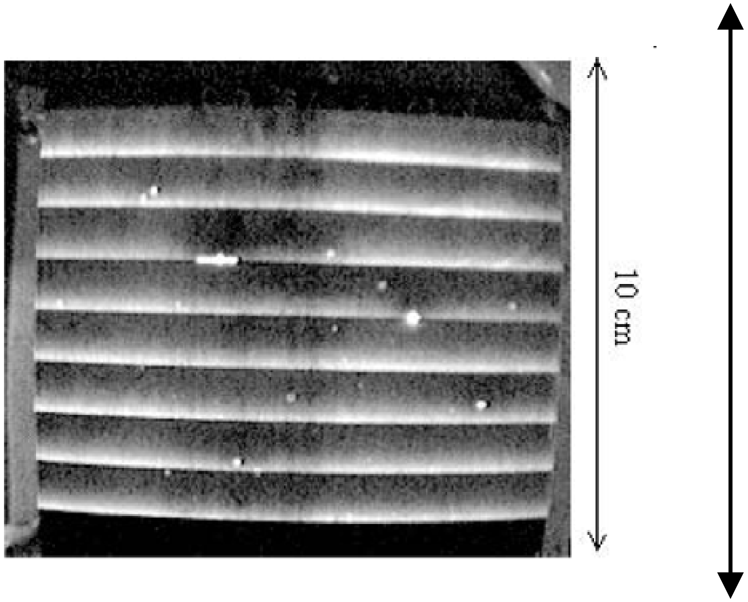
EL variation perpendicular to module motion

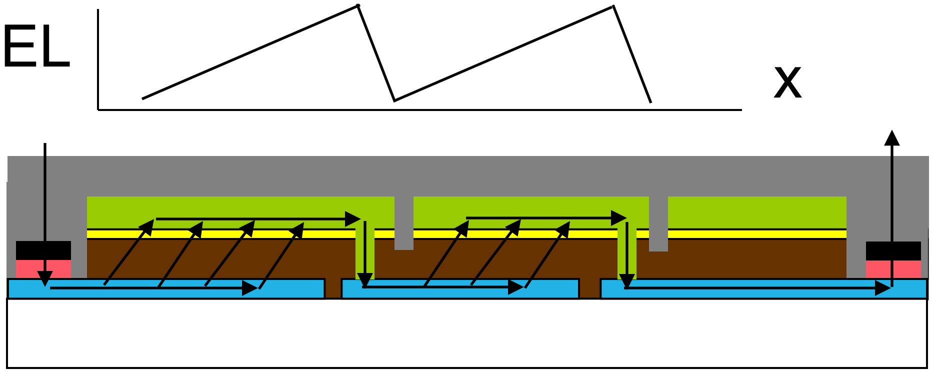




EL variations related to module structure

EL variation parallel to module motion



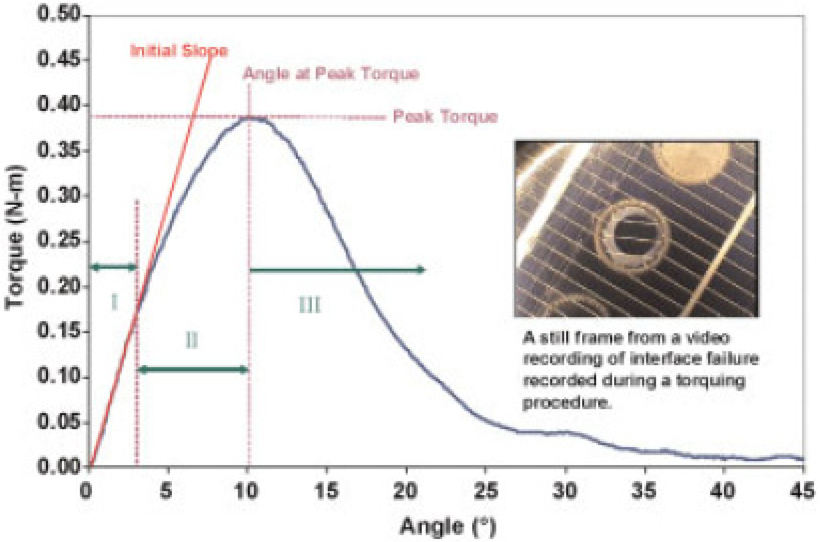


+

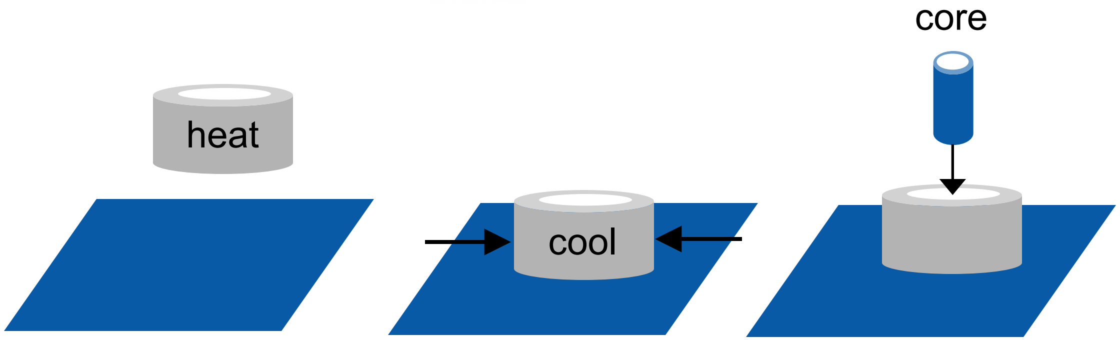
Represents ohmic loses in front and back contacts

Coring (better access to the defect)

Figure 1. (a) System with stepper motor, 5:1 speed reducer, torque sensor, and universal coupler fitting that attaches to a Phillips flat-head screw epoxied to a cored Si cell; (b) close-up image showing details of torque sensor and coupling hardware



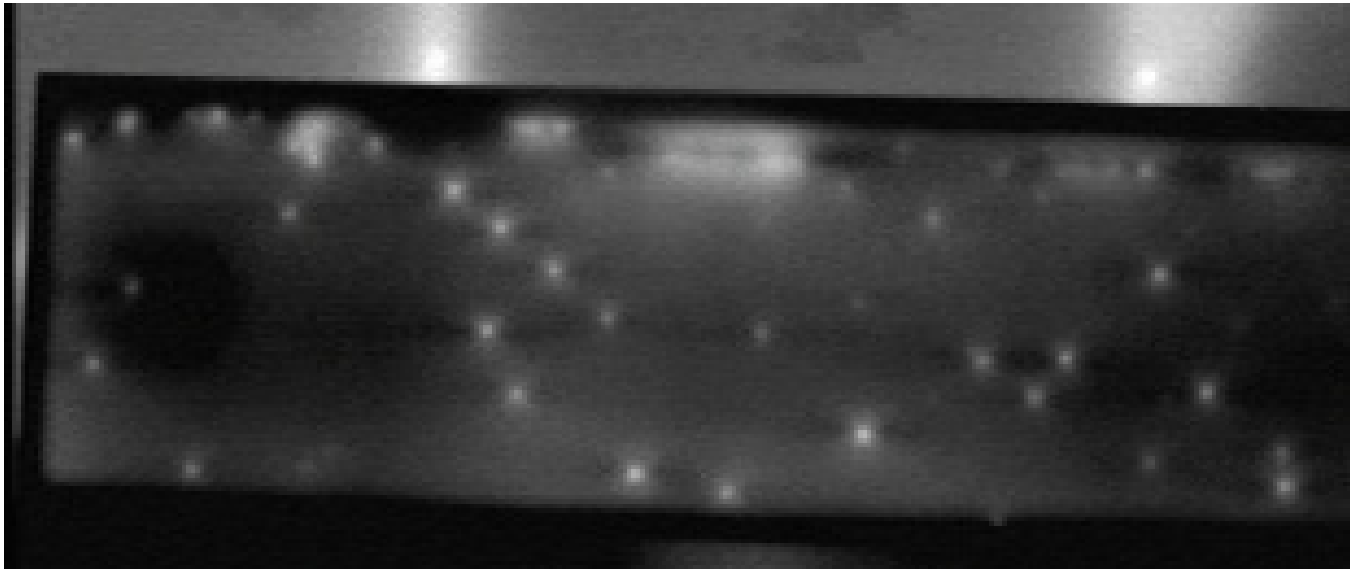
A still frame from a video recording of interface failure recorded during a torquing procedure.

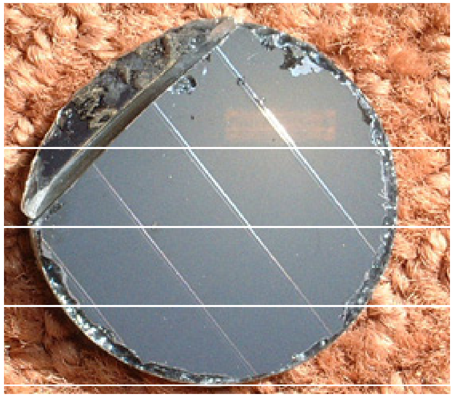


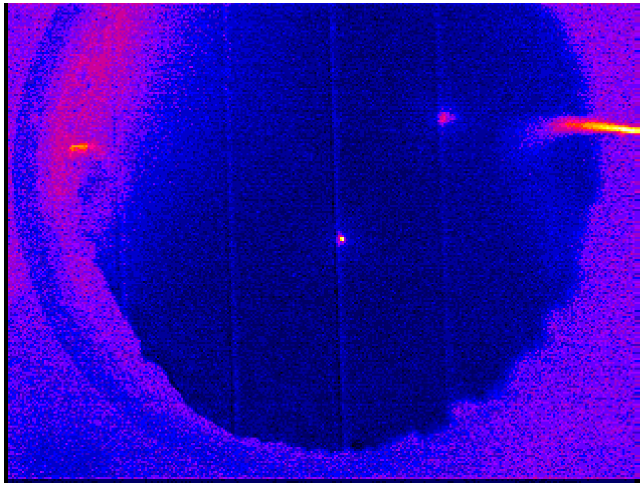
King, et al., Prog. In Photovoltaics: Research and Applications 8(2) (2000)

Jorgensen, et al., Prog. In Photovolt: Res. Appl. 2008 (16) 519-527.

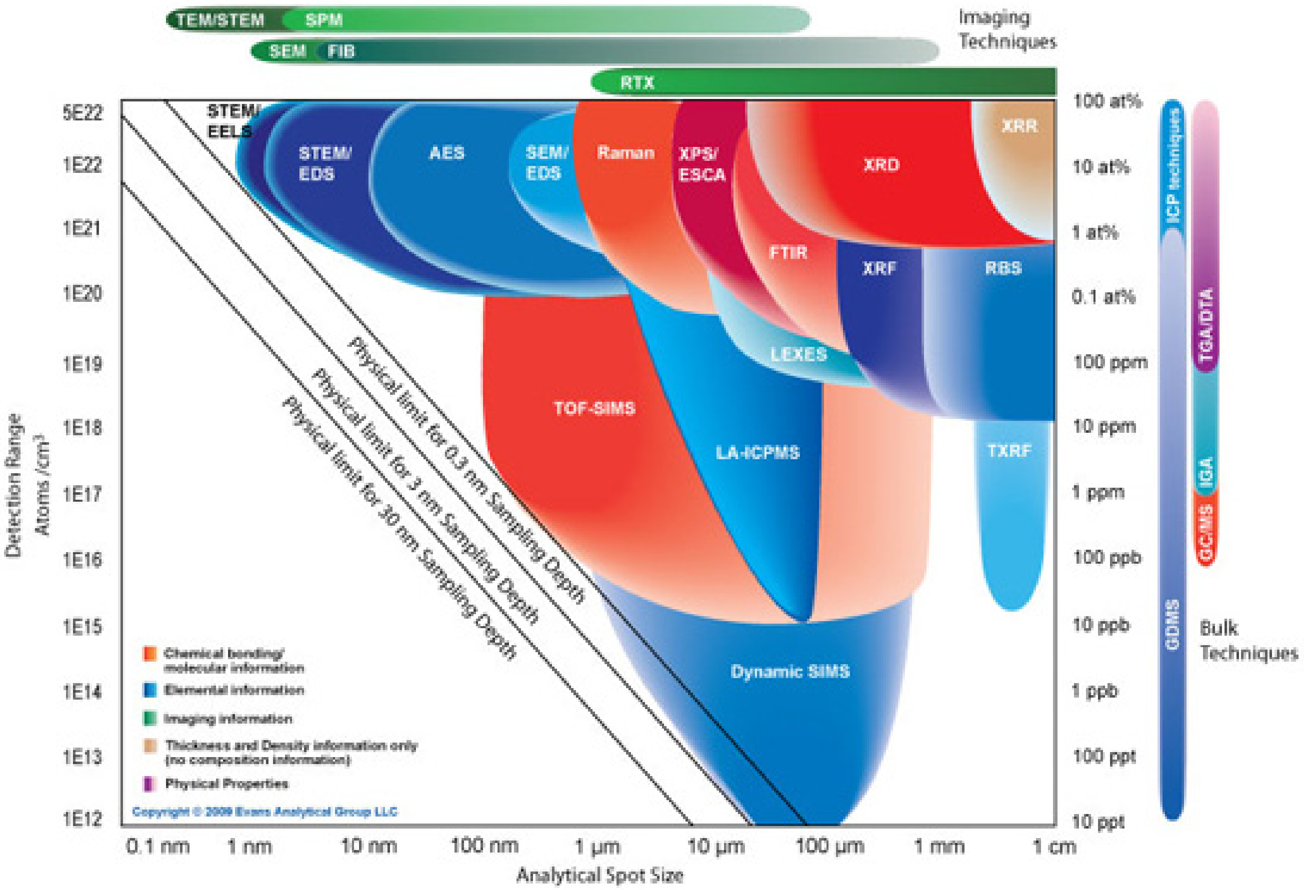
Coring (better access to the defect)







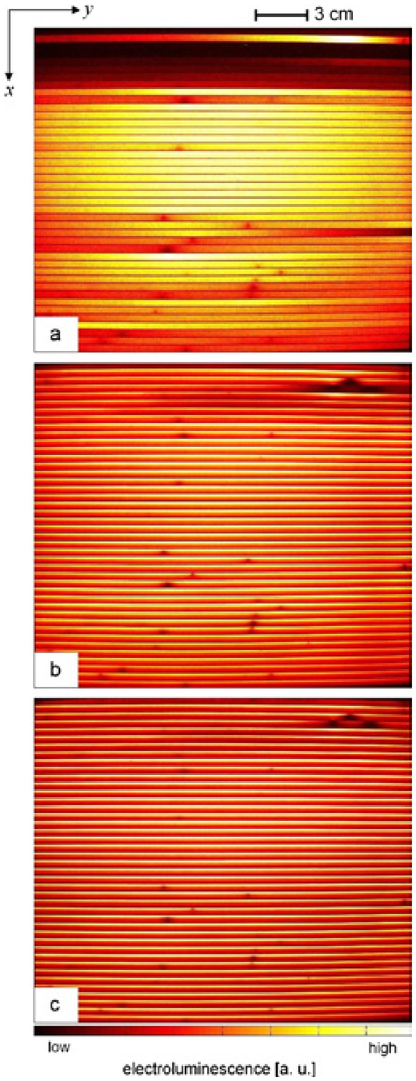
Conventional Surface Analysis Techniques

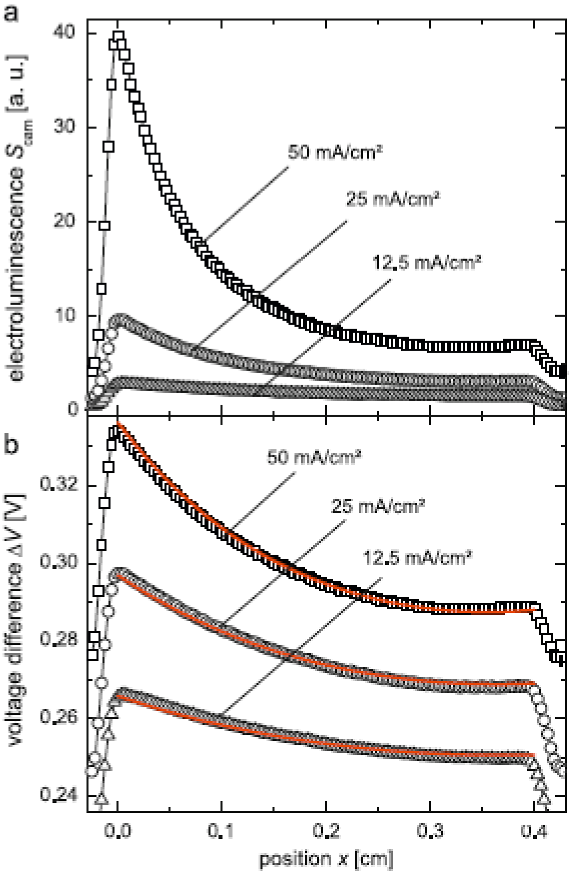


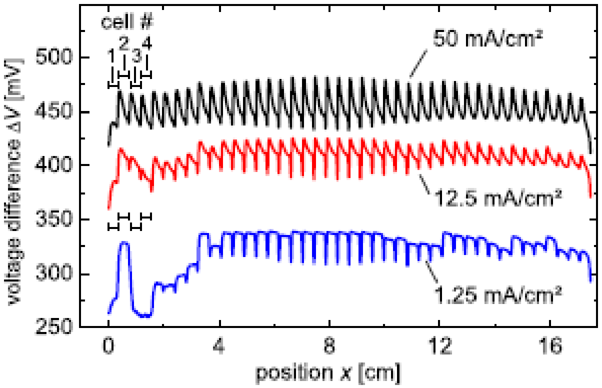
Analytical Resolution versus Detection Limit

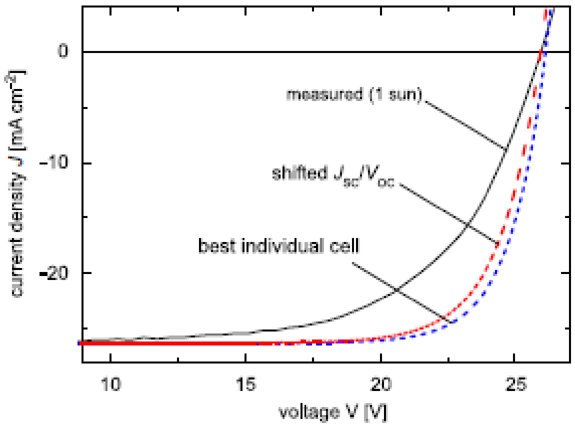
www.cea.com (EAG – Evans Analytical Group Inc.)

Non-invasive Techniques for Failure Analysis (this is the future)





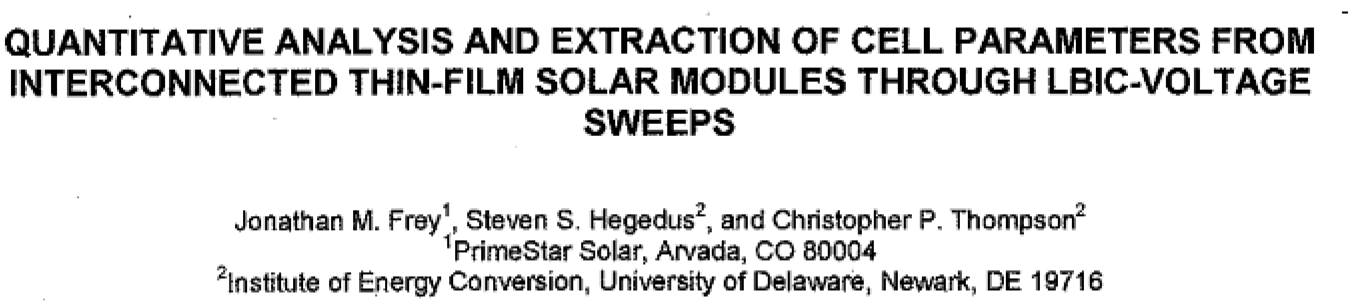




EL modeling allows for individual module cell performance extraction.

A. Helbig et al., Sol. Energy Matls & Solar Cells, 94 (2010)

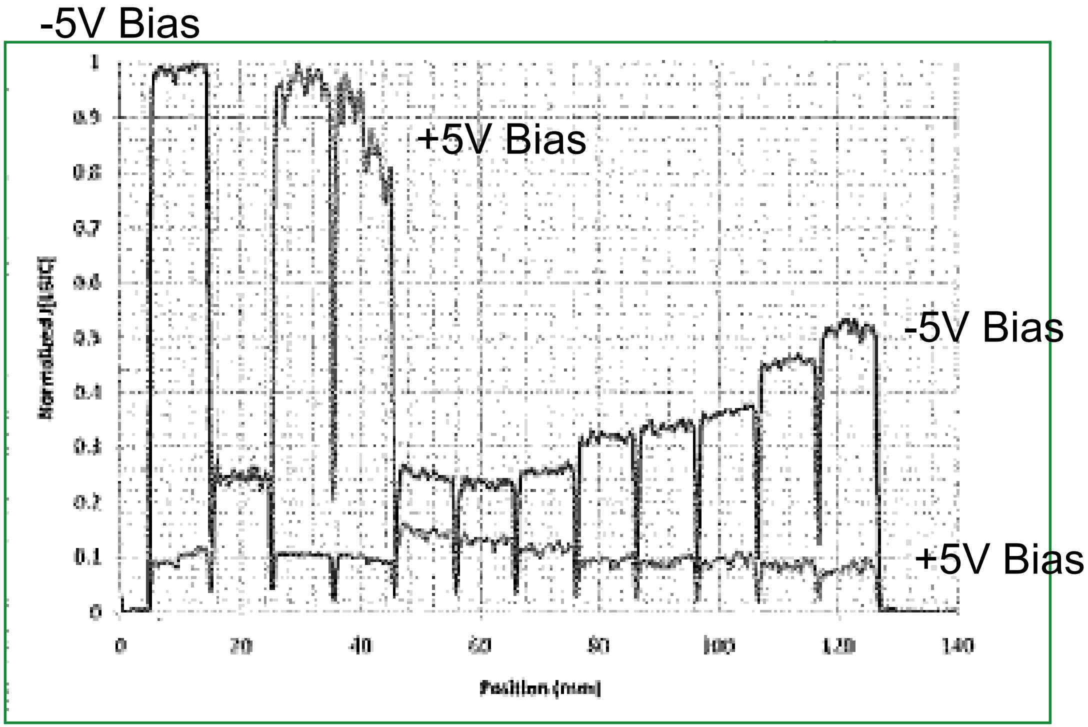
Non-invasive Techniques for Failure Analysis (this is the future)



QUANTITATIVE ANALYSIS AND EXTRACTION OF CELL PARAMETERS FROM INTERCONNECTED THIN-FILM SOLAR MODULES THROUGH LBIC-VOLTAGE SWEEPS

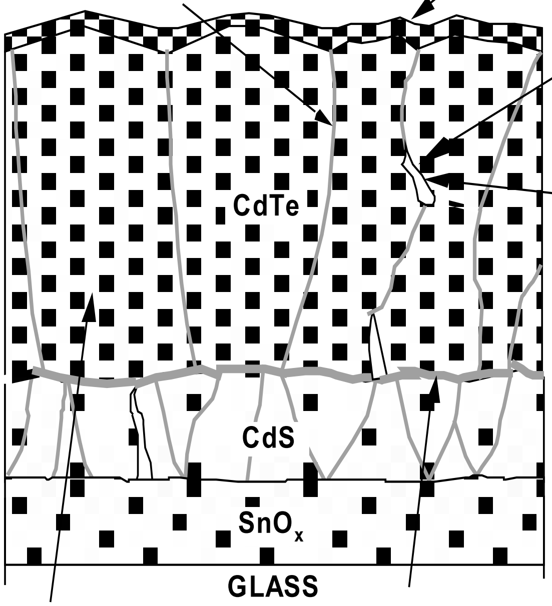
Jonathan M. Frey[1], Steven S. Hegedus[2], and Christopher P. Thompson[2]
[1]PrimeStar Solar, Arvada, CO 80004
[2]Institute of Energy Conversion, University of Delaware, Newark, DE 19716

35th-IEEE Photovoltaic Specialists Conference, Honolulu, HI (2010)



Micro non-uniformities – The big difference between single crystal solar cells and polycrystalline thin film cells both in regards to performance and durability

Polycrystalline Thin Films – very complex



GRAIN BOUNDARY
- potential barrier
- recombination
- enhanced atomic diffusion

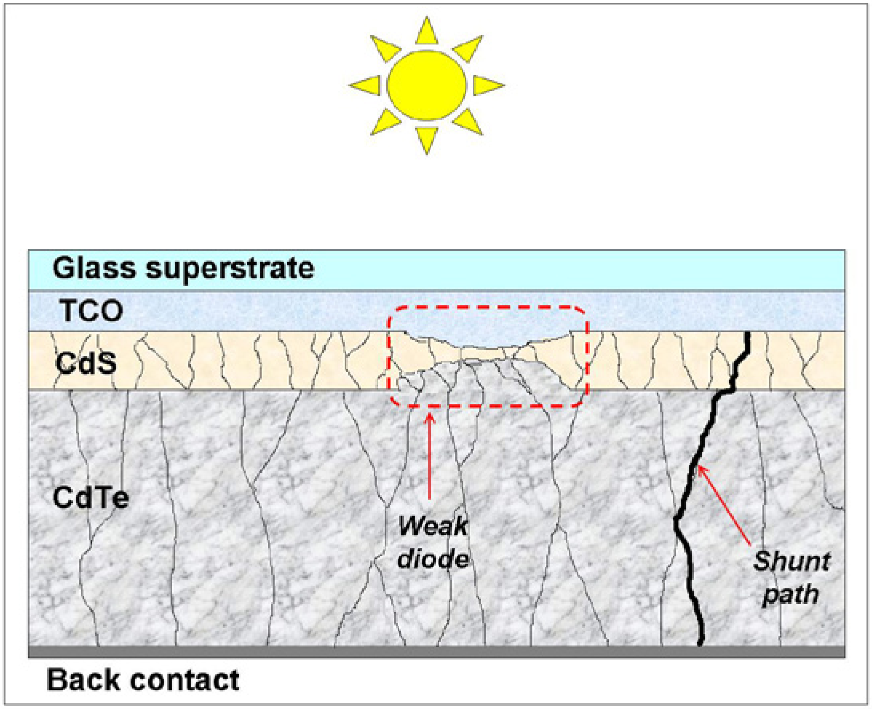
CONTACT

VOID
- gas transport

GRAIN SURFACE
- surface recombinatior
- depletion layer
- enhanced surface diffusion

GRAIN INTERIOR
- bulk recombination

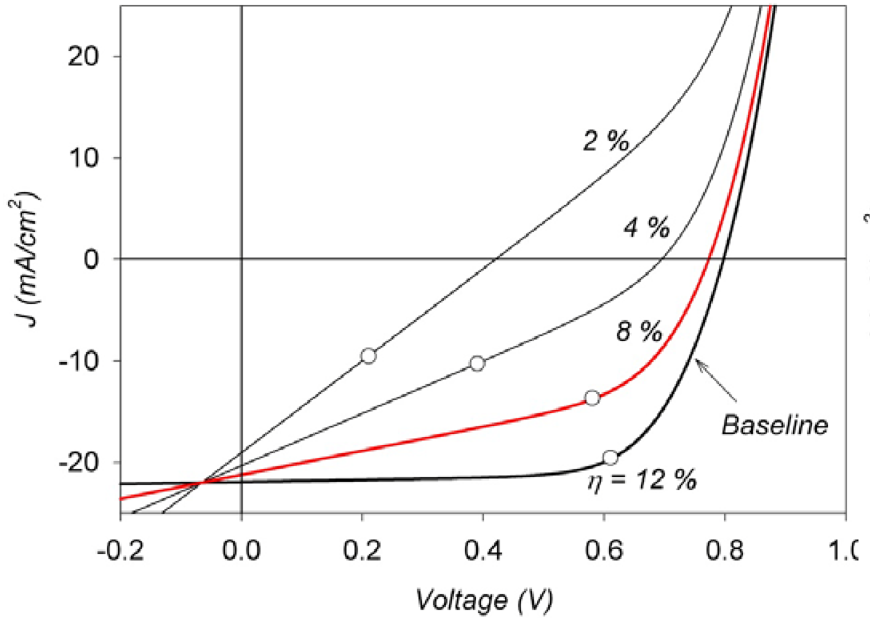
JUNCTION INTERFACE
- interface recombination
- S and Te interdiffusion



Slide from Jim Sites (CSU)

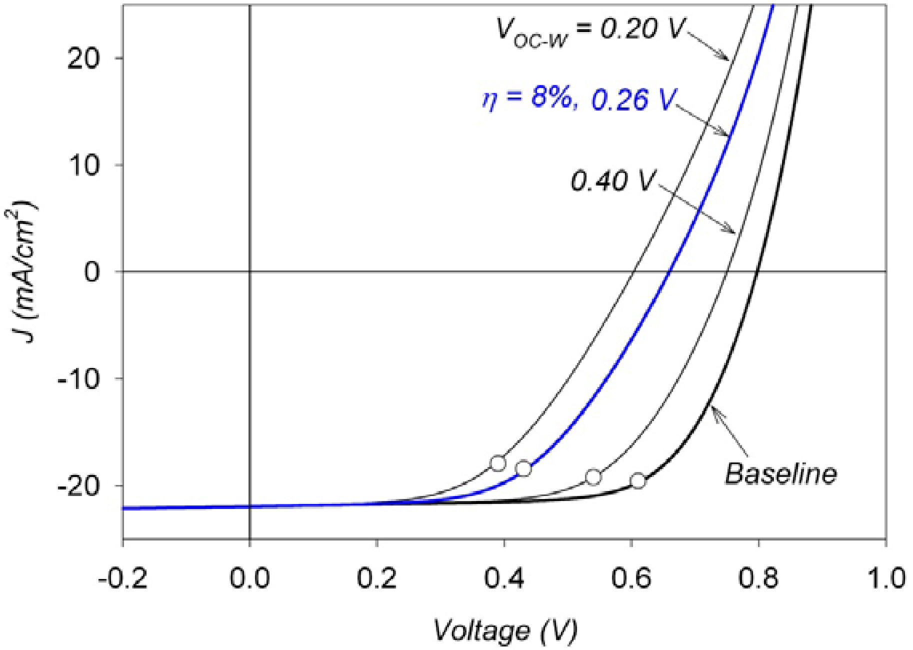
Weak Diodes (combined shunting with lower Jo)

Shunting



Avoid with thick CIGS or CdTe (BUT more material, longer deposition, more recombination)

Lower J_o

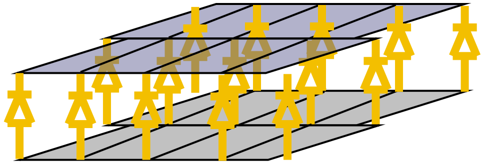


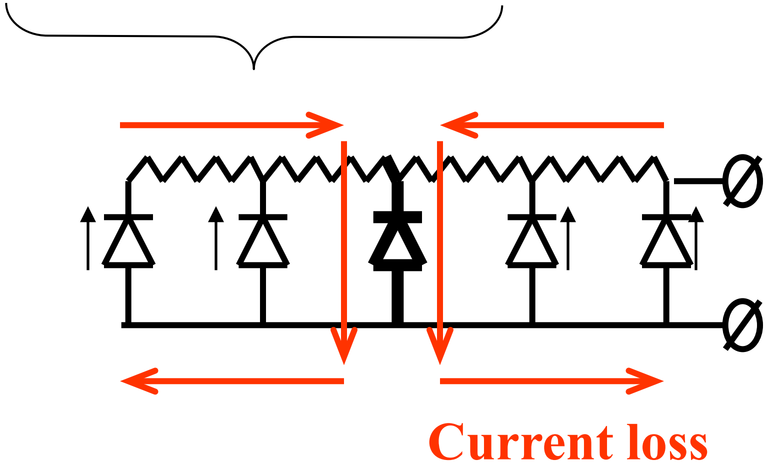
Avoid with thick CdS (BUT lowers current)

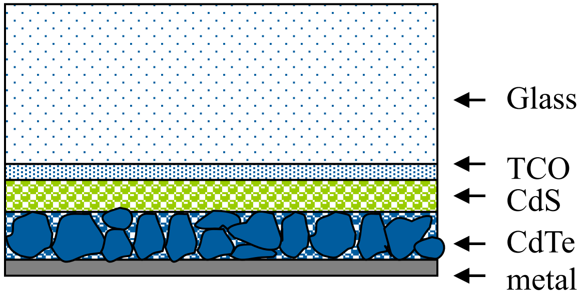
Slide from Jim Sites (CSU)

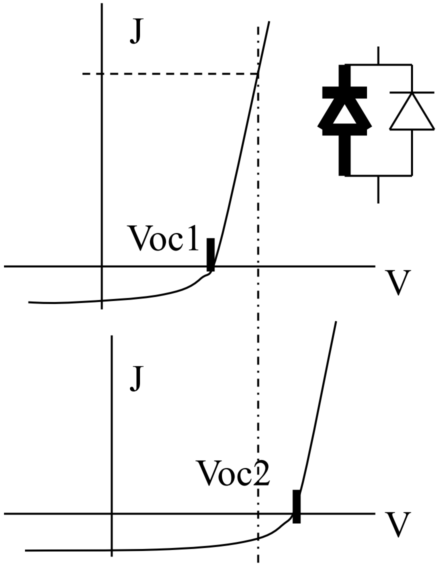
Inhomogeneities: Random Diode Arrays

Polycrystalline cell = random micro-diodes





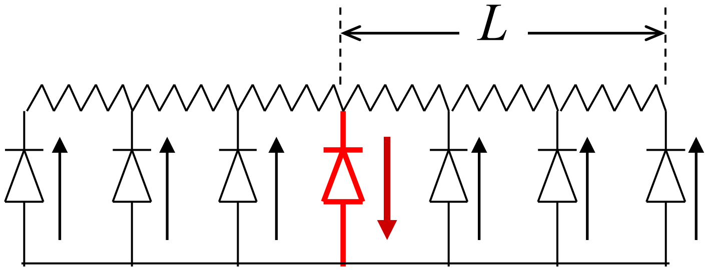


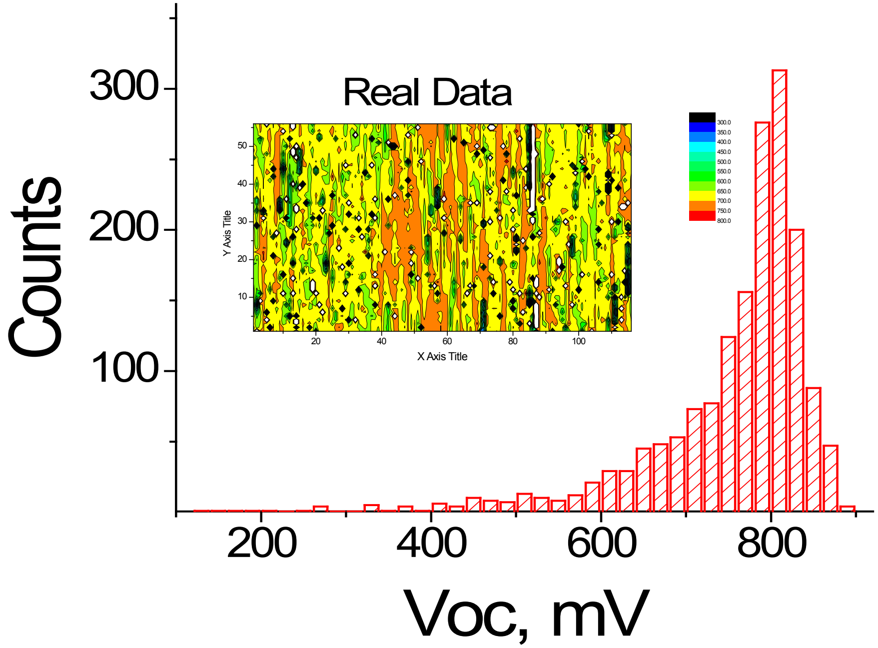


- Weak (low V_{oc}) diodes shunt the system;
- Loss, variability, local stresses on weak elements

Slide courtesy of Victor Karpov (Univ. of Toledo)
victor.karpov@utoledo.edu

Weak diodes are important

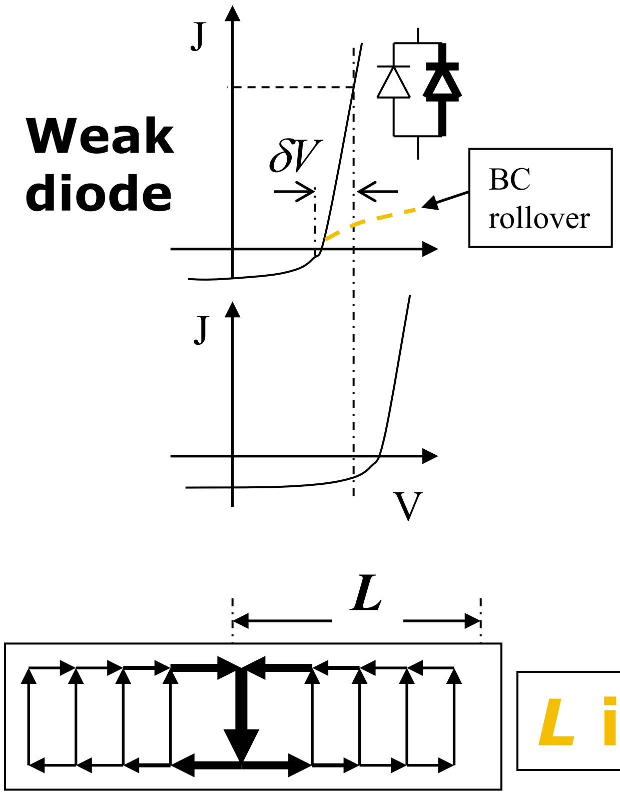




- Cutting large area sample into small pieces allows to measure Voc distribution
- Rare local low Voc elements matter

Slide courtesy of Victor Karpov (Univ. of Toledo)
victor.karpov@utoledo.edu

Lateral screening length of micro non-uniformities



$$L=\sqrt{\frac{kT}{RJ_0}\ln\left(\frac{L}{l}\right)}$$

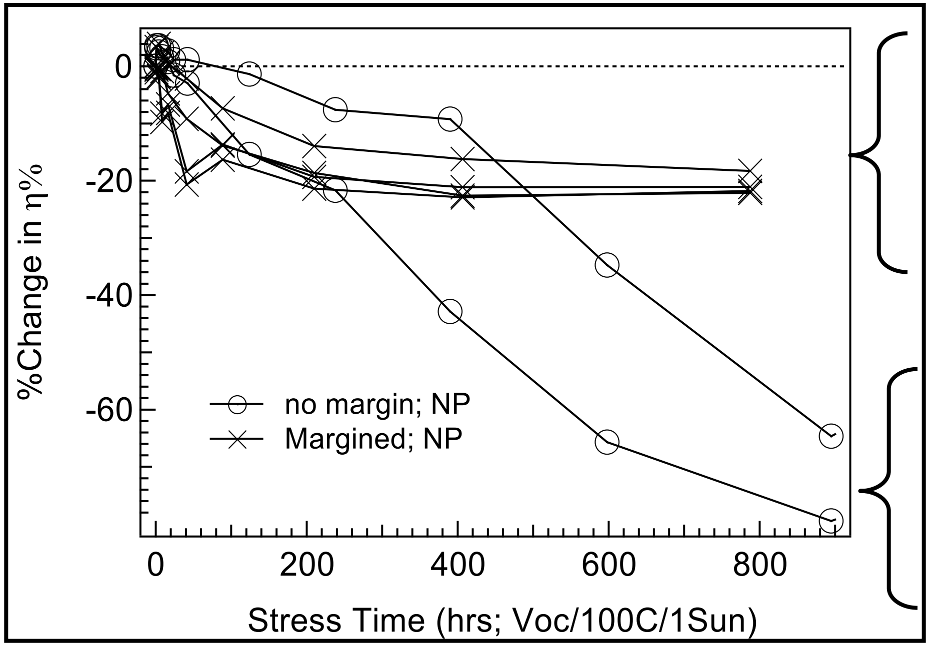
J_0 – short circuit current
R – sheet resistance
l– size of a weak diode ~ 1 μm

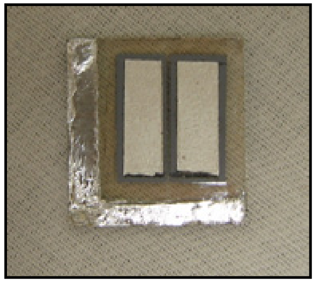
***L* in the range of 1 mm to 1 m**

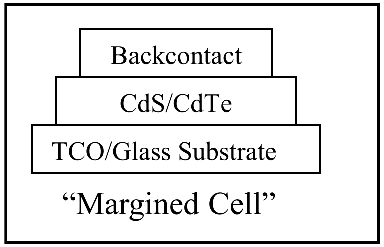
- A micron size weak diode robs currents from a region of *L*;
- Size dependent effects

Karpov et. al. (2001); Nardone et. al. (2008)

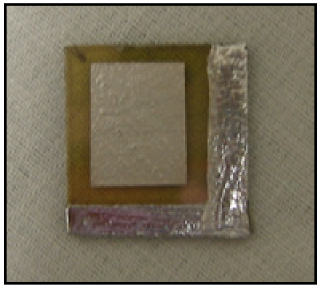
Small Defects and Big Hits to Cell Performance

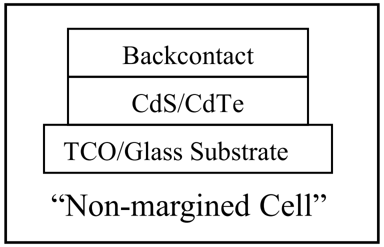






"Margined Cell"

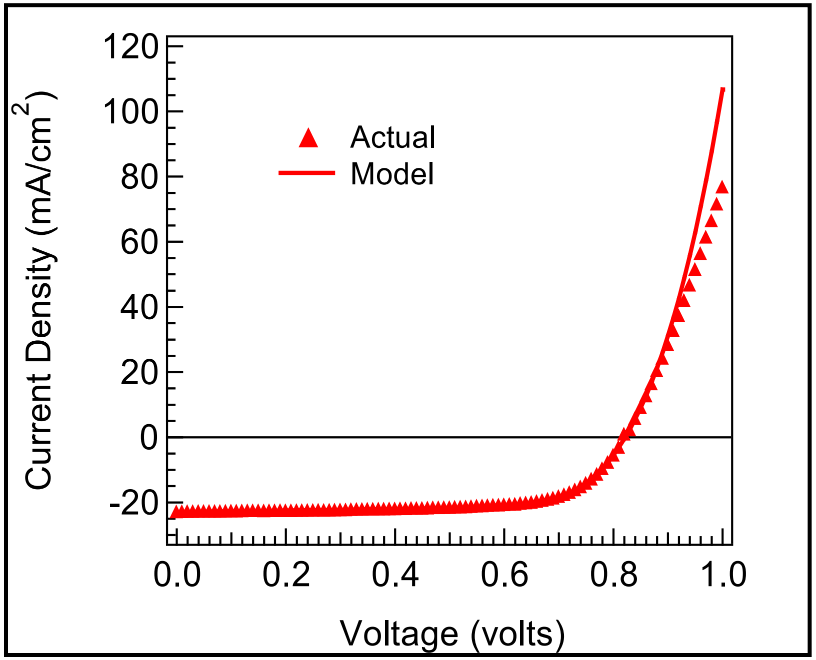




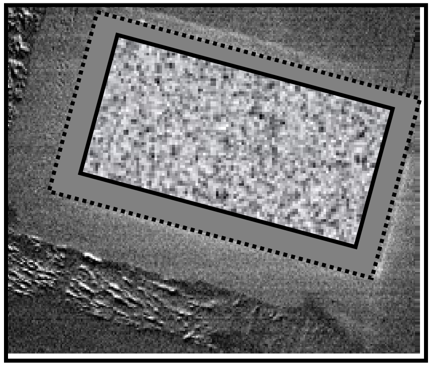
"Non-margined Cell"

- "margined" structure all but eliminates shunting in standard processing; greatly improved statistics
- "stabilized" efficiencies with ALT achieved

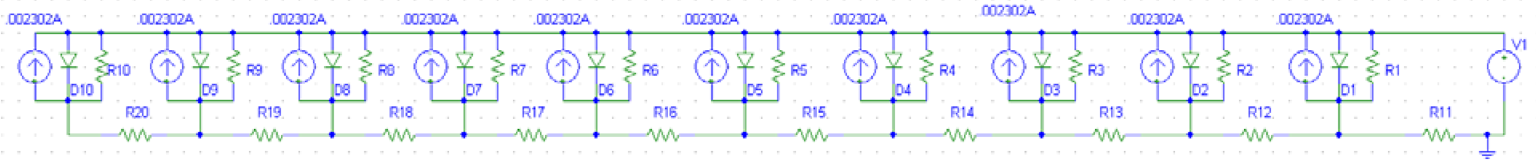
Small Defects and Big Hits to Cell Performance



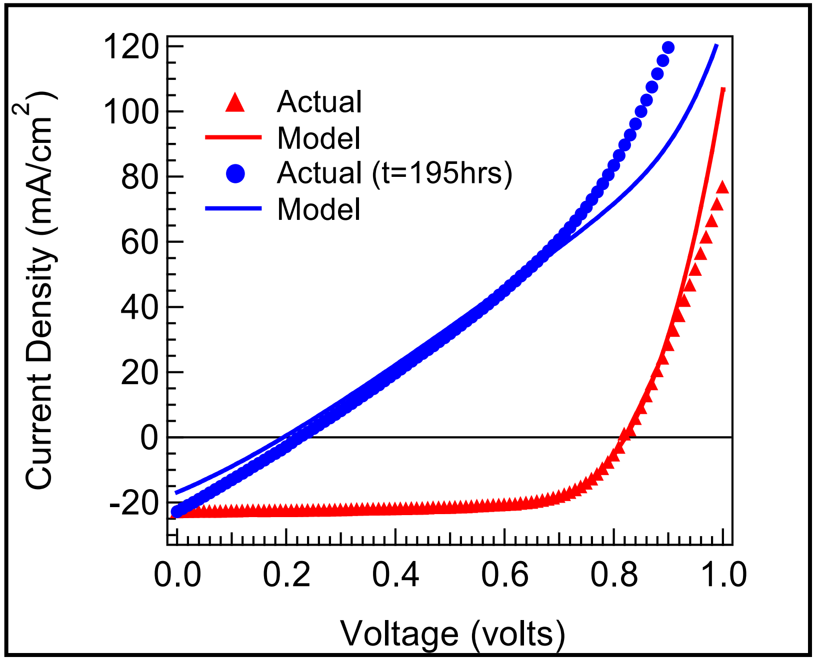
Model	Jo (A/cm2)	A	Rs (ohm*cm2)	Rsh (ohm*cm2)
10 diode distrb.	1.0E-11	1.7	0.4	4.5K



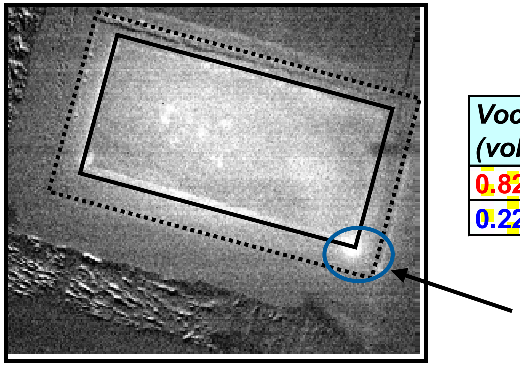
Voc (volts)	Jsc (mA/cm2)	FF	η %
0.820	23.01	69.3	13.1



Small Defects and Big Hits to Cell Performance



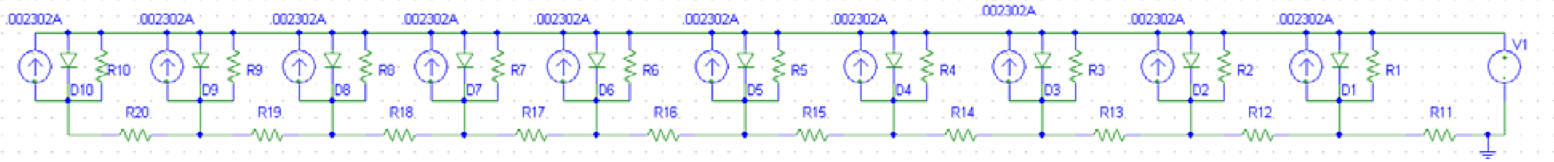
Model	*Jo (A/cm2)*	*A*	*Rs (ohm*cm2)*	*Rsh (ohm*cm2)*
10 diode distrb.	**1.0E-11**	**1.7**	**0.4**	**4.5K**
1 "weak" diode	**2.0E-03**	**2.2**	**0.2**	**20**
9 "stressed" diodes	**1.0E-10**	**1.8**	**0.8**	**4.5K**



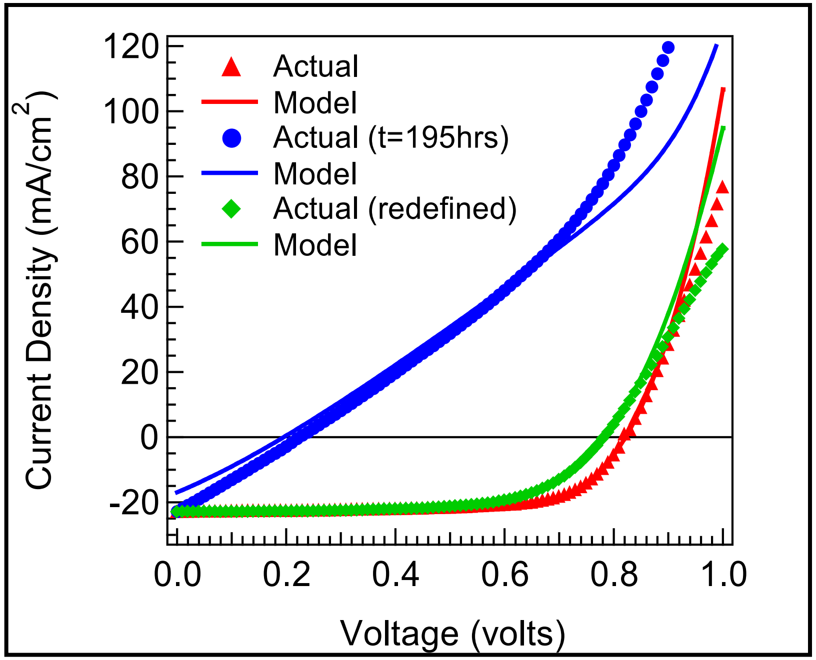
“hot spot”

Voc (volts)	*Jsc (mA/cm2)*	*FF*	η %
0.820	**23.01**	**69.3**	**13.1**
0.225	**22.84**	**25.9**	**1.33**

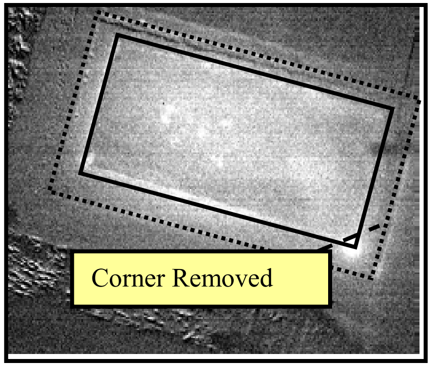
IR Thermography (+1.2V, 6.0 mA)



Small Defects and Big Hits to Cell Performance

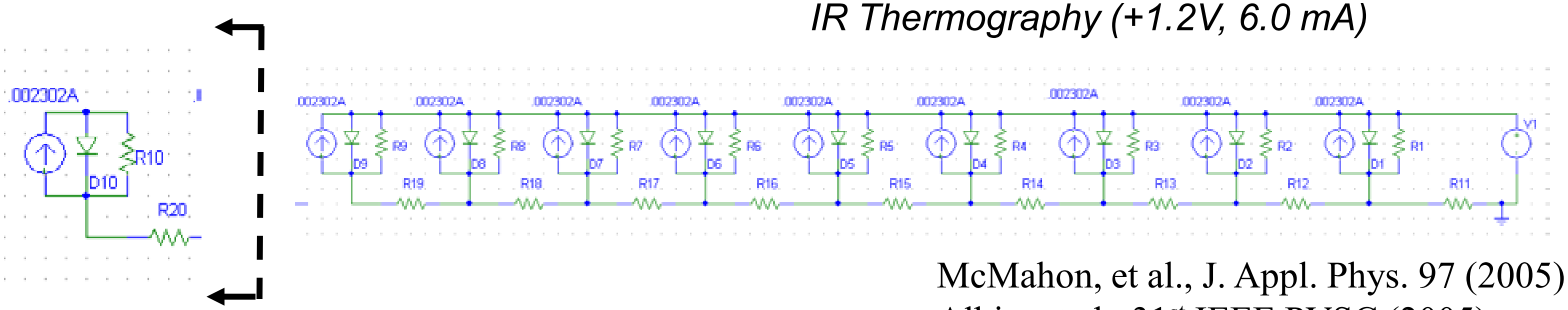


Model	Jo (A/cm2)	A	Rs (ohm*cm2)	Rsh (ohm*cm2)
10 diode distrb.	1.0E-11	1.7	0.4	4.5K
1 "weak" diode 9 "stressed" diodes	2.0E-03 1.0E-10	2.2 1.8	0.2 0.8	20 4.5K
9 "stressed" diodes	1.0E-10	1.8	0.8	4.5K



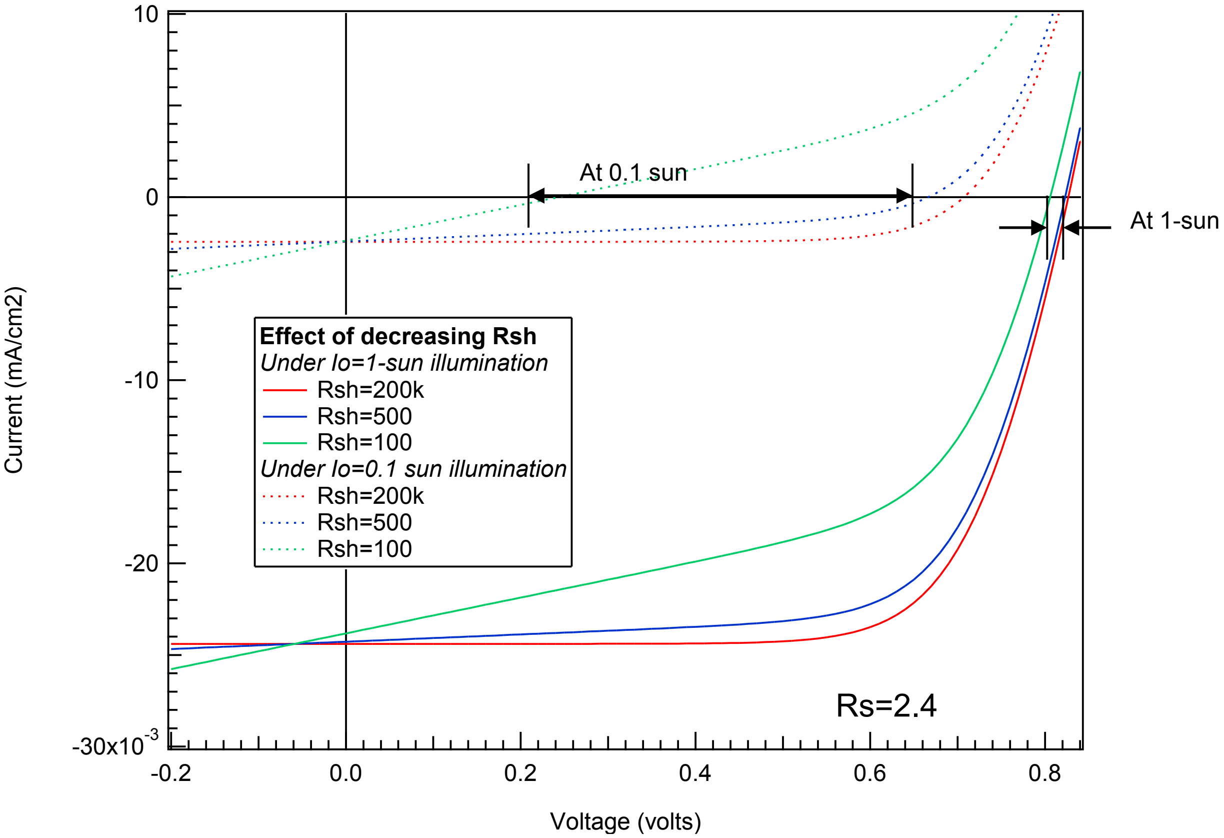
Voc (volts)	Jsc (mA/cm2)	FF	η %
0.820	23.01	69.3	13.1
0.225	22.84	25.9	1.33
0.783	23.01	66.2	11.6

IR Thermography (+1.2V, 6.0 mA)



McMahon, et al., J. Appl. Phys. 97 (2005)
Albin, et al., 31st IEEE PVSC (2005)

Low Illumination Good to Detect Shunt Defects



To detect shunts and weak diodes, reduce the illumination and measure Voc. If a cell has shunts, weak diodes, then Voc will be very sensitive to illumination intensity.

A good pre-test technique to correlate weak shunts with performance during subsequent ALT.

Low Illumination Good to Detect Shunt Defects

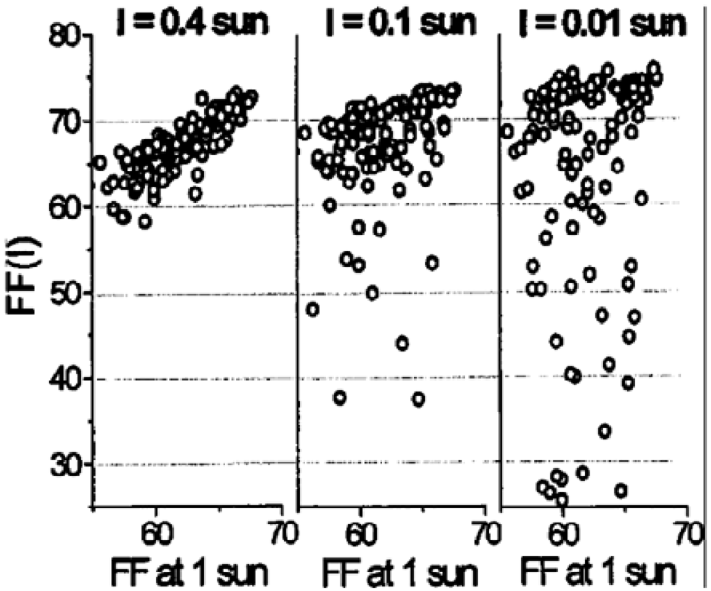


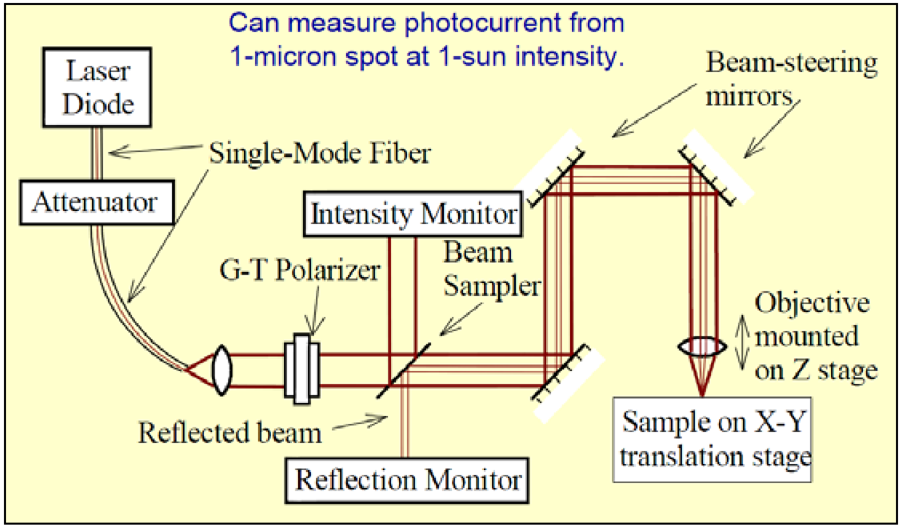
FIG. 4. Correlation between the values of cell FF under 1, 0.1, and 0.01 sun illuminations in the ensemble of 130 standard contact cells.

Low-light divergence in photovoltaic parameter fluctuations

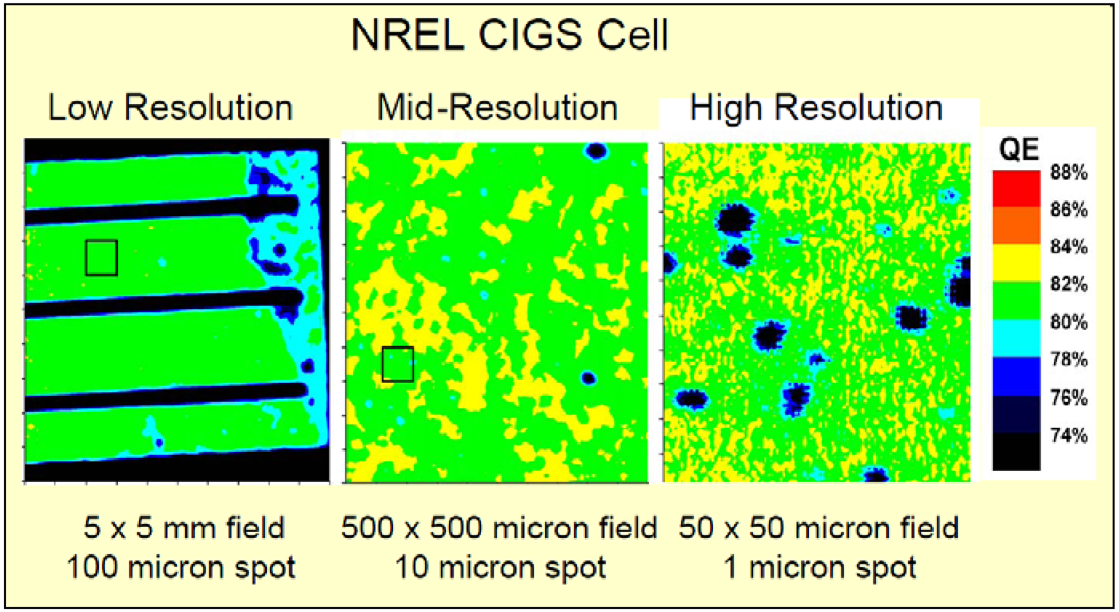
Diana Shvydka,[a)] V. G. Karpov, and A. D. Compaan
Department of Physics and Astronomy, The University of Toledo, Toledo, Ohio 43606

Appl. Phys. Lett., Vol. 82, No. 13, 31 March 2003

Light beam Induced Current (LBIC) for studying inhomogeneities


Can measure photocurrent from 1-micron spot at 1-sun intensity.

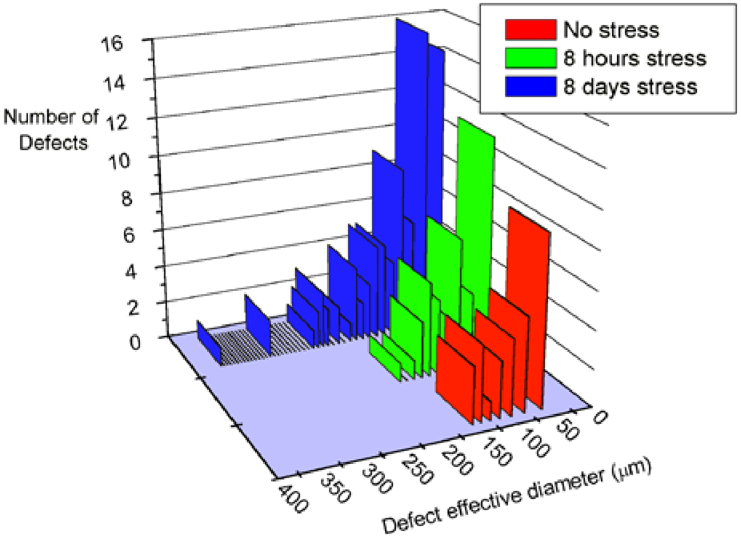
Sites and Nagle, 31st IEEE - PVSC


NREL CIGS Cell

5 x 5 mm field
100 micron spot

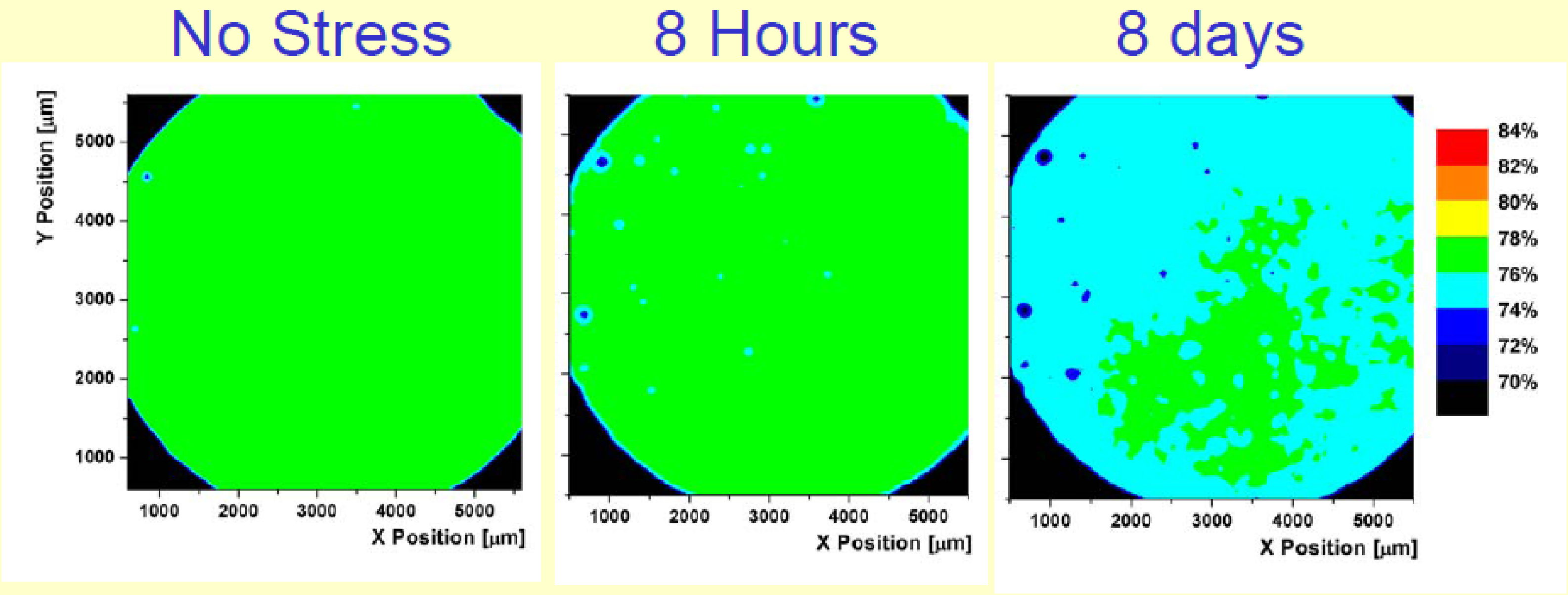
500 x 500 micron field
10 micron spot

50 x 50 micron field
1 micron spot



Light beam Induced Current (LBIC) for identifying where failure occurs

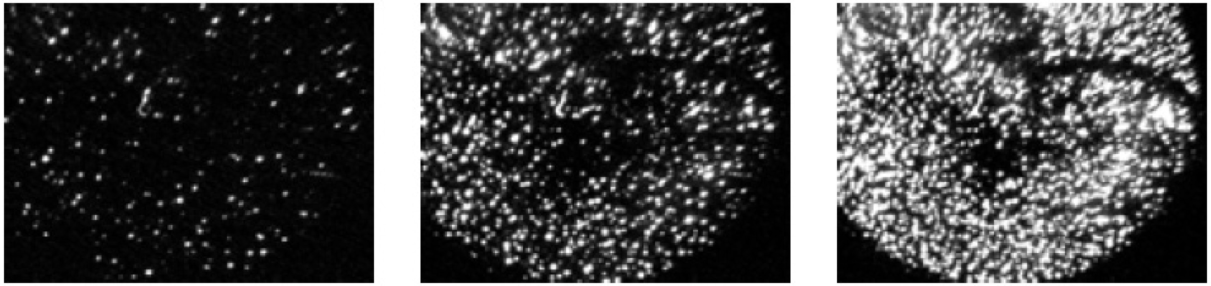
CdTe cell subjected to 100°C under illumination
at short-circuit. (Low-resolution LBIC)



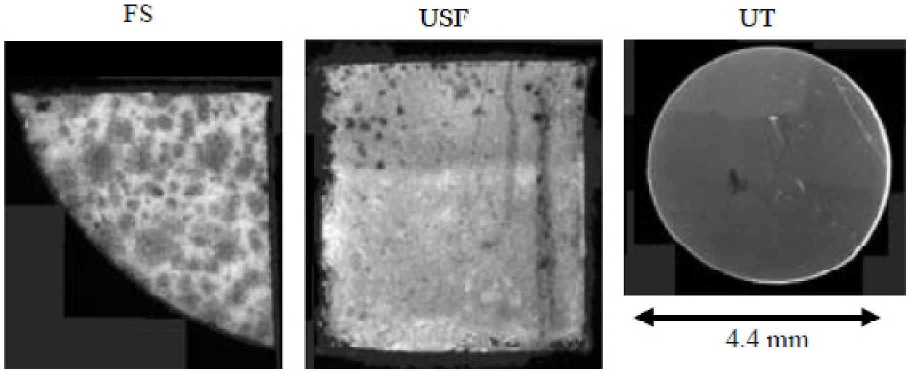
Average QE decreases by 2%

Much greater decrease for isolated spots.

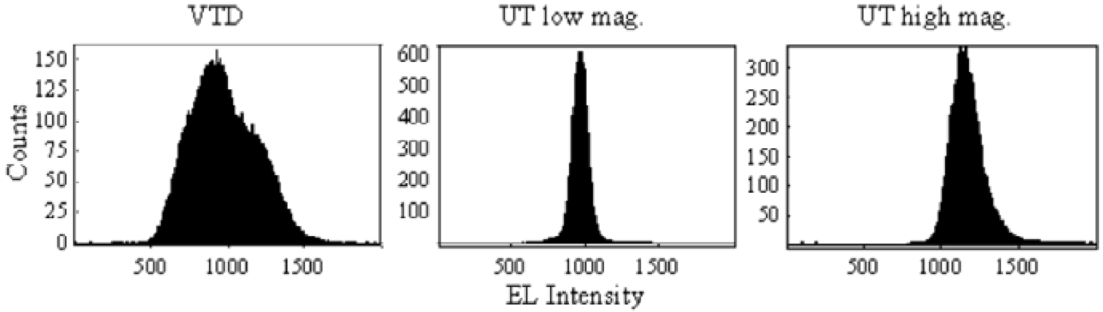
EL and non-uniformities (Colorado School of Mines)



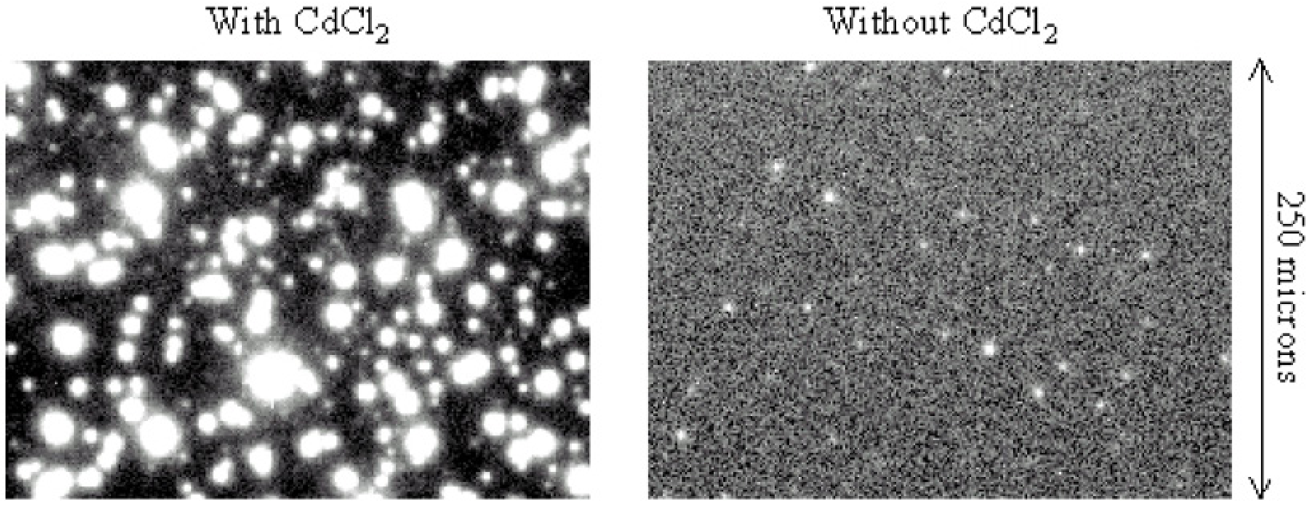
$J = 20\ mA/cm^2$ $J = 90\ mA/cm^2$ $J = 190\ mA/cm^2$

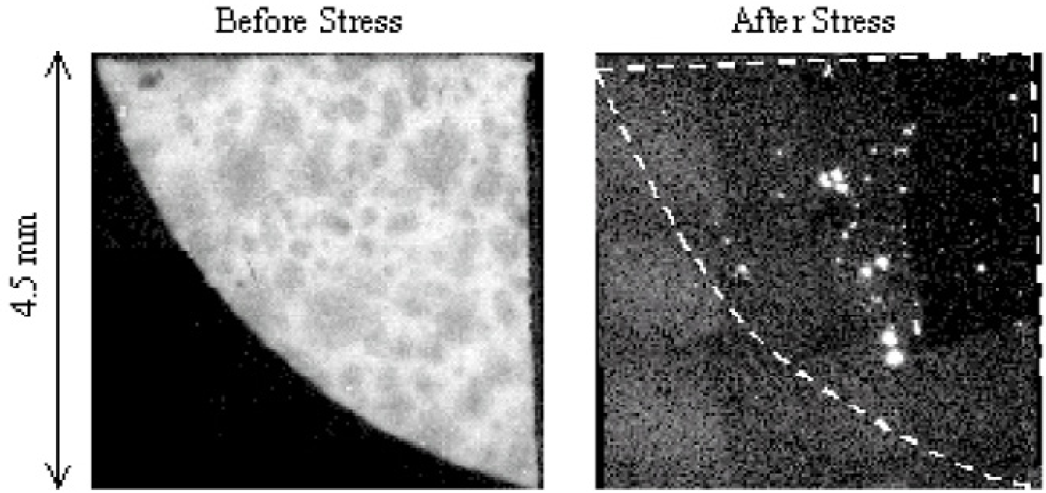


(Imaged thru glass)



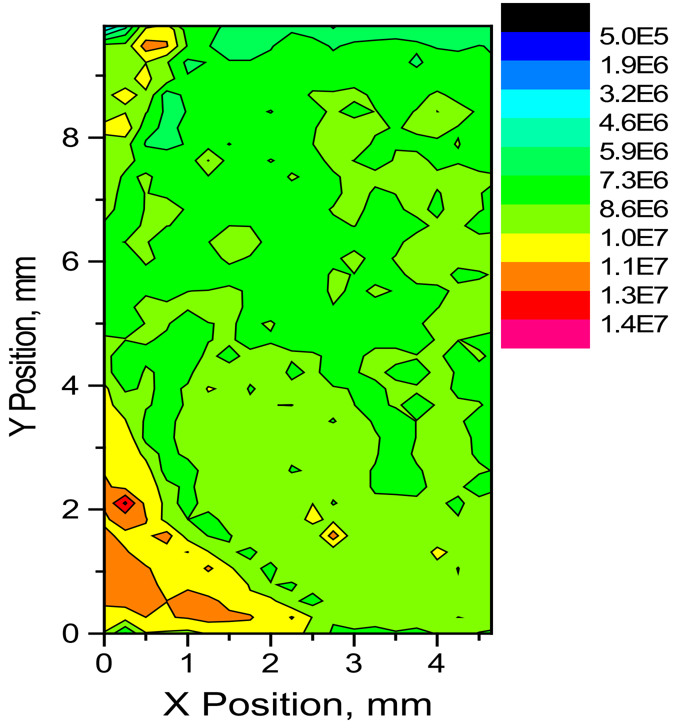
EL and non-uniformities (Colorado School of Mines)



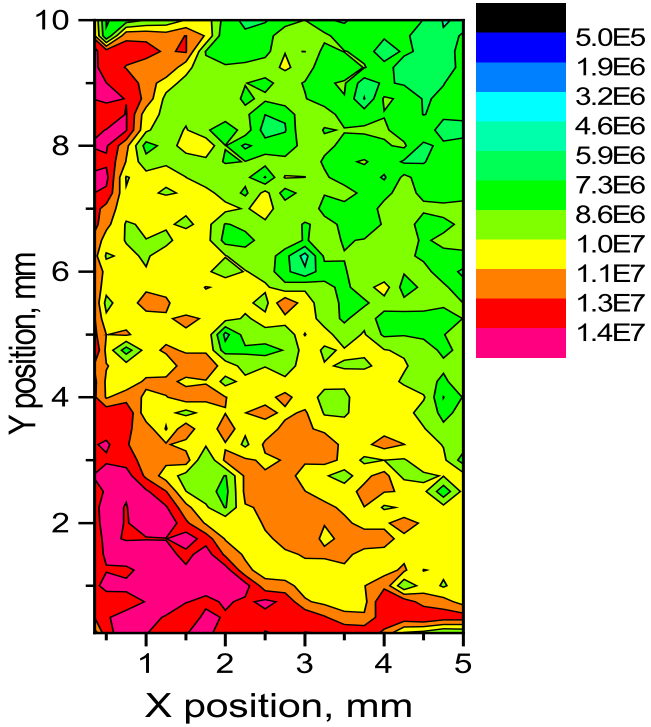


Degradation of back contact (high Rs) leading to increased non-uniformity (bright spots still retain good conduction)

Photoluminescence (PL) Mapping (through glass)



before stress

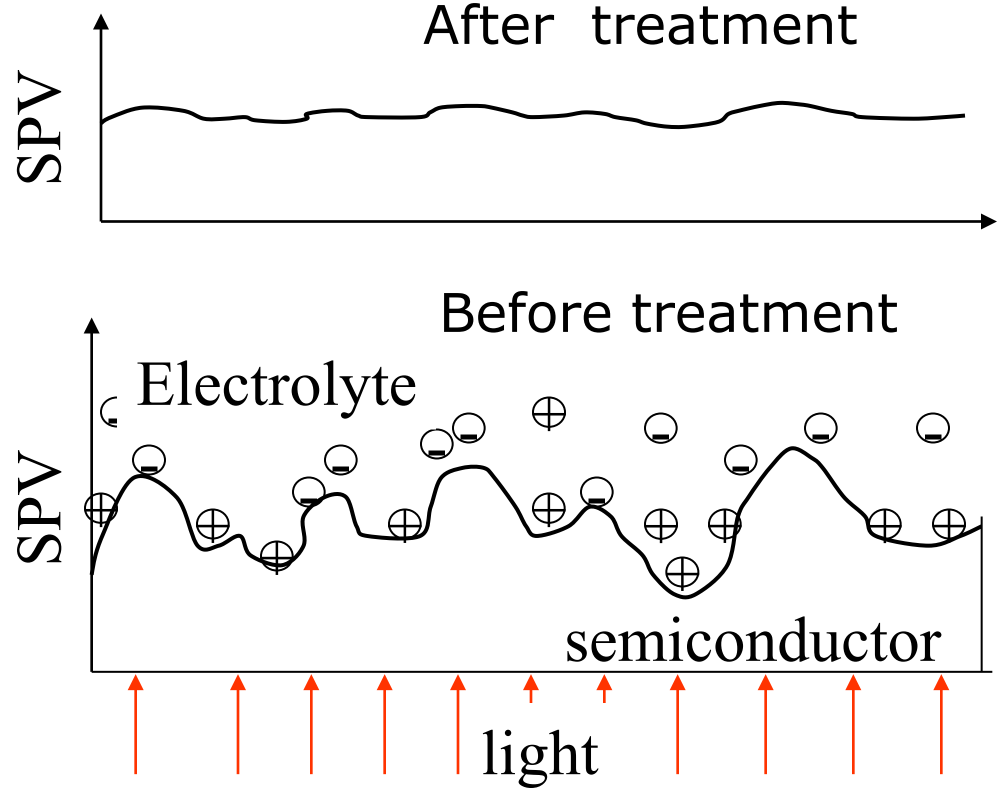


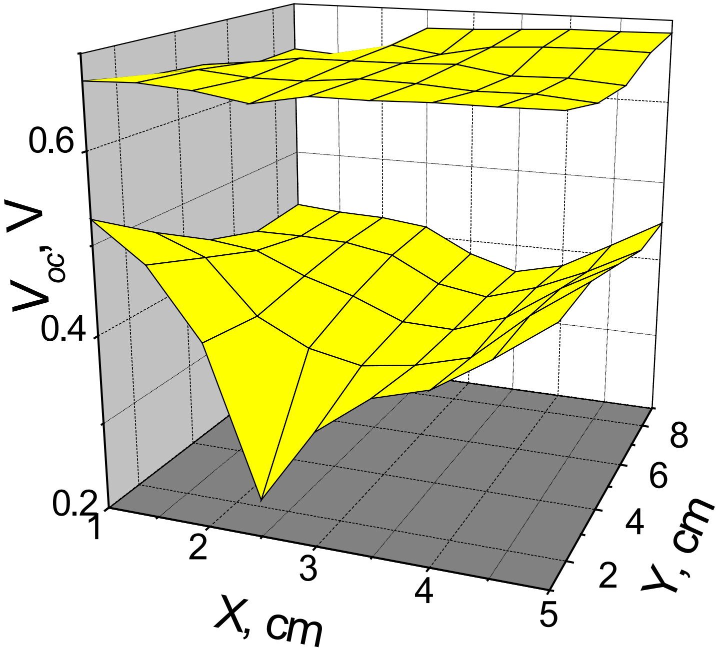
after stress

Typically indicates nonuniformity in the “mixed crystal” region CdS/CdTe.
Also, indicates back contact delamination and shunting.

Shvydka et.al. 2002

Processing to mitigate non-uniformities

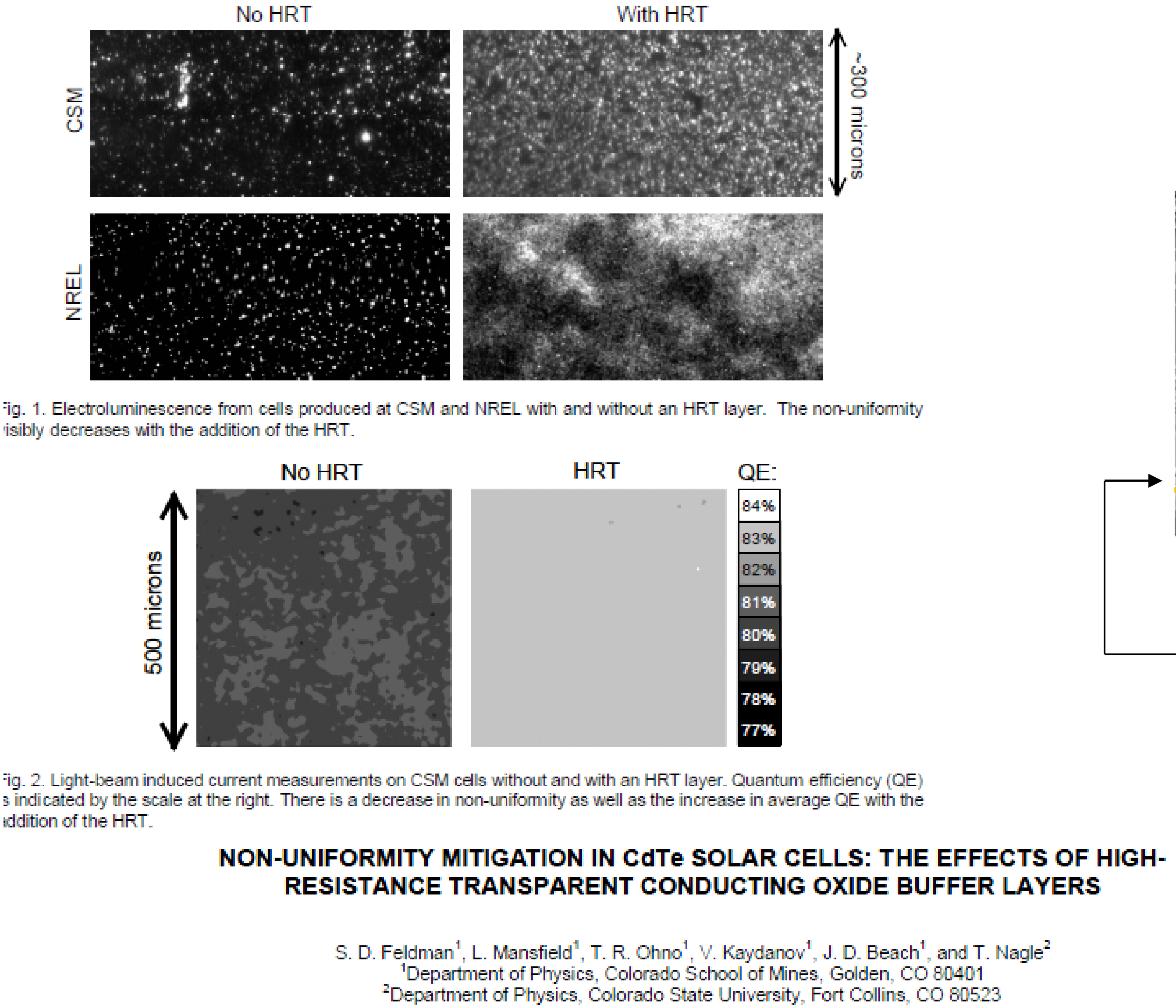




- Patching nonuniformity: act on surface, don't worry about bulk
- Approach differs from classical crystalline PV focused on defects

Roussillon et al. 2003
Patent: Karpov et al. 2006

Processing to mitigate non-uniformities

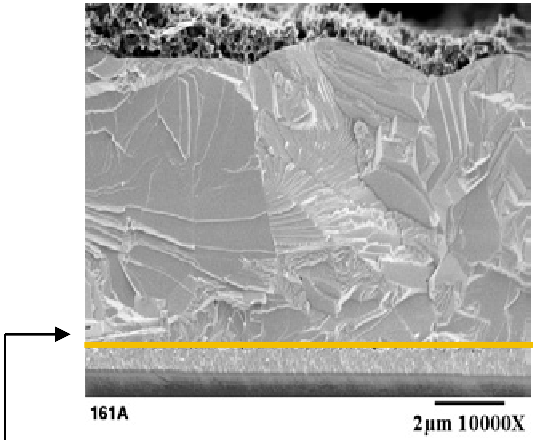


ig. 1. Electroluminescence from cells produced at CSM and NREL with and without an HRT layer. The non-uniformity isibly decreases with the addition of the HRT.

ig. 2. Light-beam induced current measurements on CSM cells without and with an HRT layer. Quantum efficiency (QE) s indicated by the scale at the right. There is a decrease in non-uniformity as well as the increase in average QE with the ddition of the HRT.

NON-UNIFORMITY MITIGATION IN CdTe SOLAR CELLS: THE EFFECTS OF HIGH-RESISTANCE TRANSPARENT CONDUCTING OXIDE BUFFER LAYERS

S. D. Feldman[1], L. Mansfield[1], T. R. Ohno[1], V. Kaydanov[1], J. D. Beach[1], and T. Nagle[2]
[1]Department of Physics, Colorado School of Mines, Golden, CO 80401
[2]Department of Physics, Colorado State University, Fort Collins, CO 80523



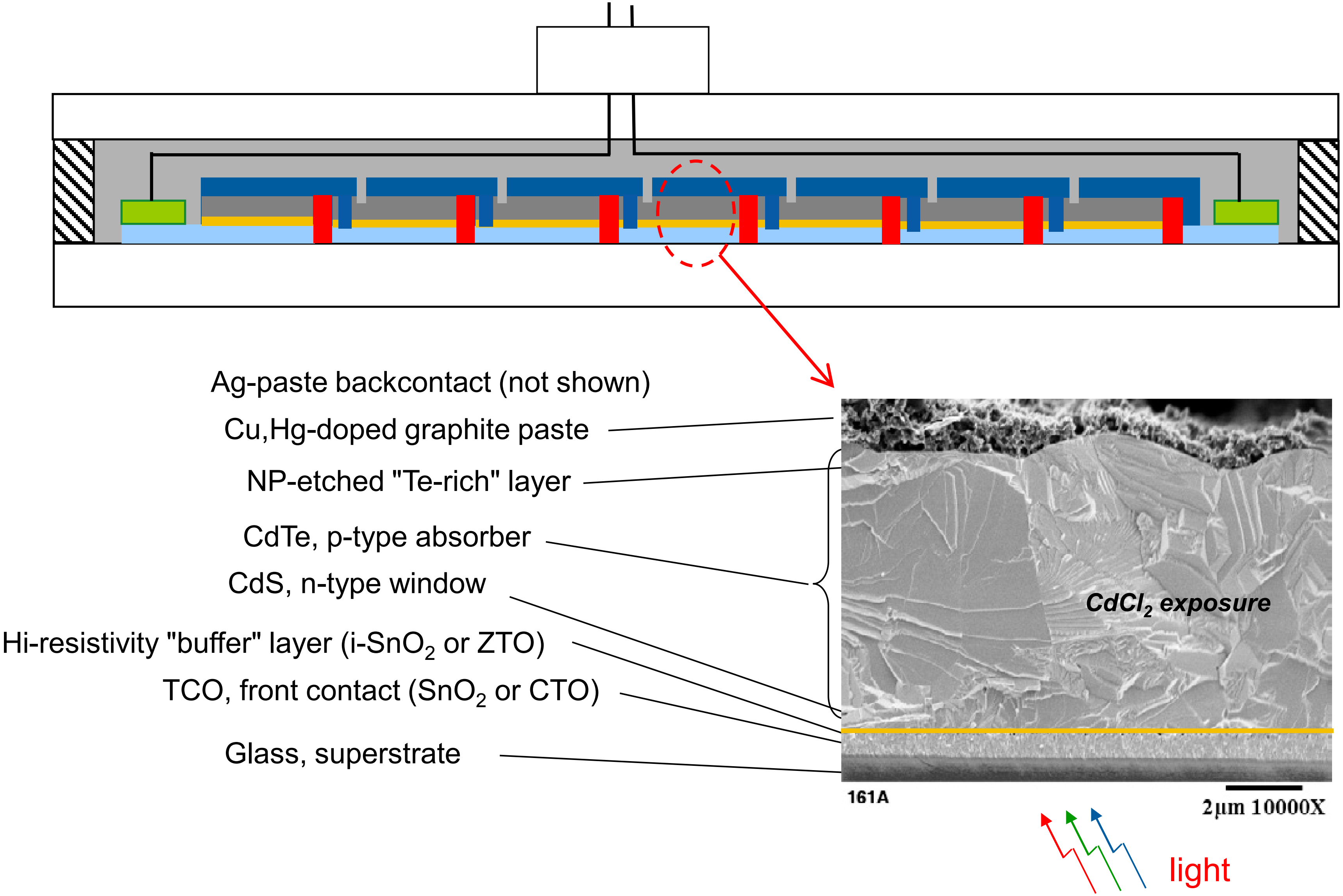
i-SnO_2, $ZnSnO_x$

Patents associated with reducing non-uniformities

Electrolytic etch for eliminating shorts for a-Si:H	Etching ITO	Swartz G. A. (1983)
Method of detecting and repairing latent defects ..	Electrically created plugs	Tickle A. C., (1983)
Barrier layer for photovoltaic devices	Buffer layer	Nath P., Izu M (1986)
Conversion process for passivating short circuit current paths ..	Activating the reagent proximate shunts	Nath P., Vogeli C. N (1992)
Detection and ablation of localized shunting defects in PV	Laser ablation of shunts in response to OBIC	Zapalac JR., G.H (2007)
Photovoltaic healing of nonuniformities PV	Red wine effect	Karpov V.G. et al (2006)
System for diagnosis and treatment of PV..	Electrically created plugs + shunt busting	Karpov V. G. Shvydka D. (2009)

CdTe Cell Fabrication – How we bake the pizza

Cell Fabrication Processes



Ag-paste backcontact (not shown)

Cu,Hg-doped graphite paste

NP-etched "Te-rich" layer

CdTe, p-type absorber

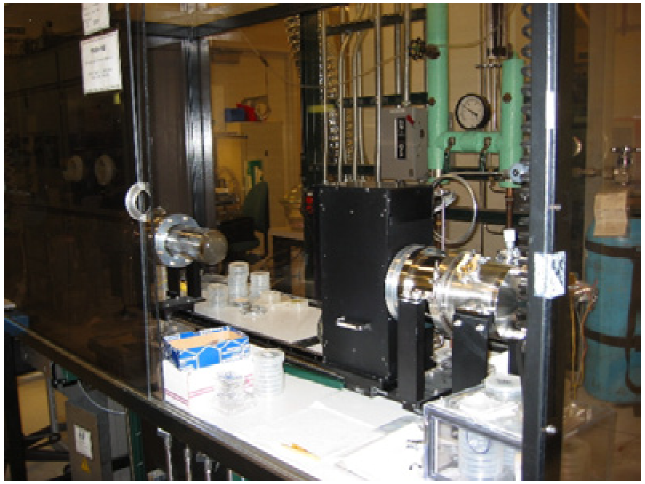
CdS, n-type window

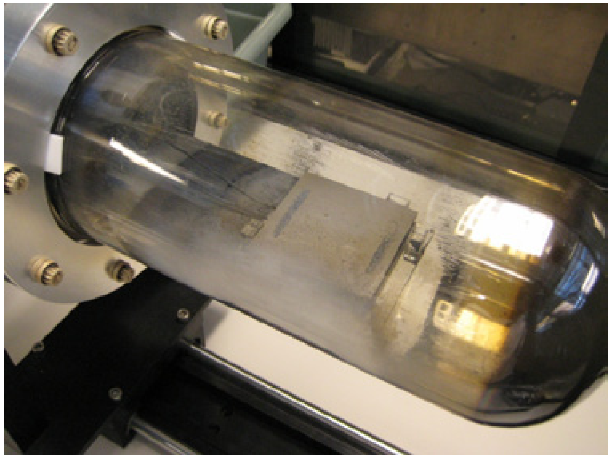
Hi-resistivity "buffer" layer (i-SnO_2 or ZTO)

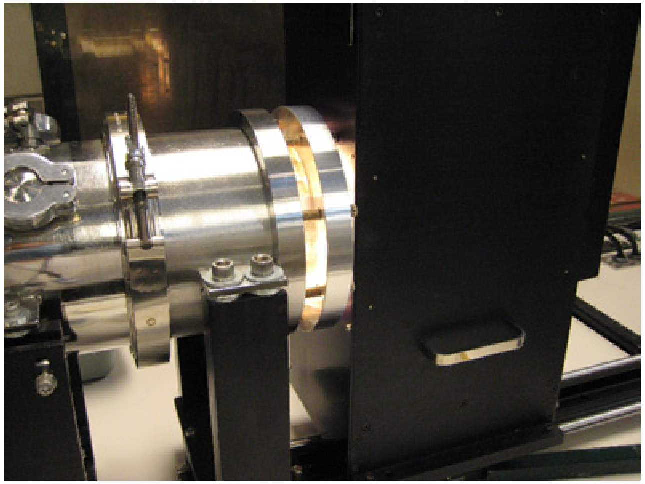
TCO, front contact (SnO_2 or CTO)

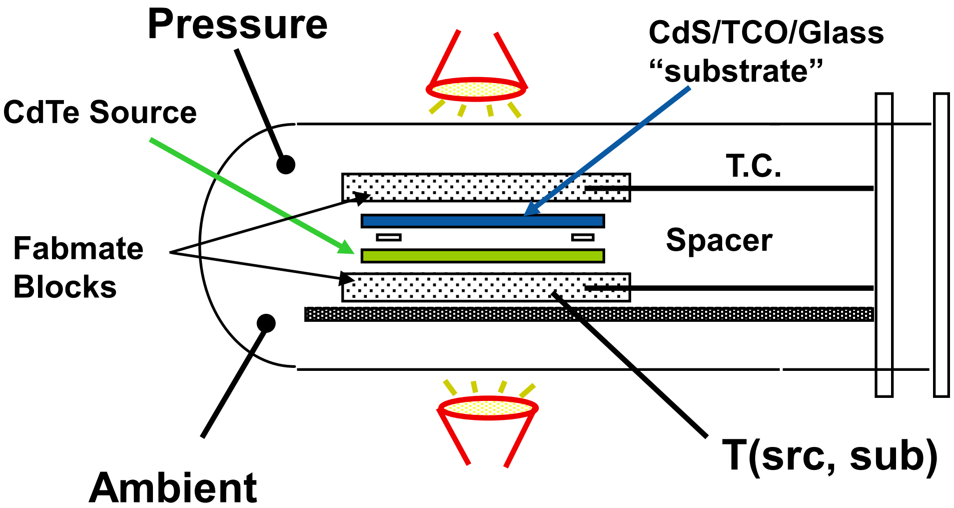
Glass, superstrate

Cell Fabrication Processes – close spaced sublimation (CSS)









Pressure

CdTe Source

CdS/TCO/Glass “substrate”

T.C.

Fabmate Blocks

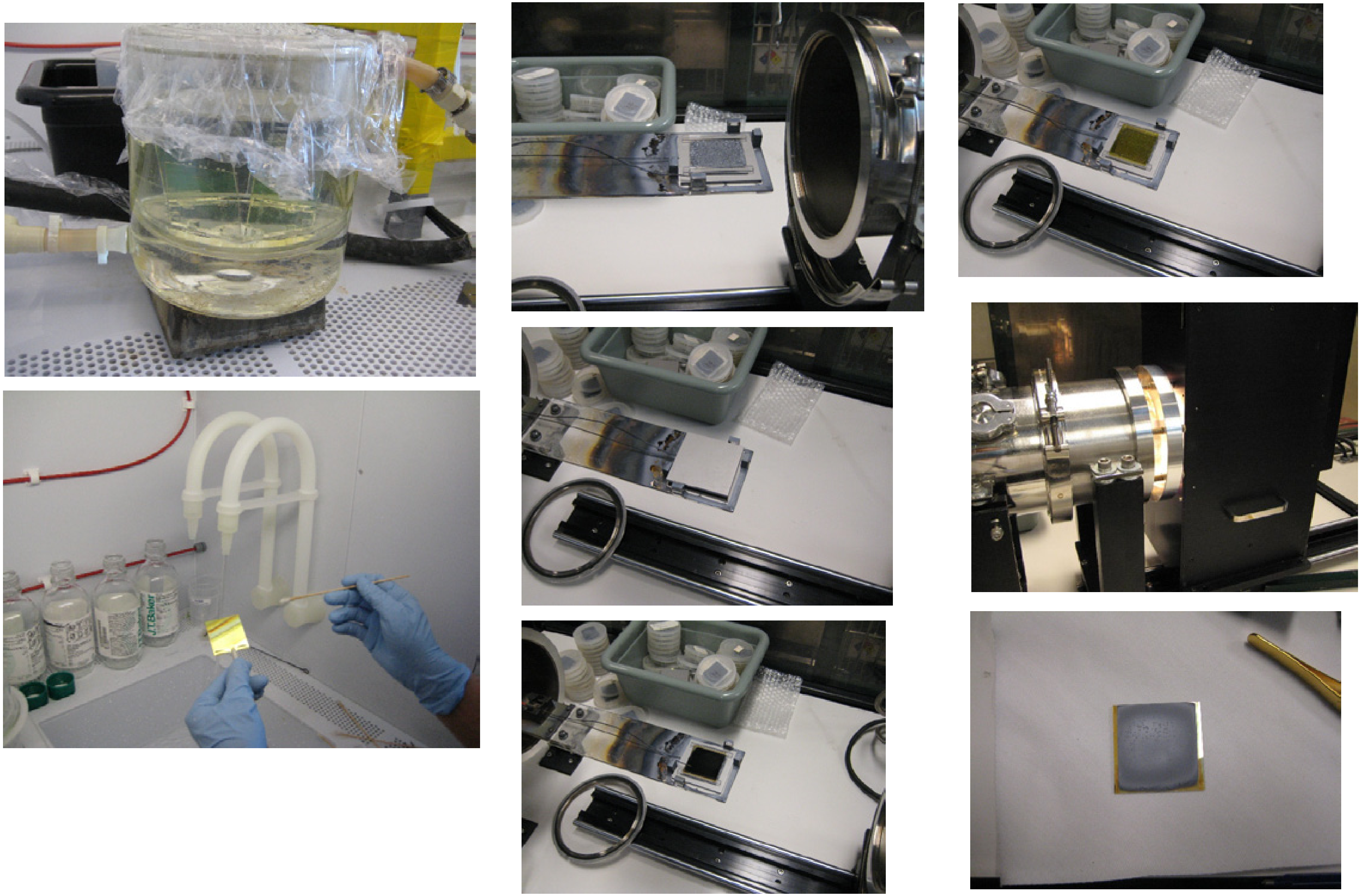
Spacer

T(src, sub)

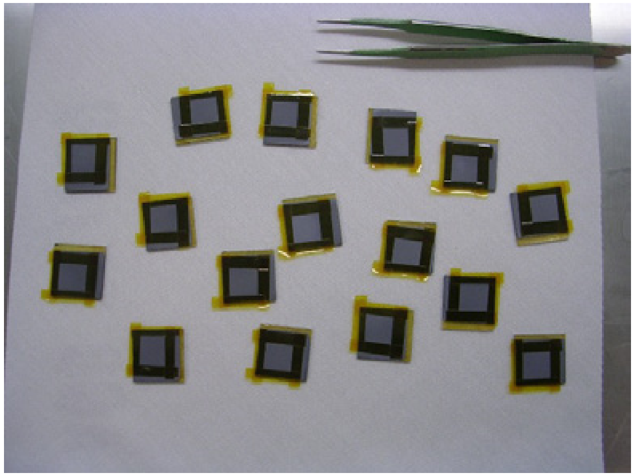
Ambient

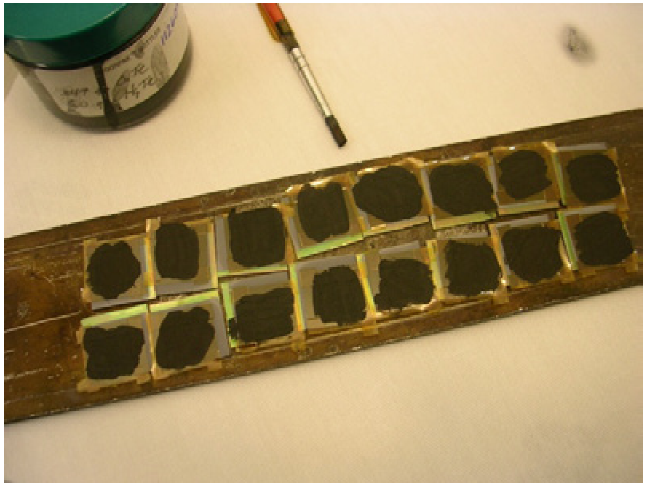
(He, N_2, O_2, H_2)

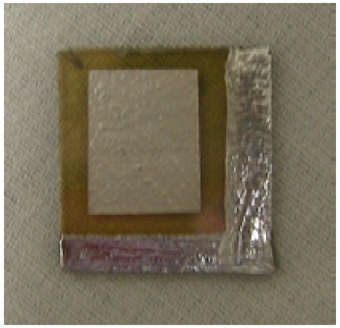
Cell Fabrication Processes – close spaced sublimation (CSS)

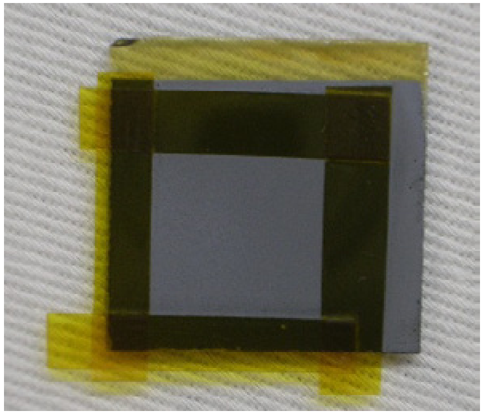


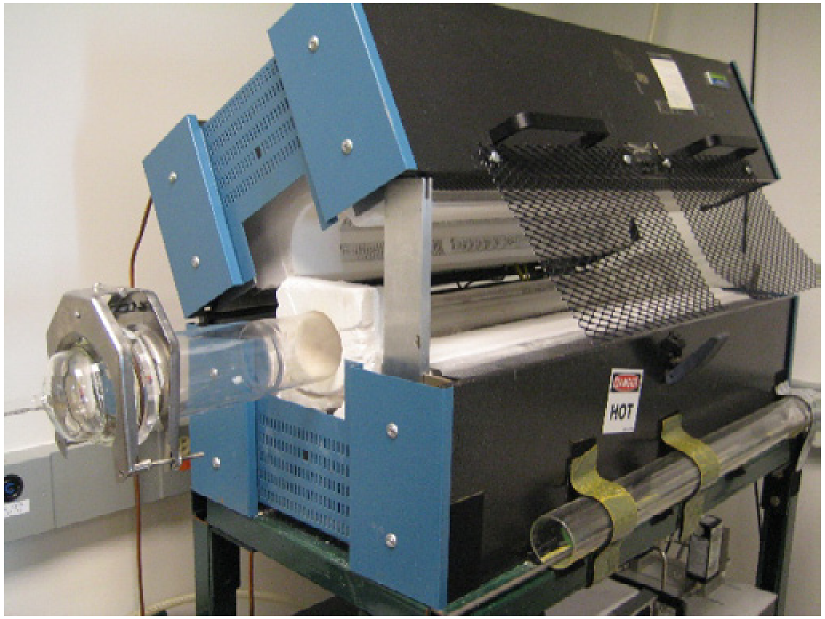
Cell Fabrication Processes – Back Contact Processing



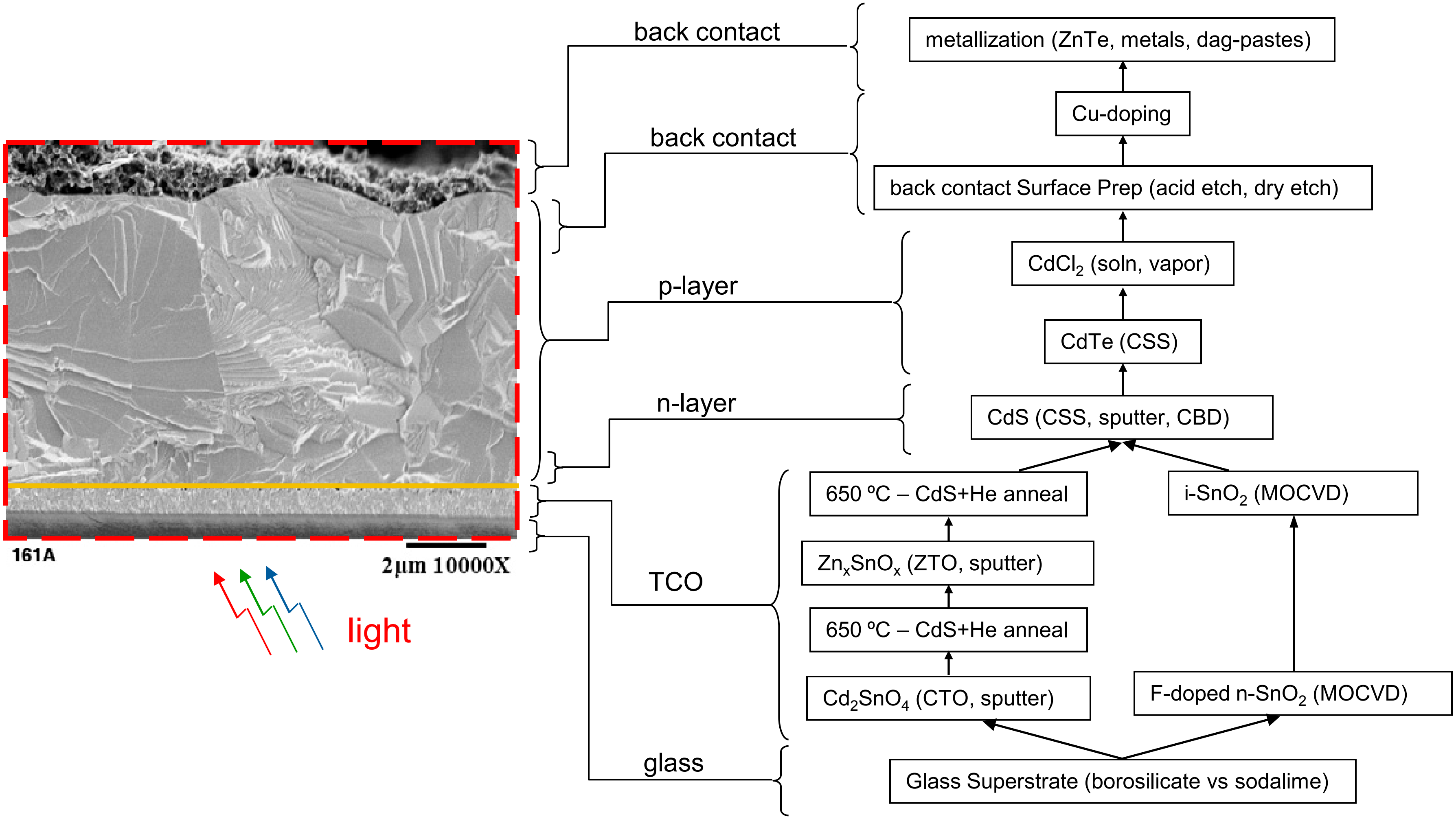








Cell durability is a function of cell fabrication – many processes and materials to study and optimize



back contact

metallization (ZnTe, metals, dag-pastes)

Cu-doping

back contact

back contact Surface Prep (acid etch, dry etch)

p-layer

$CdCl_2$ (soln, vapor)

CdTe (CSS)

n-layer

CdS (CSS, sputter, CBD)

650 ºC – CdS+He anneal

i-SnO_2 (MOCVD)

TCO

Zn_xSnO_x (ZTO, sputter)

650 ºC – CdS+He anneal

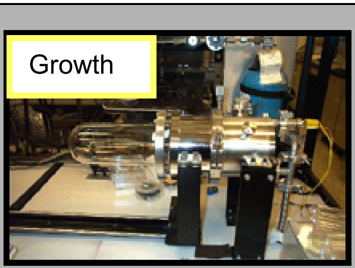
Cd_2SnO_4 (CTO, sputter)

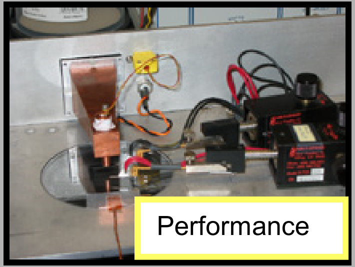
F-doped n-SnO_2 (MOCVD)

glass

Glass Superstrate (borosilicate vs sodalime)

Good Data management necessary to optimize performance/durability





automated
data
collection

Data Management

DB

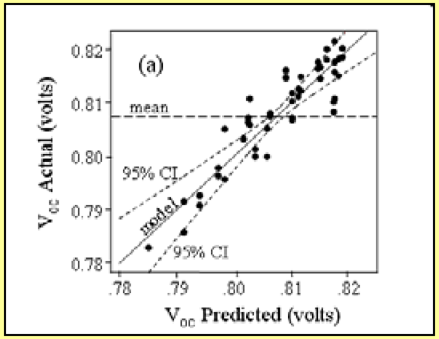
Application Layer

JMP (SAS)

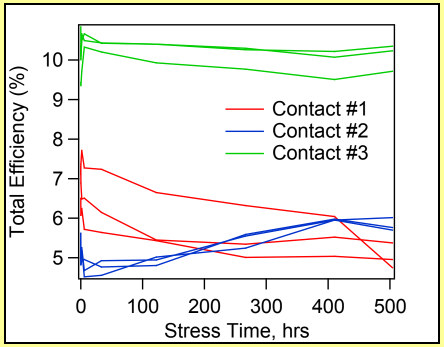
Fabrication,
Performance, Reliability
Data Collection

Database
Management

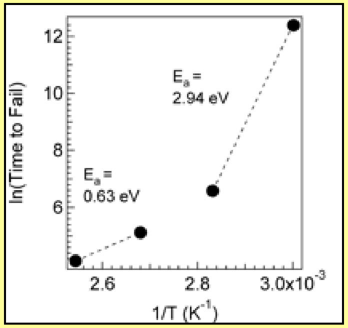
Advanced
Analysis



Performance
Optimization



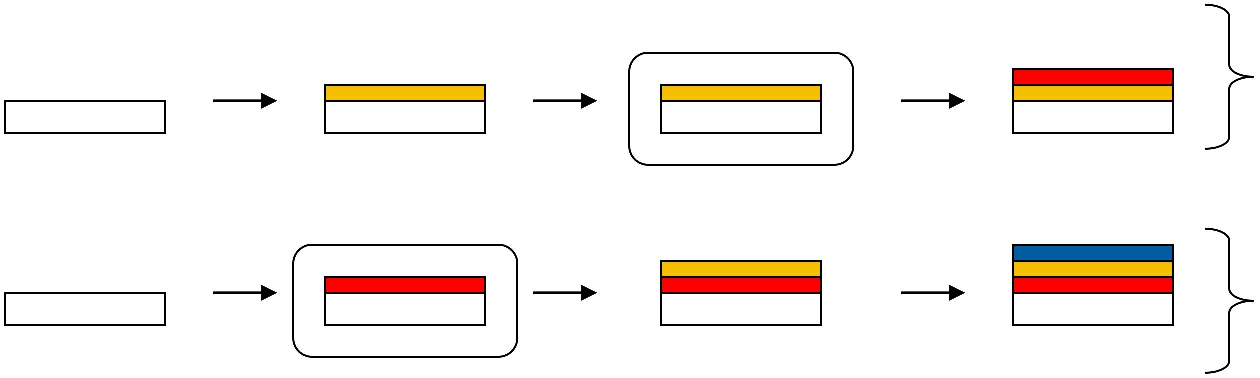
Reliability vs
Processing



Degradation
Mechanism
Studies

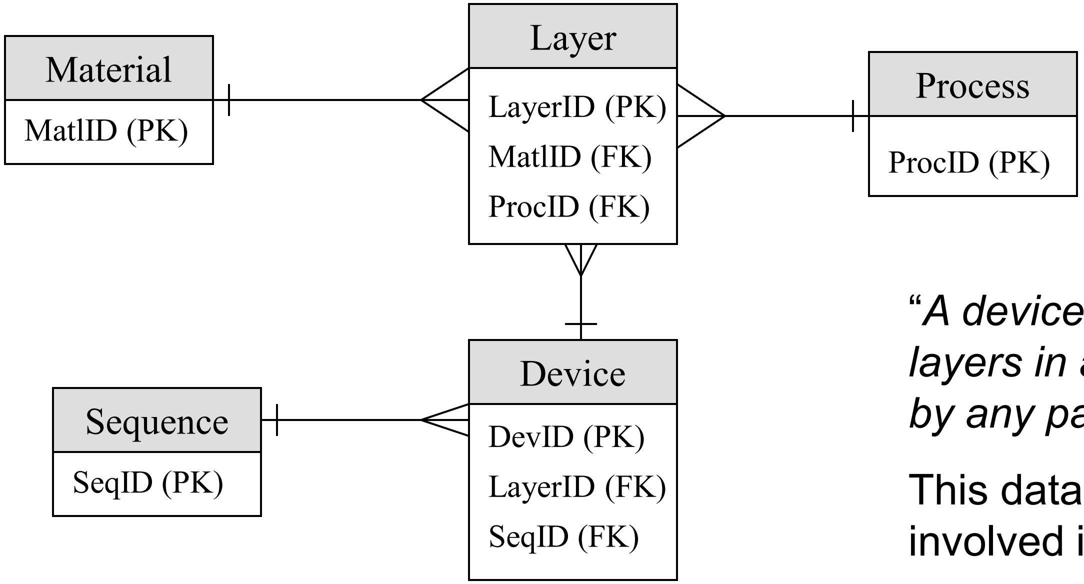
Database Structure ERD (Entity Relationship Diagram)

Variable or Dynamic Processing ERD



Blue Layer
Thermal Anneal
Red Anneal

Red Layer & Thermal Anneal
Blue Layer
Green layer



Material
MatlID (PK)

Layer
LayerID (PK)
MatlID (FK)
ProcID (FK)

Process
ProcID (PK)

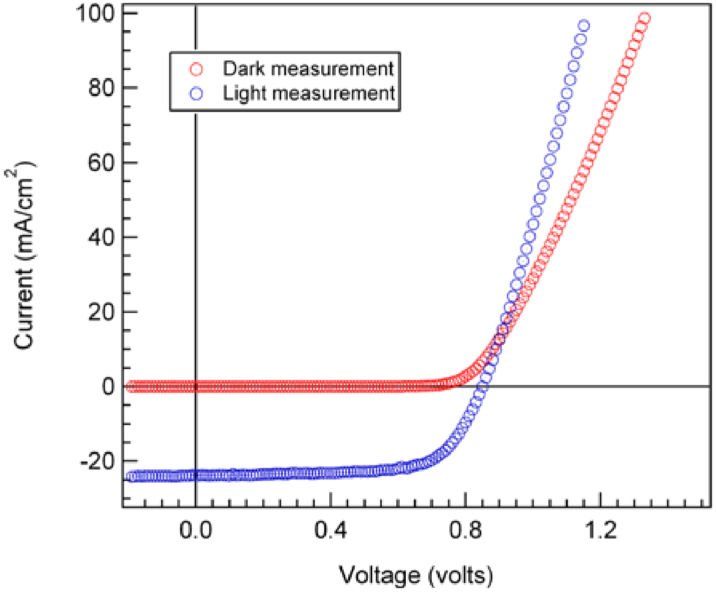
Sequence
SeqID (PK)

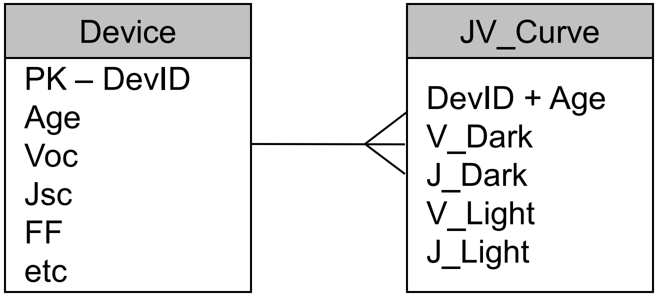
Device
DevID (PK)
LayerID (FK)
SeqID (FK)

“A device is composed of any number of layers in any order, each layer being made by any particular process.”

This data structure manages any situation involved in making solar cells

To monitor degradation need many measurements of JV data





Device

PK – DevID
Age
Voc
Jsc
FF
etc

JV_Curve

DevID + Age
V_Dark
J_Dark
V_Light
J_Light

The “JV Curve” is the most fundamental “data” associated with the performance of a solar cell

Each JV-Curve consists of stepping voltage (V) from -0.2 to 1.5 volts and measuring current (J) at each step

Typically generate 170 unique combinations of J and V per cell measurement

Perform this scan with (light) and without (dark) illumination,

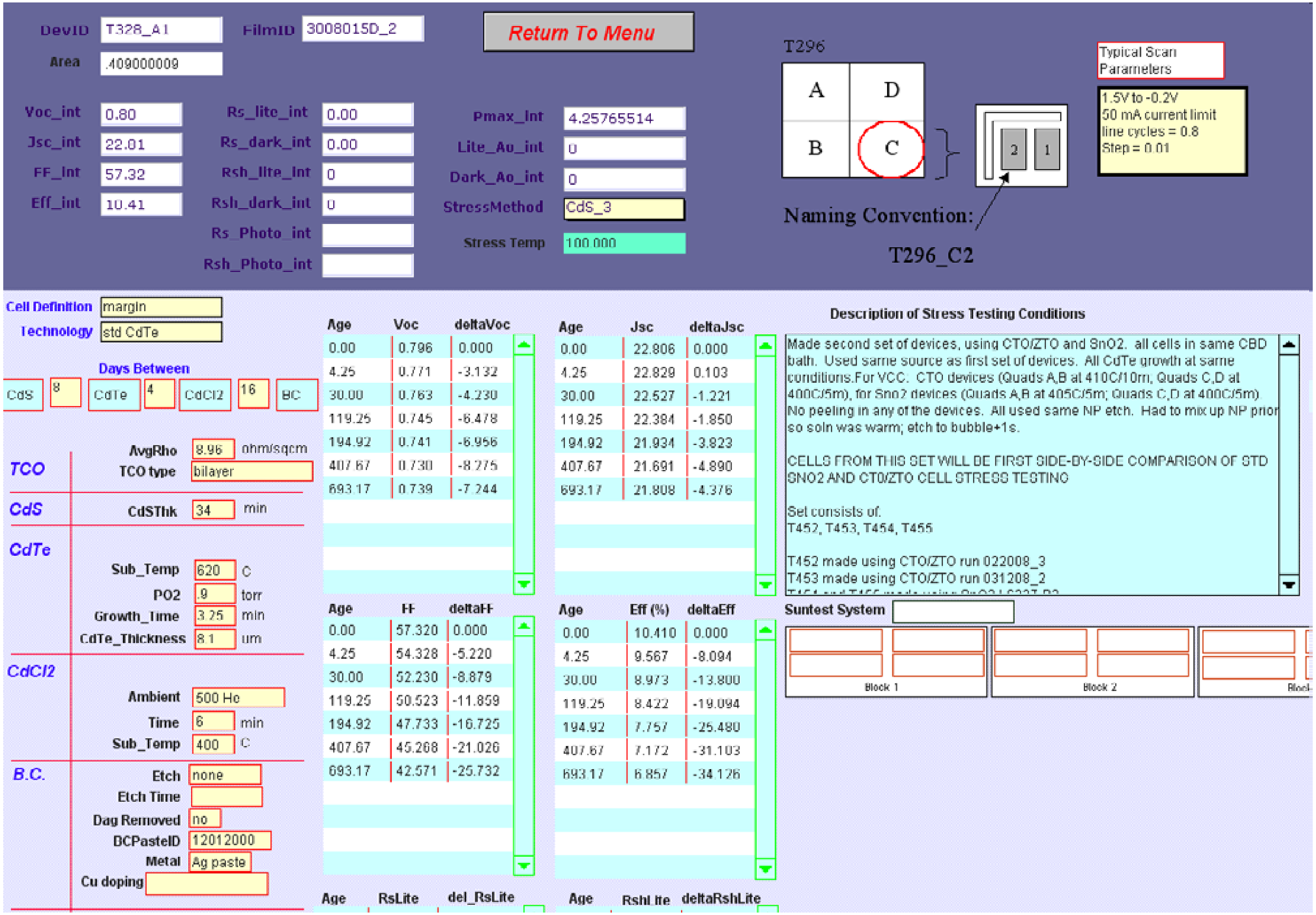
After measurement, generate (1) record in a table containing metadata (DevID, Age, Voc, Jsc, FF, etc.) as well as 170 records in a table called JV-curve containing raw dark and light JV data

Each entry in the “Device” table results in 170 entries in the “JV Curve” table

Each cell represents a unique combination of steps involved in it’s processing and performance characteristics at a particular moment in its life (age)

Tracking J-V data is the most useful if not critical component of studying not only performance, but the reliability of PV cells

Database facilitates linking of Process with Durability



DevID T328_A1
FilmID 3008015D_2
Area .409000009

Voc_int 0.80
Jsc_int 22.01
FF_int 57.32
Eff_int 10.41

Rs_lite_int 0.00
Rs_dark_int 0.00
Rsh_lite_int 0
Rsh_dark_int 0
Rs_Photo_int
Rsh_Photo_int

Pmax_int 4.25765514
Lite_Ao_int 0
Dark_Ao_int 0
StressMethod CdS_3
Stress Temp 100.000

Typical Scan Parameters

1.5V to -0.2V
50 mA current limit
line cycles = 0.8
Step = 0.01

Cell Definition margin
Technology std CdTe

Days Between

CdS 8 CdTe 4 CdCl2 16 BC

TCO
AvgRho 8.96 ohm/sqcm
TCO type bilayer

CdS
CdSThk 34 min

CdTe
Sub_Temp 620 C
PO2 .9 torr
Growth_Time 3.25 min
CdTe_Thickness 8.1 um

CdCl2
Ambient 500 He
Time 6 min
Sub_Temp 400 C

B.C.
Etch none
Etch Time
Dag Removed no
BCPasteID 12012000
Metal Ag paste
Cu doping

Age	Voc	deltaVoc
0.00	0.796	0.000
4.25	0.771	-3.132
30.00	0.763	-4.230
119.25	0.745	-6.478
194.92	0.741	-6.956
407.67	0.730	-8.275
693.17	0.739	-7.244

Age	Jsc	deltaJsc
0.00	22.806	0.000
4.25	22.829	0.103
30.00	22.527	-1.221
119.25	22.384	-1.850
194.92	21.934	-3.823
407.67	21.691	-4.890
693.17	21.808	-4.376

Age	FF	deltaFF
0.00	57.320	0.000
4.25	54.328	-5.220
30.00	52.230	-8.879
119.25	50.523	-11.859
194.92	47.733	-16.725
407.67	45.268	-21.026
693.17	42.571	-25.732

Age	Eff (%)	deltaEff
0.00	10.410	0.000
4.25	9.567	-8.094
30.00	8.973	-13.800
119.25	8.422	-19.094
194.92	7.757	-25.480
407.67	7.172	-31.103
693.17	6.857	-34.126

Age	RsLite	del_RsLite

Age	RshLite	deltaRshLite

Description of Stress Testing Conditions

Made second set of devices, using CTO/ZTO and SnO2. all cells in same CBD bath. Used same source as first set of devices. All CdTe growth at same conditions.For VCC: CTO devices (Quads A,B at 410C/10m; Quads C,D at 400C/5m), for Sno2 devices (Quads A,B at 405C/5m; Quads C,D at 400C/5m). No peeling in any of the devices. All used same NP etch. Had to mix up NP prior so soln was warm; etch to bubble+1s.

CELLS FROM THIS SET WILL BE FIRST SIDE-BY-SIDE COMPARISON OF STD SNO2 AND CT0/ZTO CELL STRESS TESTING

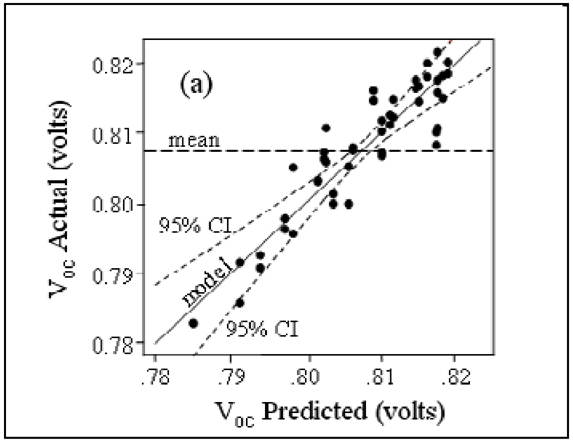
Set consists of:
T452, T453, T454, T455

T452 made using CTO/ZTO run 022008_3
T453 made using CTO/ZTO run 031208_2

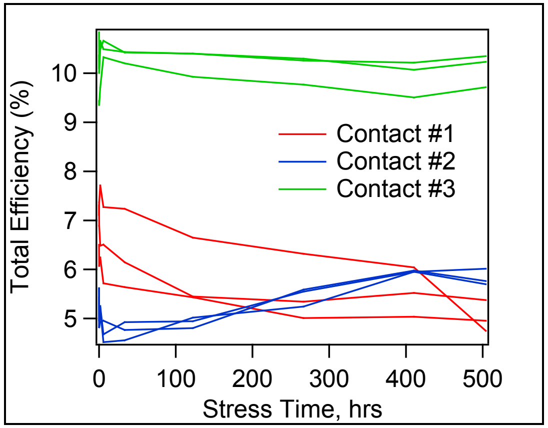
Suntest System

Block 1
Block 2

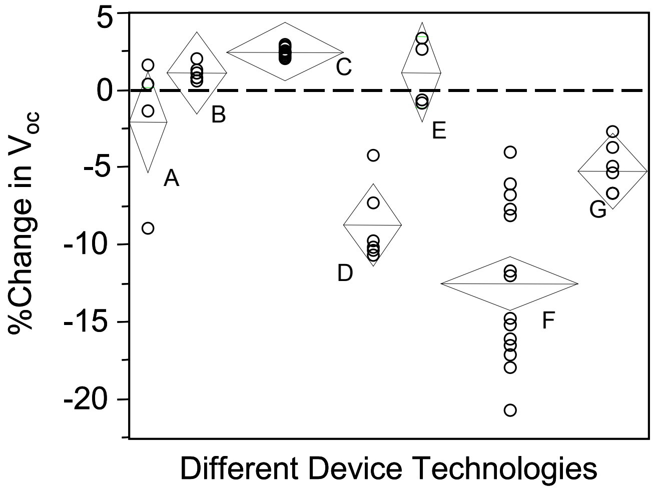
Examples of Data Management Output



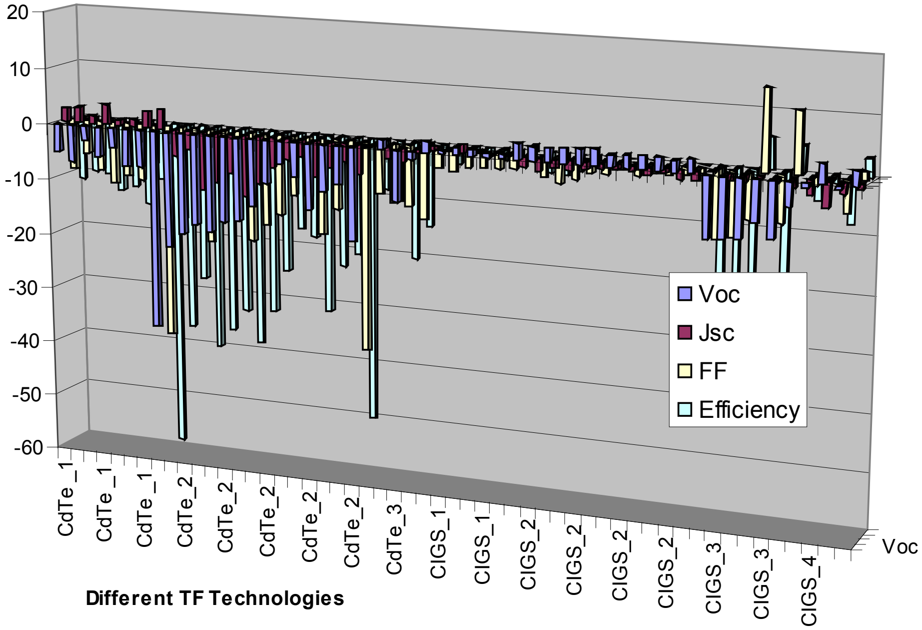
Process Models for Performance



Effects of Processing on Cell Stability

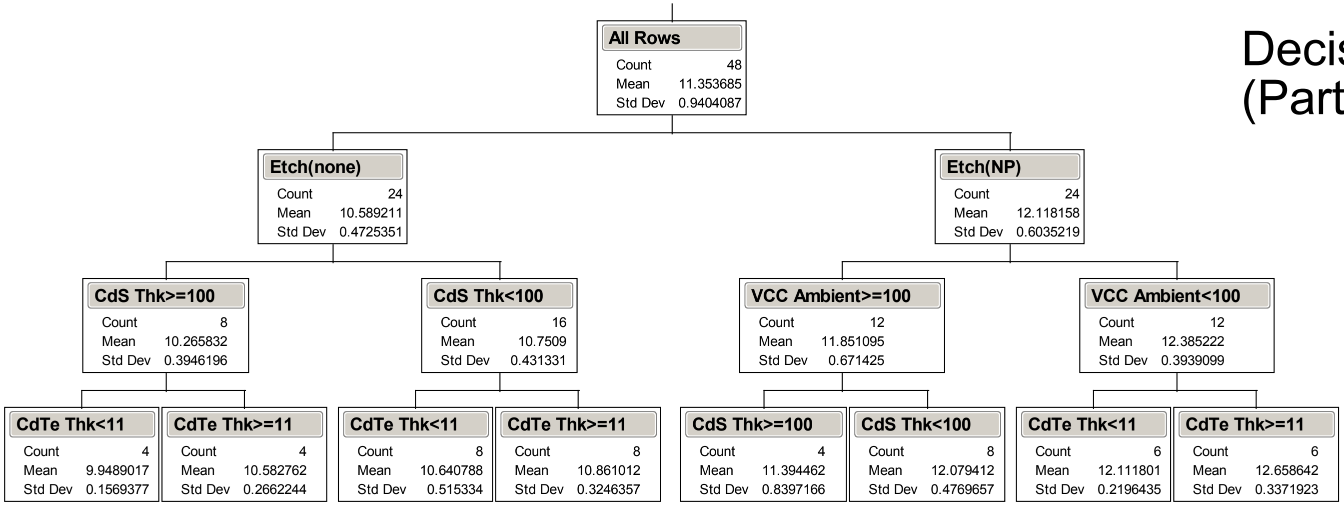


Stability shown as the %change in V_{oc} observed in different cell structures after stress testing



Examples of Data Management Output

Decision Tree Analysis (Partition Analysis)



All Rows: Count 48, Mean 11.353685, Std Dev 0.9404087

Etch(none): Count 24, Mean 10.589211, Std Dev 0.4725351

Etch(NP): Count 24, Mean 12.118158, Std Dev 0.6035219

CdS Thk>=100: Count 8, Mean 10.265832, Std Dev 0.3946196

CdS Thk<100: Count 16, Mean 10.7509, Std Dev 0.431331

VCC Ambient>=100: Count 12, Mean 11.851095, Std Dev 0.671425

VCC Ambient<100: Count 12, Mean 12.385222, Std Dev 0.3939099

CdTe Thk<11: Count 4, Mean 9.9489017, Std Dev 0.1569377

CdTe Thk>=11: Count 4, Mean 10.582762, Std Dev 0.2662244

CdTe Thk<11: Count 8, Mean 10.640788, Std Dev 0.515334

CdTe Thk>=11: Count 8, Mean 10.861012, Std Dev 0.3246357

CdS Thk>=100: Count 4, Mean 11.394462, Std Dev 0.8397166

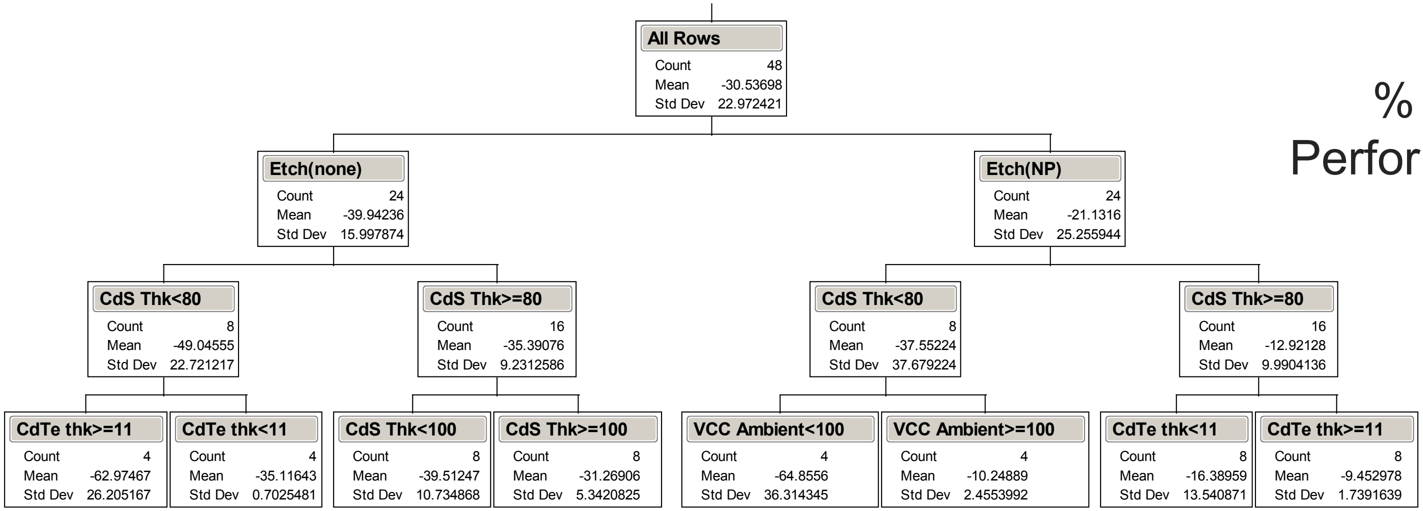
CdS Thk<100: Count 8, Mean 12.079412, Std Dev 0.4769657

CdTe Thk<11: Count 6, Mean 12.111801, Std Dev 0.2196435

CdTe Thk>=11: Count 6, Mean 12.658642, Std Dev 0.3371923

Initial Performance

→ Improved *Performance*



All Rows: Count 48, Mean -30.53698, Std Dev 22.972421

Etch(none): Count 24, Mean -39.94236, Std Dev 15.997874

Etch(NP): Count 24, Mean -21.1316, Std Dev 25.255944

CdS Thk<80: Count 8, Mean -49.04555, Std Dev 22.721217

CdS Thk>=80: Count 16, Mean -35.39076, Std Dev 9.2312586

CdS Thk<80: Count 8, Mean -37.55224, Std Dev 37.679224

CdS Thk>=80: Count 16, Mean -12.92128, Std Dev 9.9904136

CdTe thk>=11: Count 4, Mean -62.97467, Std Dev 26.205167

CdTe thk<11: Count 4, Mean -35.11643, Std Dev 0.7025481

CdS Thk<100: Count 8, Mean -39.51247, Std Dev 10.734868

CdS Thk>=100: Count 8, Mean -31.26906, Std Dev 5.3420825

VCC Ambient<100: Count 4, Mean -64.8556, Std Dev 36.314345

VCC Ambient>=100: Count 4, Mean -10.24889, Std Dev 2.4553992

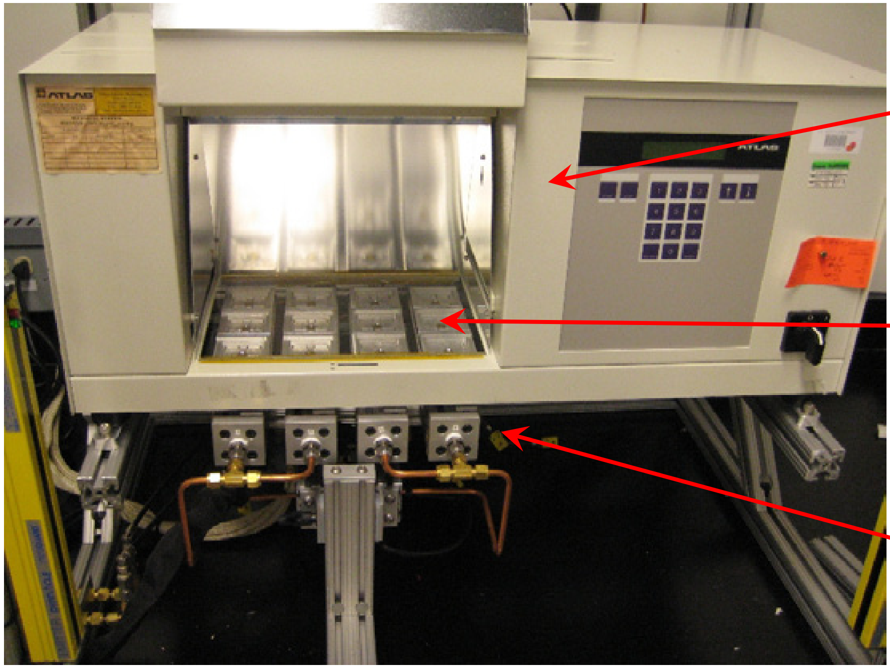
CdTe thk<11: Count 8, Mean -16.38959, Std Dev 13.540871

CdTe thk>=11: Count 8, Mean -9.452978, Std Dev 1.7391639

% Decrease in Performance after 700 hrs ALT

→ Improved *Reliability*

Light-soak Stress Test (main ALT)



Atlas Suntest CPS solar simulator with Xenon arc, 1 sun irradiance

- 1500 hrs continuous
- Light source not stable for in-situ JV measurements
- Effectively biases cells at V_{oc}

Aluminum-milled cell holders

- interchangeable holders for substrate and superstrate designs
- For substrate designs need to prevent shorting cells

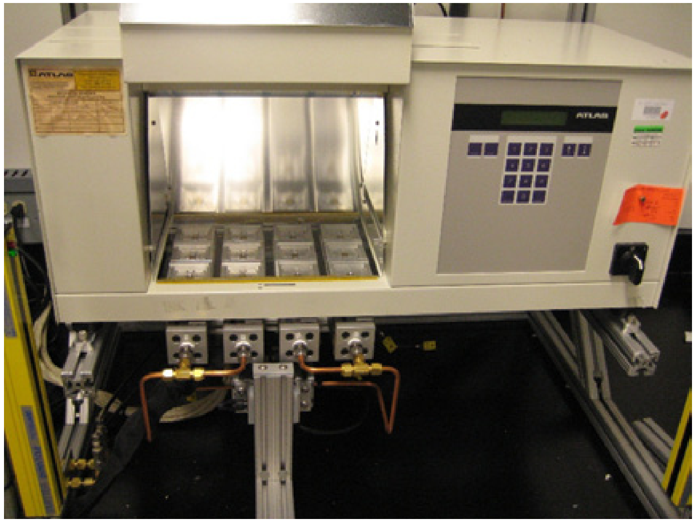
Independent heating/cooling zones

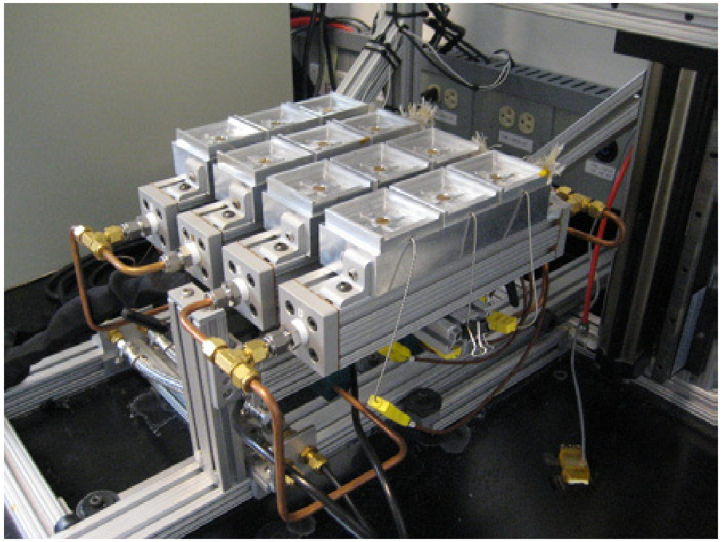
- Under 1 sun illumination, cell temperature can easily reach 60 ºC
- Active cooling necessary for controlling lower temperatures
- Independent heating necessary for temperature-activation energy studies

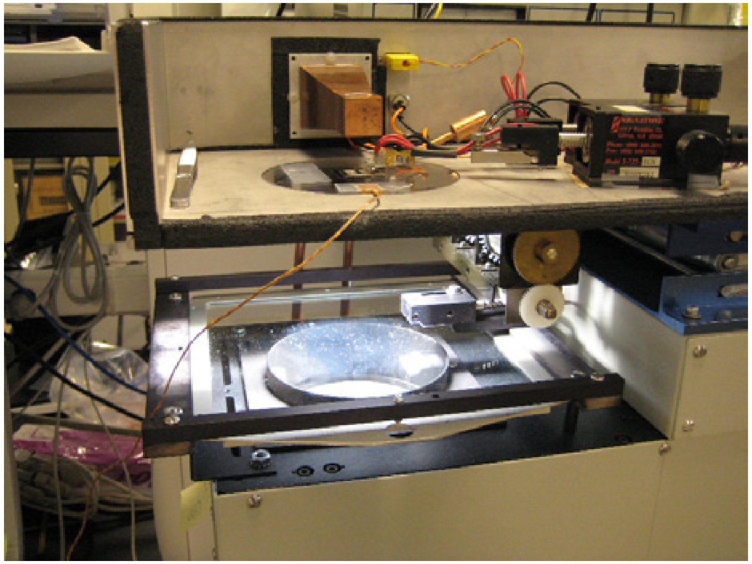
Experimental Procedure:

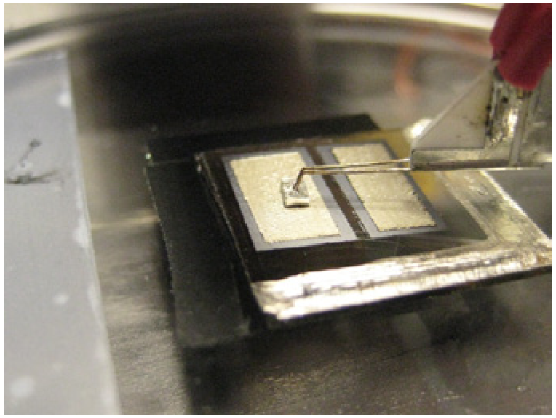
- Make initial, t=0 measurement
- Expose cells for some t
  - Estimate t based on 1 eV (if E_a=1 eV and T=100 ºC, then 1000 hrs ~ 10 years if T_{use}=50 ºC)
  - Distribute t logarithmically, t=0, 1, 10, 100, 1000)
  - Measurements at shorter times are insightful; Longer measurements useful for durability understanding
- Remove cells, perform stabilization to remove transients
- Measure cells (J-V, C-V, Q-E, etc.)
- Repeat exposure, stabilization, and measurements

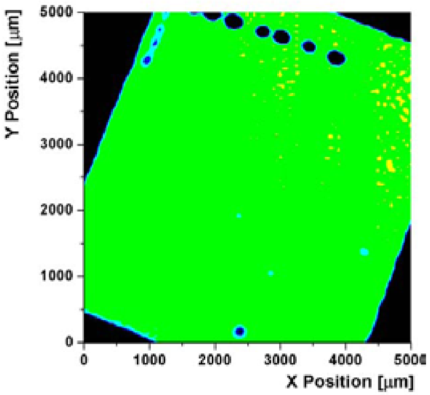
Light-soak Stress Test (main ALT)





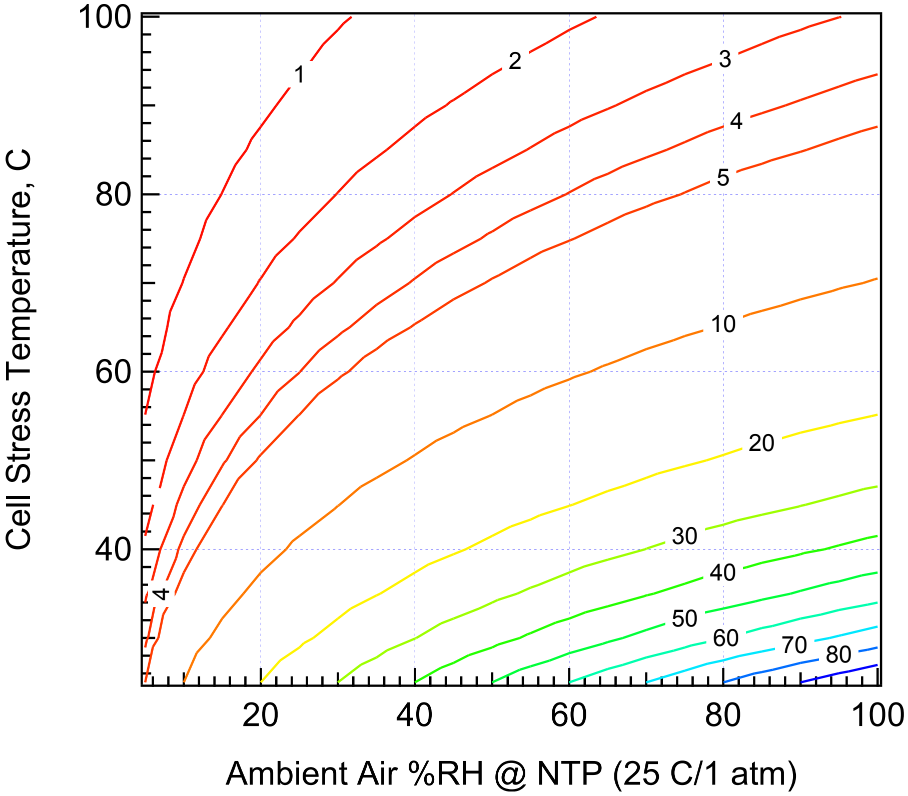






Probes can introduce local failure

Light-soak Stress Test (main ALT)

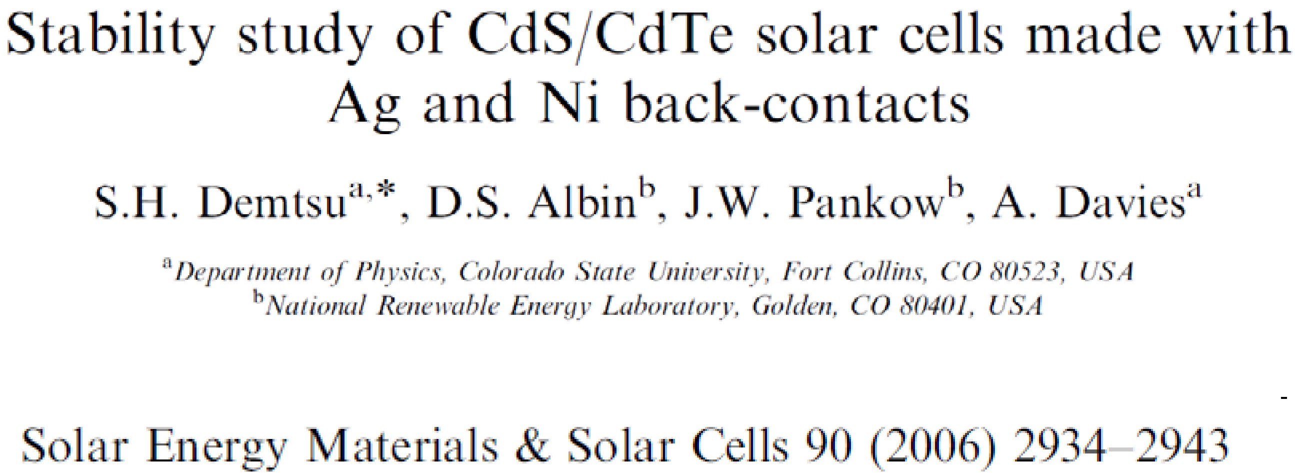


Be conscious of humidity

1) Best to shroud system in dry inert atmosphere to eliminate oxidation and humidity related effects
2) If not, then be aware that lab-air humidity is present
3) Graph at left shows that a 100 C test in a typical lab environment (RH% = 30%) implies a test RH% of around 1 RH%)
4) CdTe cell can be designed to be less sensitive to moisture
5) CIGS cells (with exposed TCOs like ZnO) not so.

Several Case Studies concerning Cell Durability Research

Back contact processing and cell durability



Stability study of CdS/CdTe solar cells made with Ag and Ni back-contacts

S.H. Demtsu[a,*], D.S. Albin[b], J.W. Pankow[b], A. Davies[a]

[a]*Department of Physics, Colorado State University, Fort Collins, CO 80523, USA*
[b]*National Renewable Energy Laboratory, Golden, CO 80401, USA*

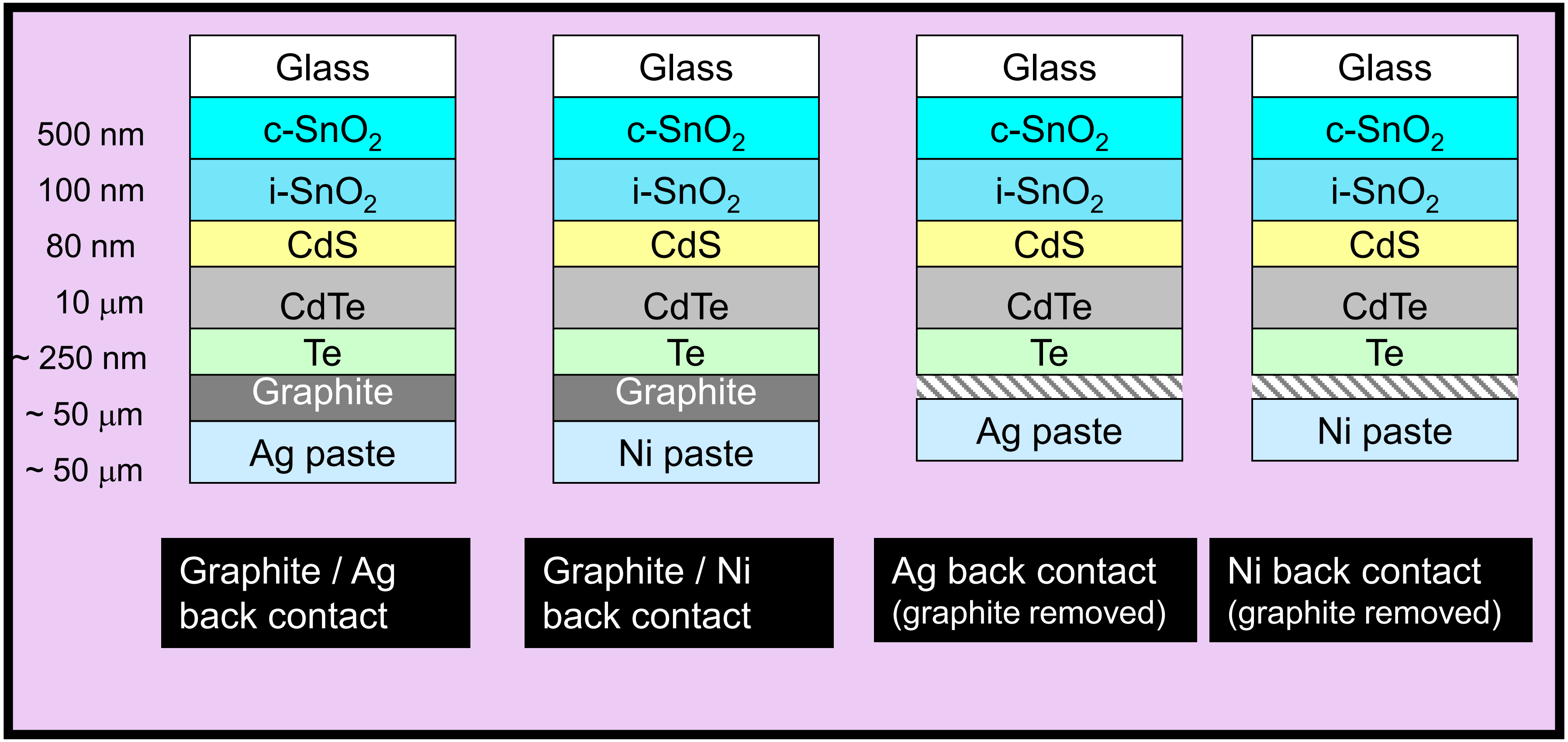
Solar Energy Materials & Solar Cells 90 (2006) 2934–2943

Outline

- Device Structure
- J-V, CV and LBIC before and after stress
- Effects of Ag and Ni diffusion
- Conclusions

Device Structure

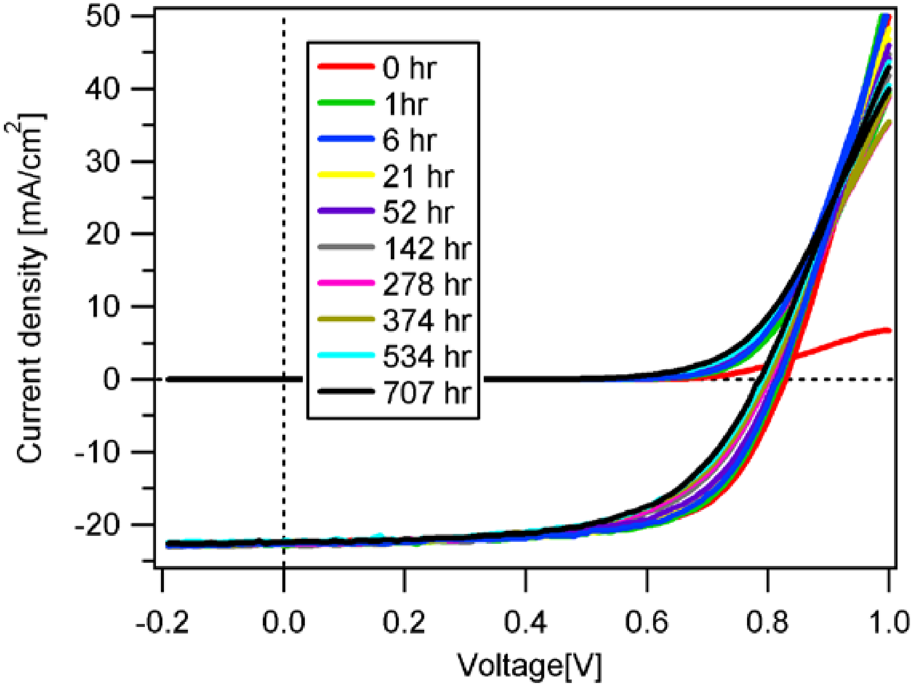
Motivation: To study the effect of Ag diffusion and graphite paste on device stability



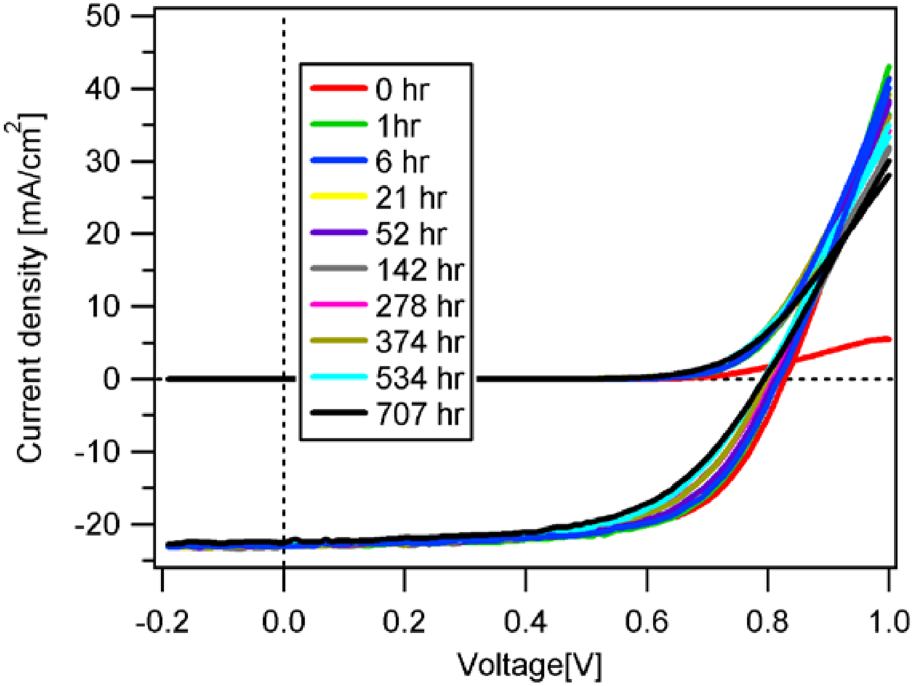
	Graphite / Ag back contact	Graphite / Ni back contact	Ag back contact (graphite removed)	Ni back contact (graphite removed)
	Glass	Glass	Glass	Glass
500 nm	c-SnO_2	c-SnO_2	c-SnO_2	c-SnO_2
100 nm	i-SnO_2	i-SnO_2	i-SnO_2	i-SnO_2
80 nm	CdS	CdS	CdS	CdS
10 μm	CdTe	CdTe	CdTe	CdTe
~ 250 nm	Te	Te	Te	Te
~ 50 μm	Graphite	Graphite	▨	▨
~ 50 μm	Ag paste	Ni paste	Ag paste	Ni paste

J-V Curves (OC, 100^{0}C, One Sun)

Graphite/Ag



Graphite/Ni



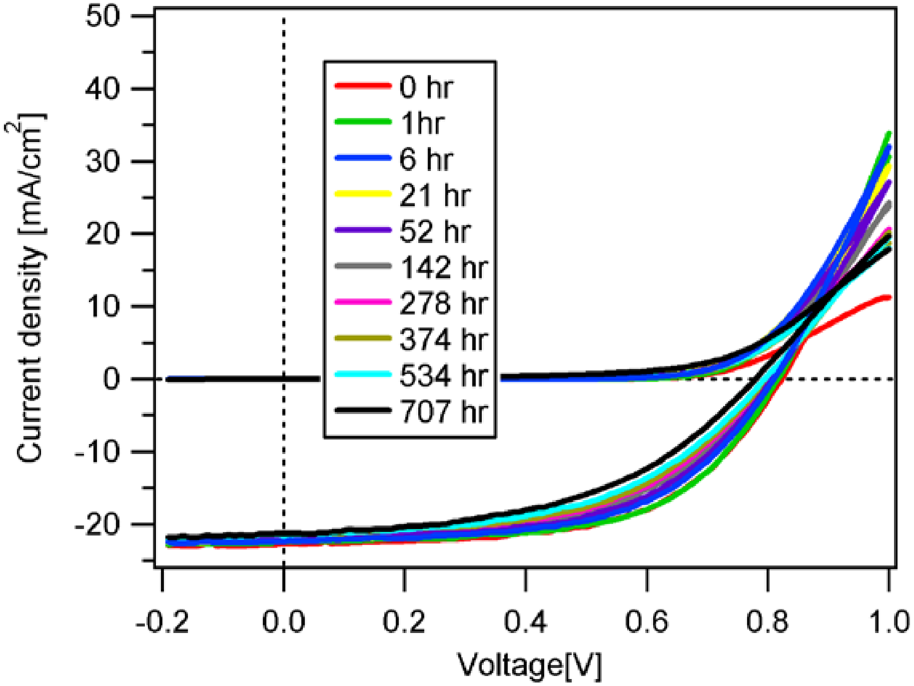
- ΔJ_{sc} = 0 mA/cm^2
- ΔV_{oc} = 42 mV
- ΔFF = 6.5 %
- $\Delta\eta$ = 1.8 %

Changes after Stress

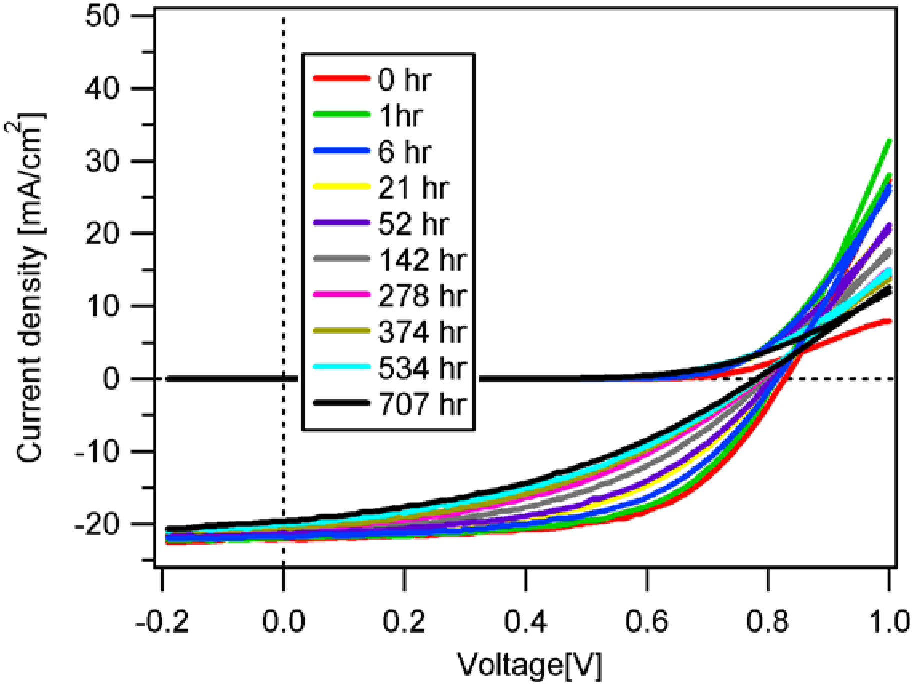
- ΔJ_{sc} = 0 mA/cm^2
- ΔV_{oc} = 37 mV
- ΔFF = 7.5 %
- $\Delta\eta$ = 2.1 %

J-V Curves (OC, 100⁰C, One Sun)

Ag only
(graphite removed)



Ni only
(graphite removed)

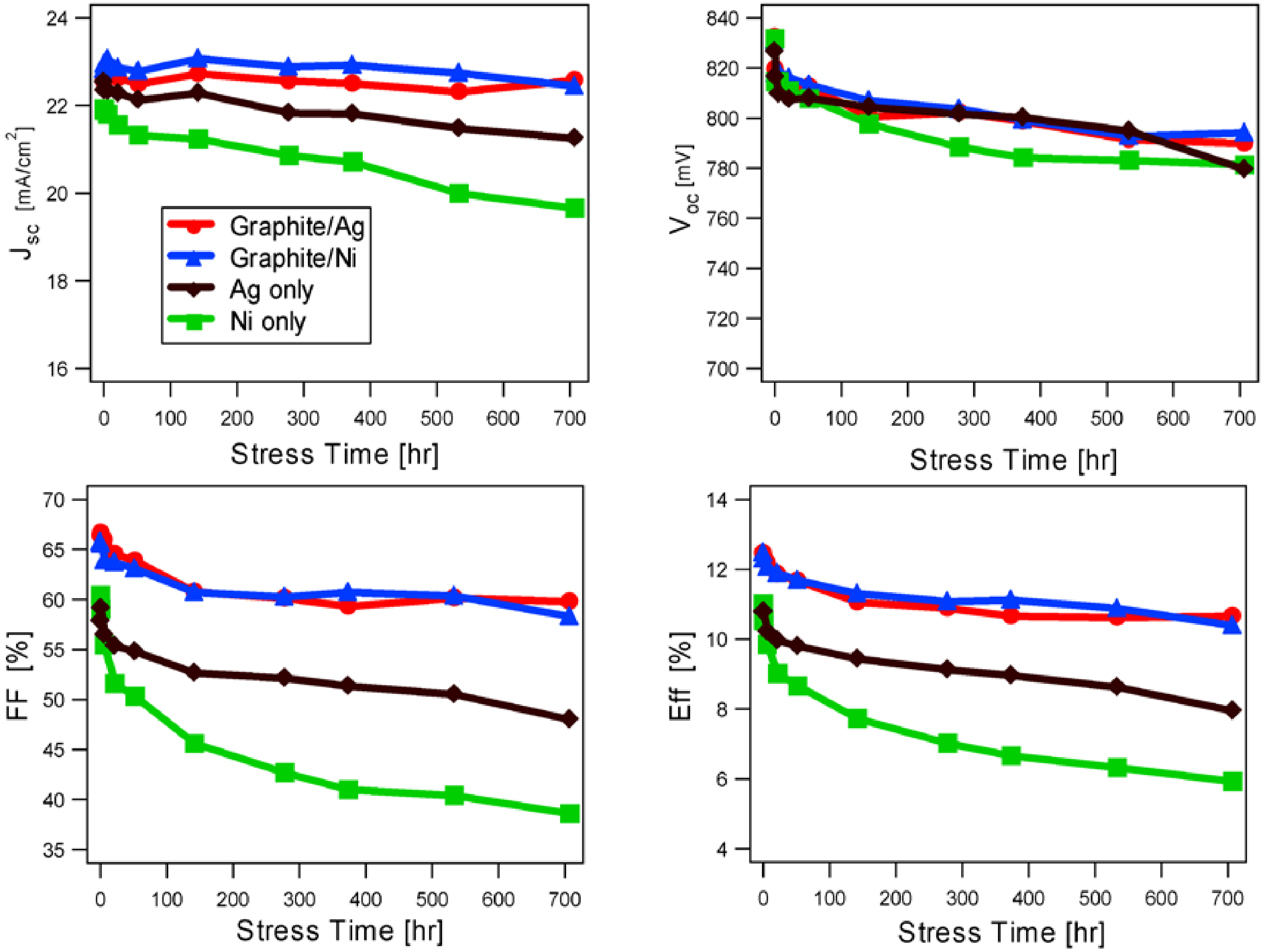


- ΔJ_{sc} = 1.3 mA/cm^2
- ΔV_{oc} = 39 mV
- ΔFF = 10 %
- Δη = 2.8 %

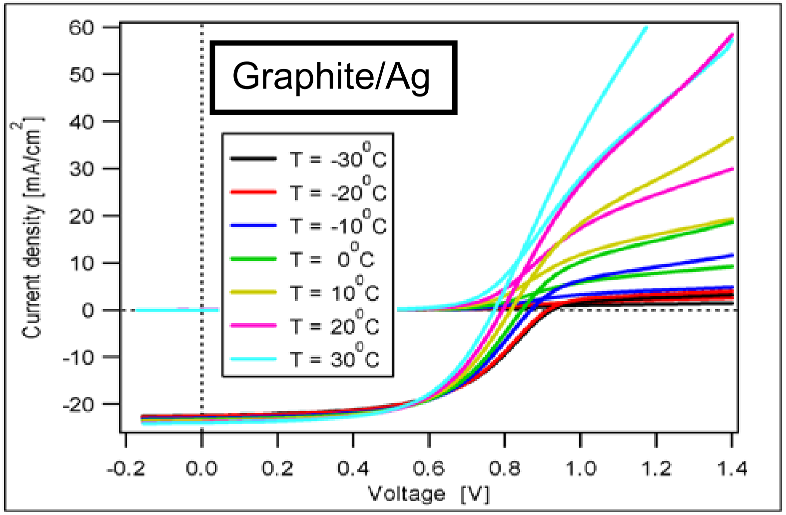
Changes after Stress

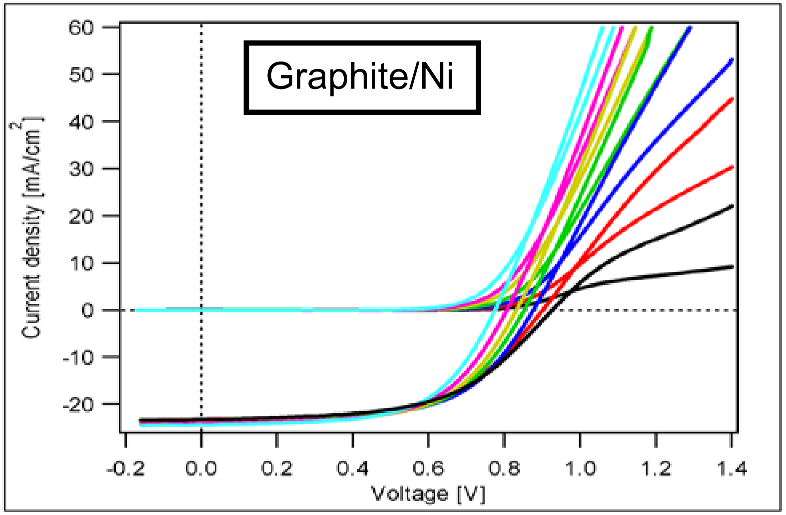
- ΔJ_{sc} = 2.3 mA/cm^2
- ΔV_{oc} = 52 mV
- ΔFF = 21 %
- Δη = 5.1 %

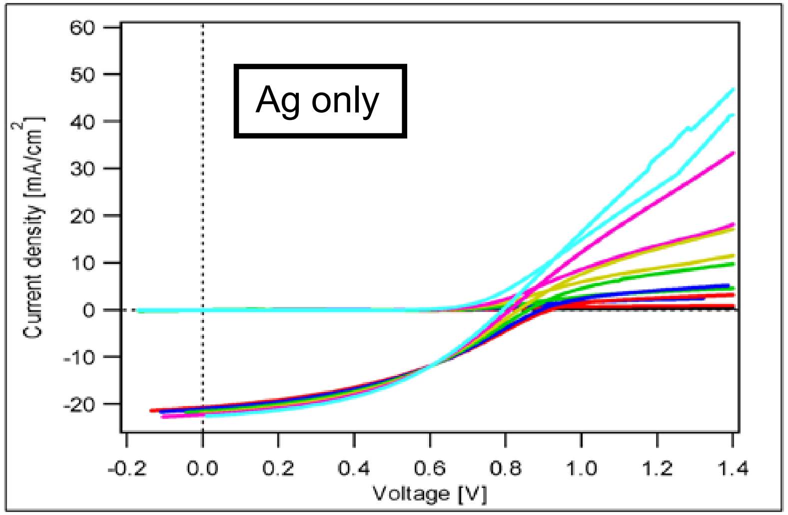
Parameters After Stress (OC, 100^{0}C)

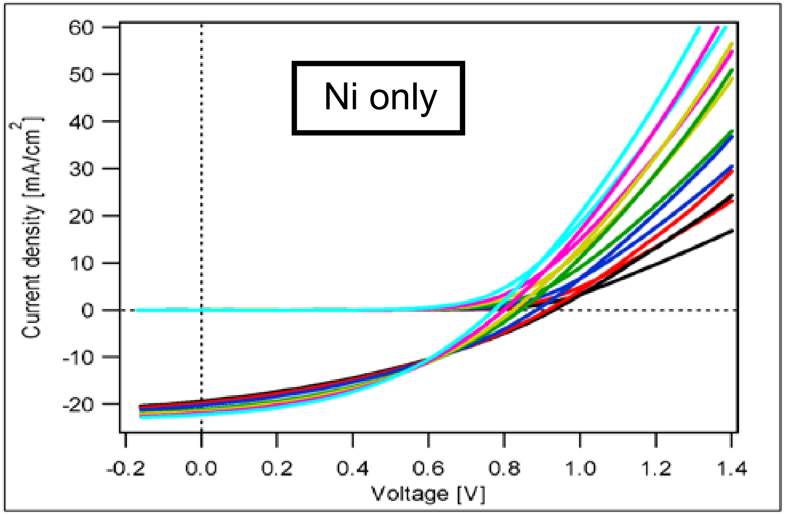


Temperature Dependence After Stress



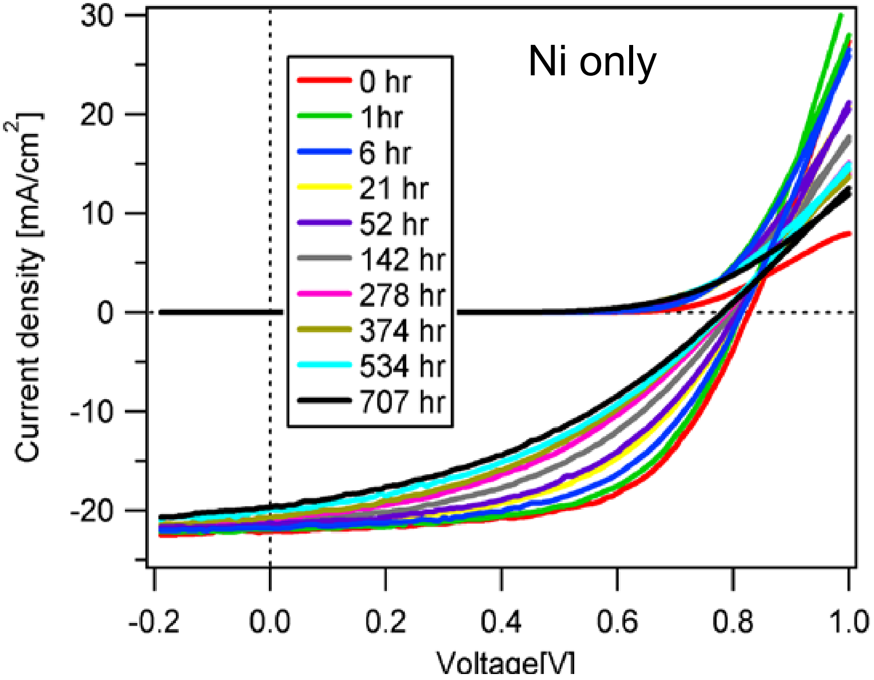




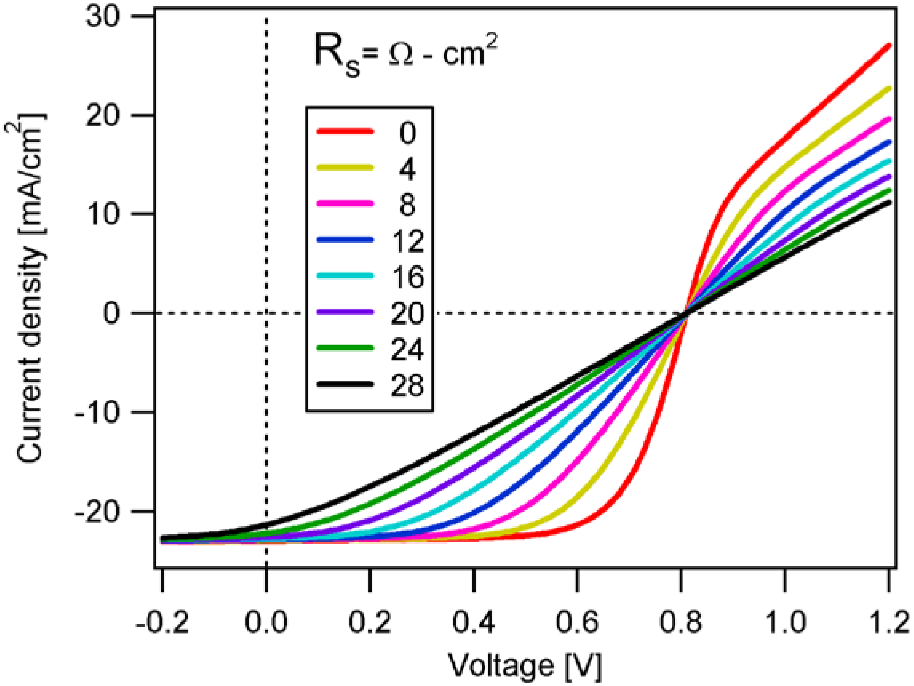


Effect of Large R_s (Simulation)

Modest rollover (Φ_b = 0.55 eV)

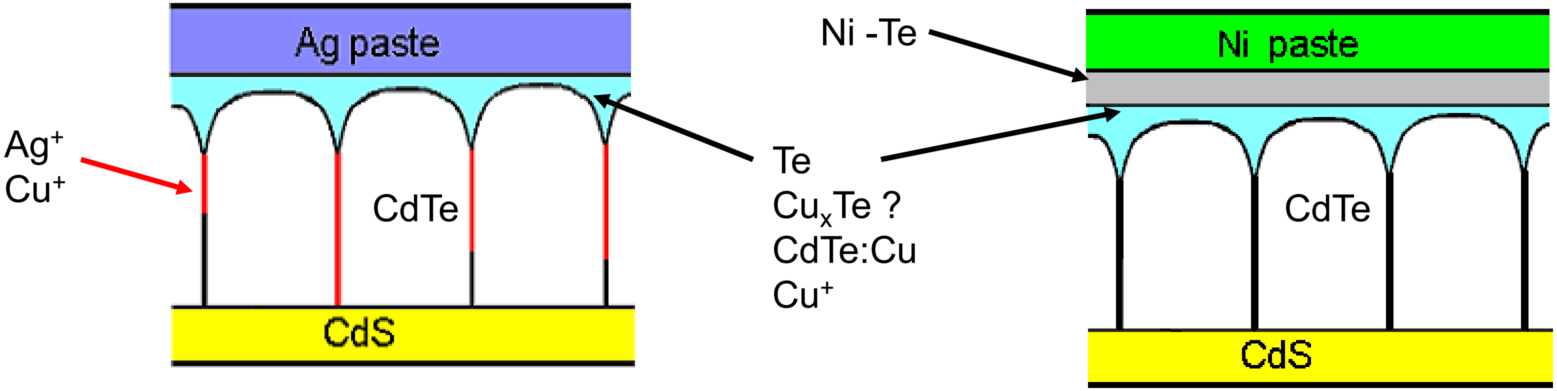


Measured



Simulated

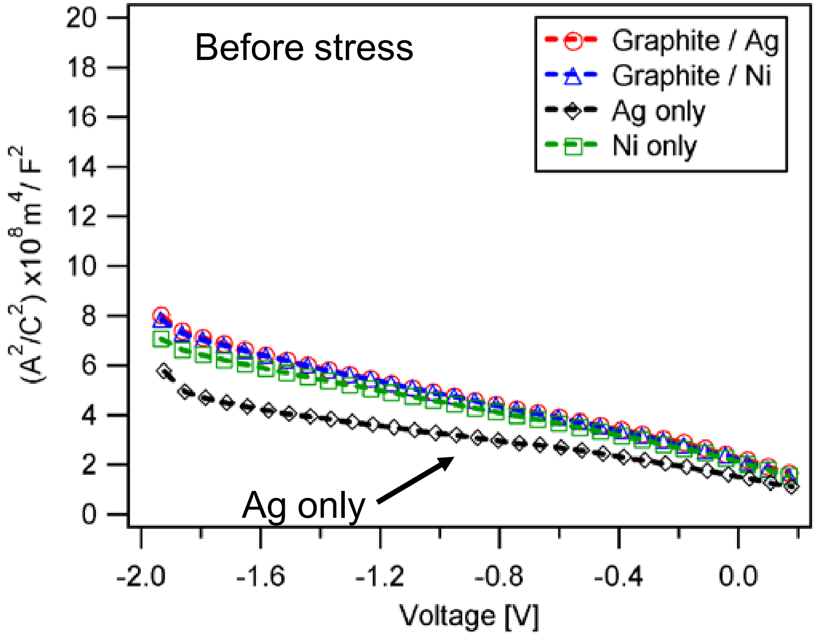
Ag and Ni Diffusion (no graphite)

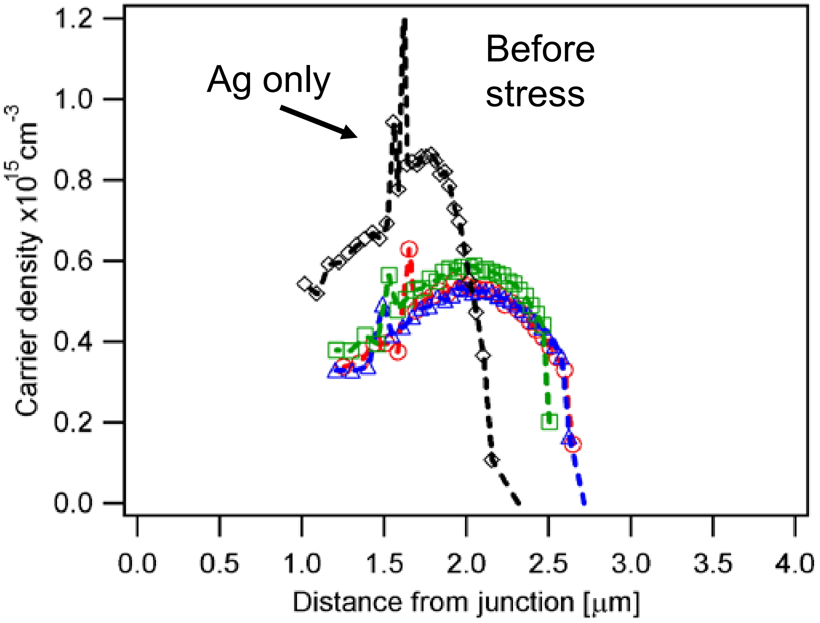


Ag^+
Cu^+

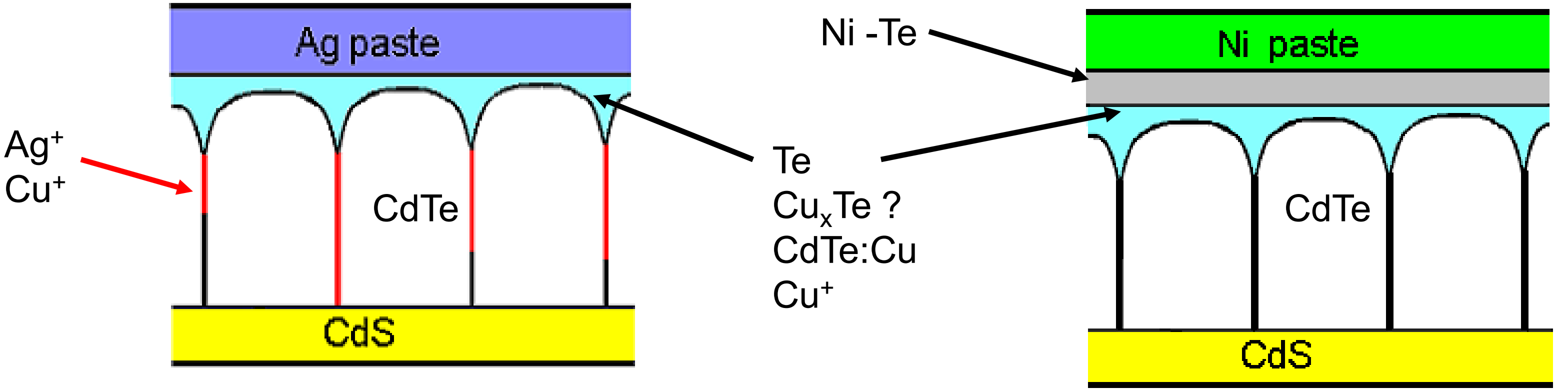
Ni -Te

Te
Cu_xTe ?
CdTe:Cu
Cu^+





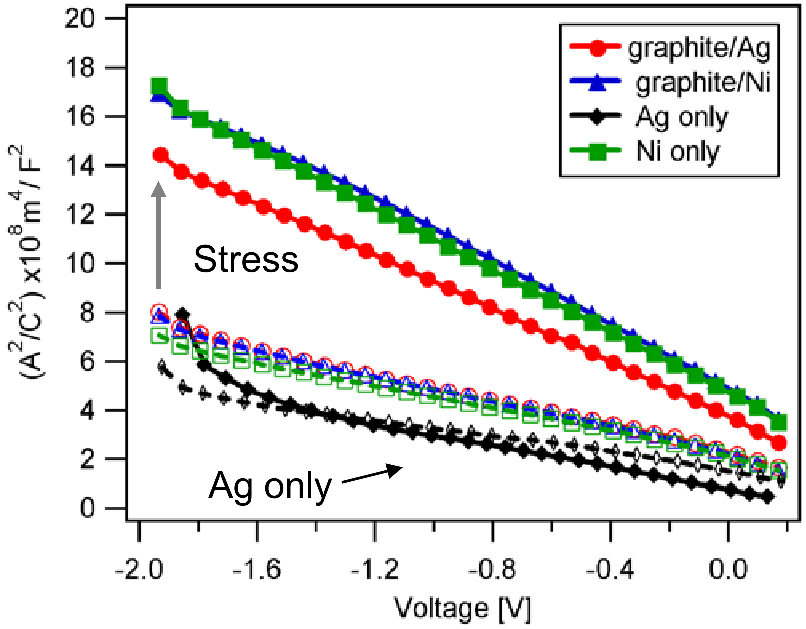
Ag and Ni Diffusion (no graphite)

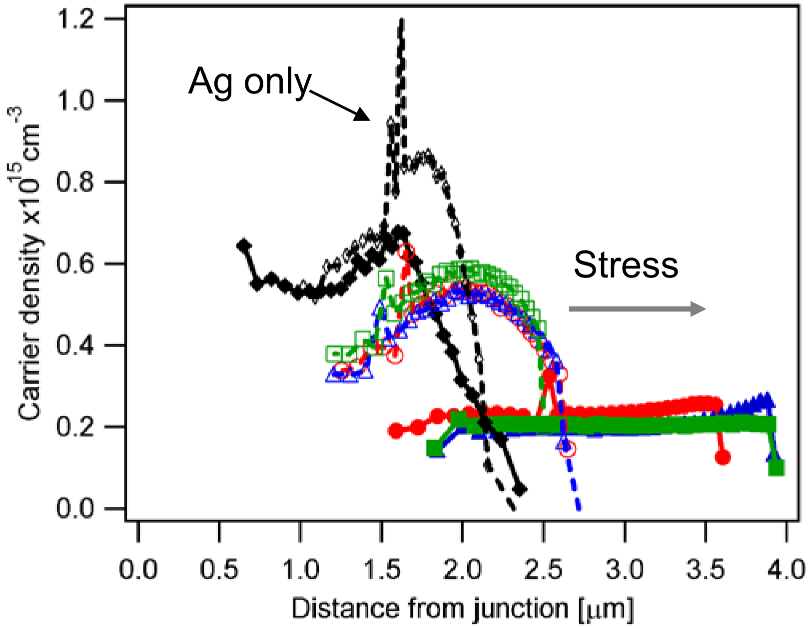


Ag^+
Cu^+

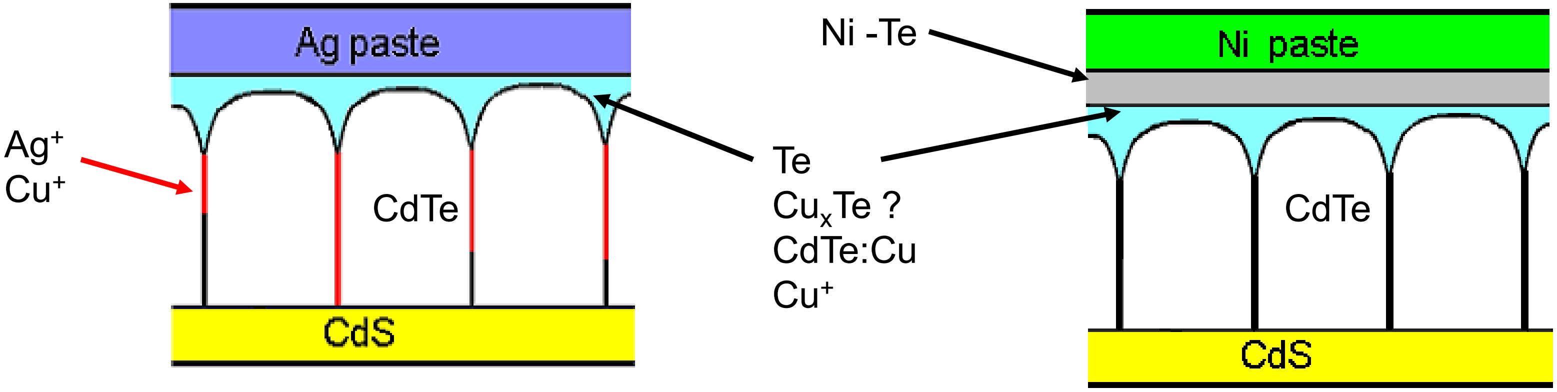
Ni -Te

Te
Cu_xTe ?
CdTe:Cu
Cu^+

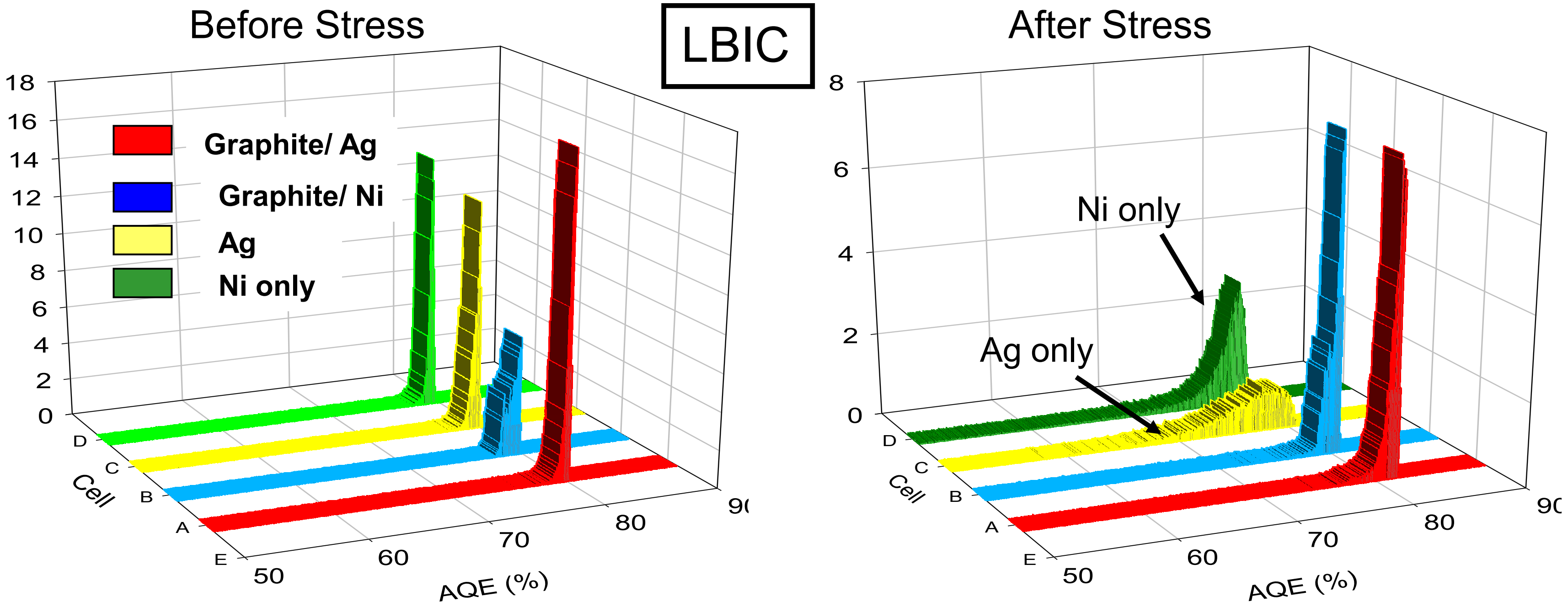




Ag and Ni Diffusion (no graphite)

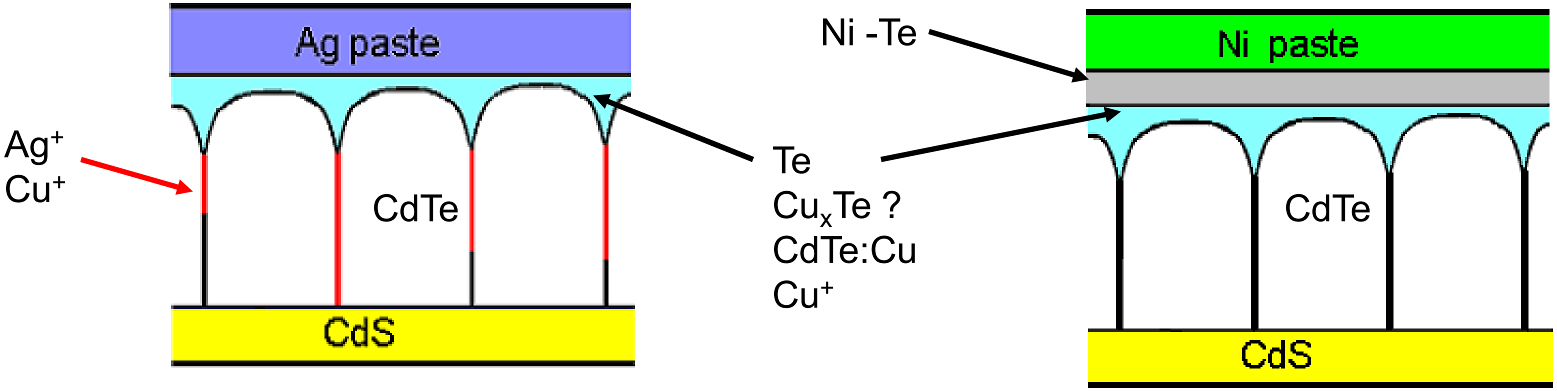


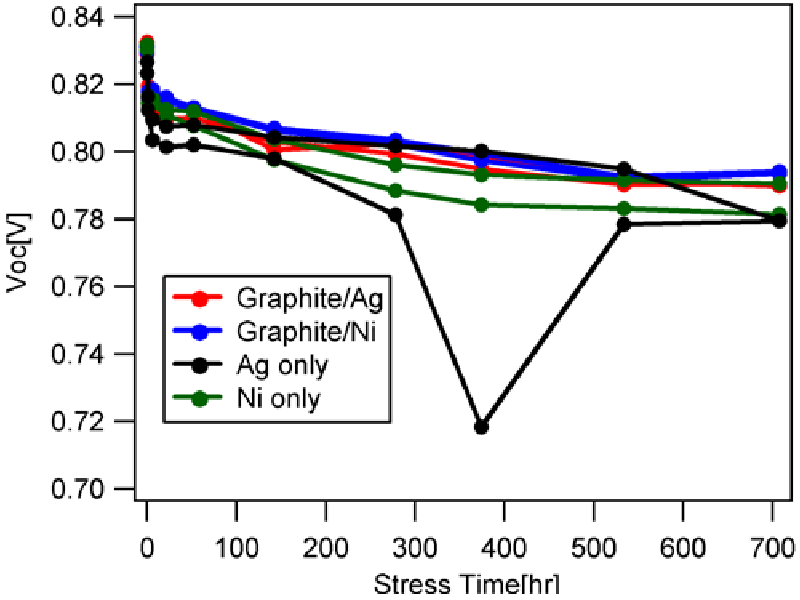
LBIC

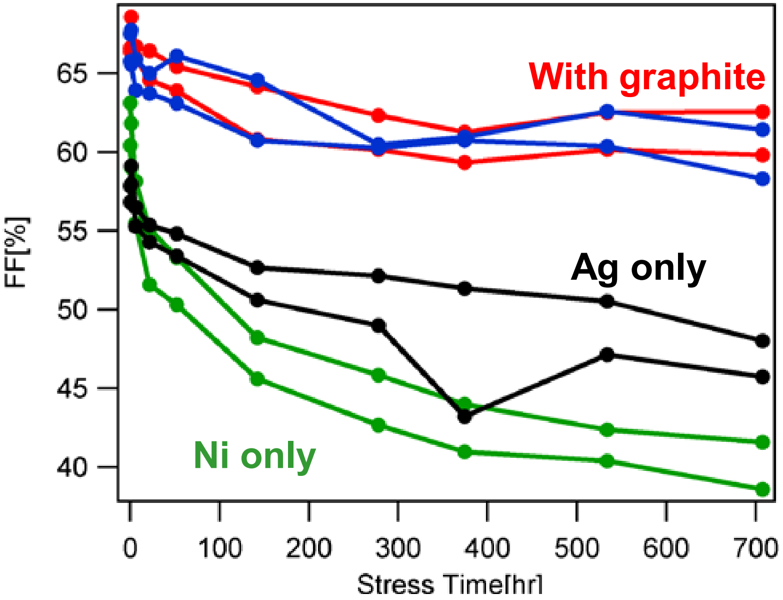

Before Stress

After Stress

Ag and Ni Diffusion (no graphite)

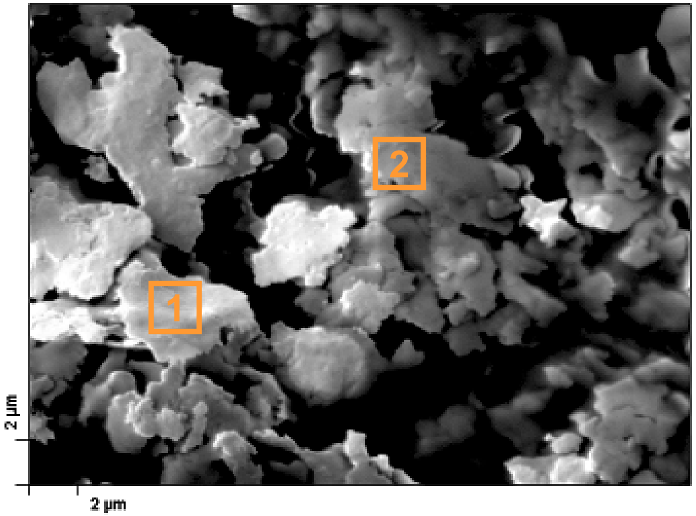






Surface Analysis Of The Silver Paste

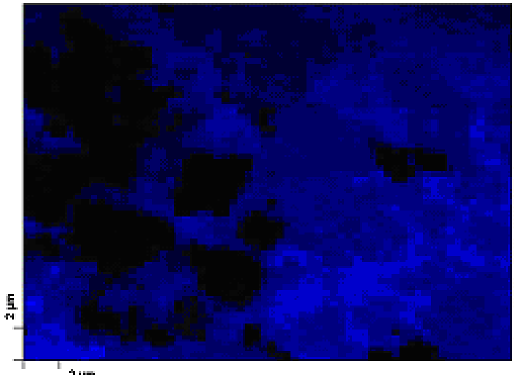
SEM



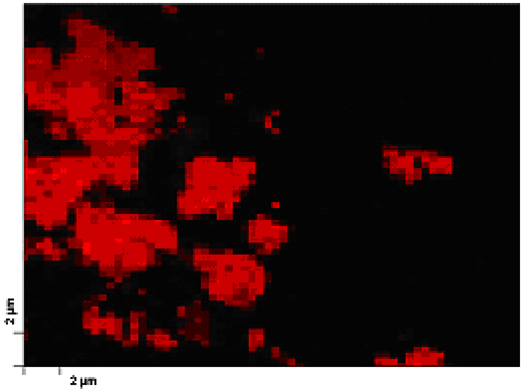
Atomic Concentration

Area	C	Ag	Cl
1	2.6	82.5	15.4
2	10	0	0

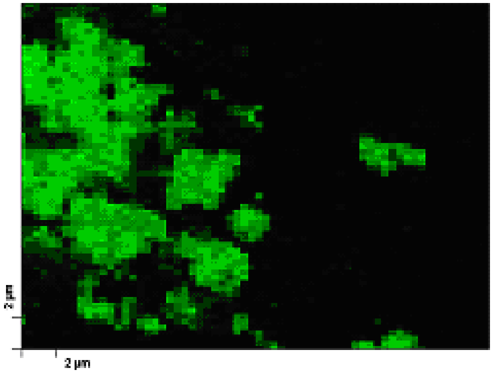
Carbon map



Silver map



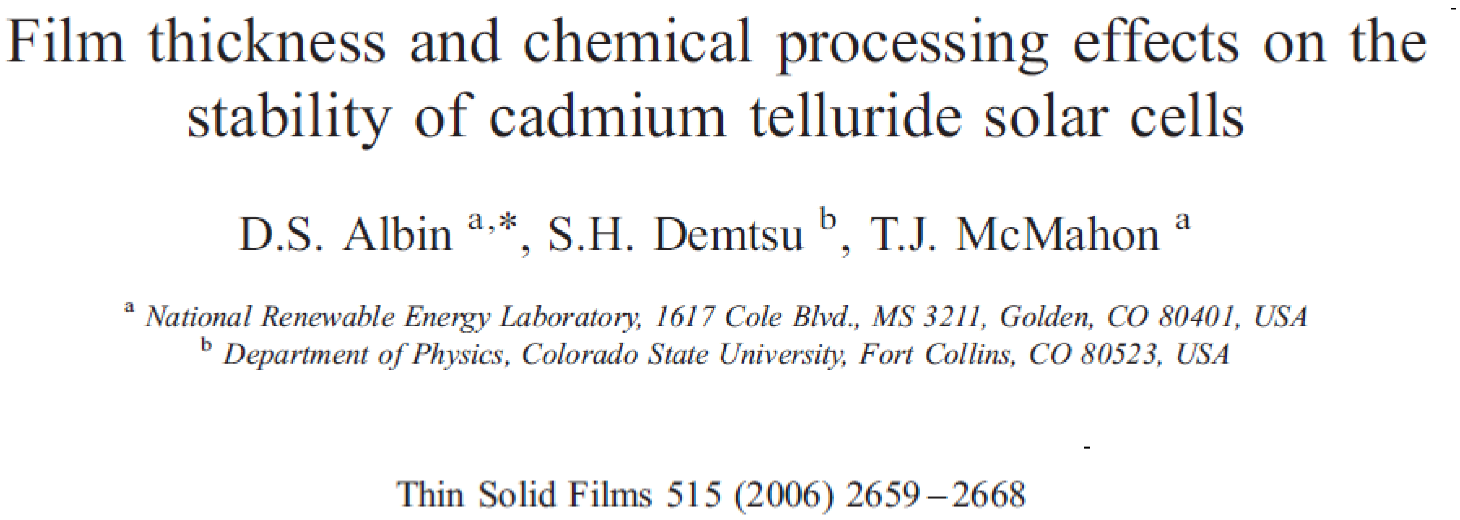
Cl map



Conclusions

1) No major difference was seen between devices made with **graphite/Ag** and **graphite/ Ni** back contacts.
2) Devices degraded faster when the graphite layer is removed.
   a) Diffusion of Ag+
   b) Formation of Ni -Te alloy
3) The graphite layer binder (polyacrylic acid) may function as a diffusion barrier, by trapping metals that diffuse from the back-contact.
4) LBIC reveals large non-uniformity when Ag metal is used in the absence of graphite. (due to Ag+ diffusion).
5) After stress large increase in series resistance that masked the increase in back-barrier height was observed when graphite is removed.

CdTe Processing and cell durability



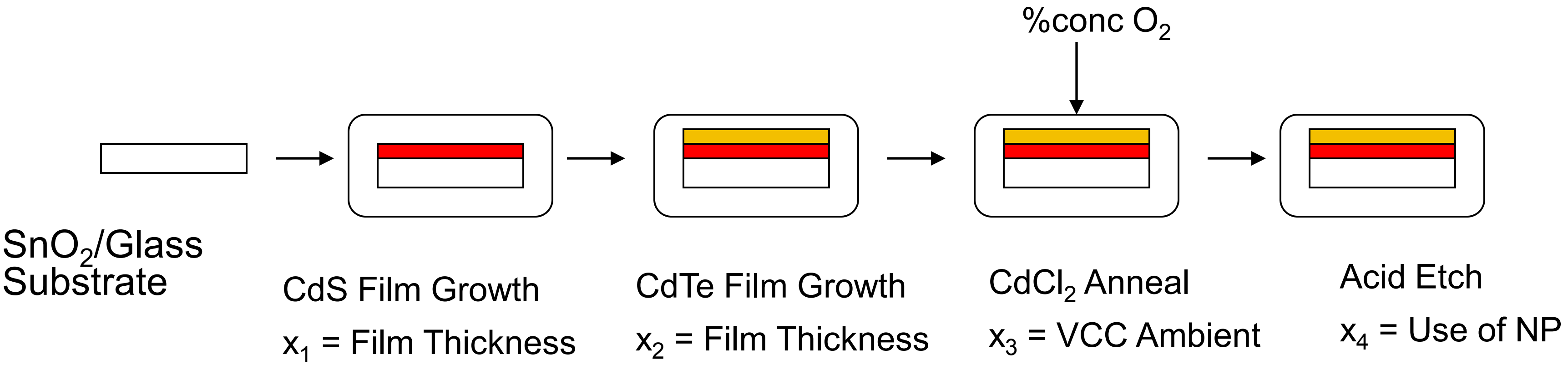
Film thickness and chemical processing effects on the stability of cadmium telluride solar cells

D.S. Albin [a,*], S.H. Demtsu [b], T.J. McMahon [a]

[a] *National Renewable Energy Laboratory, 1617 Cole Blvd., MS 3211, Golden, CO 80401, USA*
[b] *Department of Physics, Colorado State University, Fort Collins, CO 80523, USA*

Thin Solid Films 515 (2006) 2659 – 2668

DOE Example – Balancing CdTe solar cell performance and stability



%conc O_2

SnO_2/Glass Substrate

CdS Film Growth

x_1 = Film Thickness

CdTe Film Growth

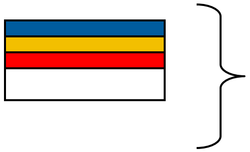
x_2 = Film Thickness

$CdCl_2$ Anneal

x_3 = VCC Ambient

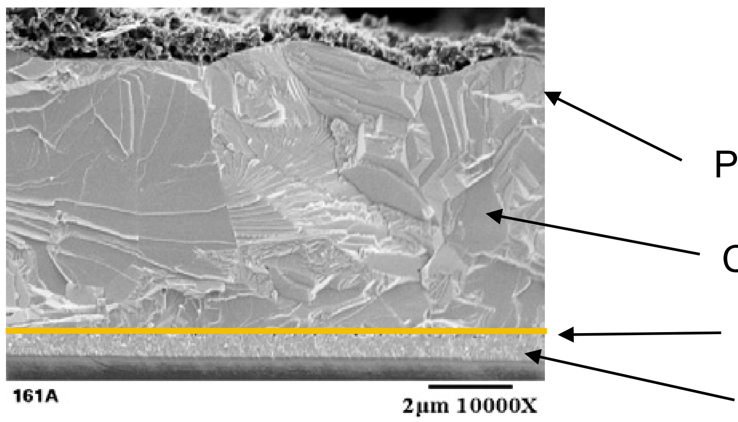
Acid Etch

x_4 = Use of NP



Measure Initial Performance (Efficiency)

Accelerated Life Testing (700 hrs)



Pre contact etch (nitric phosphoric acid)

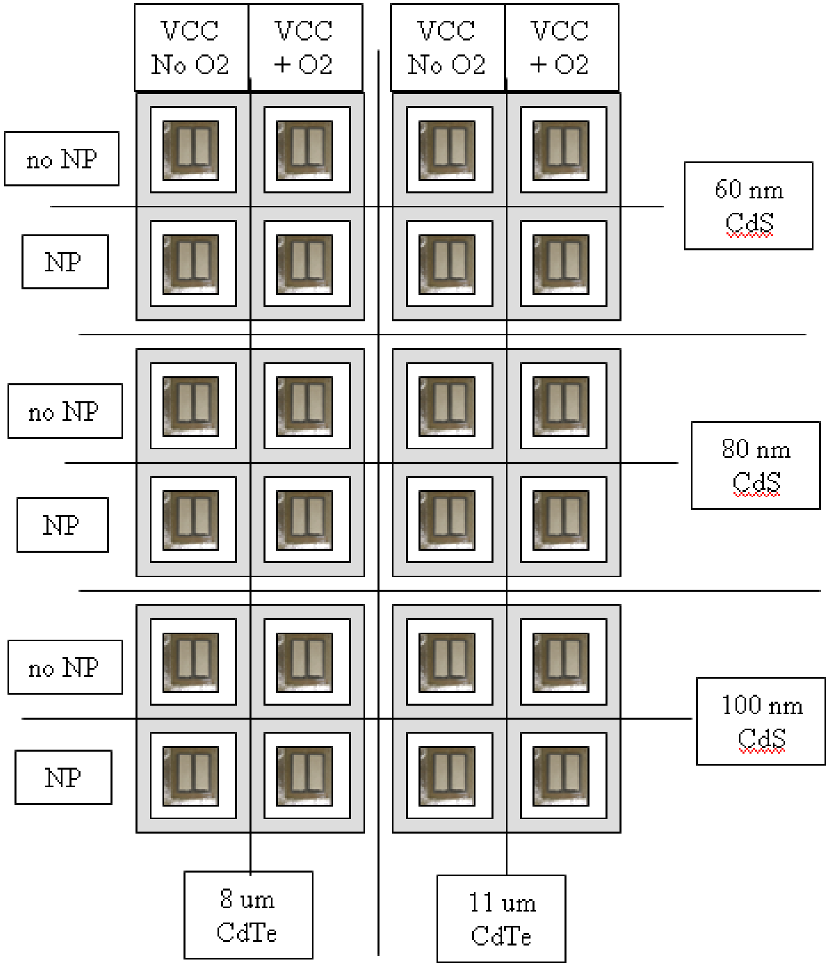
CdTe + vapor CdCl2 process (+ O_2)

CdS

SnO_2/Glass

light

DOE Example – Balancing CdTe solar cell performance and stability



VCC No O2
VCC + O2
VCC No O2
VCC + O2

no NP
NP
60 nm CdS

no NP
NP
80 nm CdS

no NP
NP
100 nm CdS

8 um CdTe
11 um CdTe

VCC = vapor $CdCl_2$ (T=400C)

NP = nitric phosphoric acid etch

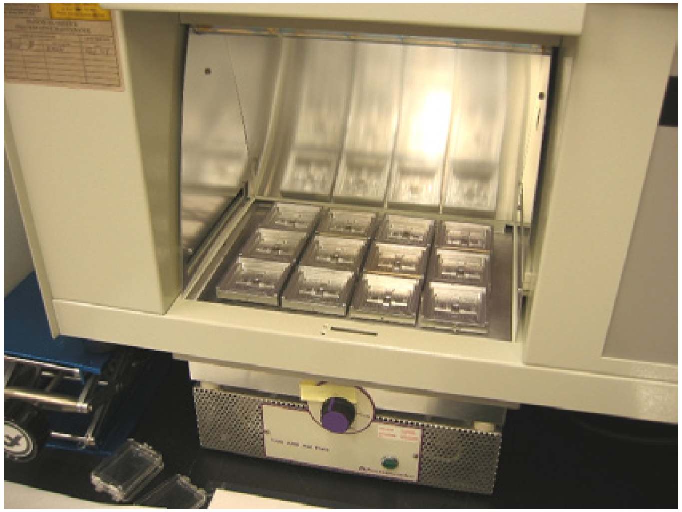
CdTe = CSS CdTe

CdS = CBD CdS

VCC no O_2= 500 torr He

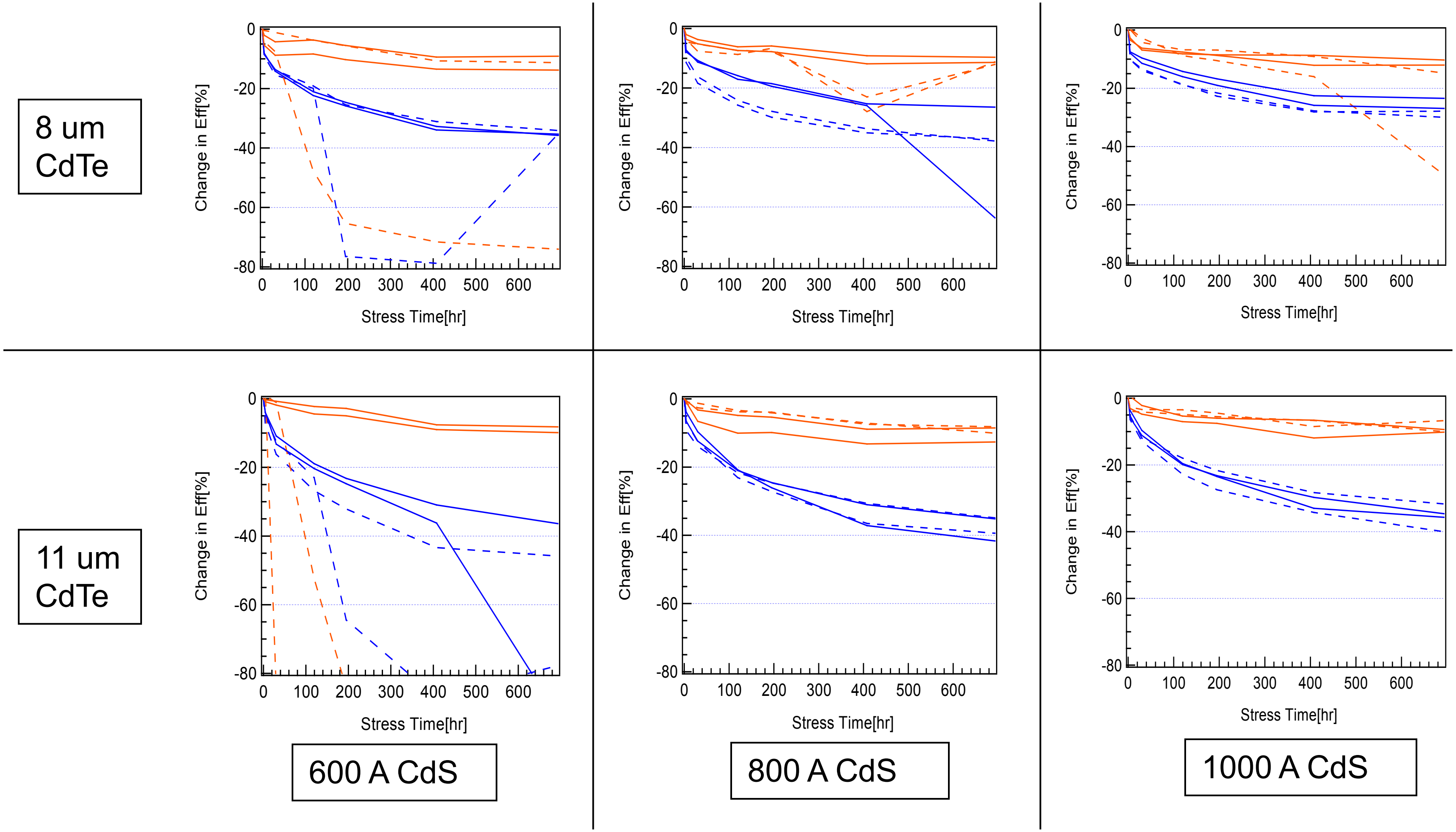
VCC + O_2 = 100/400 torr O_2/He

8 um CdTe = 3.25 min dep time 11 um CdTe = 5.25 min dep time



- 2 Replicates of 24 Variable = 48 devices
- Stress Testing: V_{oc} bias, 1 Sun, 100 ± 2 ºC
- Measurements performed at t = 0, 4.25, 30, 119, 195, 408, and 693 hrs.
- Prior to J-V measurements samples stored in dark at 25 ºC

DOE Example – Balancing CdTe solar cell performance and stability



Red – NP; **Blue** – no Etch

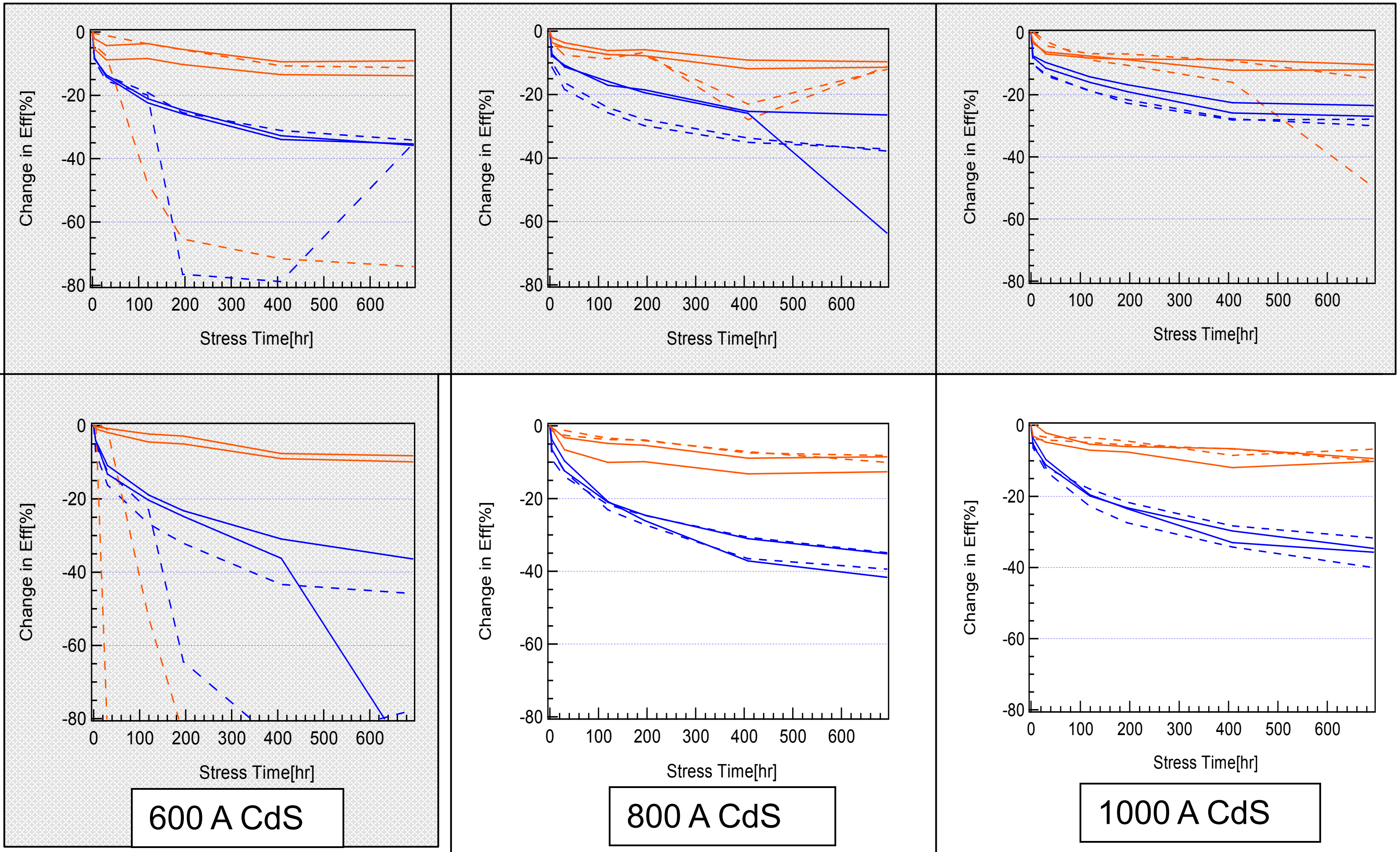
Solid - O_2 during VCC (100/400); dashed - NO O_2 (0/500)

compare **blue** with **red** – use of NP etch better

DOE Example – Balancing CdTe solar cell performance and stability

8 um CdTe

11 um CdTe



600 A CdS

800 A CdS

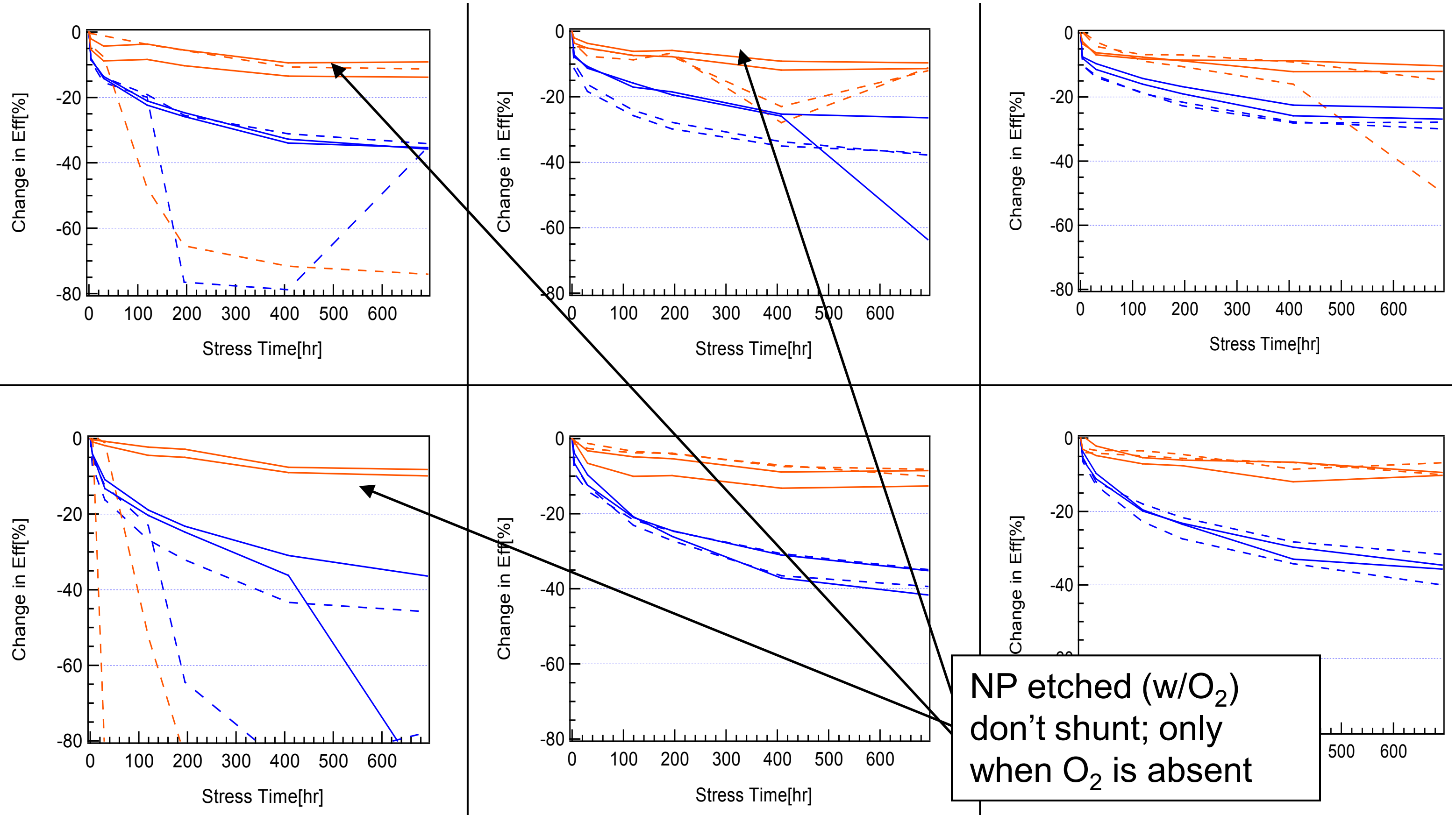
1000 A CdS

Red – NP; **Blue** – no Etch

Solid - O_2 during VCC (100/400); dashed - NO O_2 (0/500)

Notice increased shunting with thinner CdS and also (to some degree) thinner CdTe

DOE Example – Balancing CdTe solar cell performance and stability



8 um CdTe

11 um CdTe

600 A CdS

800 A CdS

1000 A CdS

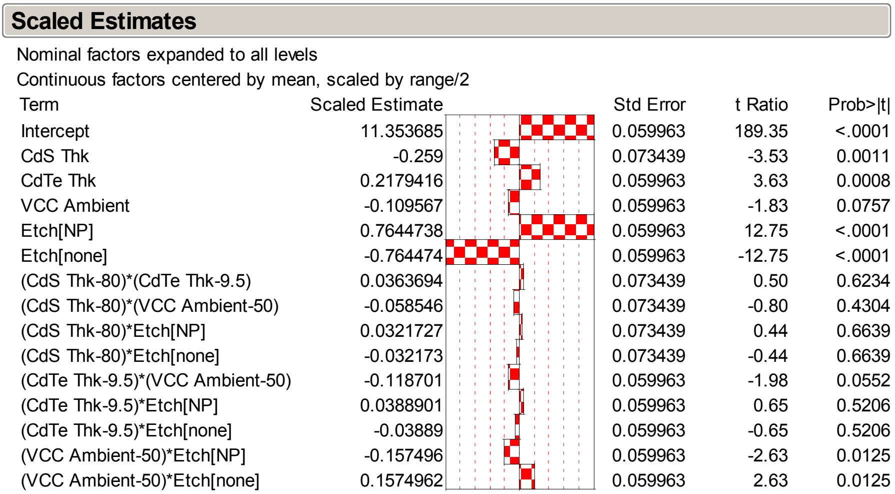
NP etched (w/O_2) don’t shunt; only when O_2 is absent

Red – NP; **Blue** – no Etch

Solid - O_2 during VCC (100/400); dashed - NO O_2 (0/500)

consider dashed (no O_2) vs solid (w O_2) lines (particularly NP etched (**red**))

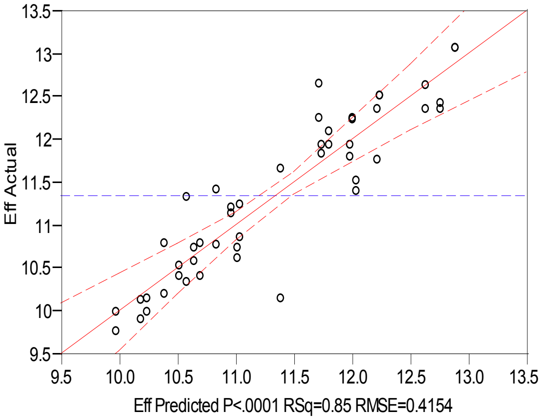
DOE Example – Balancing CdTe solar cell performance and stability



Scaled Estimates

Nominal factors expanded to all levels
Continuous factors centered by mean, scaled by range/2

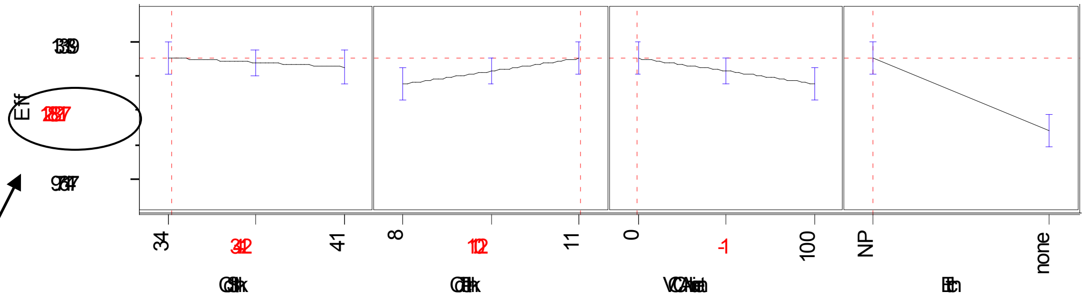
Term	Scaled Estimate	Std Error	t Ratio	Prob>|t|
Intercept	11.353685	0.059963	189.35	<.0001
CdS Thk	-0.259	0.073439	-3.53	0.0011
CdTe Thk	0.2179416	0.059963	3.63	0.0008
VCC Ambient	-0.109567	0.059963	-1.83	0.0757
Etch[NP]	0.7644738	0.059963	12.75	<.0001
Etch[none]	-0.764474	0.059963	-12.75	<.0001
(CdS Thk-80)*(CdTe Thk-9.5)	0.0363694	0.073439	0.50	0.6234
(CdS Thk-80)*(VCC Ambient-50)	-0.058546	0.073439	-0.80	0.4304
(CdS Thk-80)*Etch[NP]	0.0321727	0.073439	0.44	0.6639
(CdS Thk-80)*Etch[none]	-0.032173	0.073439	-0.44	0.6639
(CdTe Thk-9.5)*(VCC Ambient-50)	-0.118701	0.059963	-1.98	0.0552
(CdTe Thk-9.5)*Etch[NP]	0.0388901	0.059963	0.65	0.5206
(CdTe Thk-9.5)*Etch[none]	-0.03889	0.059963	-0.65	0.5206
(VCC Ambient-50)*Etch[NP]	-0.157496	0.059963	-2.63	0.0125
(VCC Ambient-50)*Etch[none]	0.1574962	0.059963	2.63	0.0125

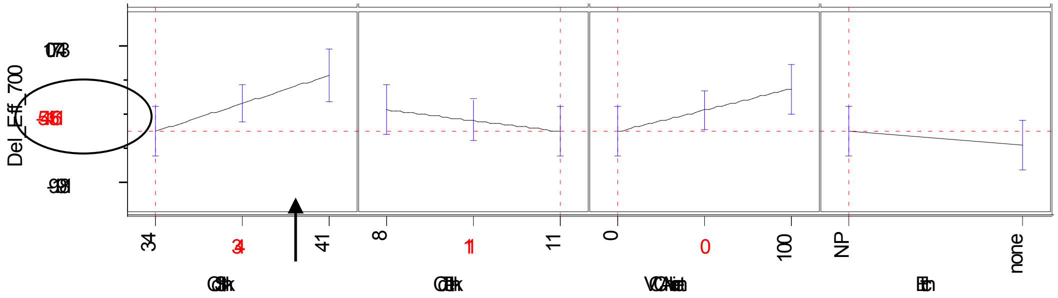


Well-correlated models between cell fabrication and performance and cell reliability are easily generated using JMP

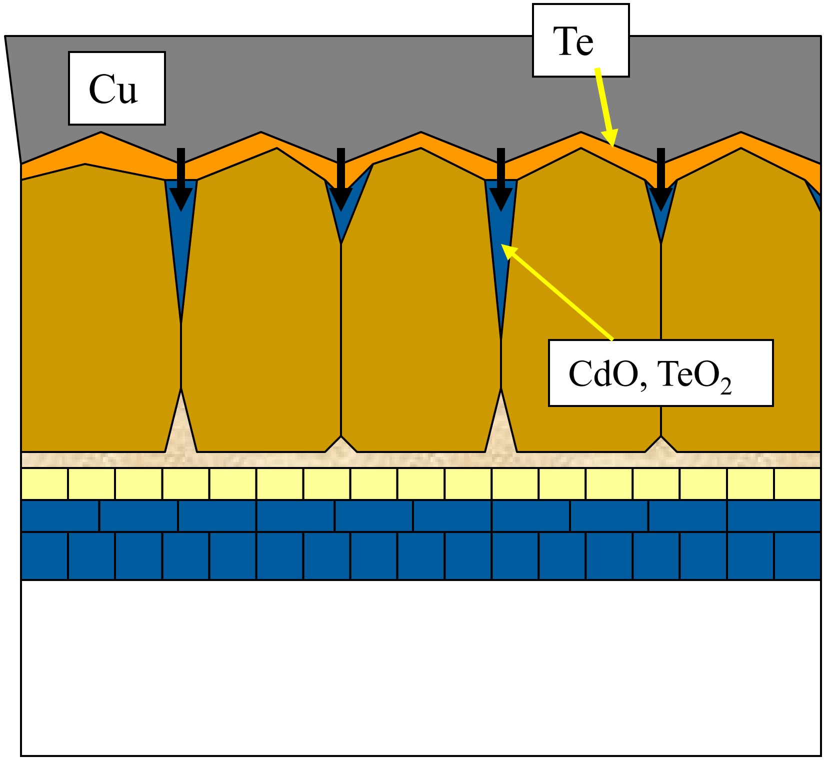
Scaled Estimates show instantly which factors and interactions are important. In the above, the most significant factor is the etch, followed by the CdS and CdTe layer thickness, and then an interaction between the CdCl$_2$ ambient and etch type.

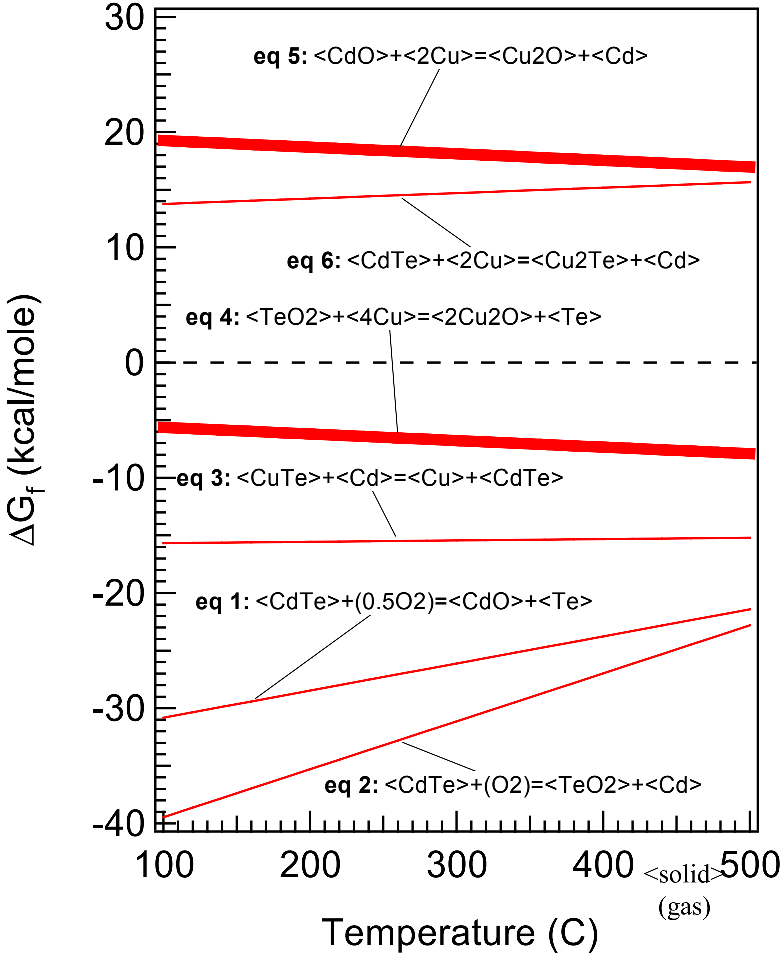
Interaction Profilers allow one to independently vary one factor and observe it's impact on an output response. In this experiment, the optimum combination of input factors (yielding an efficiency of 12.88%) yielded poor stability (54% drop in efficiency).





DOE Example – Mechanisms to Mitigate Degradation



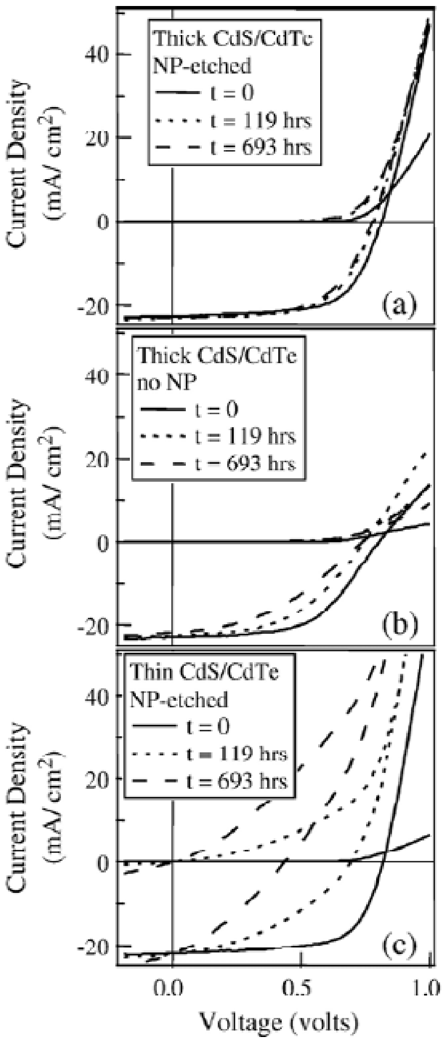


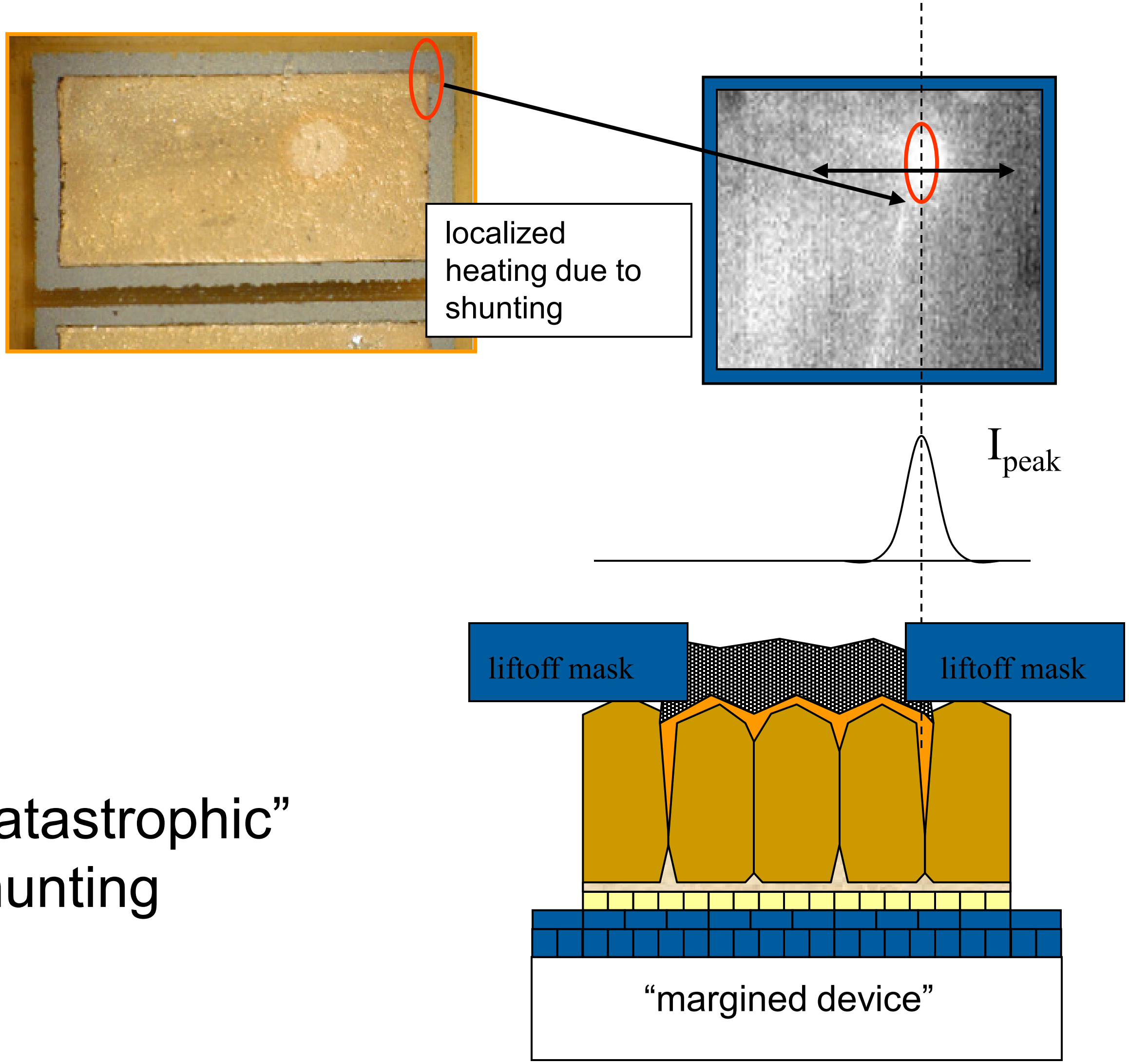
Oxides at grain boundary reduce diffusion of Cu, minimize tendency towards forming shunts of Cu at grain boundaries.

TeO$_2$ more likely to “getter” Cu than CdO. Cu will not reduce CdO.

Te at CdTe/back contact interface will “getter” Cu.

Shunt Mechanism Enhanced by Over-Etching





“catastrophic” shunting

Summary

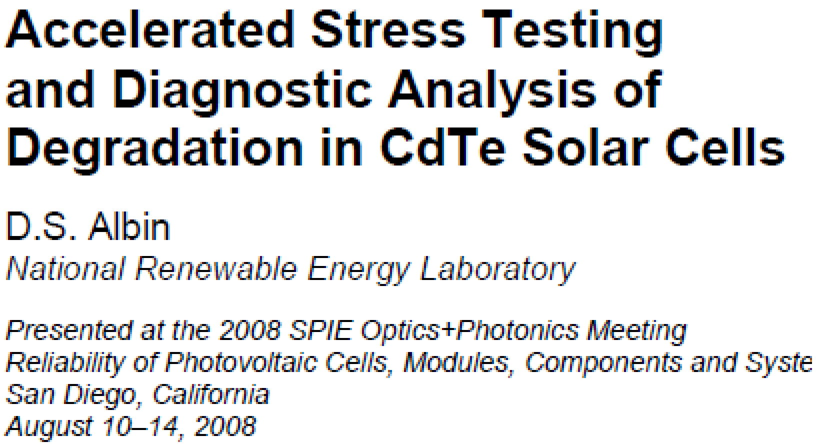
Device stability as based upon 100 ºC light-soak tests at V_{oc} bias and 1-Sun illumination show that thinner CdS and CdTe films are more prone to catastrophic shunting.

Shunting can be reduced by incorporating O_2 during the vapor $CdCl_2$ process

A thermodynamic model has been proposed suggesting that TeO_2 can “getter” Cu through the formation of Cu_2O in much the same way that Te can react with Cu to form Cu_xTe

Shunting mechanisms seen in our devices may be attributed to poor device fabrication techniques which lead to over-etching of devices near mesa corners.

Degradation Activation Energy Determination

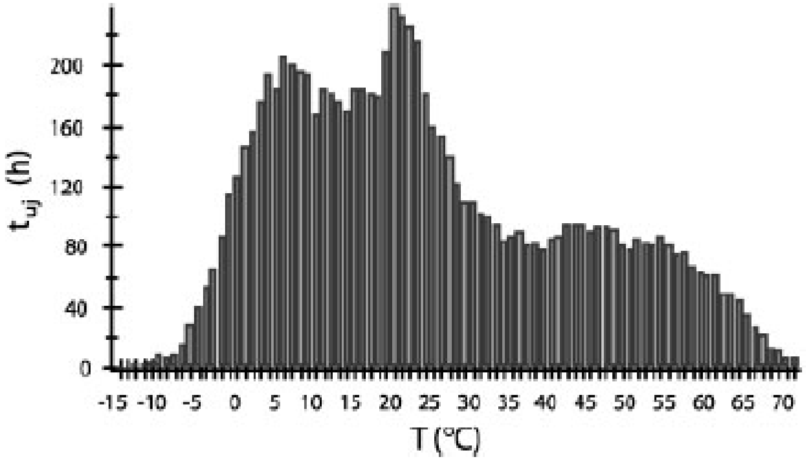


Accelerated Stress Testing and Diagnostic Analysis of Degradation in CdTe Solar Cells

D.S. Albin

National Renewable Energy Laboratory

Presented at the 2008 SPIE Optics+Photonics Meeting
Reliability of Photovoltaic Cells, Modules, Components and Syste
San Diego, California
August 10–14, 2008



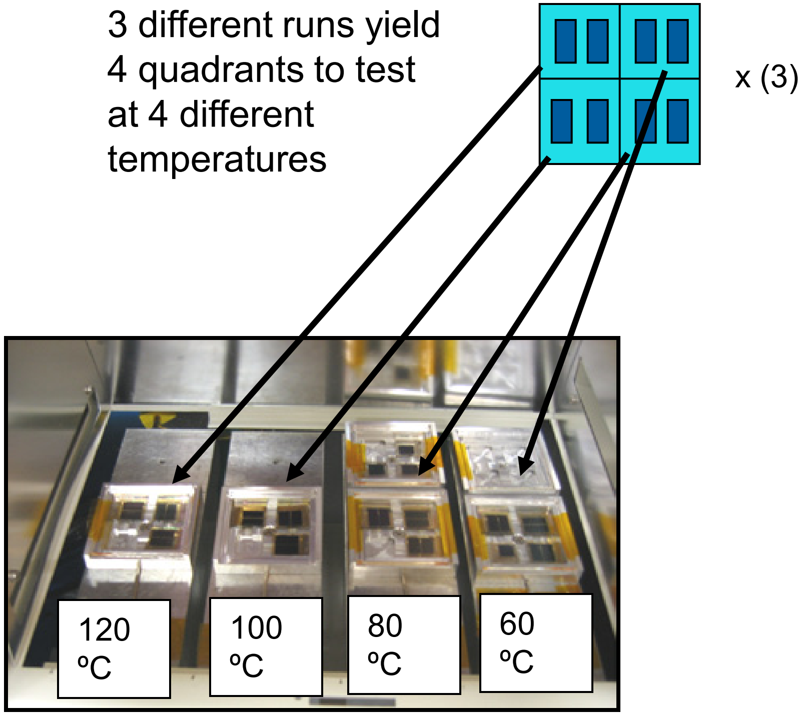
Back-of-module temperatures for Las Cruces, NM

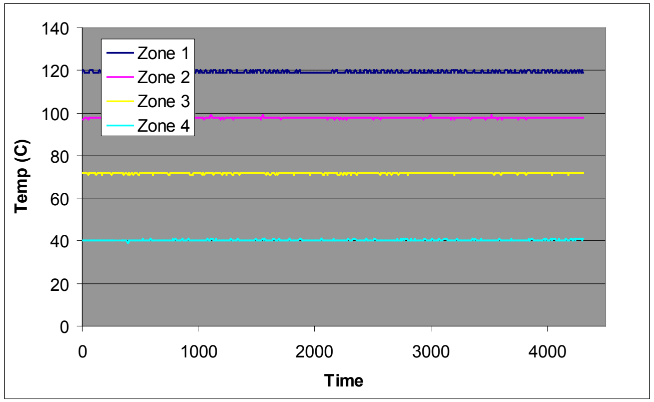
Degradation Activation Energy – Arrhenius-type study

- Light-soak stress test (1-sun, T °C, V_{oc} bias)
- Effect of varying T (60-120 °C) on CdTe cell testing
- Reproduce cells as close as possible

Device	Stress Method	Stress Temp, C	Voc	Jsc	FF	Eff
T379_A1	Combi_1	80	0.83	21.82	67.51	12.23
T379_A2	Combi_1	80	0.82	22.68	65.65	12.27
T379_B1	Combi_1	60	0.84	22.80	69.81	13.30
T379_B2	Combi_1	60	0.83	22.56	69.93	13.16
T379_C1	Combi_1	120	0.83	22.97	66.60	12.74
T379_C2	Combi_1	120	0.83	22.77	69.33	13.14
T379_D1	Combi_1	100	0.83	22.72	67.69	12.82
T379_D2	Combi_1	100	0.83	22.68	68.25	12.88
T380_A1	Combi_1	80	0.83	22.70	66.77	12.60
T380_A2	Combi_1	80	0.83	21.95	67.68	12.26
T380_B1	Combi_1	60	0.83	22.26	67.60	12.55
T380_B2	Combi_1	60	0.83	22.51	67.60	12.64
T380_C1	Combi_1	120	0.83	22.69	66.42	12.56
T380_C2	Combi_1	120	0.83	22.43	68.51	12.77
T380_D1	Combi_1	100	0.83	22.60	66.80	12.50
T380_D2	Combi_1	100	0.82	21.83	63.20	11.27
T381_A1	Combi_1	80	0.83	22.86	67.45	12.75
T381_A2	Combi_1	80	0.80	21.56	61.63	10.60
T381_B1	Combi_1	60	0.83	22.52	68.64	12.84
T381_B2	Combi_1	60	0.83	22.65	70.13	13.20
T381_C1	Combi_1	120	0.83	23.02	66.51	12.71
T381_C2	Combi_1	120	0.83	22.74	68.26	12.83
T381_D1	Combi_1	100	0.83	23.11	67.27	12.86
T381_D2	Combi_1	100	0.81	22.57	64.29	11.80

3 different runs yield 4 quadrants to test at 4 different temperatures





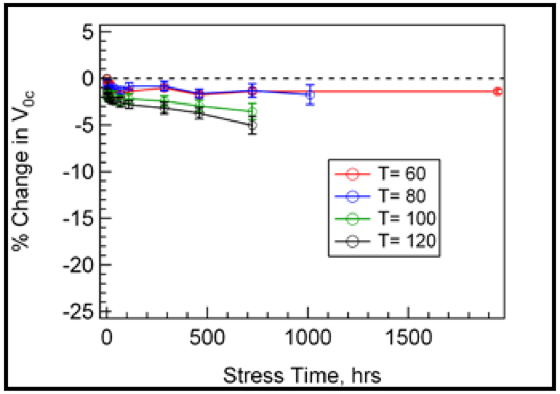
T_{dev}=120 ºC

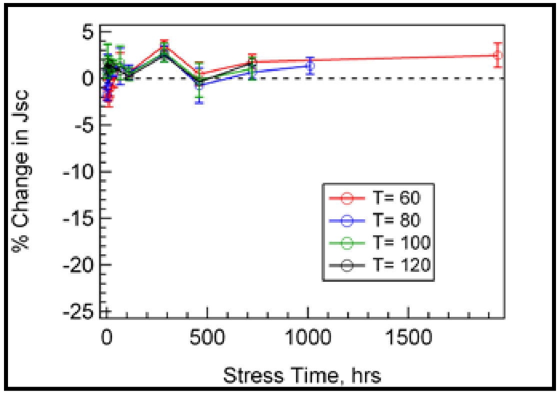
T_{dev}=100 ºC

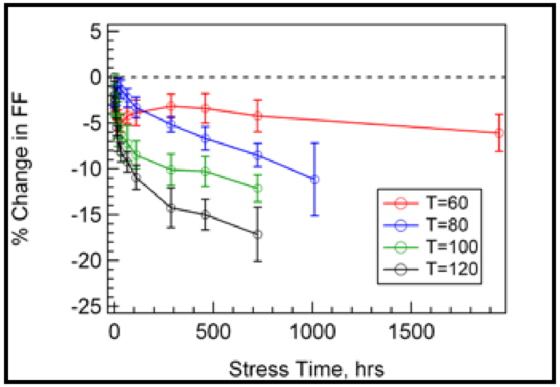
T_{dev}=80 ºC

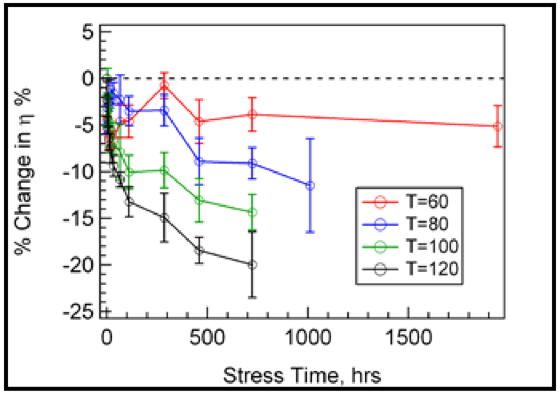
T_{dev}=60 ºC

Degradation Activation Energy – Arrhenius-type study


ΔV_{oc}

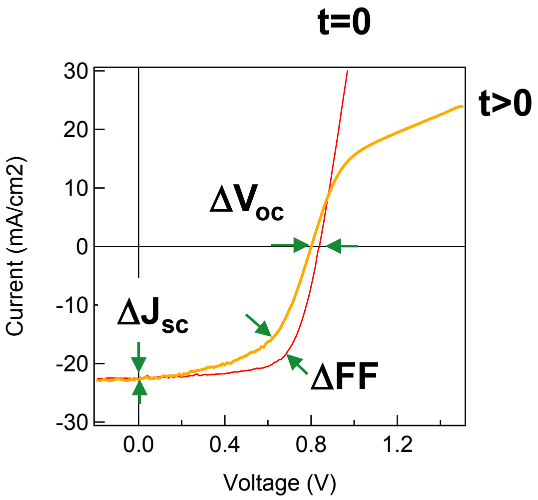

ΔJ_{sc}


ΔFF


Δη%

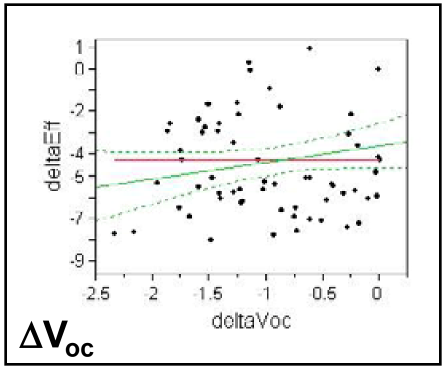
- V_{oc} more stable at 60-80°C; increased degradation at 100-120°C
- Little degradation observed in J_{sc}
- Overall % change in V_{oc} and J_{sc} small relative to FF change
- Changes in FF determine Δ%η

Degradation Activation Energy – Arrhenius-type study

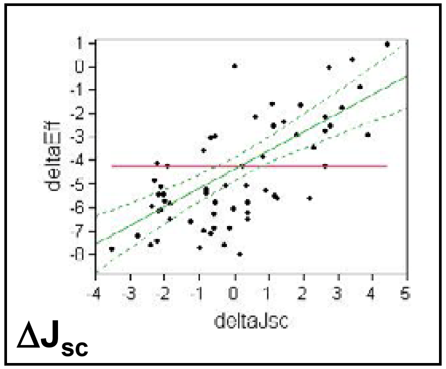


ΔEff vs

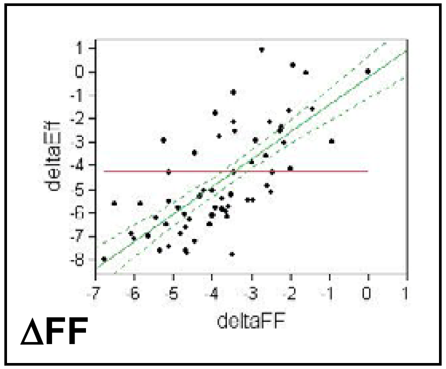
ΔV$_{oc}$, ΔJ$_{sc}$ and ΔFF



R^2 = 0.038

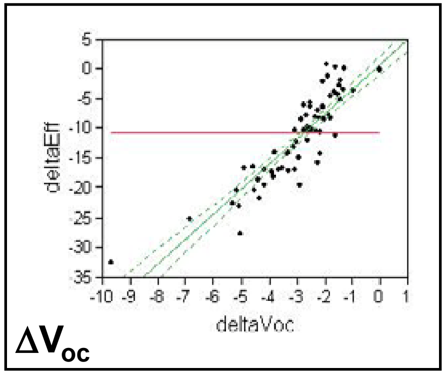


R^2 = 0.354

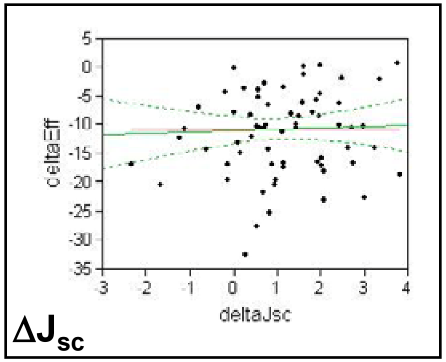


R^2 = 0.617

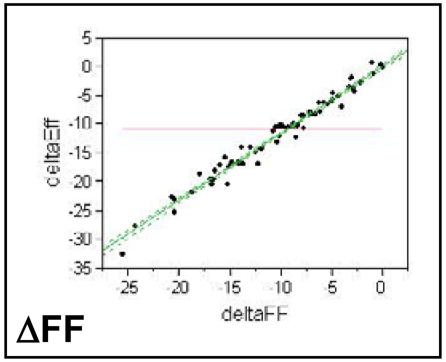
T = 60 ºC



R^2 = 0.781



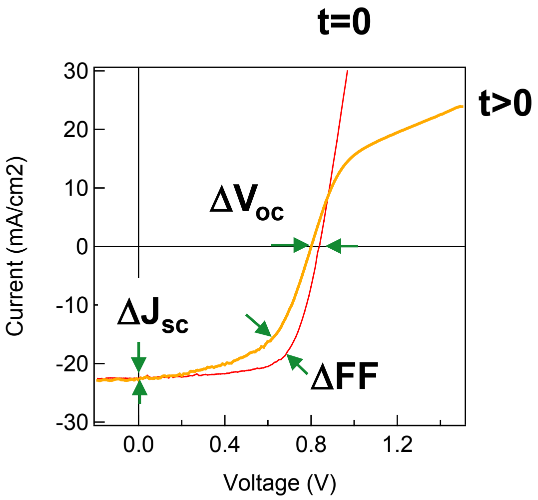
R^2 = 0.004

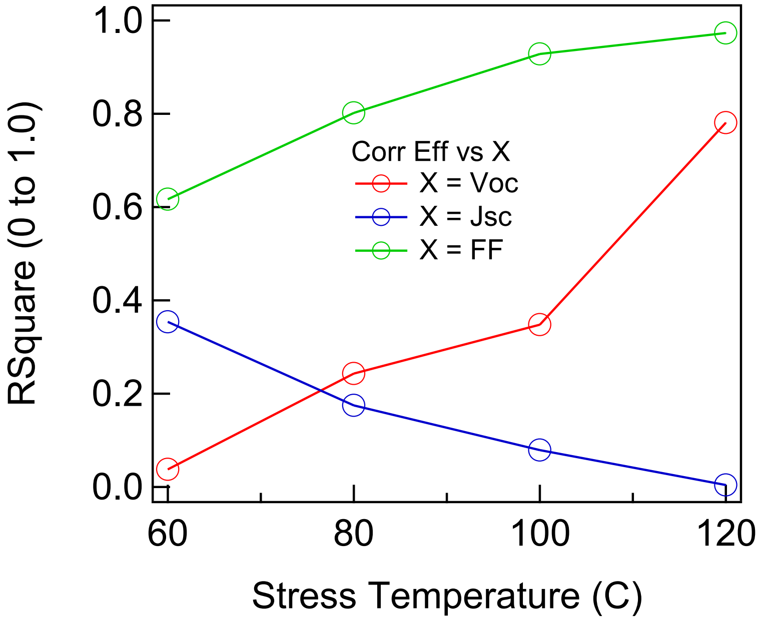


R^2 = 0.973

T = 120 ºC

Degradation Activation Energy – Arrhenius-type study



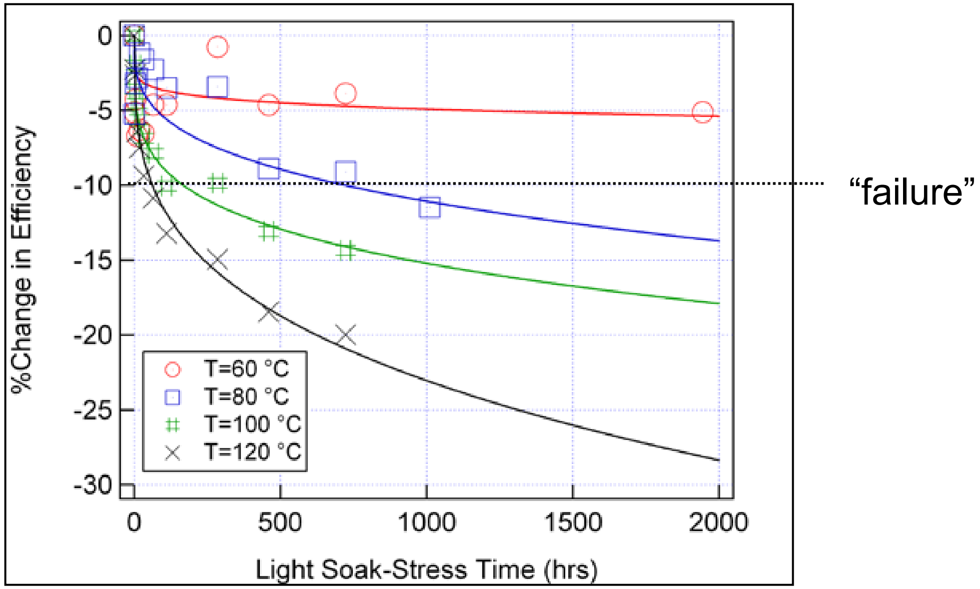


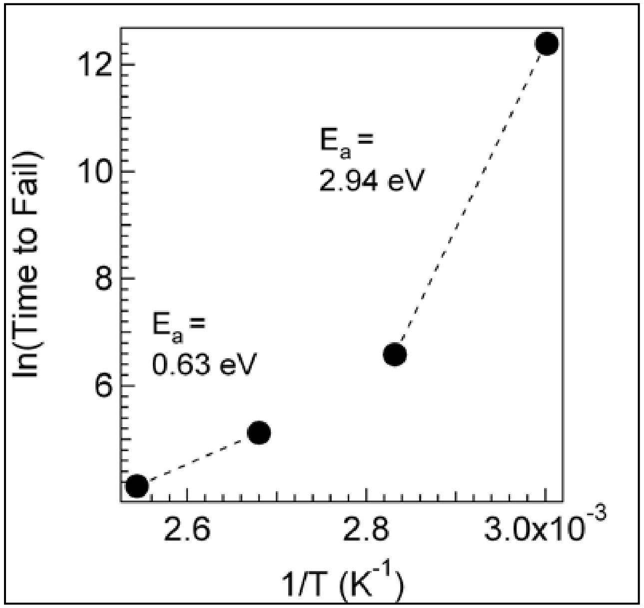
ΔEff vs

ΔV_{oc}, ΔJ_{sc} and ΔFF

- At all temperatures, changes in performance always correlate well with FF changes. This correlation (R^2) increases with increasing temperature.
- At lower stress temperatures, $\Delta\eta$% correlates with ΔJ_{sc}; at higher temperatures this is replaced by ΔV_{oc}
- *Understanding degradation requires an understanding of what affects FF.*

Degradation Activation Energy – Arrhenius-type study



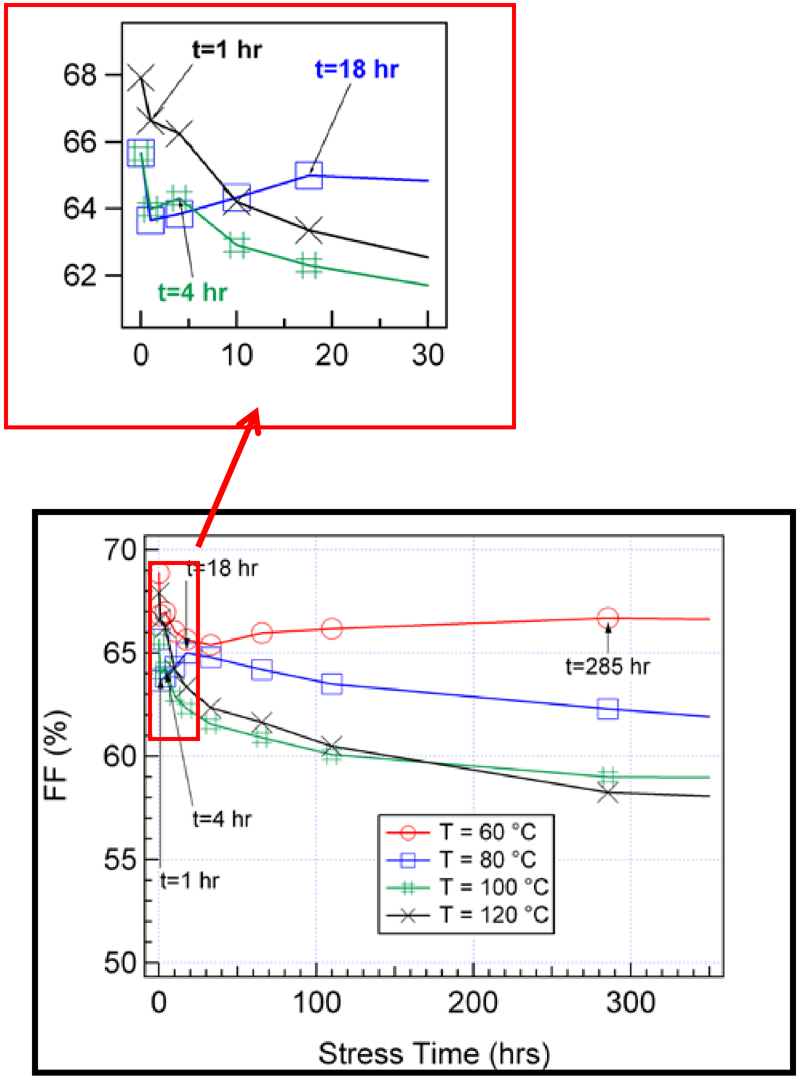


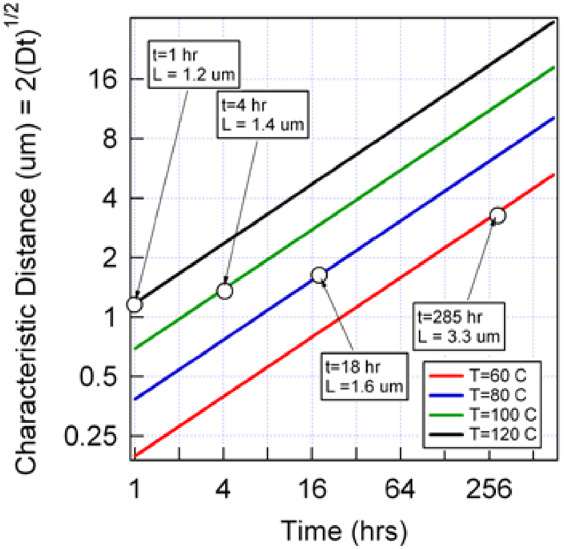
- Power-Law fit of monotonic data (longer times), $\Delta\eta\%=a \cdot t^{b}$
- Failure defined as a drop in η% of 10%

  - Arrhenius-plot of "Time to Fail" vs. inverse temperature
  - Higher temperatures dominated by E_a = 0.63 eV (Cu diffusion = 0.67 eV)
  - Lower temperatures involve higher E_a = 2.94 eV (S diffusion = 2.8 eV)

Degradation Activation Energy – Arrhenius-type study

Initial changes in FF associated with Cu diffusion





$$\frac{C(x,t)}{C_s} = erfc\left(\frac{x}{2\sqrt{Dt}}\right)$$

$$D = D_o e^{-(Ea/kT)}$$

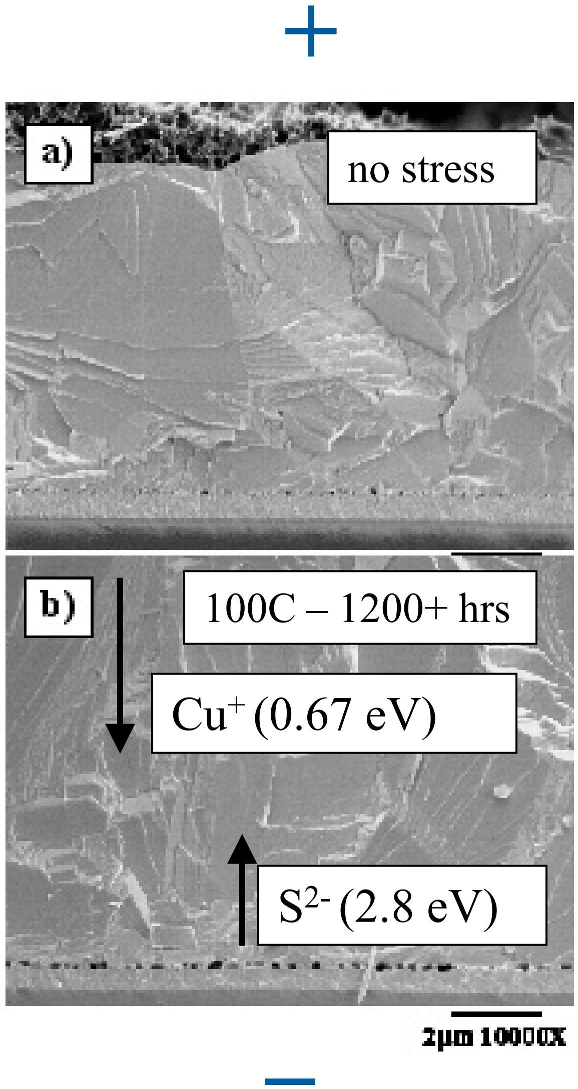
where
E_a = 0.67 eV
D_o = 3.7×10^{-4}

Woodbury and Aven, J.Appl.Phys (1968))

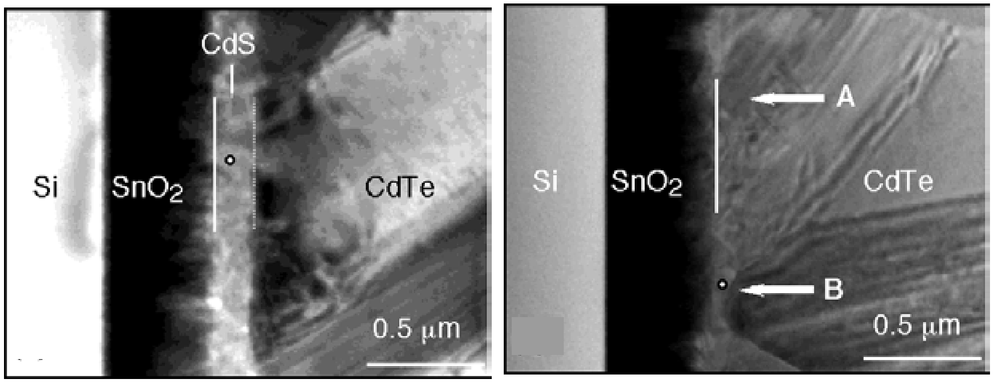
- FF changes in a non-monotonic fashion initially
- Temperature-Time changes explained by Cu diffusion
- At 80, 100, 120 °C, Cu diffusion from the backcontact into CdTe (~ 1-3 microns) increases FF beyond which further diffusion causes FF to decrease

Degradation Activation Energy – Arrhenius-type study

S-diffusion from CdS = 2.8 eV [1]



CdS consumed during growth[2]



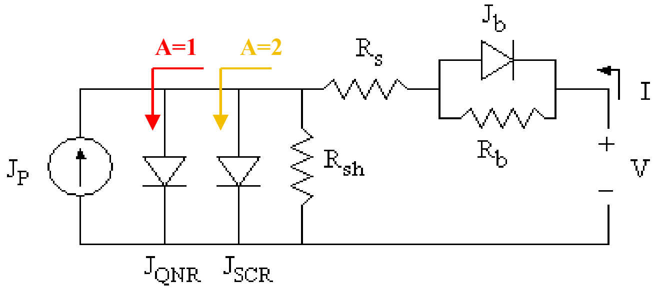
- High resolution x-sectional SEM shows formation of Kirkendall voids at the CdS interface after long stress times.
- S-diffusion > Te-diffusion at interface; at high temperatures (e.g. growth at + 600 ºC), CdS layer consumed
- At lower temperatures, less mass transport = voiding (Kirkendall voids)

[1] ***McCandless, et al., J. Appl. Phys. 89(2), 2001.***

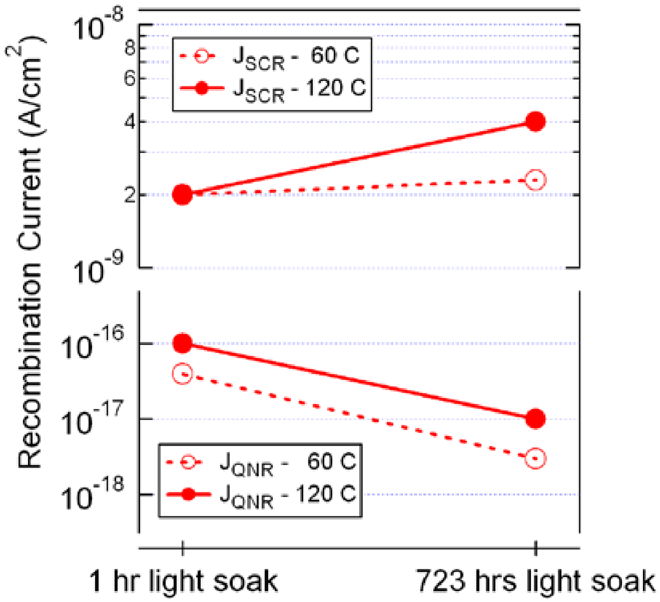
[2] ***Albin, et al., Prog. Photovolt: Res. Appl. 10, 2002.***

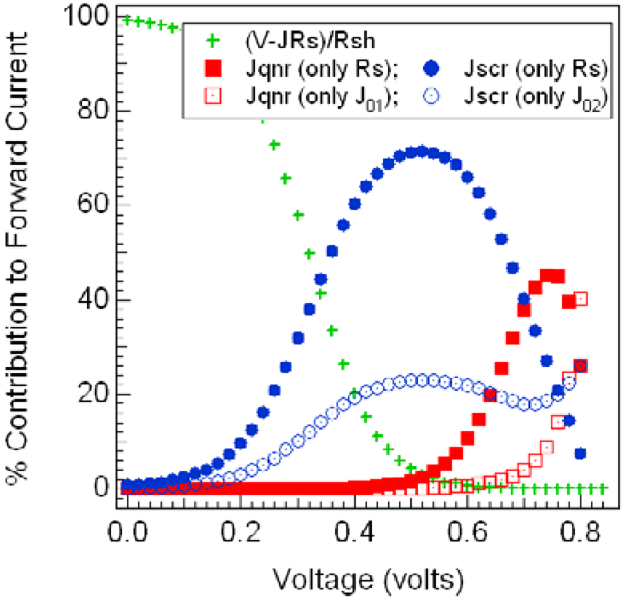
Degradation Activation Energy – Arrhenius-type study

Longer term stability degraded by increased J_{SCR}



$J_{SCR} \sim 10^{-9}$-10^{-8}, $J_{QNR} \sim 10^{-17}$-10^{-16} A/cm^2



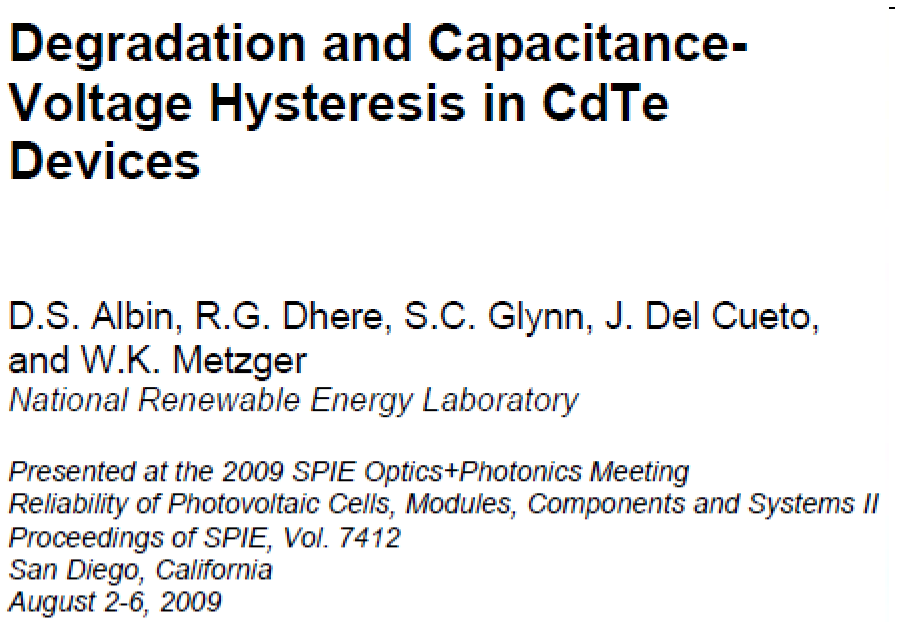


- Two-diode model considers both J_{QNR} and J_{SCR} and resistive terms
- Forward current consists almost entirely of J_{SCR} in the power quadrant, thus FF
- J_{QNR} makes contribution near V_{oc}.
- Increasing time, temperature increases J_{SCR}
- Decreasing J_{QNR} helps stabilize V_{oc} drop

Degradation Activation Energy – Arrhenius-type study

- Two different degradation mechanisms observed when stressing cells between 60 and 120 °C
- Extrapolation of monotonically-changing $\Delta\eta$% data yielded two activation energies:
  - Higher temperatures (100-120 °C); $E_a \sim 0.63$ eV→ Cu diffusion
    - FF and V_{oc} decrease (increased J_{SCR})
  - Lower temperatures (60-80 °C); $E_a \sim 2.94$ eV→ S diffusion
    - FF decrease; less V_{oc} drop (decreased J_{QNR})
    - Kirkendall voids in CdS

Transient Capacitance Observations

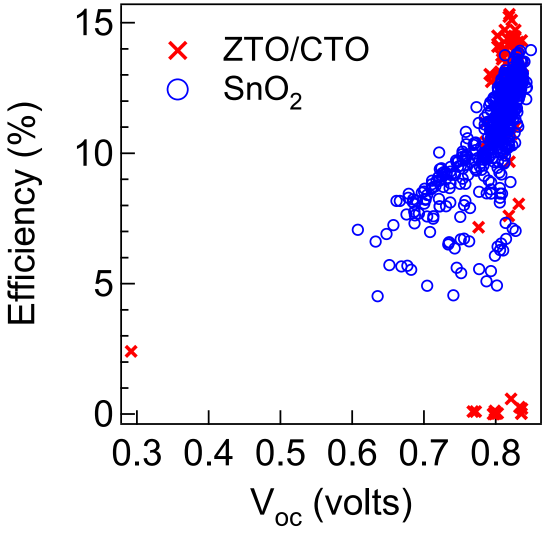


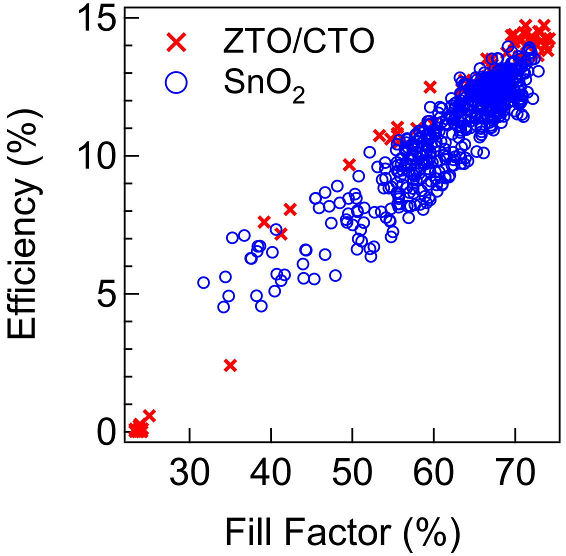
Degradation and Capacitance-Voltage Hysteresis in CdTe Devices

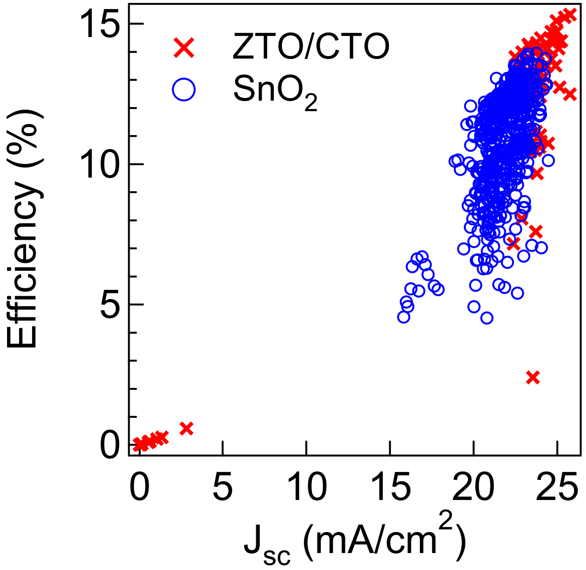
D.S. Albin, R.G. Dhere, S.C. Glynn, J. Del Cueto, and W.K. Metzger
National Renewable Energy Laboratory

Presented at the 2009 SPIE Optics+Photonics Meeting
Reliability of Photovoltaic Cells, Modules, Components and Systems II
Proceedings of SPIE, Vol. 7412
San Diego, California
August 2-6, 2009

Study Compared two different transparent conducting oxides (TCOs)







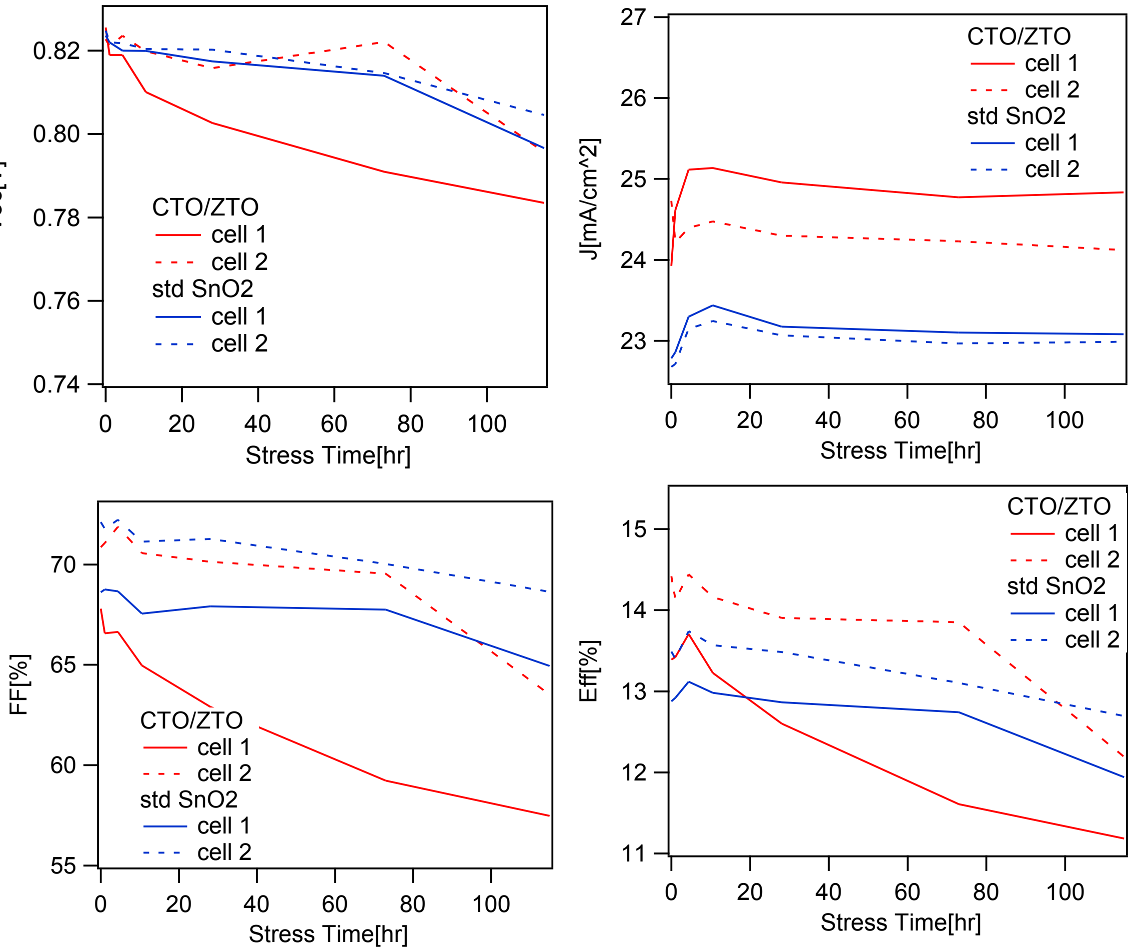
Benefits of CTO/ZTO vs. SnO$_2$ TCO layers

no difference in V$_{oc}$

FF increases 1-2 % pts

J$_{sc}$ increase of 1-1.5 mA/cm^2

More Degradation observed in “advanced” TCOs



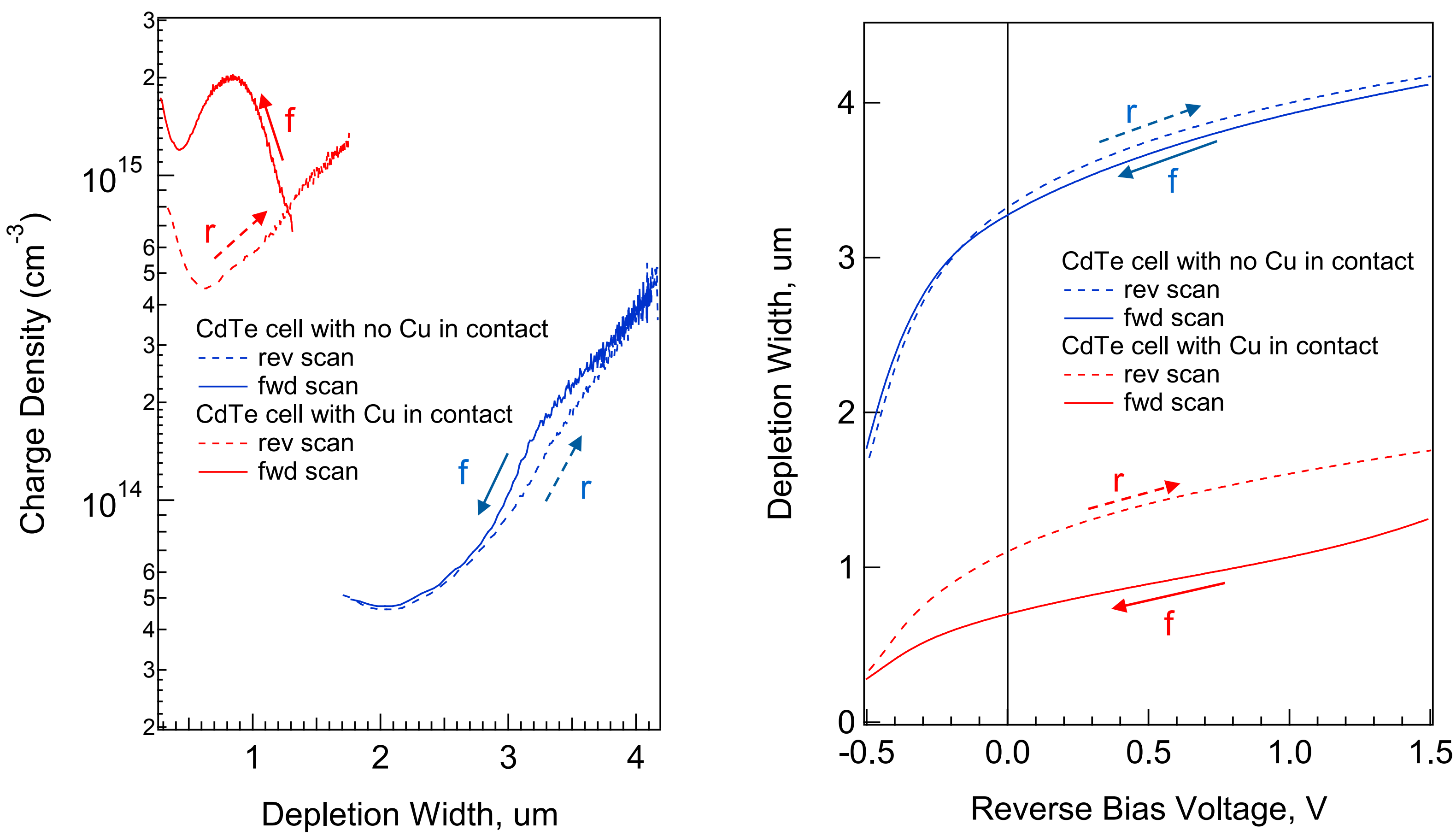
Cells fabricated identically except for TCO

(Cu,Hg) doped BC	(Cu,Hg) doped BC
CdTe	CdTe
CdS	CdS
$Zn_2Sn_2O_4$	**i-SnO_2**
Cd_2SnO_4	**n-SnO_2**
glass	glass

Light-soaked (stressed) at 100 ºC identically

Differences in degradation due to different TCO layers

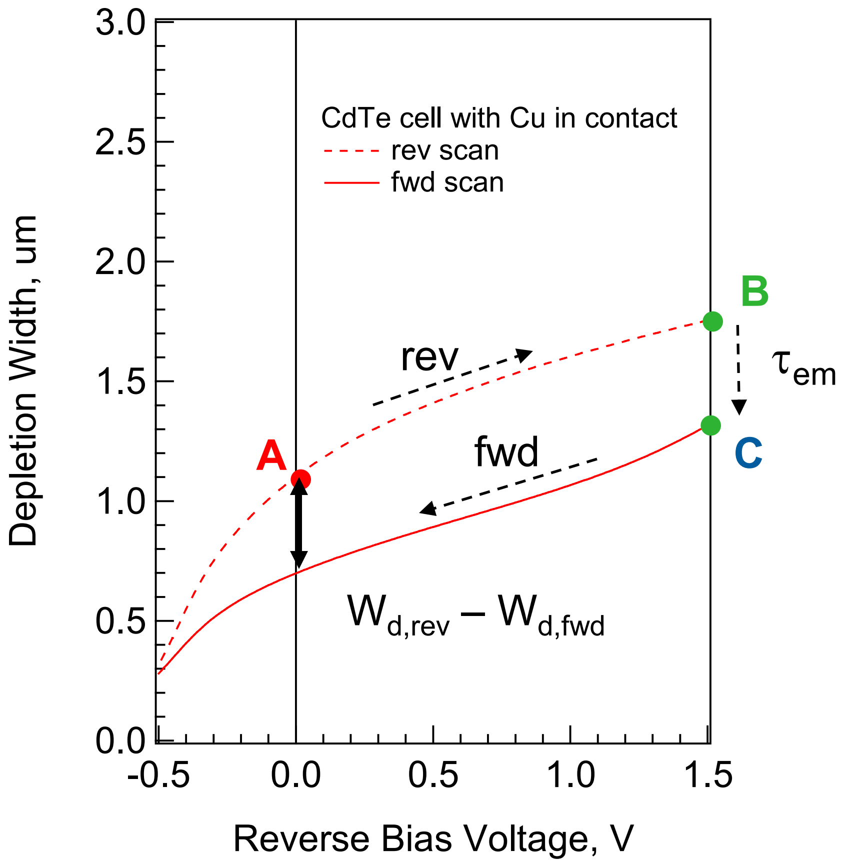
C-V hysteresis (metastability) during ALT

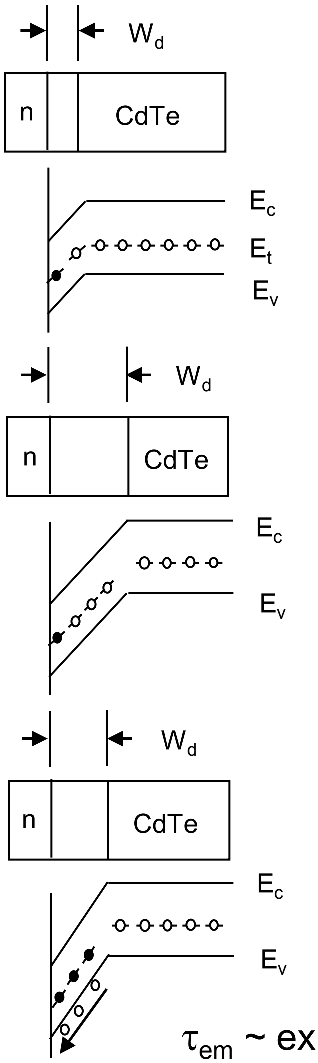


“rev scan” → +0.5 V to -1.5 V

“fwd scan” → -1.5 V to +0.5 V

C-V hysteresis (electronic processes) during ALT





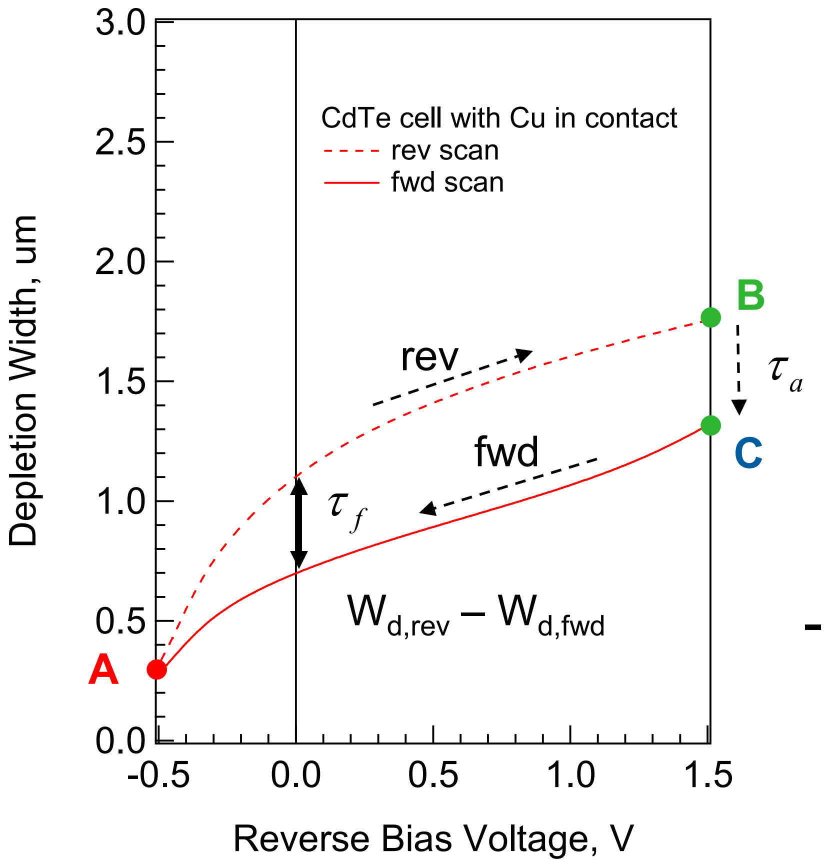
A v = 0

B v = -1.5 V; t = 0$^+$

C v = -1.5 V; t >0

$\tau_{em} \sim \exp(E_t - E_v)/kT$

C-V hysteresis (ionic processes) during ALT



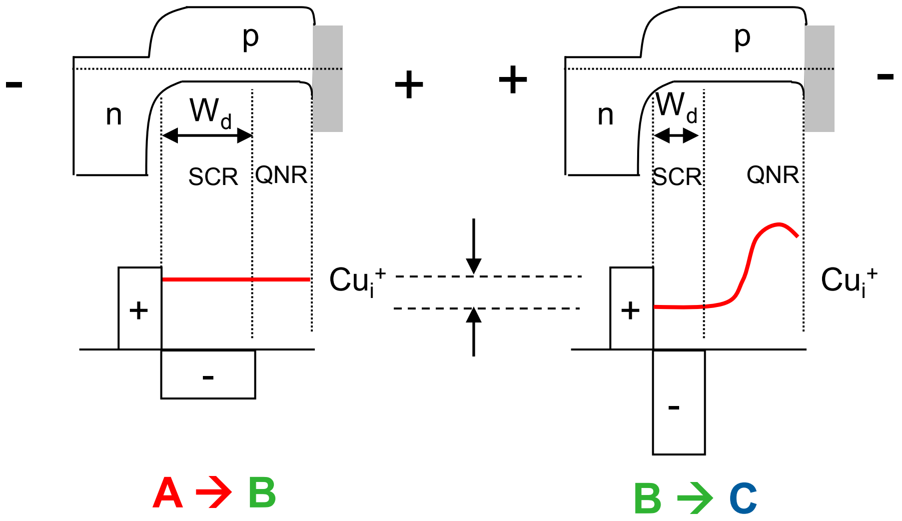
Perform “rev” scan

- *Measure SCR with Cu_i^+ screening N_a^-*

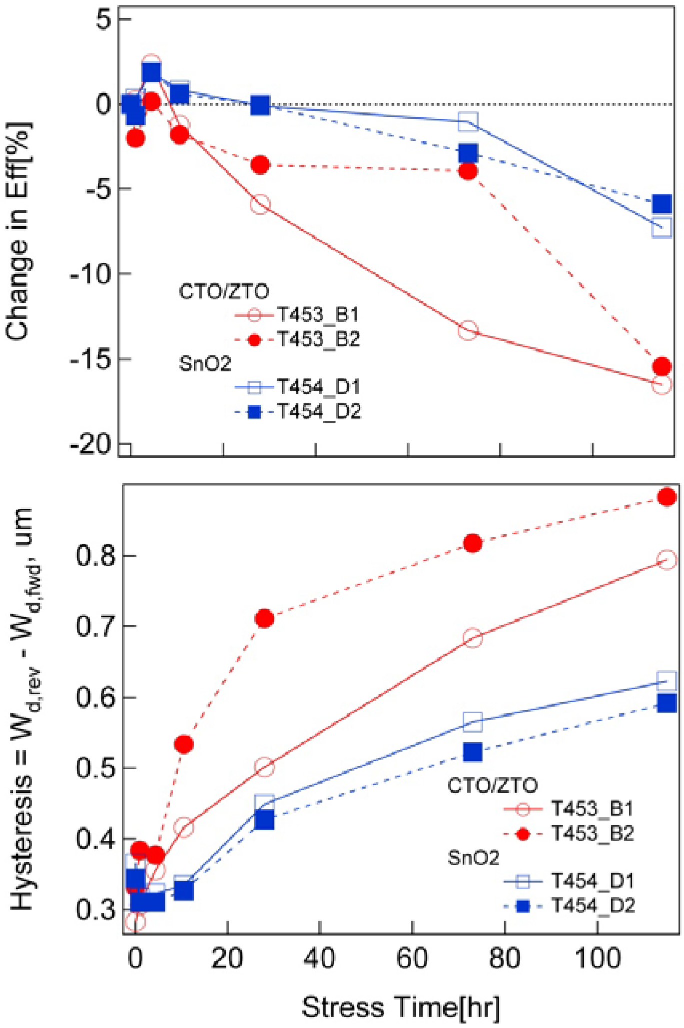
Hold cell at rev-bias for 5m (τ_a)

Perform “fwd” scan

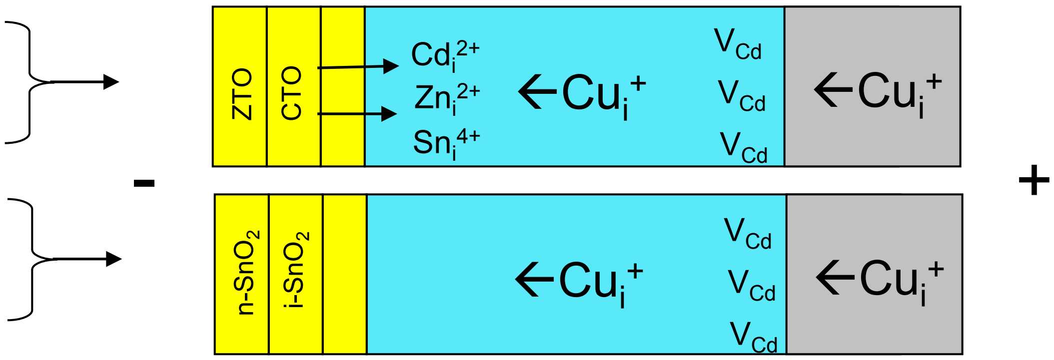
- *Measure SCR with Cu_i^+ removed from SCR*



CV-hysteresis correlates with performance during stress test

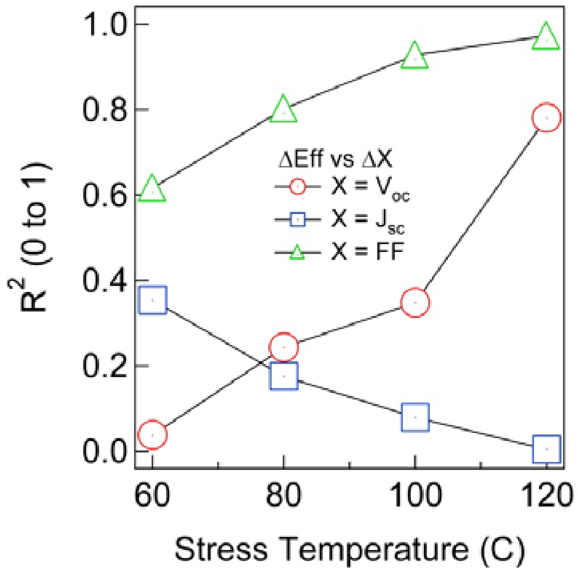


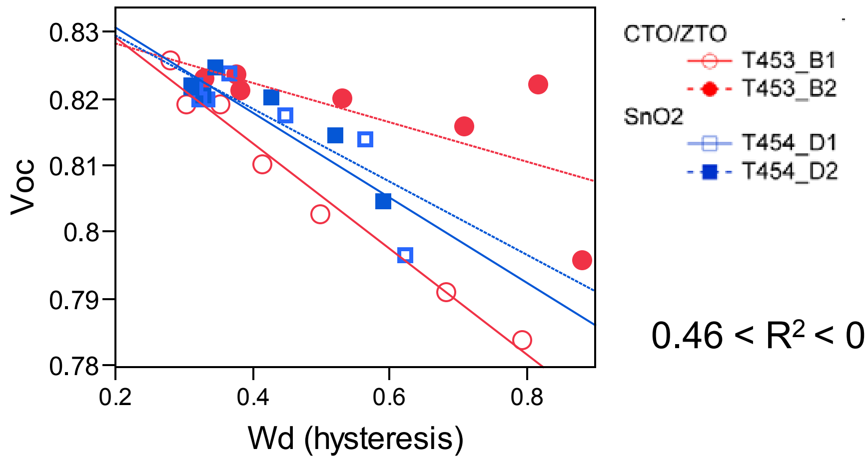
- CdTe cells grown on CTO/ZTO transparent conducting oxides *degrade faster*
- C-V hysteresis increases monotonically with degradation
- For all cells, increasing hysteresis partly due to continuous diffusion of Cu from the back contact.



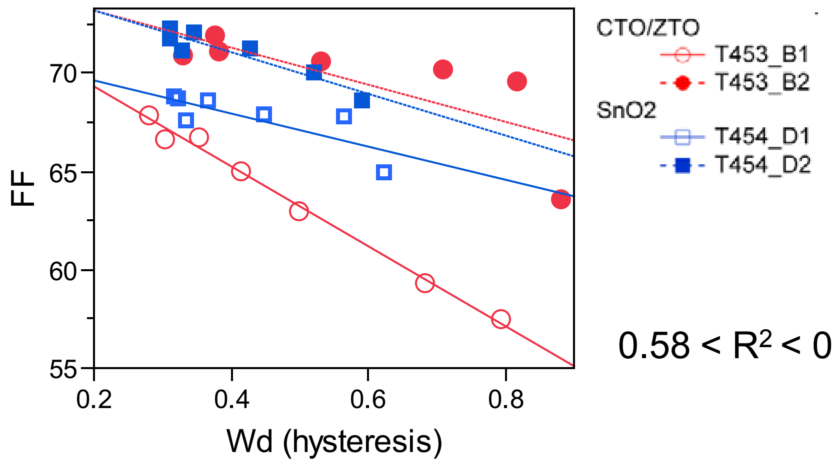
- Additional hysteresis indicative of “decomposition” of the CTO/ZTO layers

CV-hysteresis correlates with performance during stress test





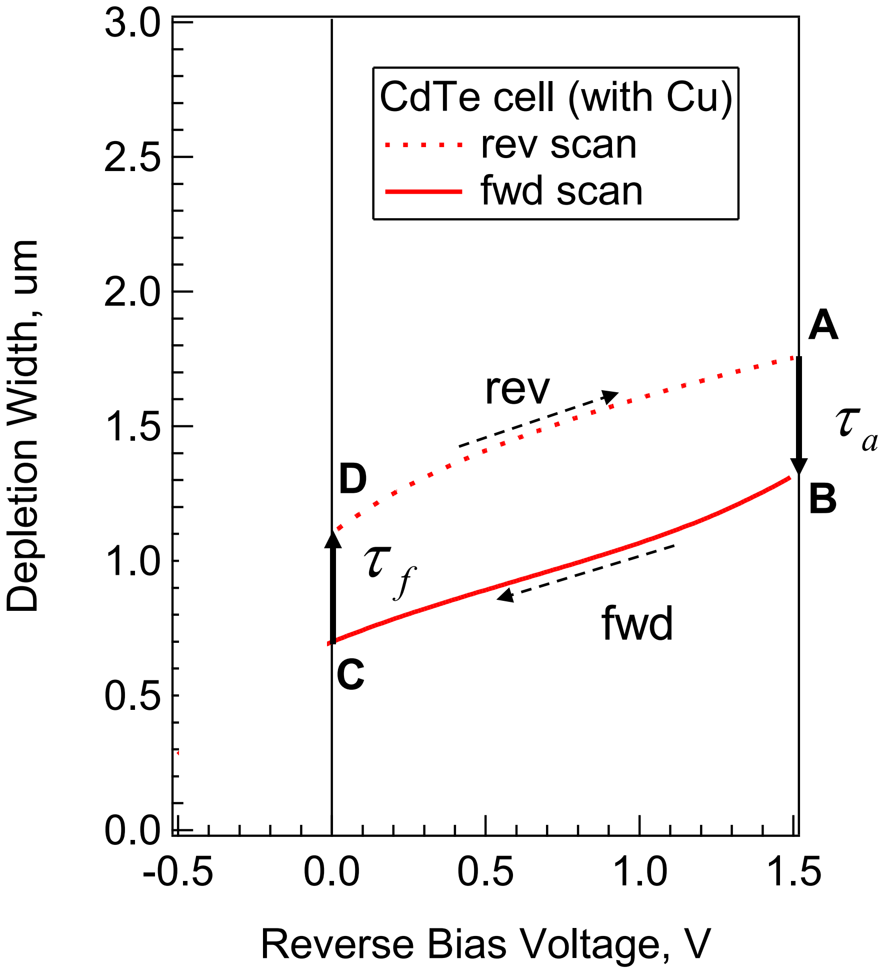
$0.46 < R^2 < 0.98$

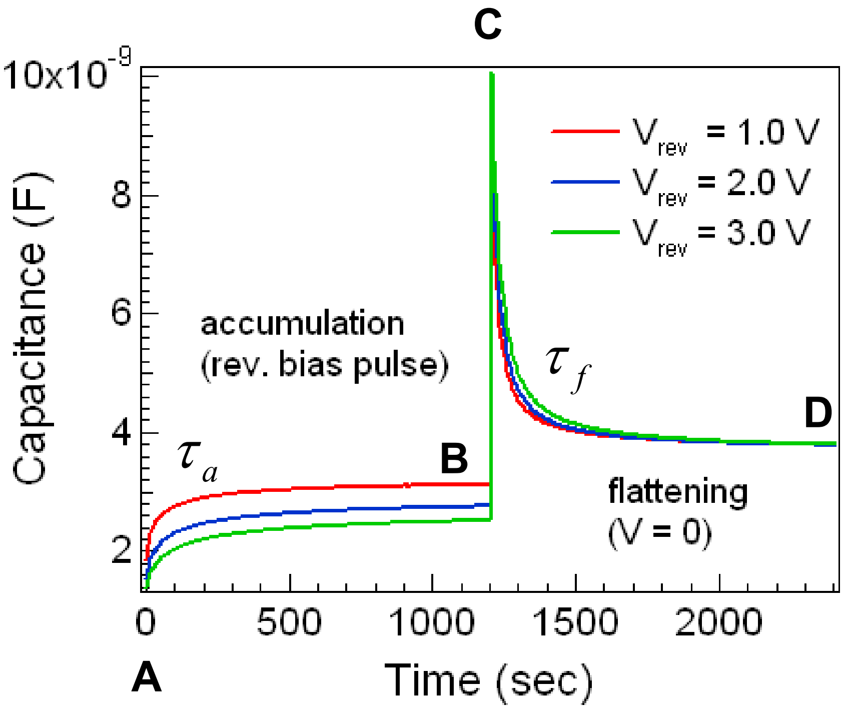


$0.58 < R^2 < 0.99$

- At 100 °C; cell stability is determined by changes in FF and V_{oc} (SPIE-2008)

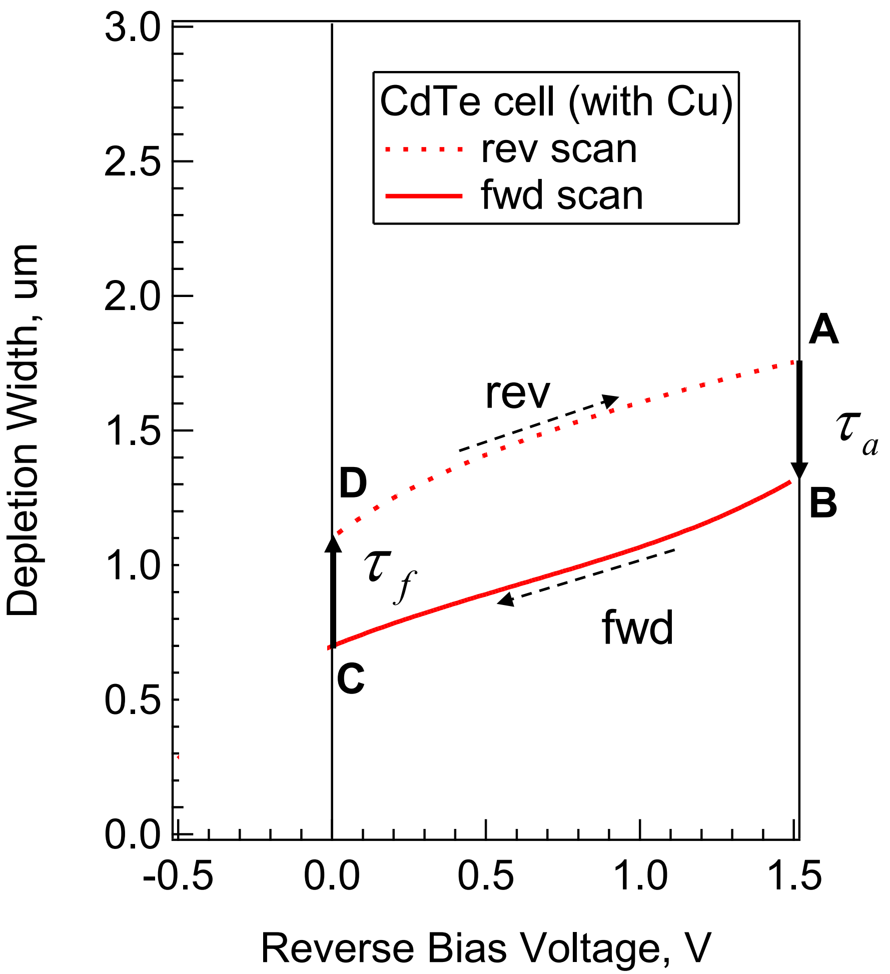
CV hysteresis (ionic or electronic ?)

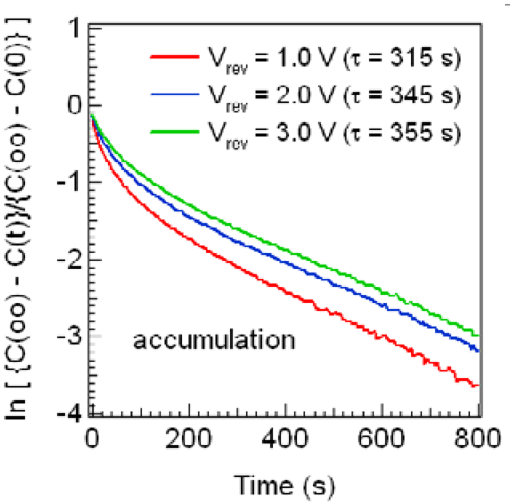


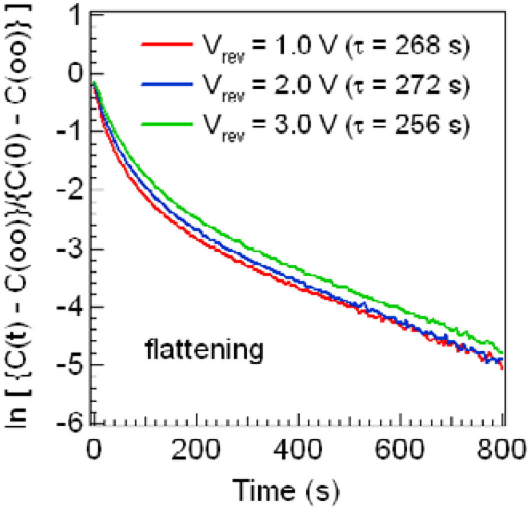


TID requirements: (1) $\tau_f / \tau_a \approx qV_{rev} / kT > 1$ (2) $\tau_a \approx \dfrac{w^2 kT}{qDV_{rev}}$

CV hysteresis (appears to be electronic)



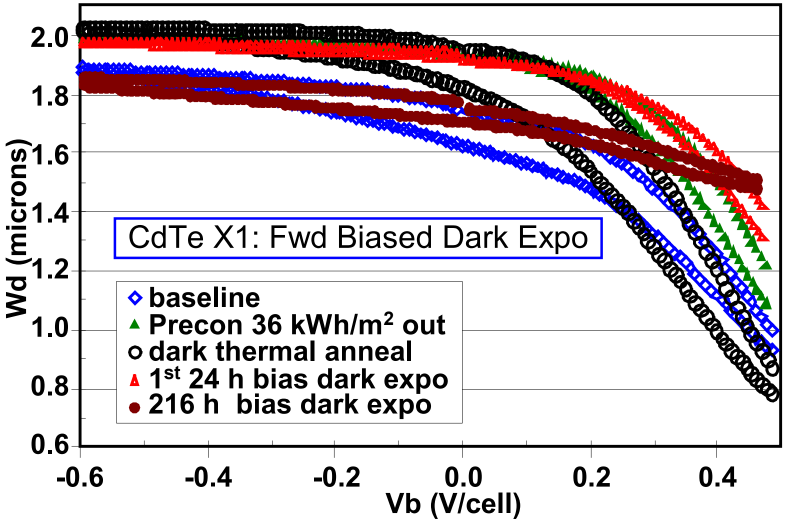




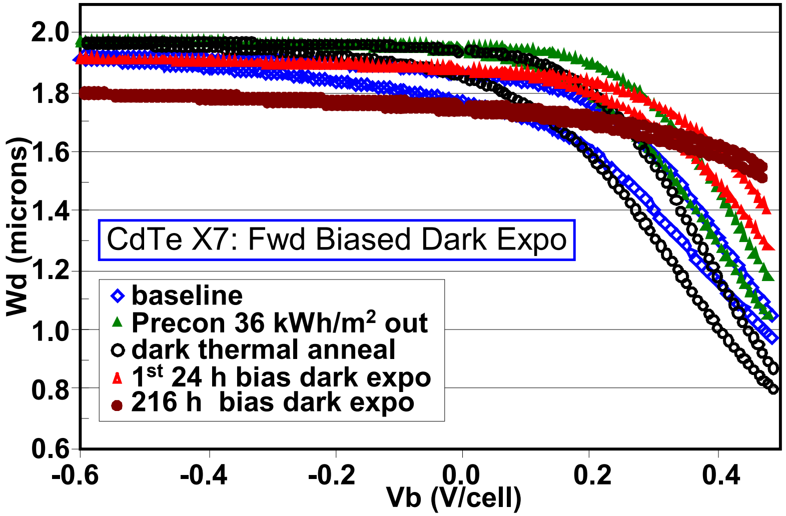
TID requirements: (1) $\tau_f/\tau_a \approx 0.85 \rightarrow 0.72 \not> 1$ (2) $\tau_a \not\approx \dfrac{w^2 kT}{qDV_{rev}}$

C-V hysteresis in industrial CdTe cells and mini-modules

~8.3% degradation



~1.0 % degradation



Special Thanks

- Of course, my thanks to the Dept. of Energy, Midwest Research, the Alliance, and NREL for supporting this work

- Past students, graduate students, and post-docs
  Tracie Berniard (now at 3M)
  Samuel Demtsu (now at Primestar Solar)
  Yoxa Mahathongdy

- NREL staff
  Joe del Cueto, Peter Hacke and Sarah Kurtz (Module Reliability Group)
  Tom McMahon (retired)
  Ramesh Dhere (fellow thin film device grower)
  Steve Glynn, Clay DeHart (processing and equipment support)
  Wyatt Metzger (ongoing discussions of all things concerning cell physics)
  Jian Li (C-V and Admittance Spectroscopy)
  Raji Sundaramoorthy (CIGS thermal and EL imaging)
  Tim Gessert (Thin Film Group Manager)
  Harin Ullal, Sarah Kurtz (the big picture – i.e., the market)

- **Special Thanks to the Following:**
  Victor Karpov (U. of Toledo)
  Diana Shvydka (U. of Toledo)
  Fred Seymour (Primestar Solar)
  Jim Sites (Colorado State University)
  Tim Ohno, Victor Kaydanov (Colorado School of Mines)
  Glenn Alers (U. of California)
  Scott Feldman (Primestar Solar)
  Ken Zweibel

Have a safe trip home!