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Oxygen Incorporation During Fabrication of Substrate CdTe Photovoltaic Devices

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***Abstract* — Recently, CdTe photovoltaic (PV) devices fabricated in the nonstandard substrate configuration have attracted increasing interest because of their potential compatibility with flexible substrates such as metal foils and polymer films. This compatibility could lead to the suitability of CdTe for roll-to-roll processing and building-integrated PV. Currently, however, the efficiencies of substrate CdTe devices reported in the literature are significantly lower (~6%-8%) than those of high-performance superstrate devices (~17%) because of significantly lower open-circuit voltage (V_{oc}) and fill factor (FF). In our recent device development efforts, we have found that processing parameters required to fabricate high-efficiency substrate CdTe PV devices differ from those necessary for traditional superstrate CdTe devices. Here, we investigate how oxygen incorporation in the CdTe deposition, $CdCl_2$ heat treatment, CdS deposition, and post-deposition heat treatment affect device characteristics through their effects on the junction. By adjusting whether oxygen is incorporated during these processing steps, we have achieved V_{oc} values greater than 860 mV and efficiencies greater than 10%.**

***Index Terms* — photovoltaic cells, cadmium compounds, current-voltage characteristics, heterojunctions, II-VI semiconductor materials, solar energy, thin film devices.**

I. Introduction

The majority of CdTe thin-film PV research and development has been conducted on CdTe devices and modules fabricated in the superstrate configuration. All CdTe modules in commercial production currently are constructed in this configuration. In the superstrate configuration, light enters the device through a transparent material, typically glass, that is used both to support the thin-film layers during deposition and to provide a transparent front seal during deployment. Advantages of the superstrate design include that the back surface of the CdTe is easily accessed for the challenging task of forming a suitable ohmic back contact. Recently, however, CdTe PV devices fabricated in the nonstandard substrate configuration have attracted increasing interest. In the substrate design, the thin-film layers are deposited onto materials that may be opaque, including metal foils, high-temperature polymers, or ceramics. Because of the potential compatibility of the substrate design with flexible substrates, product advantages likely exist for substrate-configured CdTe modules in aerospace (high power/mass) and building-integrated PV. The substrate design may also enable low-cost production designs such as roll-to-roll processing. In addition to the manufacturing and deployment benefits, optical losses can be reduced further in substrate CdTe devices than in traditional superstrate devices because the light is incident directly on the film stack, rather than through a superstrate, potentially leading to higher short-circuit current. Currently, however, the efficiencies of substrate CdTe devices reported in the literature are significantly lower (~6%-8%) [1-3] than those of high-performance superstrate devices (~17%) [4] because of significantly lower V_{oc} and FF. In this work, we investigate how O_2 incorporation in the CdTe deposition, $CdCl_2$ heat treatment, CdS deposition, and post-deposition heat treatment affects device characteristics though effects on the junction. By adjusting the amount of O_2 incorporated during these processing steps, we have achieved V_{oc} values greater than 860 mV and device efficiencies exceeding 10%.

II. Experimental Details

Substrate CdTe devices used in this study were fabricated in the following manner (Fig. 1). Substrates were prepared by depositing a thin layer (~10 nm) of Cr and 800 nm of Mo by direct-current sputtering onto cleaned Corning 7059 glass of 0.8 mm thickness. Next, a Cu-containing back contact interface layer was deposited by radio-frequency (RF) magnetron sputtering. In initial work, a Cu-doped ZnTe back contact interface layer was used. In later work, 10 nm of Cu_xTe was used. CdTe films were deposited by close-spaced sublimation (CSS) from a CdTe source plate [5] to a thickness of ~5-8 μm at a substrate temperature of 450°C. The O_2-free ambient used in this study for the CdTe deposition was 16 torr of He. Following the CdTe deposition, a $CdCl_2$ vapor heat treatment was performed at 400°C by CSS. The O_2-free

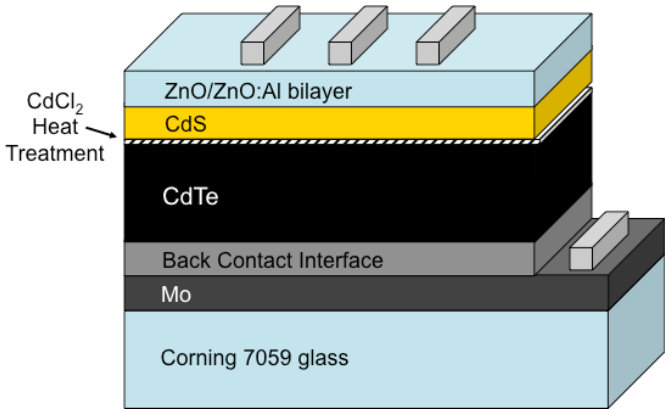

Fig. 1. Structure of the substrate CdTe devices used in this study.

ambient used was 400 torr of He. The O_2-containing ambient used was 80 torr of O_2 plus 320 torr of He. The CdS layer, 125 nm thick, was deposited by RF magnetron sputtering. O_2 was introduced into the sputtering ambient in the range from 0 to 5 vol.% in our early studies. The 2 vol.% O_2 amount was used in this study in the comparison between O_2-containing and O_2-free CdS deposition ambients. The front contact consisted of a bilayer of 100 nm of intrinsic ZnO and 120 nm of Al-doped ZnO (from a target containing 2 wt.% Al_2O_3 in ZnO) deposited by RF magnetron sputtering. A grid consisting of 50 nm Ni and 3 μm Al deposited by electron beam evaporation completed the devices. A post-CdS (or post-contact) anneal was performed at temperatures of 175° to 300°C for 30 min. to compare O_2-free (100 sccm He) and O_2-containing (20 sccm O_2 plus 80 sccm He) ambients. Initial characterization of the devices was performed using current-density voltage (JV) and quantum efficiency (QE) measurements. Further characterization is ongoing, including capacitance-voltage, Auger electron spectroscopy, time-resolved photoluminescence (PL), low-temperature PL, admittance spectroscopy, and temperature-dependent JV measurements.

III. Results and Discussion

Recent substrate CdTe work at NREL was begun using processing parameters similar to those typically used for superstrate device fabrication. For example, in our typical superstrate CdTe device fabrication procedure, the CdTe layer is deposited by CSS in an ambient that contains 1 torr O_2 and 15 torr He. Initial efforts utilizing this approach with a Cu-containing back contact (Cu-doped ZnTe), however, led to poor results. Furthermore, it was discovered that any O_2 exposure of the CdTe source used for substrate CdTe fabrication was detrimental to device performance. Though this comparison (Fig. 2) between substrate CdTe PV devices grown with O_2-exposed and O_2-free CdTe sources was performed before our processing technique was fully developed, results indicate that an O_2-free CdTe source produces substrate CdTe PV devices of higher efficiency than a CdTe source previously exposed to O_2. This was primarily because of differences in short-circuit current (J_{sc}) and FF. Oxidation of the Cu-doped ZnTe back contact interface layer is suspected to have contributed to this poor performance. Subsequent CdTe depositions have been performed in an O_2-free environment.

Later, a critical component of the substrate CdTe device fabrication procedure was discovered. It was found that a medium-temperature (175° to 300°C) post-CdS heat treatment significantly improved device performance. This heat treatment was initially performed in an O_2-free environment. The effect of O_2 incorporation in the heat treatment ambient was investigated in this study and is described below. The post-CdS heat treatment yields a significant improvement in V_{oc}, J_{sc}, FF, and efficiency (Fig. 3). As a result of the heat treatment, V_{oc} increases from values typically ≤700 mV to values commonly exceeding 800 mV. Our maximum V_{oc} value obtained to date is 863 mV. FF typically increases from ≤30% to values exceeding 60% in some cases.

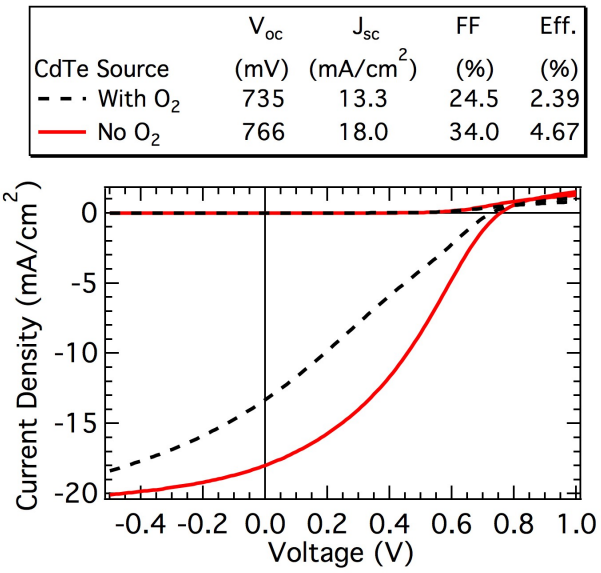

Fig. 2. Dotted line: JV curve for a substrate CdTe PV device deposited using a CdTe source that had previously been exposed to O_2, though the ambient during the CdTe deposition used in fabricating this PV device was O_2-free. Solid line: JV curve for a device in which no O_2 exposure occurred in the CdTe deposition step.

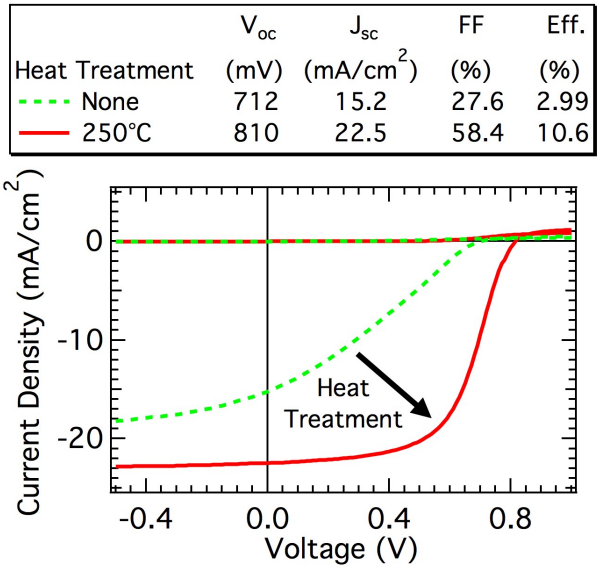

Fig. 3. Dotted line: JV curve of a substrate CdTe PV device before the post-CdS heat treatment was performed. Solid line: JV curve of the same device after the post-CdS heat treatment. This device was fabricated with O_2 absent from the CdTe deposition but present in the $CdCl_2$ heat treatment and CdS deposition processing.

This significant discovery opened doors to further investigation, including study of the effects of O_2 in other processing steps. Initial indications in our previous studies had suggested that the presence or absence of O_2 during the $CdCl_2$ vapor heat treatment and CdS sputter deposition processing could have significant effects on device performance. Here, we systematically study these effects and the effect of O_2 in the post-CdS heat treatment ambient.

In examining the effects of O_2 incorporation in substrate CdTe PV device-processing steps (Fig. 4, top panel), we first observe that when O_2 is incorporated into neither the $CdCl_2$ heat treatment ambient nor the CdS sputtering ambient, device performance is poor. V_{oc} values are abysmal, in the 300 mV range, J_{sc} values are in the single digits, and FF values are ~30%. The presence or absence of O_2 in the post-CdS anneal ambient plays no significant role in this case. Incorporating O_2 into the $CdCl_2$ heat treatment ambient but not into the CdS deposition ambient yields a slight improvement in device performance, though efficiencies remain less than 2%. J_{sc} increases with the addition of O_2 to the post-CdS anneal ambient, but the value remains low. The incorporation of O_2 into the CdS sputter deposition ambient, forming CdS:O [6], proved most significant in improving device performance. By incorporating O_2 into both the $CdCl_2$ heat treatment ambient and the CdS deposition, V_{oc} values improve to greater than 800 mV, J_{sc} reaches reasonable values, and FF exceeds 50%. A slight difference in J_{sc} is observed between the samples processed with and without 20 vol.% O_2 in the post-CdS anneal ambient, though this is a much smaller effect than that observed for the incorporation of O_2 during the CdS film deposition.

QE data were collected for the same PV devices (Fig. 4, bottom panel). Uniform differences in QE across the wavelength range are observed between the samples with and without O_2 incorporated in the $CdCl_2$ and CdS processing steps. The uniformly poorer collection in the depletion region in the samples without O_2 incorporation indicates a weaker electric field in these devices. The greater J_{sc} for the devices with O_2 incorporated into the CdS deposition step is not solely a result of improved transparency in the sub-517-nm range where CdS absorbs.

Effects of O_2 incorporation were further investigated as a function of the post-CdS heat treatment temperature (Fig. 5). Again, the best performance was observed for devices in which O_2 had been incorporated into both the $CdCl_2$ and CdS processing steps. At higher post-CdS annealing temperatures (275° to 300°C), results were similar for the devices in which O_2 was absent from the $CdCl_2$ heat treatment processing. At lower post-CdS annealing temperatures, however, the FF limited the performance of the devices without O_2 in the $CdCl_2$ processing. Including O_2 in both processes enables higher device performance when lower post-CdS heat treatment temperatures are used. The broader acceptable post-CdS heat treatment temperature range enabled by incorporation of O_2 into the $CdCl_2$ heat treatment processing may have production advantages.

Substrate CdTe O_2 Series				V_{oc}	J_{sc}	FF	Eff.
O_2 in	$CdCl_2$	CdS	Anneal	(mV)	(mA/cm^2)	(%)	(%)
-	-	-	O_2	338	2.12	30.4	0.22
-	-	-	-	324	4.75	31.1	0.48
O_2	-	O_2		405	13.1	27.1	1.44
O_2	-	-		541	5.75	23.5	0.73
O_2	O_2	O_2		811	19.2	50.9	7.93
O_2	O_2	-		808	20.2	50.2	8.17

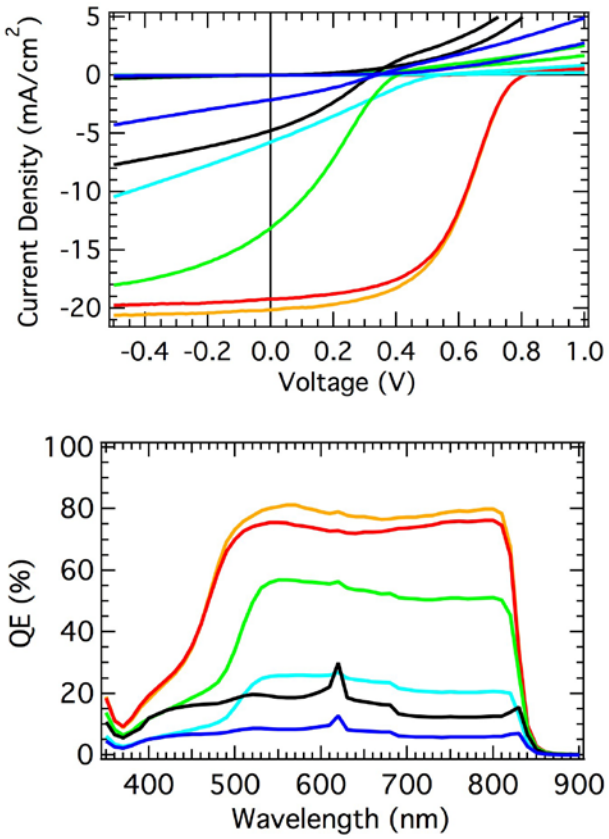

Fig. 4. Top panel: JV curves for substrate CdTe PV devices deposited with a 10-nm Cu_xTe back contact interface layer and no O_2 exposure during the CdTe deposition. The post-CdS anneal was performed at 250°C. The devices grown without O_2 exposure in either $CdCl_2$ or CdS show the poorest performance. Devices with O_2 exposure during the $CdCl_2$ heat treatment, but not during the CdS deposition, have intermediate performance. Those with O_2 incorporated into both the CdS deposition and $CdCl_2$ heat treatment ambients have the highest performance. O_2 incorporation in the post-CdS annealing ambient has a relatively small effect compared to O_2 incorporation in the other steps. Bottom panel: QE spectra for the same PV devices. Note that the addition of O_2 to CdS affects the spectra across the wavelength range, not only in the sub-517-nm range limited by CdS.

We also investigated the effects of the amount of O_2 incorporated into the CdS RF magnetron sputtering ambient (Fig. 6). Incorporation of 2-4 vol.% O_2 in Ar led to the highest V_{oc} values and device efficiency (not shown). These amounts of O_2 are comparable to the amounts required for high performance in superstrate CdTe devices.

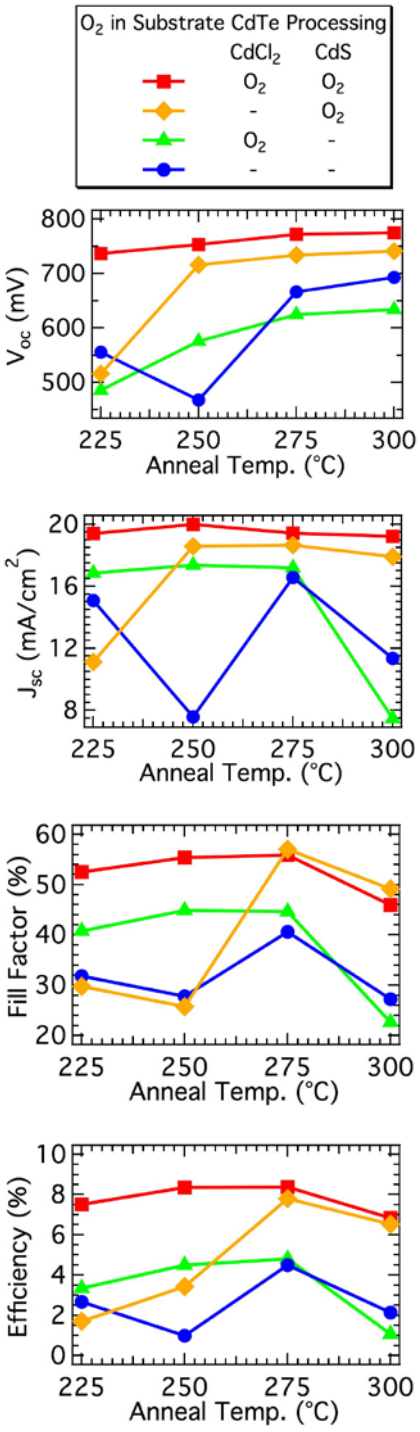

Fig. 5. Effects of O_2 incorporation during $CdCl_2$ heat treatment and CdS deposition processing on device characteristics as a function of the post-CdS heat treatment temperature.

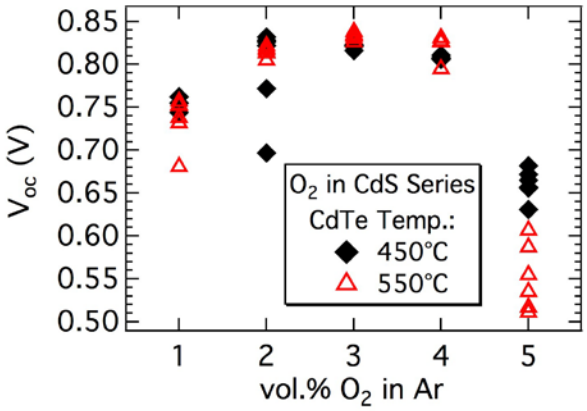

Fig. 6. V_{oc} as a function of the vol.% of O_2 incorporated in the CdS RF sputter deposition ambient. The CdTe films were deposited in an O_2-free ambient followed by a $CdCl_2$ heat treatment in an O_2-containing ambient.

VI. Conclusions

We have conducted a preliminary investigation of the effects of O_2 incorporation in the CdTe deposition, $CdCl_2$ heat treatment, CdS deposition, and post-CdS heat treatment steps in the fabrication of CdTe PV devices grown in the nonstandard substrate configuration. We found that elimination of O_2 from the CdTe deposition is beneficial, likely because it prevents oxidation of the Cu-containing back contact interface layer. When O_2 is not incorporated into the CdTe layer, it is important to incorporate oxygen at the CdS/CdTe interface by other means. The greatest benefit to device performance occurs when O_2 is incorporated both into the $CdCl_2$ heat treatment and the subsequent CdS film deposition. The presence or absence of O_2 in the post-CdS heat treatment step shows only a minor effect.

In future work, we will characterize the devices in greater detail, including investigations of the chemical composition of the junction region, minority carrier lifetime, and transport mechanisms. We will also examine defect levels present in the material at each step of device growth using PL techniques.

Acknowledgement

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