Design of Epitaxial CdTe Solar Cells on InSb Substrates

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***Abstract*—Epitaxial CdTe has been shown by others to have a radiative recombination rate approaching unity, high carrier concentration, and low defect density. It has, therefore, become an attractive candidate for high-efficiency solar cells, perhaps becoming competitive with GaAs. The choice of substrate is a key design feature for epitaxial CdTe solar cells, and several possibilities (CdTe, Si, GaAs, and InSb) have been investigated by others. All have challenges, and these have generally been addressed through the addition of intermediate layers between the substrate and CdTe absorber. InSb is an attractive substrate choice for CdTe devices, because it has a close lattice match with CdTe, it has low resistivity, and it is easy to contact. However, the valence-band alignment between InSb and p-type CdTe, which can both impede hole current and enhance forward electron current, is not favorable. Three strategies to address the band-offset problem are investigated by numerical simulation: heavy doping of the back part of the CdTe layer, incorporation of an intermediate CdMgTe or CdZnTe layer, and the formation of an InSb tunnel junction. Each of these strategies is predicted to be helpful for higher cell performance, but a combination of the first two should be most effective.**

***Index Terms*—CdTe, epitaxial, InSb, single-crystal, solar cells, substrate.**

I. Introduction

OVER the past few years, the record energy-conversion efficiency for polycrystalline (poly) CdTe solar cells has broken through the 20% threshold and continues to increase, primarily benefiting from the photocurrent enhancement [1], [2]. However, the open-circuit voltage (V_{OC}) has remained in the 840–870 mV range and is as a major limitation to the conversion efficiency [2]. Several material properties of polycrystalline CdTe [3], [4], such as recombination at the grain boundaries, low carrier concentration, compensation from impurities, and low bulk lifetime, have been suggested as reasons for V_{OC} deficit. To overcome the poly-CdTe material limitations, single-crystal CdTe structures with high-purity and well-controlled parameters have been grown by molecular beam epitaxy (MBE). High minority carrier lifetimes (>200 ns) and impressive radiative efficiency approaching unity were recently reported by researchers from Arizona State and Texas State Universities [5], [6] on CdTe/CdMgTe double heterostructures grown by MBE on InSb substrates. Nevertheless, a major challenge for successful fabrication of epitaxial CdTe solar cells is having a suitable substrate for growth of actual solar cells. Four crystalline substrates, i.e., Si [7], InSb [8], CdTe [9], and GaAs [10], have been employed to grow the epitaxial CdTe solar cells by different research groups. However, efforts to understand the mechanisms involved with each substrate have been limited. A comprehensive epitaxial CdTe model system with specific consideration of substrate choices is, therefore, instructional to provide guidance for the future fabrication of high-efficiency CdTe solar cells. This paper explores practical problems of four substrate candidates (Si, GaAs, InSb, and CdTe) using detailed numerical simulations and then focuses more specifically on InSb. In particular, it proposes three strategies to overcome the valence-band offset between InSb and CdTe.

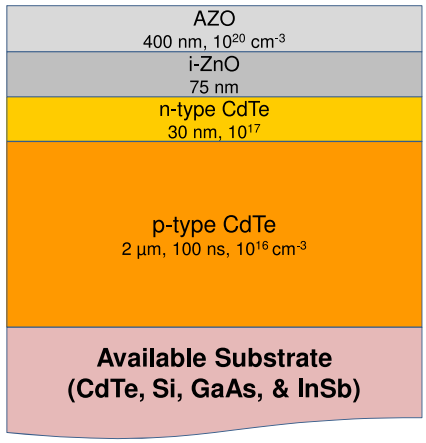

Fig. 1. Schematic of epitaxial CdTe photovoltaic (PV) device architecture used in numerical simulations. Four potential substrates are considered: CdTe, Si, GaAs, and InSb.

II. Baseline Model for an Epitaxial CdTe Cell

The superstrate configuration usually used for poly-CdTe devices cannot be easily translated into epitaxial CdTe cells; therefore, a substrate device structure is assumed for epitaxial CdTe, as shown in Fig. 1. Numerical simulations were performed with the TCAD device simulator Sentaurus Device by Synopsys [11]. The simulated cell features an Al-doped ZnO layer for its front contact, a CdTe homojunction for the collection of photons, and an 800-μm substrate for the growth of epitaxial CdTe. The CdTe carrier density is 10^{17} cm^{-3} for the n-type emitter and 10^{16} cm^{-3} for the p-type absorber. Radiative and Shockley–Read–Hall recombination are included in the model, while Auger recombination is assumed to be negligible [5] and, therefore, is not

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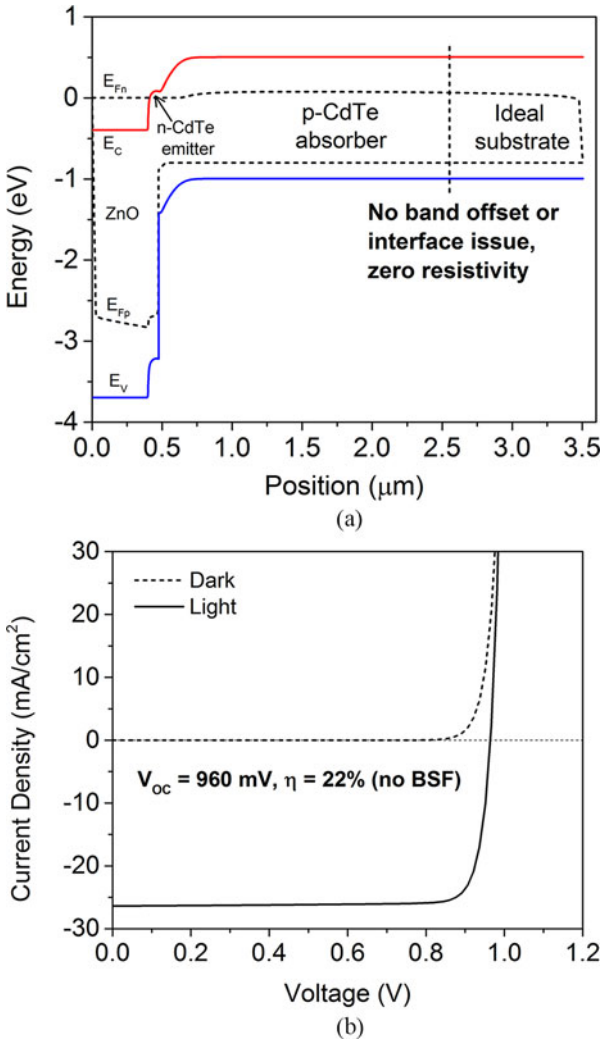

Fig. 2. (a) Energy-band diagrams with ideal substrate (baseline) at 0.8 V under illumination. (b) Calculated *J–V* curves with an ideal substrate and no BSF included.

included. The baseline minority carrier lifetime is 100 ns, and the CdTe radiative recombination coefficient $B_{\rm rad} = 1 \times 10^{-10}$ cm$^3 \cdot$ s^{-1} [5]. The back-surface recombination velocity for electrons is 2.5×10^6 cm/s. Other material parameters in the simulations were taken from our previous work [12], [13].

The baseline epitaxial-CdTe PV-device design assumes an ideal substrate without band alignment, interfacial trap, or series resistance issues. A comprehensive comparison of the available substrates will be examined in detail later. Fig. 2(a) shows the calculated energy-band diagram with an ideal substrate (baseline), at 0.8-V bias and under illumination (approaching $V_{\rm OC}$); Fig. 2(b) shows the corresponding dark and light current–voltage (*J–V*) curves. With higher carrier density ($p = 10^{16}$ cm^{-3}) and minority carrier lifetime ($\tau_n = 100$ ns), the calculated $V_{\rm OC}$ for epitaxial CdTe device should be approximately 100 mV greater than traditional poly-CdTe ($p \sim 10^{14}$ cm^{-3}, $\tau_n \sim 10$ ns) [2], [3]. The calculated band diagram and *J–V* shown in Fig. 2 assume device architecture without advanced features, such as a graded absorber to harvest more photocurrent, or a back-surface field (BSF) to mitigate back-surface recombination. In addition, material limitations of the substrate were not considered.

TABLE I
SUBSTRATE MATERIAL COMPARISON FOR CDTE [17], [18], SI [19], GAAS [20], AND INSB [21], [22]

Substrate	a(Å)	*Eg* (eV)	χ (eV)	ϕ_M to match E_v (eV)	carrier density (cm^{-3})	μ_h (cm^2/V·s)	Resistivity ρ (Ω cm)
CdTe	6.48	1.47	4.30	5.77	~2×10^{15}	~50	~62.5
Si	5.43	1.12	4.05	5.17	~10^{16}	~400	~1.5
GaAs	5.65	1.42	4.07	5.49	~10^{17}	~400	~0.1
InSb	6.48	0.17	4.60	4.77	~10^{16-20}	~850	~10^{-3}

Typical carrier densities were taken for each material.

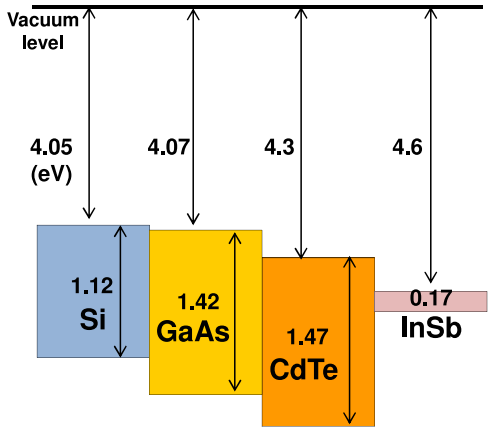

Fig. 3. Band alignment for Si, GaAs, CdTe, and InSb [17], [19]–[21]. The valence-band offset $\Delta E_V = 0.3$ eV between GaAs and CdTe; $\Delta EV = 0.6$ eV between Si and CdTe; $\Delta E_V = 1.0$ eV between InSb and CdTe.

III. COMPARISON OF SUBSTRATE MATERIALS

In reality, the growth of epitaxial layers on a substrate creates a nonideal interface caused by lattice mismatch and/or nonideal band alignment between absorber and substrate. In addition, the substrate itself may introduce parasitic effects such as series resistance and nonohmic contact. Therefore, an appropriate substrate choice is crucial for epitaxial CdTe solar cells to achieve high efficiency. It is known that the GaAs technology achieves high conversion efficiency partially due to the high material quality of a GaAs (or Ge) substrate and the well-controlled interfacial recombination between the main junction and the substrate [14]–[16]. Here, four potential candidates, CdTe, Si, GaAs, and InSb, have been considered as the substrate choices for growing epitaxial CdTe absorber.

Table I compares the material properties of the four substrates. Choosing CdTe or InSb for the substrate avoids the lattice mismatch problem, since CdTe and InSb have nearly identical lattice constants (~6.48 Å), and thus, CdTe should grow on an InSb or CdTe substrate without creating significant interfacial traps. A large lattice mismatch of 19% between CdTe and Si (or 14% lattice mismatch between CdTe and GaAs), however, is likely to cause dislocations at the interface and generate electronic defects. Compared with the negligible resistivity of the other three substrates, the available CdTe substrates have an excessive resistivity due to low doping concentration and hole mobility. Thus, their large series resistance will significantly reduce the cell's fill

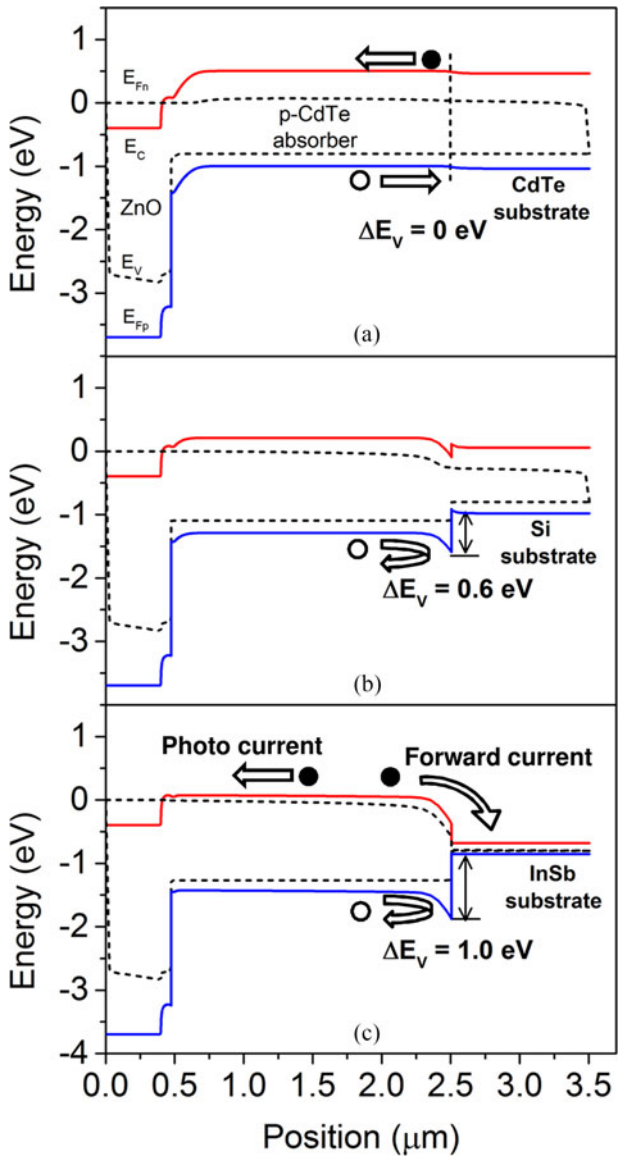

Fig. 4. Energy-band diagrams at 0.8-V bias under illumination for a PV device with CdTe, Si, and InSb substrates. The solid and open circles represent the electrons and holes, respectively, and the arrows represent the direction of carrier flow.

TABLE II
CALCULATED CELL PERFORMANCE WITH CDTE, SI, AND INSB SUBSTRATES

Substrate	P_{sub} (cm^{-3})	R_s ($\Omega \cdot cm^2$)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
Baseline	1×10^{16}	0	960	26.4	86.2	21.9
CdTe	2×10^{15}	5	960	26.3	74.0	18.8
Si	1×10^{16}	0.1	700	25.9	83.2	15.1
InSb	1×10^{18}	0	380	28.7	75.2	7.3

factor. Furthermore, it is challenging to find an appropriate back metal contact for p-CdTe substrate with a large work function to match the valence band of CdTe.

In terms of electronic properties, InSb should serve as the best substrate material. However, there exists a band alignment problem between CdTe absorber and InSb substrate. Fig. 3 shows the natural band alignment of Si, GaAs, CdTe, and InSb. As opposed to a CdTe substrate where band alignment is nonissue, a heterointerface between an InSb (or Si, GaAs) substrate and a p-type CdTe absorber creates a large valence-band offset due to bandgap plus electron affinity (χ) difference. The resulting valence-band barrier will impede hole transport and cause severe carrier recombination (note that if InSb substrate connects to an n-type CdTe absorber, the valence-band barrier should not be an obstacle). Next, we use numerical simulations to investigate how the material limitations for each substrate affect the cell performance. Since Si and GaAs have similar lattice-mismatch and valence-band offset problems, for simplicity, only Si is chosen for device simulation later.

Fig. 4 shows the energy-band diagrams of the three substrates (CdTe, Si, and InSb) under 1-sun illumination and at 0.8-V forward bias. The CdTe substrate has continuous band alignment with the CdTe solar cell and hence generates the largest V_{OC} ($\sim$960 mV, see Table II). However, the high resistivity of CdTe (see Table I) produces a large series resistance with an 800-μm-thick wafer ($R_S \approx 5\,\Omega \cdot \mathrm{cm}^2$) compared with the negligible resistance of Si and InSb. As a result, the large R_S compromises the fill factor for CdTe substrate choice. To date, it has proven difficult to either reduce the wafer thickness or increase the wafer doping density to lower the series resistance of CdTe substrate [18]. Thus, even though CdTe substrate has no band alignment or lattice mismatch problem, it does not appear to be a straightforward substrate for growing epitaxial CdTe cells.

For both Si and InSb substrates, there is a large valence-band offset ($\Delta E_V = 0.6$ eV for Si and $\Delta E_V = 1.0$ eV for InSb), which can seriously impede the transport of photogenerated holes and thus enhance the hole recombination. In addition, as shown in the band diagram with the InSb substrate in Fig. 4(c), the severe conduction-band bending caused by the electron-affinity differences between the two materials allows a large forward current to flow to the back surface. The distance between the conduction-band energy E_C and electron quasi-Fermi level E_{Fn} is much narrower than with a Si or CdTe substrate, and it enhances the forward electron current [23]. Overall, without an enhancement layer, the calculated V_{OC} for InSb ($\sim$380 mV) are much lower compared with the V_{OC} with CdTe substrate ($\sim$960 mV), as shown in Table II.

IV. ENHANCEMENT LAYERS TO IMPROVE V_{OC} FOR AN INSB SUBSTRATE

InSb is a favorable substrate choice because of excellent lattice match and negligible resistivity, but has an unfavorable energy-band alignment with the CdTe absorber. In addition, the conduction-band bending may enhance severe back-surface recombination [see Fig. 4(c)]. It should be helpful to raise the conduction band or add a BSF at CdTe/InSb interface to effectively reflect electrons away from the back contact. A BSF layer can be created either by heavy doping or alloying with elements, which would expand the bandgap. On the other hand, the large valence-band barrier caused by chemical potential difference blocks the photogenerated holes. To assist hole

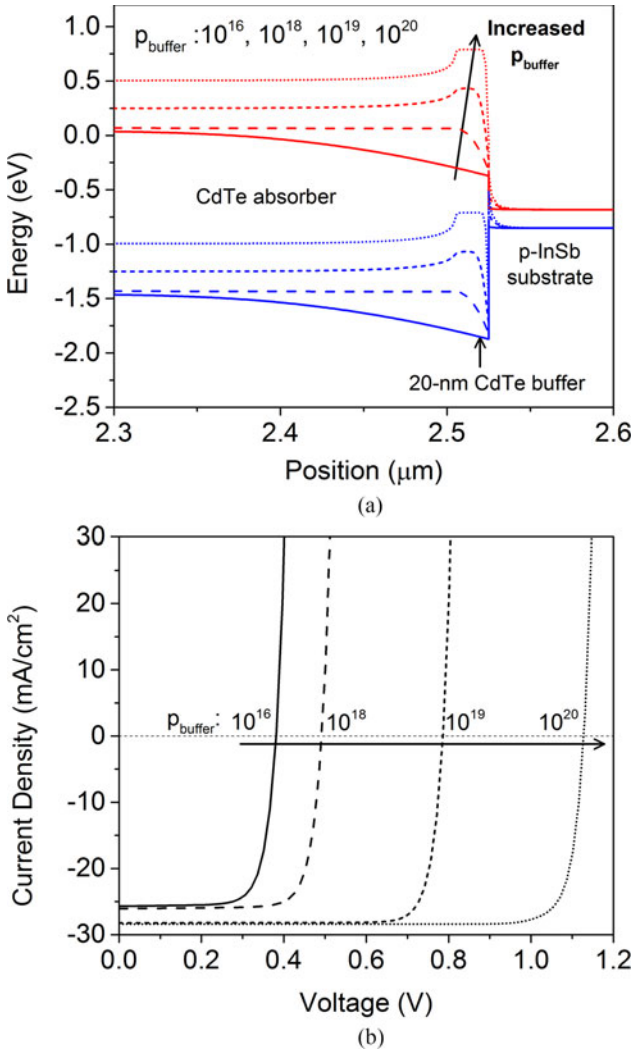

Fig. 5. (a) Conduction and valence bands of an epitaxial CdTe cell with a 20-nm CdTe buffer layer at 0.8-V bias under illumination, zoomed at the back to emphasize the impact of the CdTe buffer. $p_{\rm buffer}$ varied from 10^{16} to 10^{20} cm^{-3}. (b) Corresponding *J–V* curves.

transport, a highly doped thin buffer layer at the CdTe/InSb interface could narrow the valence-band barrier and thus allow holes to tunnel across the interface. In this section, three enhancement features are proposed to overcome the $V_{\rm OC}$ limitations imposed by usage of InSb substrate and thus create an opportunity for the epitaxial CdTe device to achieve better performance. The strategies described should be applicable for other substrates as well.

A. Highly Doped CdTe Buffer Layer

Insertion of a highly doped $(\rm p^{++})$ CdTe buffer layer between the CdTe absorber and InSb substrate can mitigate the large forward electron current caused by severe conduction-band bending at this interface, and in this study, it will be referred to as a CdTe buffer layer. This kind of buffer layer is often referred to as a BSF in Si-based solar cells [24] or an electron reflector in polycrystalline CdTe solar cells [25]. Fig. 5(a) shows the simulated band diagram with a 20-nm-thick CdTe buffer at 0.8-V bias under illumination. The conduction-band energy (E_C) near the interface is gradually raised as the carrier density of the buffer layer ($p_{\rm buffer}$) is increased, as shown in Fig. 5(a). An effective electron reflector is formed with $p_{\rm buffer}$ above 10^{18} cm^{-3}, which can reflect electrons away from the back surface and mitigate the back-surface recombination. Meanwhile, with increasing $p_{\rm buffer}$, the valence-band energy (E_V) of CdTe buffer is lifted near the interface to approach the E_V of InSb. Thus, a thinner valence-band barrier is formed to allow the holes to tunnel across the interface. As a result, in Fig. 5(b), $V_{\rm OC}$ is enhanced significantly with increased $p_{\rm buffer}$ due to electron reflection and better hole transport near the interface. In addition, the highly doped CdTe buffer improves the collection of long-wavelength photons; therefore, a small $J_{\rm SC}$ enhancement is also observed in the short-dashed (10^{19} cm^{-3}) and dotted (10^{20} cm^{-3}) *J–V* curves in Fig. 5(b). Note that it is extremely difficult to obtain a heavily doped CdTe buffer with $p_{\rm buffer} = 10^{20}$ cm^{-3}, which means that the effectiveness of a highly doped CdTe buffer by itself is likely to be limited.

B. Expanded-Bandgap Buffer Layer (CdZnTe)

Adding a higher bandgap buffer layer to act as an electron reflector can be more effective than a highly doped CdTe buffer, since the expanded bandgap can create an abrupt barrier in the conduction band, while the barrier height remains constant with external bias. Alloying CdTe with Mg and Zn to form CdZnTe (CZT) or CdMgTe (CMT) could serve this purpose. The CZT and CMT bandgaps can be determined by adjusting the composition ratios. For CZT, the bandgap varies as $E_g(x) = 1.47 + 0.45x + 0.30x^2$ [17], where x is the Zn/(Cd+Zn) ratio. The bandgap ranges from 1.47 to 2.25 eV, and most of the expansion is in the conduction band. For CMT, the bandgap variation with Mg fraction is $E_g(x) = 1.47 + 1.35x + 0.55x^2$ [17], where the bandgap ranges from 1.47 to 3.4 eV, and the expansion happens in both the conduction and valence bands. The electron affinities of CdTe, ZnTe, and MgTe have been reported as 4.3, 3.53, and 3.25 eV, respectively [26]–[28], and here, we assume a linear dependence of electron affinity on Zn or Mg fraction. Fig. 6 shows the natural band alignment of CdTe, $\rm Cd_{0.6}Zn_{0.4}Te$, and $\rm Cd_{0.8}Mg_{0.2}Te$. CdTe/CZT forms a type-II heterojunction, creating a positive conduction-band barrier to reflect photogenerated electrons and a negative valence-band offset to assist hole transport; however, CdTe/CMT forms a type-I heterojunction, where there is electron reflection, but the positive valence-band barrier can at least partially impede the hole current. Therefore, the CZT alloy should be a better choice from the band-alignment considerations.

Next, the combined impact of alloying and high carrier density in CZT buffer is examined in Fig. 7, which shows the conduction and valence bands with varying Zn/(Zn+Cd) ratio (0, 0.2, 0.4, and 0.5) in a 20-nm-thick CZT buffer with carrier densities of 10^{16} and 10^{19} cm^{-3} and under illumination and 0.8-V bias. In Fig. 7(a), with $p_{\rm buffer} = 10^{16}$ cm^{-3} and a 20% Zn/(Zn+Cd) ratio, the electron reflector due to the expanded gap is marginal because of the severe conduction-band bending, and the curved region near the interface forms a potential well that

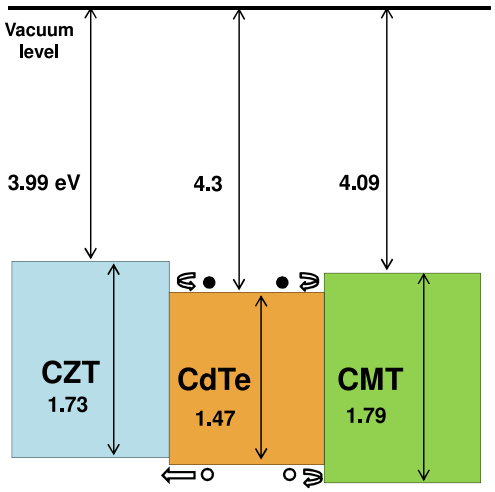

Fig. 6. Band alignment of CdTe, CZT (40%Zn), and CMT (20%Mg) [17], [28]. CdTe/CZT forms a type-II heterojunction, which reflects electrons and assists holes; CdTe/CMT forms a type-I heterojunction, which reflects electrons and blocks holes.

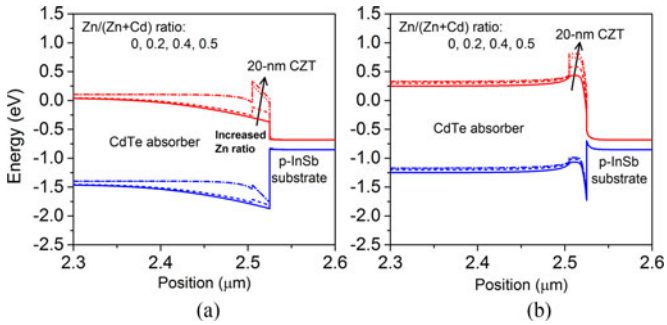

Fig. 7. Energy-band diagram under illumination, at 0.8-V bias, with a 20-nm expanded-bandgap CdZnTe layer, at (a) $p_{\mathrm{CZT}} = 10^{16}$ and (b) 10^{19} cm^{-3}.

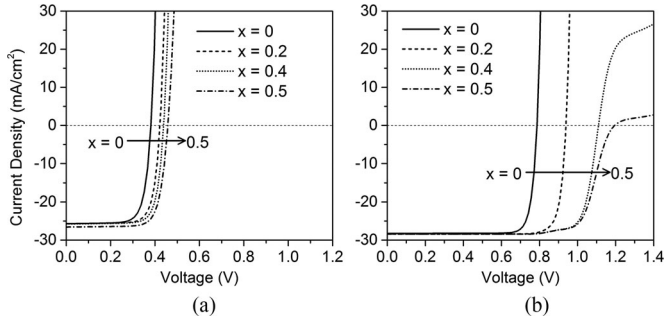

Fig. 8. Calculated light *J–V* curves with a 20-nm CdZnTe buffer layer, varying Zn ratio, at (a) $p_{\mathrm{CZT}} = 10^{16}$ and (b) 10^{19} cm^{-3}.

can trap electrons. Additionally, there is only a small valence-band modification with increasing Zn ratio. Hence, there is only a slight V_{OC} improvement with increased Zn ratio, as shown in Fig. 8(a). In comparison, higher carrier density, $p_{\mathrm{buffer}} = 10^{19}$ cm^{-3} [see Fig. 7(b)], forms a more effective electron reflector in the conduction band, and the valence-band barrier narrows to assist hole tunneling across the interface. Therefore, as shown in Fig. 8(b), both J_{SC} and V_{OC} should increase significantly with the addition of a thin CZT buffer layer. Note that the rollover of *J–V* curves above V_{OC} is due to the suppression of forward

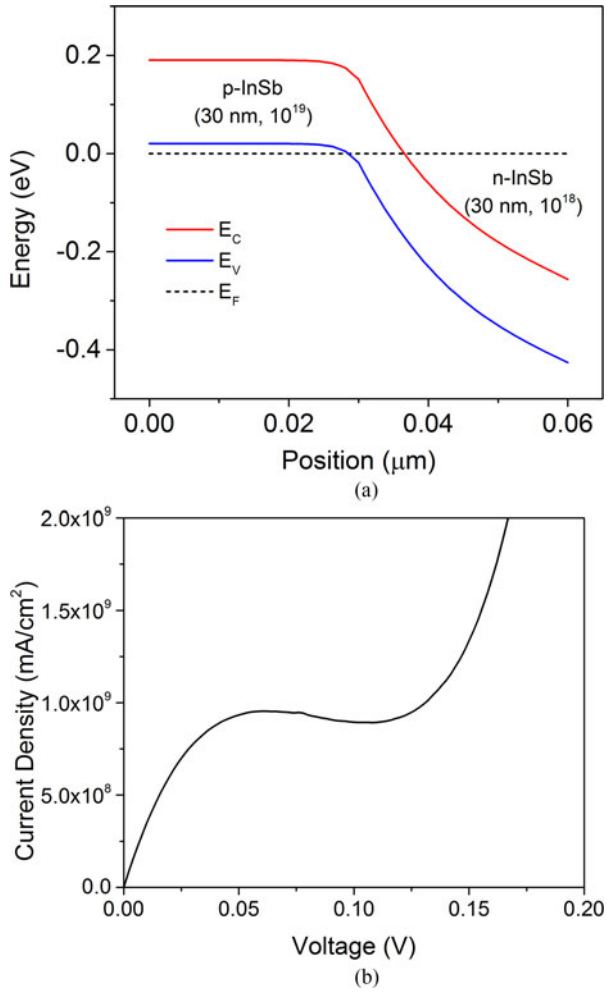

Fig. 9. (a) Energy-band diagram of an InSb TD at equilibrium, consisting of 30-nm 10^{19} cm^{-3} p-InSb and 30-nm 10^{18} cm^{-3} n-InSb layers. (b) Calculated *J–V* curves of the InSb TD.

current if there is an excessive conduction-band offset at CZT/InSb interface. Additionally, there is some lattice mismatch between CdTe and CZT, which may cause interfacial recombination. The simulations, however, show that the cell performance has little variation when the interfacial recombination velocity S_i is below 10^4 cm/s although large S_i values can compromise the cell performance.

C. *Incorporation of an InSb Tunnel Diode*

The third modification considered here is the incorporation of an InSb tunnel diode (TD) to possibly mitigate the unfavorable band alignment issue. The InSb TD [29], [30] considered consists of a simple p-n junction in which both n and p sides are degenerate, and there is a sharp transition between them, as shown in Fig. 9(a). For the InSb TD simulation, a nonlocal direct band-to-band tunneling model was employed to better simulate the true carrier transport through the barrier [31]. With small forward bias, the electrons in conduction band on the n-side of the diode can tunnel through the bandgap to the valence band on the p-side and recombine with the holes to produce the tunneling current. Fig. 9(b) shows the corresponding *J–V*

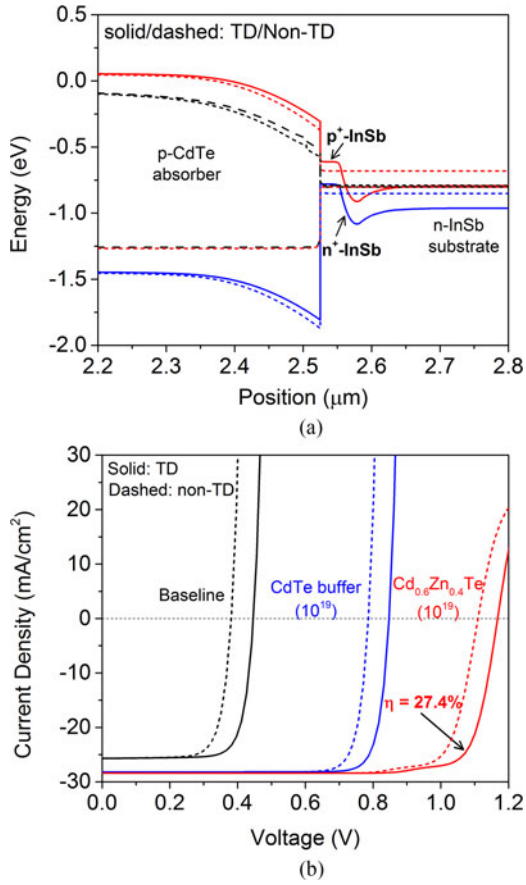

Fig. 10. (a) Energy-band diagram at 0.8-V bias under illumination, with (solid) and without (dashed) an InSb TD. (b) Calculated light *J–V* curves with and without an InSb TD for the baseline case and adding 20-nm 10^{19} cm^{-3} CdTe and CdZnTe (40% Zn) buffer.

curves of the InSb TD with effective masses $m_c = 0.014\ m_0$ and $m_v = 0.4\ m_0$ [22]. Because of its very narrow bandgap, an InSb TD will have a very large current response even at small bias. This indicates there should be little voltage drop for photocurrent transport in solar cells.

When an InSb TD is inserted before a p-CdTe absorber, the n-side of the InSb TD contacts the n-InSb substrate to smooth the carrier flow, differing from the p-substrate in previous two approaches. Fig. 10(a) shows the energy-band diagram of a baseline cell with and without the InSb TD (solid lines represent the bands with TD and dashed lines without TD). It is seen that both the conduction and valence bands shift slightly upwards with TD, indicating a small mitigation of the band bending. Therefore, in Fig. 10(b), all the *J–V* curves with TD (solid lines) show a small degree of $V_{\rm OC}$ improvement. The combination of a thin CZT buffer (40%Zn, 10^{19} cm^{-3}) and an InSb TD yields a calculated conversion efficiency of 27.4%: the highest of any of the cases considered. Therefore, a combination of enhancement layers is likely to improve cell performance more than applying individual layers.

V. Conclusion

Several materials have been considered as the crystalline substrate for epitaxial CdTe solar cells. Each has its advantages and disadvantages. Available CdTe substrates have excessive series resistance; however, Si and GaAs have large lattice mismatch with CdTe absorber, and Si, GaAs, and InSb substrates all have issues with band offsets, which impede the flow of holes and allow excessive forward current. To address the unfavorable band alignment for InSb substrate, three enhancement strategies were considered: a highly doped CdTe buffer, an expanded-bandgap layer, and the application of an InSb TD. Table III summarizes how these approaches affect CdTe cell performance. A highly doped CdTe buffer can play a role in both reflecting electrons and assisting holes; however, its effectiveness is likely to be limited due to the difficulty in achieving heavy doping. Since a CZT buffer has an expanded bandgap in the conduction band, it can more easily form an electron reflector and thus can improve the cell performance more effectively. The incorporation of an InSb TD adds a small additional mitigation of the band bending and should produce a slightly better $V_{\rm OC}$. Over all, each approach has different degrees of performance improvement; however, a combination of the approaches is advised for the highest efficiencies. In addition, it is noted that CdTe cells with an n-type CdTe absorber might be another solution to the negative effect of the valence-band barrier and is also worthy of investigation.

TABLE III
Effectiveness Comparison of the Three Performance Enhancement Strategies

Approaches	$V_{\rm OC}$ Improvement	
	Degree	Supplemental Explanation
Highly doped CdTe buffer	+ +	Both reflects electrons and assists hole transport.
Expanded-bandgap CdZnTe	+ + +	More effective than highly doped CdTe.
Application ofInSb TD	+	Modest help with the mitigation of E_C bending and E_V barrier.

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Authors' photographs and biographies not available at the time of publication.