A Robust Technique for Measuring and Simulating Silicon Wafer Quality Characteristics that Enable the Prediction of Solar Cell Electrical Performance of MEMC Silicon Wafer

Cooperative Research and Development Final Report

CRADA Number: CRD-11-438

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In accordance with Requirements set forth in Article XI, A(3) of the CRADA document, this document is the final CRADA report, including a list of Subject Inventions, to be forwarded to the Office of Science and Technical Information as part of the commitment to the public to demonstrate results of federally funded research.

Parties to the Agreement: MEMC Electronic Materials, Inc.

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CRADA Title: A Robust Technique for Measuring and Simulating Silicon Wafer Quality Characteristics that Enable the Prediction of Solar Cell Electrical Performance of MEMC Silicon Wafer

Joint Work Statement Funding Table Showing DOE Commitment:

Estimated Costs	NREL Shared Resources
Year 1	$100,000.00
Year 2	$100,000.00
Year 3	$100,000.00
Mod 1	$40,000.00
Mod 2	$140,000.00
TOTALS	$200,000.00

Abstract of CRADA Work:

NREL and MEMC Electronic Materials are interested in developing a robust technique for monitoring material quality of mc-Si and mono-Si wafers—a technique that can provide relevant data to accurately predict the performance of solar cells fabricated on them. Previous work, performed under two TSAs between NREL and MEMC, has established that dislocation clusters are the dominant performance-limiting factor in MEMC mc-Si solar cells. The work under this CRADA will go further in verifying these results on a larger data set, evaluating possibilities of faster method(s) for mapping dislocations in wafers/ingots, understanding dislocation generation during ingot casting, and helping MEMC to have an internal capability for basic characterization that will provide feedback needed for more accurate crystallization simulations. NREL has already developed a dislocation mapping technique and developed a basic electronic model (called Network Model) that uses spatial distribution of dislocations to predict the cell performance. In this CRADA work, we will use these techniques to: (i) establish dislocation, grain size, and grain orientation distributions of the entire ingots (through appropriate design of experiments) and compare these with theoretical models developed by MEMC, (ii) determine concentrations of some relevant impurities in selected wafers, (iii) evaluate potential of using

photoluminescence for dislocation mapping and identification of recombination centers, (iv) evaluate use of diode array analysis as a detailed characterization tool, and (v) establish dislocation mapping as a wafer-quality monitoring tool for commercial mc-Si production. We will also continue studies on P-type wafers/cells and study the nature of defects and impurities in N-type Si.

Summary of Research Results:

1. Characteristics of diamond wire sawing of silicon wafers were determined. It was found that surface damage can be 4 to 7 microns deep. The surface damage can be laterally nonuniform and follows the periodicity of the wire motion. The depth of damage is primarily controlled by the diamond grit size.
2. Dislocation generation and their propagation within a cast multicrystalline silicon ingot were studied. Dislocations are generated preferentially in certain grains at the start of the crystallization. These dislocations can multiply and, more importantly, annihilate as the crystal growth continues. This is determined by the nature of the thermal stresses.
3. We developed a theoretical model that predicts the performance of a solar cell fabricated on a wafer having a known distribution of dislocations. This model agrees very well with the experimental results.
4. Light induced degradation (LID) was studied in monocrystalline silicon solar cells. It was determined that it takes 72 hours under 1-sun illumination to have complete LID. We also determined that the degradation occurs primarily because of degradation in the bulk minority carrier lifetime. However, we also discovered that a fraction of LID occurs because of the interface degradation due to increase in Dit at the SIN-Si interface.

Subject Inventions Listing:

None

Report Date:

October 21, 2015

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