Fast Determination of Distribution-Connected PV Impacts Using a Variable Time-Step Quasi-Static Time-Series Approach

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Fast Determination of Distribution-Connected PV Impacts Using a Variable-Time-Step Quasi-Static Time-Series Approach

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***Abstract* — The increasing deployment of distribution-connected photovoltaic (DPV) systems requires utilities to complete ever more complex interconnection studies. Relatively simple interconnection study methods worked well for low penetrations of photovoltaic systems, but more complicated quasi-static time-series (QSTS) analysis is required to make better interconnection decisions as DPV penetration levels increase. Tools and methods must be developed to support this type of complex analysis to enable efficient completion of PV impact studies. This paper presents a variable-time-step solver for QSTS analysis that significantly shortens the computational time and effort to complete a detailed analysis of the operation of a distribution circuit with many DPV systems. Specifically, it demonstrates that the proposed variable-time-step solver can reduce the required computational time by as much as 84% without introducing any important errors to metrics, such as the number of voltage regulator tap operations and highest and lowest voltage occurring on the distribution circuit during a 1-yr simulation period. Further improvement in computational speed is possible with the introduction of only modest errors in these metrics, such as a 91% reduction with less than 5% error when predicting voltage regulator operations. Furthermore, an alternate variable time-step method is also shown to perform adequately and shows promise of even greater reductions in simulation runtime.**

***Index Terms* — Distribution system modeling, PV grid integration, QSTS, time-series analysis, variable time-step.**

I. Introduction

Worldwide, many distribution utilities are experiencing increasing deployments of distribution-connected photovoltaic (DPV) systems, which necessitates these utilities to consider and study increasingly complex photovoltaic (PV) interconnection scenarios. When the number of DPV systems interconnected to a single circuit is relatively low, simpler interconnection screening [1] and study processes [2] are adequate to provide the utilities with enough information to guide DPV interconnection approval. These methods employ many worst-case assumptions regarding the operation of the distribution system and the behavior of the DPV systems. These assumptions not only simplify the screening and study processes but also add considerable conservatism to the DPV interconnection outcomes in many circumstances. To provide more accurate, informative, and realistic information regarding the expected impact of DPV on the distribution system, quasi-static time-series (QSTS) analysis methods have been developed and demonstrated for DPV interconnection studies [3]–[4]. These methods have been proven to be very useful, but they introduce another challenge because QSTS-based DPV interconnection studies require considerable computational effort, making them both costly and potentially untimely for use by utilities on a daily basis or for every requested interconnection. For instance, a yearlong QSTS simulation of a realistic distribution circuit at a temporal resolution of 1 s can take 24–96 hours to complete using business grade computing resources typically available to distribution utility engineers.

To enable regular utility use of QSTS study techniques, the research detailed in this paper was completed with the express goal of significantly shortening the computational time and effort required for DPV interconnection analysis. Specifically, this paper focuses on the temporal nature of the QSTS analysis and presents a method wherein two different time steps are employed to move quickly through the simulation when possible and proceed at the minimum time step during periods when the circuit is undergoing material change. In this paper, this QSTS solution method is referred to as the variable-time-step solver. A number of additional efforts as part of the same project are also under way [5]. Additionally, previous work with this goal included temporal down-sampling and vector quantization (discretization of the system state) [6] and efforts to select better power flow solution initial conditions for each time-step in a time-series analysis to increase simulation speed [7].

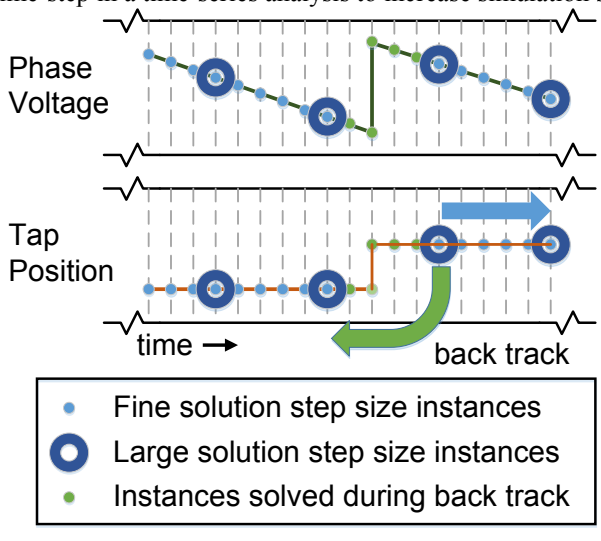

Fig. 1. Conceptual diagram of the operation of the variable-time-step solver.

Section II provides a description of the two versions of the variable-time-step solver of the QSTS analysis developed.

Section III presents the results of the two variable-time-step solvers when applied to two distribution circuits: one simple test circuit and one complex utility circuit. Also included are results on the accuracy of determining the number of automatic voltage regulation (AVR) equipment operations and the minimum and maximum voltages modeled on a circuit over a 1 year period. Section IV concludes the paper.

II. Description of Variable-Time-Step Solver

Two variations of variable-time-step solver implementations are described in the following subsections. The first describes the most basic variable-time-step solver, which simply implements a backtrack function to complete higher temporal resolution analysis when needed. The second adds a binary search feature to the backtrack function to further intelligently reduce the number of individual power flow solutions. Additionally, a time-seeking functionality was incorporated wherein once the point at which a pending automatic voltage regulation device is determined using the binary search algorithm, the solution skips ahead to the point in time at which the action will either take place or expire depending on the circuit conditions at that time.

A. Backtrack-Based Variable-Time-Step Solver

The variable-time-step solver was conceptualized from existing methods used in transient simulation solvers. The idea is to vary the temporal time step of the QSTS solution so that periods of interest in circuit operation are analyzed at the highest temporal resolution possible and periods when the circuit is relatively static are analyzed at coarser temporal resolutions to reduce computational time. The variable-time-step solver uses a backtrack method wherein coarse time steps are taken until a system state change is detected. Then the solver backtracks to the previous large time-step instance and proceeds with small time steps for a period of time until large time-stepping is resumed. Fig. 1 shows a conceptual diagram of the variable-time-step solver including the large and small time-step instances as well as the backtrack functionality when a voltage regulator tap position changes.

The primary purpose of DPV interconnection studies is to evaluate the voltage- and equipment-related impacts of the interconnection of additional PV. Thus, the variable-time-step solver uses a change in voltage regulator tap position to detect time periods when a higher resolution analysis would yield higher accuracy in results in terms of determining the number of voltage regulator operations and the minimum and maximum voltages experienced on the circuit being studied.

Fig. 2 shows the programmatic implementation of the variable-time-step solver. It matches the functionality shown in Fig. 1 with the addition of a few features that were added to improve the accuracy of the solver. The number of solutions completed at a small time-step resolution (after a temporal backtrack) is equal to the maximum step size ($t_{max,ss}$) employed in the solver. The existence of other pending control actions is checked again, and additional small time steps are taken until all control actions are resolved. These features were added because multiple, successive changes to the voltage regulator tap position are fairly common, and thus the solver attempts to resolve multiple changes without recursively backtracking.

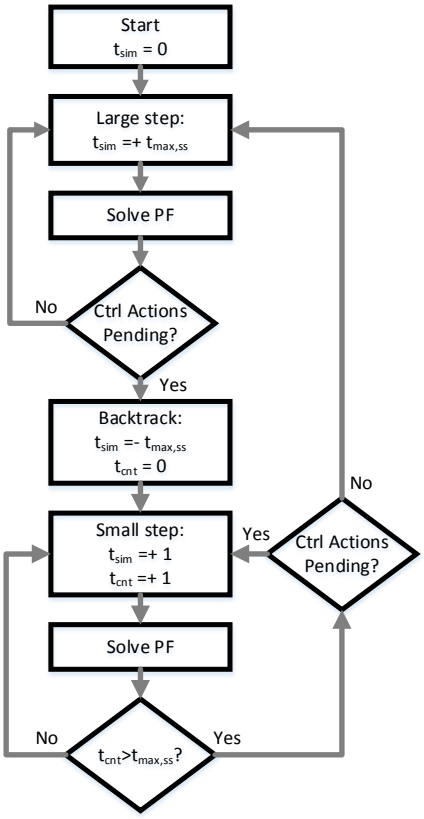

Fig. 2. Flow diagram of the variable-time-step solver.

B. Addition of Binary Search and Time-Seeking to Variable Time-Step Solver

In the variable-time-step solver, as shown in Fig. 2, once a pending control action is detected during a large time-step analysis, no actionable information is available about when a pending control action was instantiated other than the pending control action that occurred between the current solver time and the last time point that showed no pending control actions. The length of time in this window is equal to the large time step. Because this time step can be quite large, a more efficient search method for the possible pending control action time window was implemented. Once the point in time at which a pending control action is determined, a time-seeking function is implemented wherein the time at which the control action will be acted upon—instead of instantiated as pending—is gathered directly from the QSTS power flow solver, and the solution time is advanced directly to that time to avoid unnecessary power flow solutions. Fig. 3 shows the flow diagram of the variable-time-step solver with the binary search and time-seeking implemented. The variables t_l and t_u denote

the diminishing time interval being bisected during the binary search. When t_l and t_u are consecutive time points, the binary search is complete. Then the time at which a pending control action is planned to occur (assuming no circuit conditions change and reset the pending control action) is queried directly from the control queue of the QSTS simulation. This time is referred to as t_{act} in Fig. 3. The QSTS simulation time is set to t_{act} and a power flow solution and control iteration are completed to determine if a pending control action took place or expired due to the delay reset functionality of the AVR controllers. This time-seeking functionality eliminates completing a number of power flow solutions that are approximately equal to the length of the delay of the automatic voltage regulation equipment.

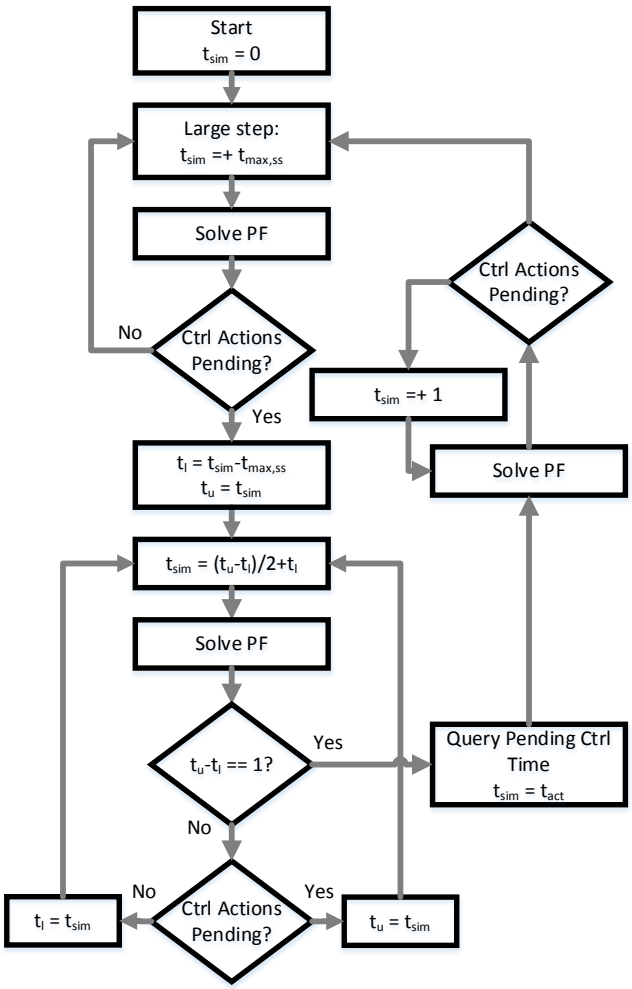

Fig. 3. Flow diagram of the variable-time-step solver with binary search and time-seeking implemented.

III. Results

Both the backtrack-based variable-time-step solver and the binary search and time-seeking solver were evaluated to determine the expected improvement in analysis speed as well as their resulting errors compared to a yearlong 1-s resolution QSTS analysis. Two distribution circuits were used to evaluate the solvers' performance. The first was the IEEE 13-node circuit [8], which contains three single-phase voltage regulators and two fixed shunt capacitors. A 3-MW PV system connected to bus 675 was added to the model for evaluation purposes. Realistic yearlong 1-s resolution load and PV generation profiles were developed to drive the QSTS analysis. The control delay of the voltage regulators was 30 s. This means that the regulators changed tap positons after their control deadband had been exceeded for 30 s or more. Yearlong 1-s resolution analysis of this circuit without the use of a variable-time-step solver was approximately 55 min, making the circuit useful to quickly determine the efficacy of the variable-time-step improvements. The second circuit was a 3,000+ node model of a 15-kV circuit from a utility. The model was modified via the inclusion of 50 PV systems (48 15-kw single-phase residential systems and 2 100-kW three-phase commercial systems). This model includes three single-phase voltage regulators and four three-phase switched capacitors that are controlled based on a measured single-phase voltage. The duration of a yearlong 1-s resolution analysis of this circuit without the use of a variable-time-step solver was approximately 79 h using laptop workstation (2.4 GHz Intel i7-2760QM), making this circuit representative of real-world challenges when completing detailed QSTS analysis on complicated circuits. OpenDSS [9] was used as the base distribution system analysis package but extensive use of the COM via Matlab was used to implement the variable time-step solver routines. Runtime percent reduction, used as a metric to determine the speed increase of the variable time-step methods, is based on actual computer runtimes and thus includes time incurred due to the implementation of the variable time-step solver routines in Matlab and COM communications to OpenDSS. If such routines were added in native formats to OpenDSS or other distribution system analysis packages, runtime reductions should be greater.

A. Voltage Regulator Operations

The only selectable parameter in the presented variable-time-step solvers is the choice of the maximum time step of the simulation, $t_{max,ss}$, (the large time step). The sensitivity of the selection of this parameter was investigated, and the results are presented in this subsection.

The ability to analyze DPV impact on voltage regulation devices is a major benefit of QSTS-based analysis, so the accuracy of such voltage regulation operational impacts is paramount. An acceptable error of ±5% was targeted for this work based on input from practicing distribution engineers.

TABLE 1. RUN-TIME REDUCTION AND ERROR/IMPROVEMENT OF THE VARIABLE-TIME-STEP SOLVER WITH BINARY SEARCH AND TIME-SEEKING—IEEE 13-NODE

	Operations (% of base case)			MAPE	Runtime
max step (s)	Reg1-A	Reg1-B	Reg1-C	(Reg. Ops.)	(% reduction)
5	101.89	104.14	141.10	2.83	22.8%
10	103.27	108.57	141.68	4.91	60.1%
15	102.33	108.71	140.10	4.26	72.5%
30	101.46	108.25	137.88	3.28	85.1%
60	94.05	99.79	127.98	4.41	90.8%
120	80.61	86.92	109.47	17.66	94.7%

TABLE 2. RUN-TIME REDUCTION AND ERROR/IMPROVEMENT IN THE BACKTRACK VARIABLE-TIME-STEP SOLVER—3,000+ NODE UTILITY CIRCUIT.

	Operations (% of base case)				MAPE	Runtime
max step (s)	Reg1-A	Reg1-B	Reg1-C	Cap3	(AVR. Ops.)	(% reduction)
5	100.00	100.00	100.00	100.00	0.00	80.1%
10	100.00	100.00	100.00	100.00	0.00	88.8%
15	100.00	100.00	100.00	100.00	0.00	92.4%
30	100.00	100.00	100.00	100.00	0.00	95.9%
60	100.00	99.55	99.40	100.00	0.26	98.8%
120	100.00	97.30	98.80	100.00	0.98	98.5%
300	93.10	94.14	97.01	100.00	3.94	99.3%

TABLE 3. RUN-TIME REDUCTION AND ERROR/IMPROVEMENT COMPARED TO DOWN-SAMPLED QSTS ANALYSIS OF THE VARIABLE-TIME-STEP SOLVER—IEEE 13-NODE

	Operations (% of base case/% improvement[1])			MAPE	Runtime
max step (s)	Reg1-A	Reg1-B	Reg1-C	(Reg. Ops.)	(% reduction)
5	100.00 / 0.74	99.96 / 0.15	99.97 / 1.27	0.02	38.1%
10	100.00 / 2.11	99.96 / 1.11	99.97 / 2.52	0.02	46.8%
15	100.00 / 3.10	100.04 / 1.99	100.03 / 4.28	0.00	73.3%
30	100.00 / 7.25	100.04 / 5.47	99.97 / 7.67	0.02	83.9%
60	95.66 / 23.00	95.83 / 23.09	94.94 / 23.21	4.53	91.3%
120	84.68 / 27.42	84.72 / 27.72	83.29 / 27.23	15.78	95.2%

[1] Improvement in the additional percentage of regulator operations compared to down-sampled QSTS analysis with time step equal to max. time step.

Table 1 shows the results of implementing the variable-time-step solver with various maximum step sizes ranging from 5–120 s. The number of voltage regulator operations determined by the analysis is shown for all three phases of the voltage regulator. Additionally, the number of voltage regulator operations resolved by the solver was compared to simply down-sampling the QSTS analysis. Down-sampling simply means that the simulation was run at a fixed step size. This comparison allows for determining the value of the variable-time-step solver in balance with its beneficial reduction in run time because the down-sampled analysis also reduces the run time in a fashion that is similar to that of the variable-time-step solver. The mean absolute percentage error (MAPE) is given for each test run as well as the run-time percentage reduction. As shown, the variable-time-step solver has effectively no

error in voltage regulator operations for maximum time steps up to 30 s. For higher maximum time-steps, some error is introduced because the large time steps potentially skip over short-duration tap position changes. However, even at a maximum step size of 60 s, the MAPE is less than the targeted 5%. At this setting, the time required for the simulation is reduced by 91.3%.

When the backtracking variable-time-step solver is used to complete a yearlong QSTS analysis of the 3,000+ node utility circuit, the run-time reduction shown in TABLE 2 is attained. The accuracies of the voltage regulators and the third switched capacitor are also shown. Only the operations for switched capacitor #3 are shown because the other three capacitors were either always off or always on for the duration of the QSTS simulation. The AVR MAPE is less than the estimated 5% accuracy necessary for making good distribution grid planning decisions up to a maximum step size of 300 s. The 3000+ node utility feeder sees less variability than the IEEE 13 node case due to a lower amount of integrated PV and lower impedance construction. Still, the backtrack algorithm provides accurate results with up to 99.3% runtime reduction.

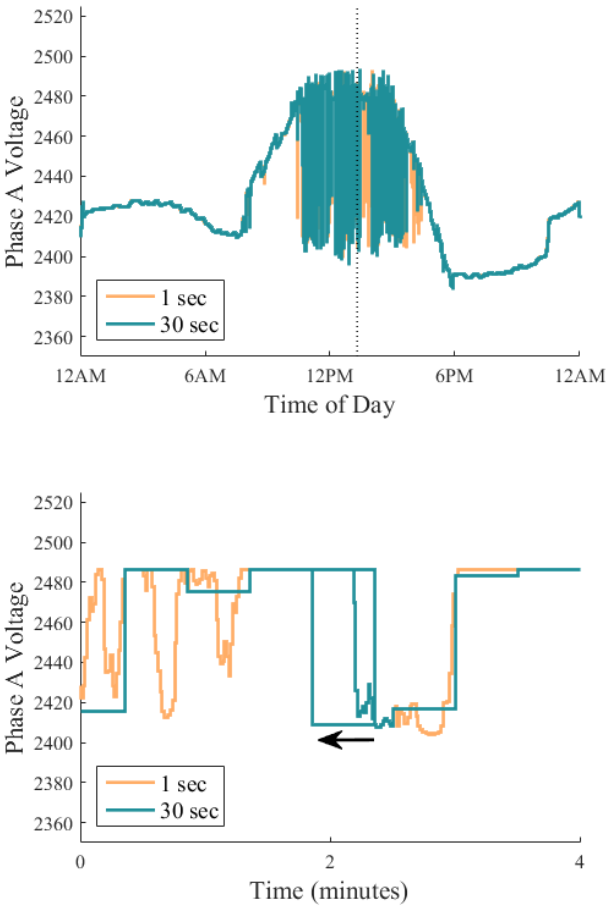

Fig. 4. Example voltage profiles calculated using traditional analysis and the variable-time-step solver with a tmax,ss of 30 s. The top plot shows voltage profile during an entire day, and the bottom plot shows the detail of a 4-min. period.

Evaluation of the variable time-step solver with binary event search and time-seeking once a pending event instantiation is determined, using the IEEE 13 node circuit, is shown in TABLE 1. Comparing Table 1 and TABLE 1 reveals that the basic backtrack variable time-step solver has a larger runtime reduction. This is likely due to the specific implementation of the binary event search/time-seeking algorithms as discussed later. For a maximum step-size of 60 s the back track method has a runtime reduction of 91.3% versus 90.8% for the binary search/time-seeking algorithm. The accuracy of determining the regulator operations is comparable between the two methods with the exception of higher error at lower maximum time-steps for the binary search/time-seeking algorithm. The increased error seems to be due to potential for pending regulator control actions to expire between instantiation and the end of the control delay period. Both the binary search and time-seeking part of the algorithm introduce erroneous or mistimed regulator actions when these pending events expire during the delay period. There is also some additional error over the simple backtrack method due to more numerous power flow solutions being solved without previous time-step initial conditions as happens when the time-series analysis experiences a discontinuity in simulation time.

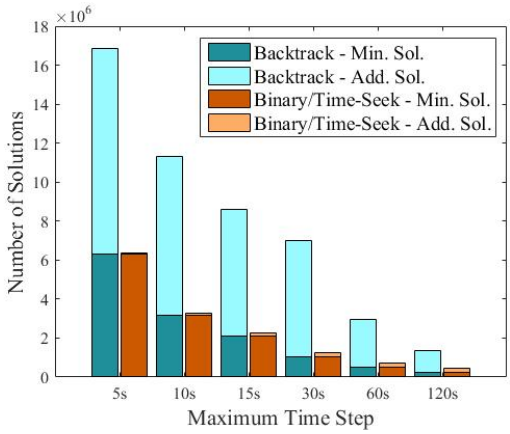

Figure 4. The number of additional solutions completed by the two variable time-step algorithms for a yearlong analysis of the IEEE 13 node test feeder.

For the IEEE 13 node test circuit case the amount of time during which no regulator control actions are pending is above 98% - during these period the variable time-step solvers move through the simulation with large time- steps. The remaining time one or more regulator control action(s) are pending the variable time-step algorithms attempt to resolve control action occurrences and timings. The number of power flow solutions required to complete a yearlong analysis of the IEEE 13 node circuit are shown in Figure 5. The figure shows both the

minimum number of time-steps, equivalent to the simulation length divided by the maximum time-step and the number of additional solutions incurred to determine voltage regulator operations. The number of additional solutions required by the binary search/time-seeking method is considerably less than the backtrack method. This would indicate that the runtime reduction of the binary search/time-seeking method could significantly out preform the backtrack method if the algorithm was implemented directly in the distribution system analysis tool. The current implementation which uses Matlab and the COM to manage solutions provided by OpenDSS is too slow to directly demonstrate the runtime reductions possible.

B. Max./Min. Voltages

The maximum and minimum voltages experienced on a circuit is another very important metric for PV interconnection studies. As the maximum time step of the variable-time-step solver increases, the chance of missing a short-duration voltage peak or valley increases. Fig. 4 shows the calculated daily voltage profiles for the point of interconnection of the modeled PV system for standard 1 s resolution analysis and the backtrack variable-time-step solver with a $t_{max,ss}$ of 30 s. The lower plot shows a 4-min period of the solution during which a backtrack event (denoted by an arrow) occurred. During the backtrack period the two voltage time-series overlap. After the back track period the variable time-step algorithm returns to large time steps. Also shown is how short-duration voltage swings are not detected in the voltage profile calculated by the variable-time-step solver with a $t_{max,ss}$ of 30 s. Still, the error of the maximum and minimum voltages for the voltage at the PV system's point of interconnection, calculated by the variable-time-step solver and traditional 1-s analysis, is effectively zero. Any error seems limited to well within the convergence tolerance of the power flow algorithm itself or stems from short-duration voltage excursions. Such excursions certainly occur but their impact in distribution planning activities is not typically of great concern thus not being able to ensure the detection of maximum and minimum voltages occurring from such events is not a great disadvantage of the variable time-step solution methods. Accurately solving for the expected operations of AVR produces accurate maximum and minimum voltages on the timeframe expected by distribution system planners completing PV interconnection impact studies.

IV. Conclusions

This paper presented variable-time-step solvers for use in advanced, complex DPV interconnection studies. Two versions of the variable-time-step solver are described and evaluated via yearlong 1-s resolution QSTS analysis of PV variability-induced automatic voltage regulation equipment operations on both the IEEE 13-node test feeder and a 3,000+ node utility feeder. The developed backtrack variable-time-step solver reduces the computational time required for such studies by 83.9% with no appreciable error and by 91.3% with acceptable error. The variable time-step solver which uses binary time search and control action time-seeking reduces computational time by 90.8%. The maximum and minimum sustained voltages calculated by the variable time-step solver methods are also accurately determined. The overall number of power flow solutions needed to complete yearlong analysis is significantly lower for the binary time search/time-seeking variable time-step method indicating that the method, if implemented directly in a distribution system analysis package, would outperform the backtrack variable time-step method.

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References

[1] M. Coddington et al., "Updating Interconnection Screens for PV System Integration," NREL Tech. Report TP-5500-54063, Feb. 2012.

[2] R. Seguin, J. Woyak, D. Costyk, J. Hambrick, and B. Mather, "High-Penetration PV Integration Handbook for Distribution Engineers," NREL Tech. Report TP-5D00-63114, Jan. 2016.

[3] R. J. Broderick et al., "Time Series Power Flow Analysis for Distribution Connected PV Generation," Sandia Report SAND2013-0537, Jan., 2013.

[4] B. Mather, "Quasi-Static Time-Series Test Feeder for PV Integration Analysis on Distribution Systems," in *Proc. IEEE Power and Energy Soc. Gener. Meet.*, San Diego, USA, Jul. 22–26, 2012.

[5] B. Mather, "Presentation: Comparison of Distribution-Connected PV Impact Studies: Steady-State and QSTS," pres. at IEEE Power and Energy Soc. Gener. Meet., Boston, USA, Jul., 17–21, 2016.

[6] C.D. Lopez, B. Idlbi, T. Stetz, and M. Braun, "Shortening Quasi-Static Time-Series Analysis of Low Voltage Network Operation with Photovoltaic Feed-In," in *Proc. Power and Energy Stud. Summit*, Dortmund, DE, Jan. 12–14, 2015.

[7] A. Selim, M. Abdel-Akher, M. M. Aly and S. Kamel, "Efficient Time Series Simulation of Distribution Systems with Voltage Regulation and PV Penetration," in *Proc. Mid. East Pwr. Sys. Conf,* Cairo, Egypt, Dec. 27-29, 2016.

[8] IEEE, PES Distribution System Analysis Subcommittees' Distribution Test Feeder Working Group, www.ewh.ieee.org/soc/pes/dsacom/testfeeders/index.html.

[9] OpenDSS – EPRI Distribution System Simulator, online resource: https://sourceforge.net/projects/electricdss/