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Modeling and Compensation Design for a Power Hardware-in-the-Loop Simulation of an AC Distribution System

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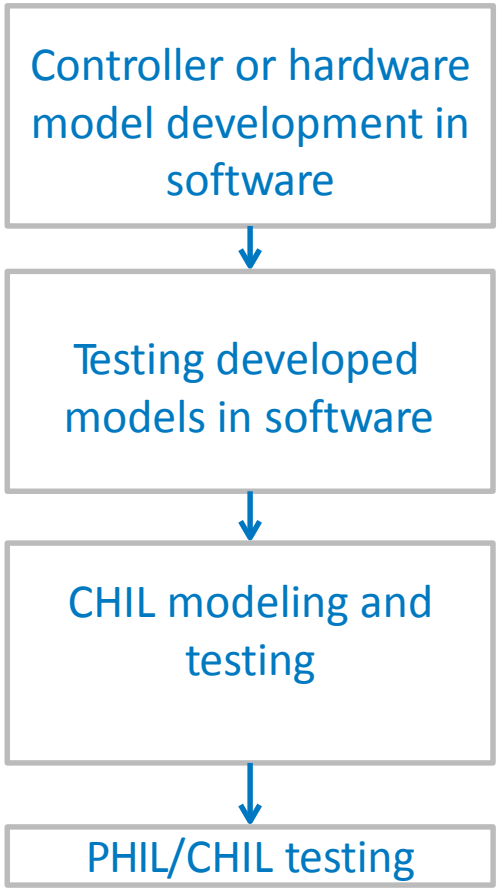
Introduction to Hardware-in-the-Loop Simulation

- Hardware-in-the-loop (HIL) testing is performed for testing and benchmarking novel controllers and power hardware.
- HIL is performed in the following industries
  - Automotive
  - Aeronautics
  - Power electronics
  - Power systems.
- Different HIL
  - Controller-hardware-in-the-loop (CHIL)
  - Power-hardware-in-the-loop (PHIL)
  - Combined.

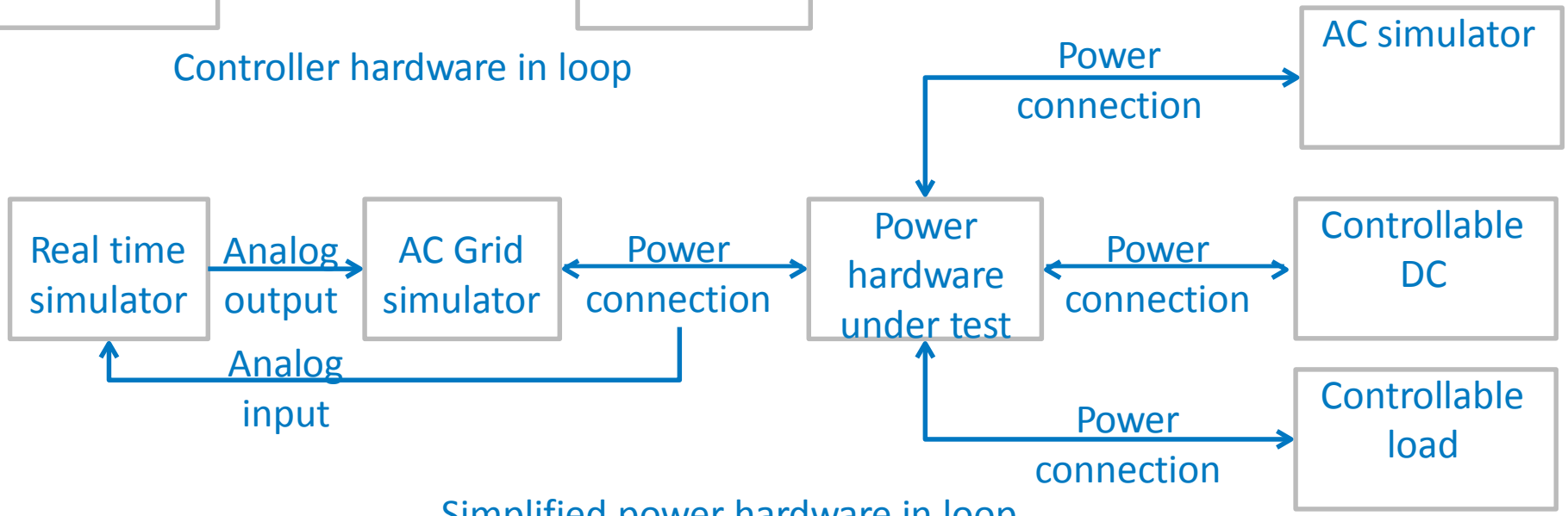


Typical controller/hardware development flow

Simplified CHIL & PHIL Setup

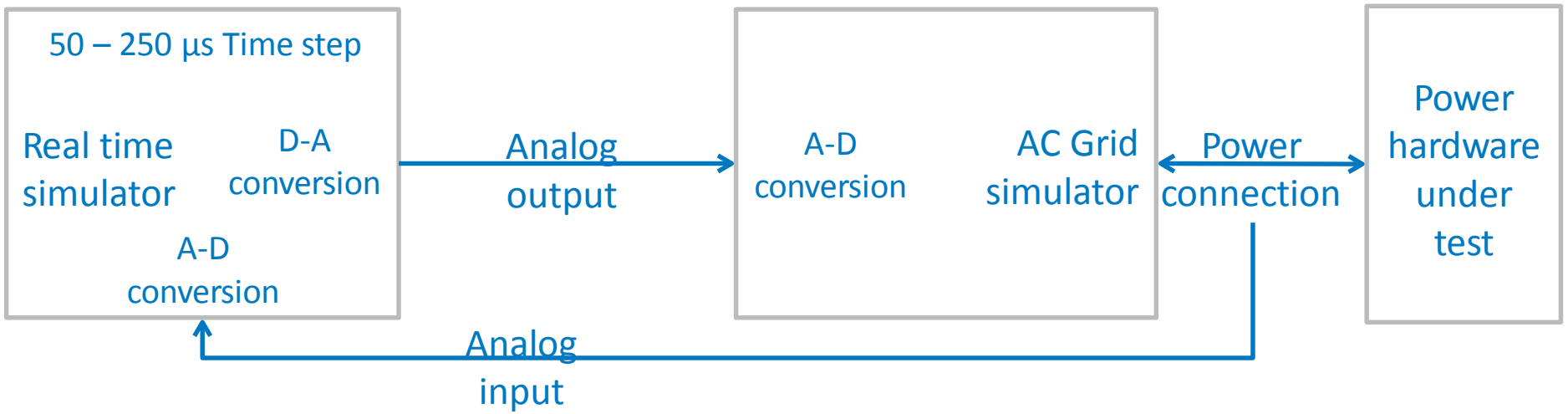
- CHIL: Simple
- PHIL: Complex and can become unstable

Controller hardware in loop



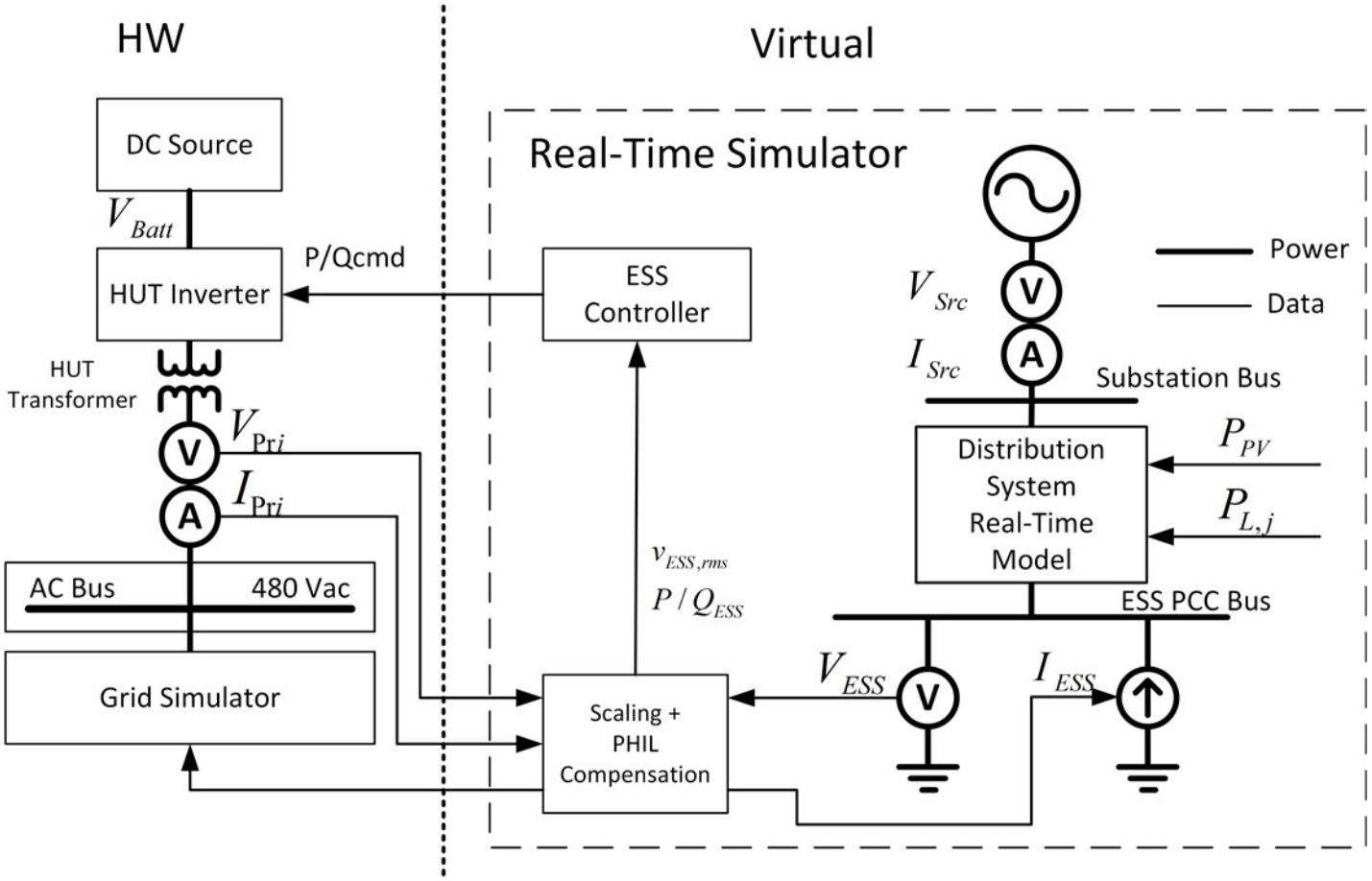
Simplified power hardware in loop

Time Delay and Error Introduced in PHIL Testing



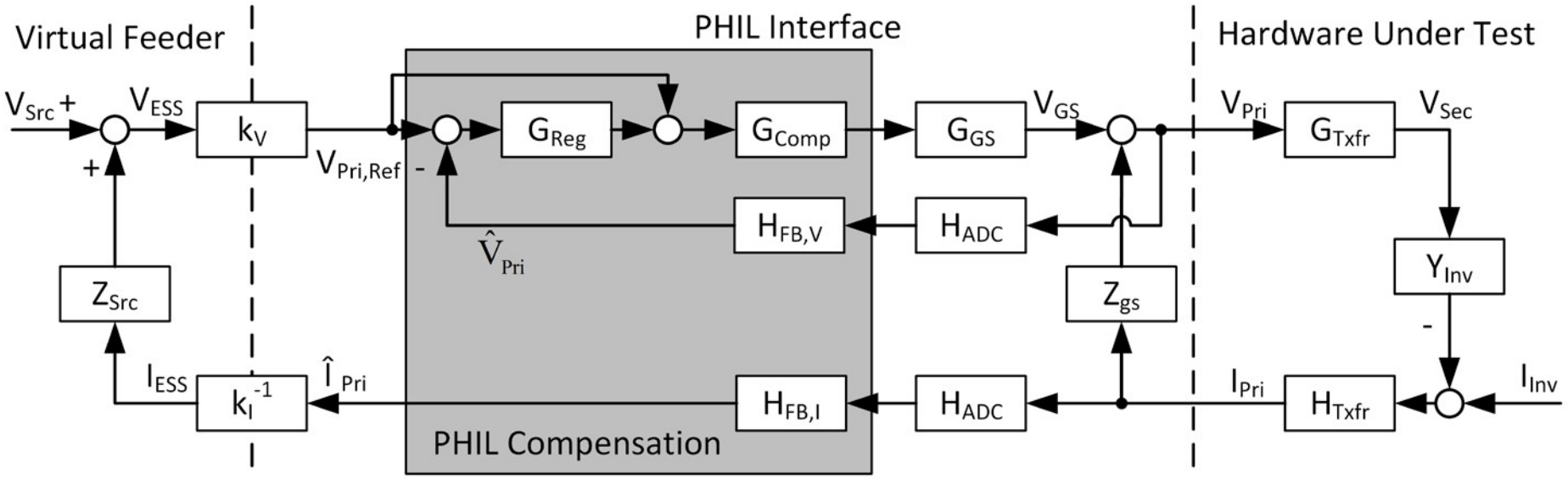
- Real time simulator runs at a time step of 50-250 µ second time step.
- Delays are introduced by analog to digital and digital to analog conversion.
- Noise is present in the signal carrier adding more error in the testing.

Modeling of Distribution System in PHIL



- HUT operates at 480 V 3-Φ, with a power rating of 450 kVA,
- Distribution feeder PCC is 12kV at 3-MVA rating.

Dynamic Modeling of PHIL Voltage and Current Loops



PHIL voltage and current loop control model

- Virtual feeder corresponds to the modeled distribution network.
- PHIL interface models the interface between RTS and power hardware. The delays and the proposed compensation are modeled here.
- Hardware under test models the hardware setup.

Modeling of Major Loop Components

- Distribution feeder model

$$V_{ESS} = V_{Src} + Z_{Src} I_{ESS}$$

- Digital to analogue and analogue-to-digital converter
  - Assumed to have unity gain. The delay introduced is modeled

$$G_{DAC} = 1 \qquad H_{ADC} = e^{-sT_{RTS}}$$

- Grid simulator – delay and a single pole filter

$$G_{GS} = \frac{V_{out}}{V_{ref}} = \frac{1}{\frac{s}{2\pi f_{GS}} + 1} e^{-sT_{GS}}$$

- Hardware under test transformer

$$G_{Txfr} = H_{Txfr} = \sqrt{3} N_{Txfr}$$

- Hardware under test inverter

$$Y_{Inv} = \frac{2}{3} s C_{Inv}$$

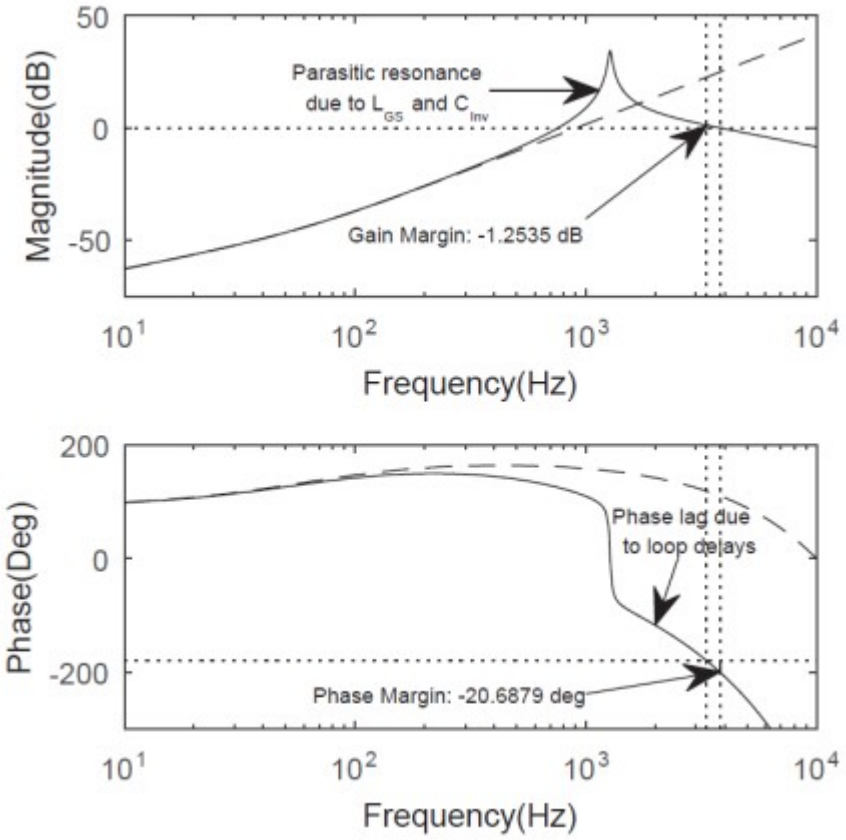
Uncompensated Stability and Performance

- Open loop transfer function of conventional VITM

$$G_{OL,VITM} = \frac{k_V k_I^{-1} Z_{Src}}{Z_L} e^{-sT_{GS}}$$

- Uncompensated ESS PHIL loop transfer function

$$G_{OL,Uncomp} = \frac{k_V k_I^{-1} Z_{Src}}{(\frac{s}{2\pi f_{GS}} + 1)(Z_L + Z_{GS})} e^{-s(T_{RTS}+T_{GS})}$$



Bode plot of PHIL current loop without compensation (solid) versus conventional VITM model

Voltage Tracking Error

- The uncompensated ESS PHIL have poor tracking at the AC fundamental frequency (60 HZ)

$$V_{Error} = \frac{1 + Z_{GS} H_{Txfr} Y_{Inv} G_{Txfr} - H_{ADC} G_{GS}}{1 + Z_{GS} H_{Txfr} Y_{Inv} G_{Txfr}} V_{Pri,Ref} - \frac{H_{ADC} Z_{GS} H_{Txfr}}{1 + Z_{GS} H_{Txfr} Y_{Inv} G_{Txfr}} I_{Inv} \quad (10)$$

- This function exhibits ~7% error under no load and ~11% under loaded conditions
- It is desirable to compensate for the voltage error to ensure that V_{pri} accurately tracks $V_{Pri,Ref}$

Illusionary Real and Reactive Power Due to PHIL Setup

- For the uncompensated PHIL loop,

$$\tilde{S}_{ESS} = P_{ESS} + jQ_{ESS} = \tilde{V}_{ESS}\tilde{I}^{*}_{ESS}$$

- Assuming unity magnitude for G_{Vff} and H_I at fundamental frequency

$$P_{ESS} = k_V^{-1}k_I^{-1}[P_{Pri}\cos\delta - Q_{Pri}\sin\delta]$$
$$Q_{ESS} = k_V^{-1}k_I^{-1}[Q_{Pri}\cos\delta + P_{Pri}\sin\delta]$$

- Where $\delta = -\angle G_{Vff}(j\omega_F) - \angle H_I(j\omega_F)$
- Introduction of the phase shift δ by the PHIL loop at the fundamental frequency skews the value of P_{ESS} and Q_{ESS}. This introduces illusionary P and Q of 8%.

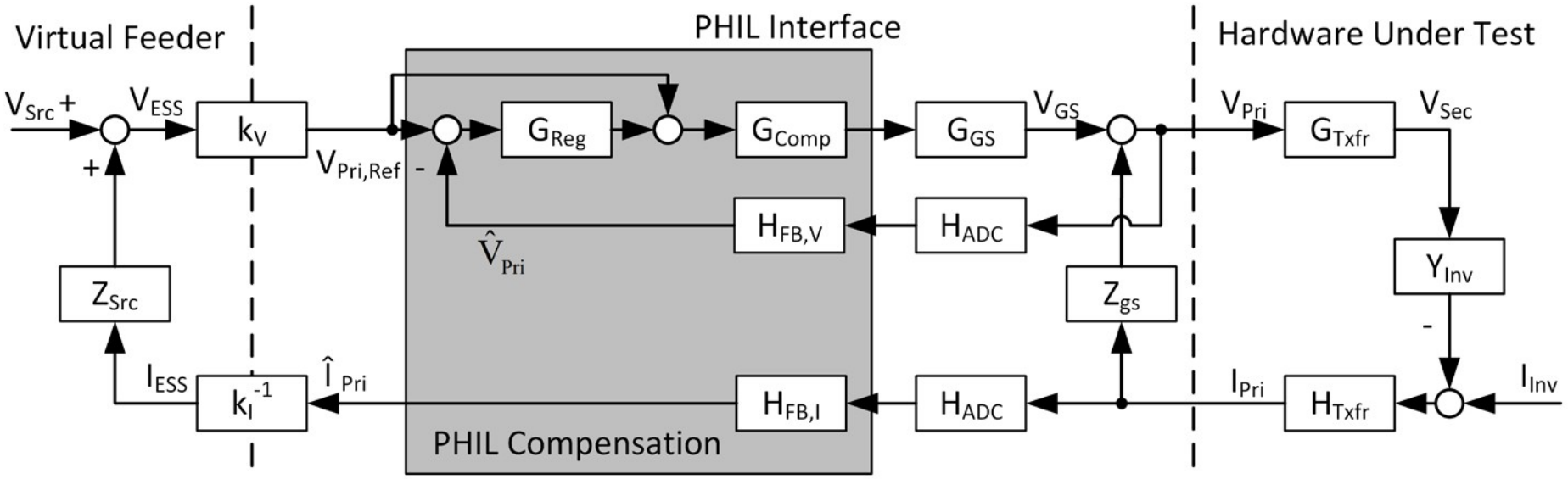
Design Requirements

- The main issues that will affect the stability and accuracy of the PHIL simulation are:
  - Instability of the PHIL current loop due to resonance and loop time delays
  - Voltage difference between measured primary voltage (V_{Pri}) and the commanded reference ($V_{Pri,Ref}$) due to the parasitic impedance Z_{GS}
  - Illusionary effect in P and Q due to the time delay
  - Parasitic resonance due to the interaction between the grid simulator inductance L_{GS} and the inverter filter capacitance C_{inv}

Proposed Compensation Method

- Forward compensator (G_{comp}) ensures stability of the current loop and addresses the resonance issue.
- Feedback filter $H_{FB,I}$ and $H_{FB,V}$ – accounts for the time delays in the interface and also eliminate the illusionary P and Q effect.
- Addition of the inner voltage regulation loop and voltage compensator G_{reg}, which will use a voltage feedback signal to enhance the voltage tracking capability

Dynamic Modeling of PHIL Voltage and Current Loops



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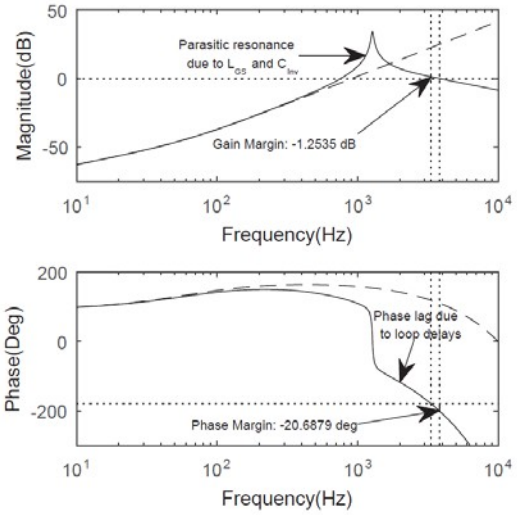
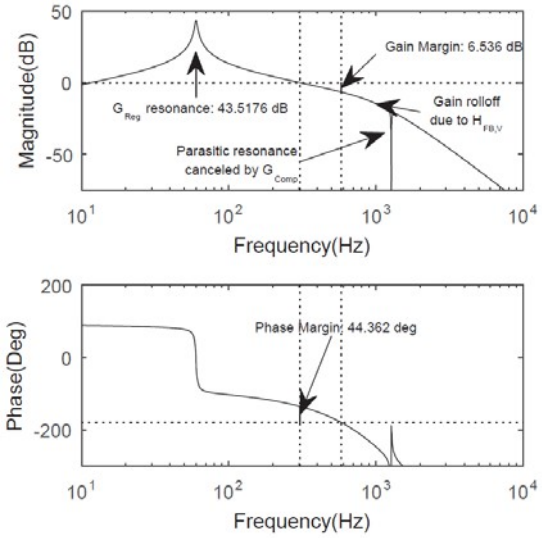
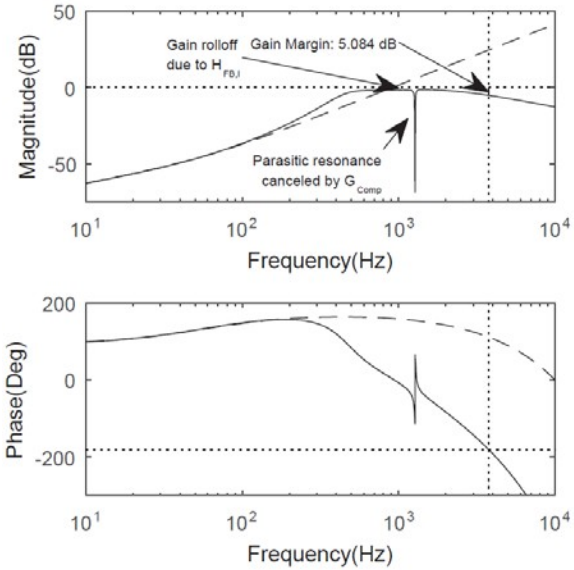
Performance



Unstable system before compensation



Open loop Bode plot of voltage tracking loop with compensation



Open loop Bode plot of PHIL current loop with compensation (solid) vs. the conventional VITM model (dashed)

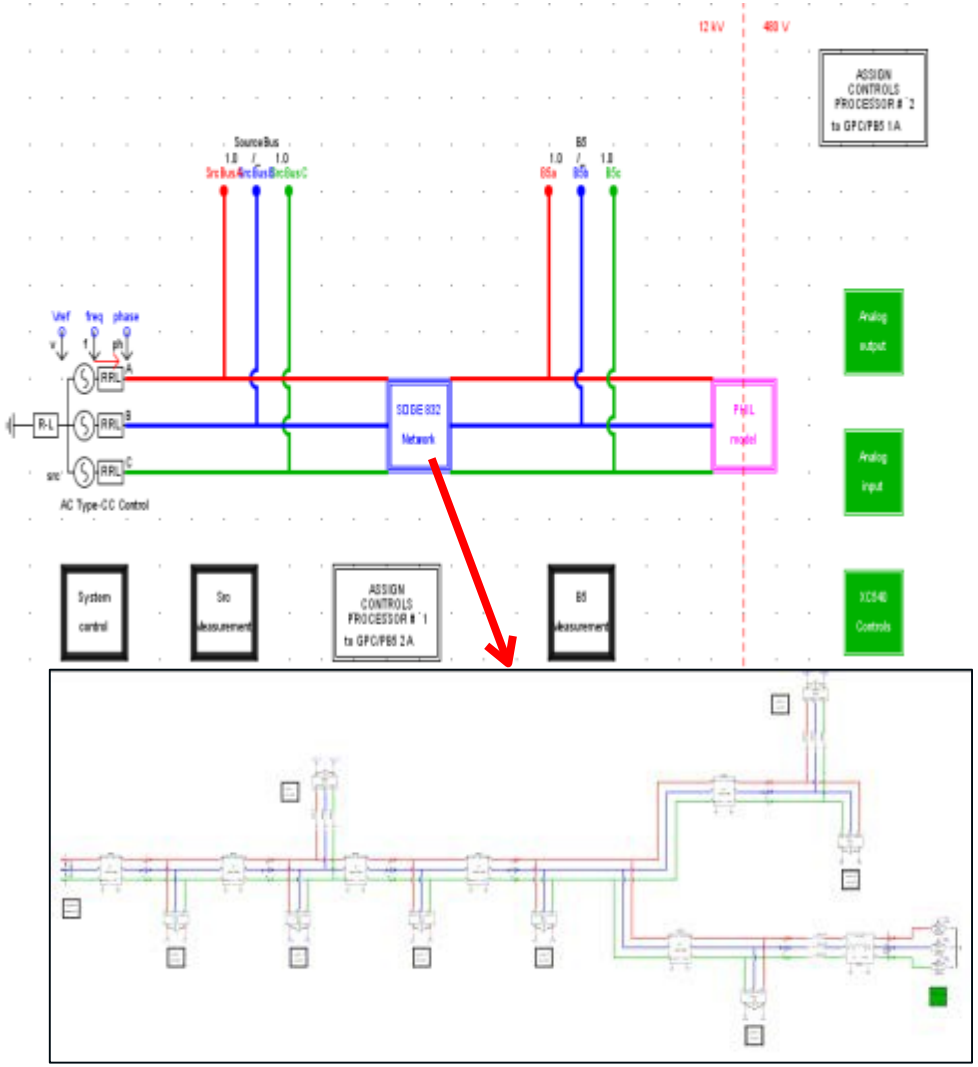
Hardware

NREL, 34513

NREL, 34526

NREL, 34519

Virtual



SDG&E CRADA: PHIL Stability and Accuracy Design

PHIL results without voltage regulation

TABLE I: Test Results for Compensated PHIL Current Loop w/o Voltage Regulation

P_{Inv}	Q_{Inv}	$k_V k_I$ Q_{ESS}	$V_{Pri,Ref}$	V_{Pri}	V_{Err}	Q_{Err}
kW	kVAr	kVAr	Vrms	Vrms	%	%
99.6	9.3	22.2	274.9	278.0	17.5	-13.4
199.8	11.0	40.5	275.0	279.3	18.3	-15.2
-102.8	-8.5	-16.2	274.7	275.6	18.8	-22.4
-205.5	-5.2	-30.6	274.6	274.0	19.2	-29.9

PHIL results with voltage regulation

TABLE II: Test Results for Compensated PHIL Current Loop w/ Voltage Regulation

P_{Inv}	Q_{Inv}	$k_V k_I$ Q_{ESS}	$V_{Pri,Ref}$	V_{Pri}	V_{Err}	Q_{Err}
kW	kVAr	kVAr	Vrms	Vrms	%	%
99.8	7.3	5.9	274.9	275.0	0.6	1.4
200.0	2.2	9.0	275.0	275.0	0.6	-3.4
-102.7	-5.6	-4.1	274.7	274.8	0.5	-3.3
-205.5	-5.0	-9.0	274.7	274.8	0.6	-7.8

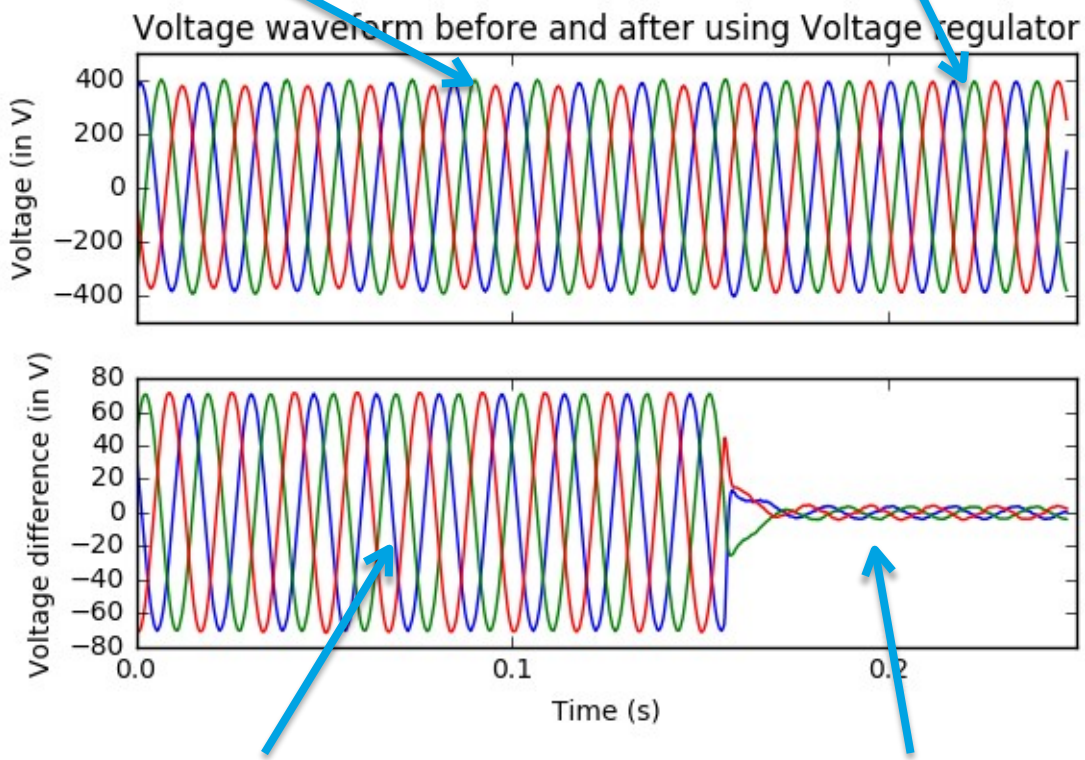
Voltage error reduced to < 1%

Reactive power error reduce to < 7%

Closed-loop PHIL Voltage Control Filter

Smoother waveforms

Uneven peak



Difference between
set point and observed voltage

After turning on voltage regulator

Summary

- Models for PHIL test setup was developed for hardware ESS inverter and simulated distribution system.
- Uncompensated PHIL loop exhibited instability under some operating conditions due to parasitic effects and loop delays.
- Compensation method based around a voltage regulation loop and forward and feedback compensators was presented.
- The proposed method was validated both analytically and experimentally to provide stable PHIL system with improved accuracy.

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