Modeling and Compensation Design for a Power Hardware-in-the-Loop Simulation of an AC Distribution System

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***Abstract*—Power hardware-in-the-loop (PHIL) simulation, where actual hardware under test is coupled with a real-time digital model in closed loop, is a powerful tool for analyzing new methods of control for emerging distributed power systems. However, without careful design and compensation of the interface between the simulated and actual systems, PHIL simulations may exhibit instability and modeling inaccuracies. This paper addresses issues that arise in the PHIL simulation of a hardware battery inverter interfaced with a simulated distribution feeder. Both the stability and accuracy issues are modeled and characterized, and a methodology for design of PHIL interface compensation to ensure stability and accuracy is presented. The stability and accuracy of the resulting compensated PHIL simulation is then shown by experiment.**

***Index Terms*—Power system simulation, Power system dynamics, Stability analysis, Power Hardware-in-the-Loop**

I. Introduction

As the penetration of power electronics and controllable devices in power distribution systems increases, it is necessary that new technologies and control methods are tested and validated under realistic conditions before they are deployed. However, realistic test conditions can be very difficult to generate in simple laboratory environments, and it is often prohibitively expensive to construct an entire demo distribution system to test a new technology. One possible approach to enable realistic testing of new power technologies is power hardware-in-the-loop (PHIL) simulation, in which an actual power hardware device or system is coupled with a real-time digital simulation of a test power system in closed loop, allowing realistic test conditions to be generated more easily.

PHIL simulation is generally accomplished by the use of a real-time simulator (RTS), grid simulator (GS), and the power hardware under test (HUT). The GS (power amplifier/controllable AC source) is used to generate the voltage signals to drive the HUT based on reference signals produced by the digital model in the RTS [1]. The power interface of a PHIL simulation introduces errors due to inherent non-idealities such as time delays, hardware bandwidth limitations, and distortions such as harmonic injections that could lead to instability issues and inaccuracy in the results [2]. Therefore, the choice of a proper interface technique is crucial for the stability of the PHIL simulation. Different PHIL interface algorithms were tested in [2] to demonstrate the relation between the interface algorithms and the stability of the PHIL simulation. Different case-specific methods for PHIL stabilization have been proposed in [3]-[5].

A stable PHIL simulation does not guarantee an accurate simulation. Feedback control has been applied in [6] to ensure accuracy by evaluating the error functions and compensating accordingly. Another method proposed in [7] uses feedback current filtering to maintain accurate results. Other methods including phase compensation [8] and impedance matching [9] have also been implemented to improve the accuracy of PHIL simulations.

This paper considers the design of the PHIL interface and compensation for a PHIL simulation constructed in the Energy Systems Integration Facility (ESIF) at the National Renewable Energy Lab (NREL). The purpose of this PHIL simulation is to assess the effect of grid-support functions performed by an inverter-interfaced energy storage system (ESS) on a test distribution feeder. The focus of this paper is on the dynamic modeling of the PHIL test system, characterization of its stability and accuracy, and the design of the interface and compensation to address the characterized stability and accuracy issues. While this compensation design is targeted to the particular PHIL test system in question, it can be generalized to apply to other similar PHIL test system designs.

II. Modeling and Characterization of a PHIL Test System for an AC Distribution System

A. PHIL Test System Under Consideration

A functional block diagram of the PHIL setup under consideration is shown in Fig. 1. The main objective of this PHIL setup is to understand the impact of an ESS on the distribution system under test.

There are three major parts of the ESS PHIL setup shown in Fig. 1. The first part (on the left) is the hardware setup with GS, HUT transformer, HUT inverter, and DC source. The second part (on the right) is the RTS, which simulates

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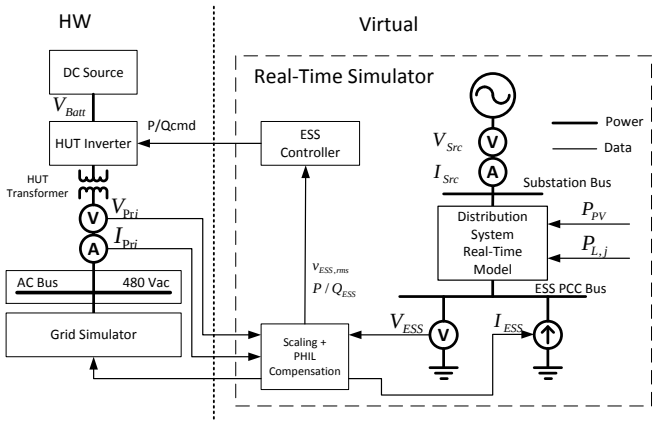

Fig. 1: Block diagram of the ESS PHIL setup

the distribution feeder under test in real time. The final part is the interface between the hardware setup and RTS, which consists of a set of signals exchanged via analog I/O and the associated signal processing and compensation.

The RTS controls the GS to ensure that the primary-side voltage V_{Pri} of the HUT transformer tracks the (scaled) voltage V_{ESS} at the distribution system point of common coupling (PCC) of the ESS inverter. The HUT inverter implements a specified grid-support function, resulting in a current injection I_{Pri} (measured at the primary side of the HUT transformer) based on measurements of voltage, power, etc. The current injection is then measured by current transformers (CT) that are interfaced to the RTS through burden resistors where it is scaled and compensated appropriately, and injected into the PCC bus of the simulated distribution feeder, thus resulting in a closed-loop interaction between the HUT and the simulated distribution feeder. The focus of this paper is the design of the PHIL interface; the details of the distribution feeder model, test conditions, and ESS inverter controller are out of scope.

The HUT system operates at $V_{Inv,Rated} = 480$ V three-phase with a power rating of $S_{Inv,Rated} = 450$ kVA, while the simulated ESS in the distribution feeder operates at $V_{ESS,Rated} = 12$ kV three-phase with a power rating of $S_{ESS,Rated} = 3$ MVA. Therefore, the following voltage and current scalings are selected (from simulation to hardware):

$$k_V = V_{Inv,Rated}/V_{ESS,Rated} \tag{1}$$

$$k_I = \frac{S_{Inv,Rated}/V_{Inv,Rated}}{S_{ESS,Rated}/V_{ESS,Rated}} \tag{2}$$

B. Dynamic Modeling of PHIL Voltage and Current Loops

Fig. 2 shows a (simplified) dynamic model of the PHIL closed-loop feedback, including the compensation and voltage regulation to be designed. While the system to be designed is three-phase, the cross-coupling between the phases is weak, and it can therefore be reasonably modeled as three identical and independent single-phase systems.

The PHIL closed-loop feedback consists of a PHIL current loop (outer loop) and a voltage regulation loop (inner loop). The diagram is divided into three sections to mirror the physical structure in Fig. 1. The "Virtual Feeder" section corresponds to the distribution network that is modeled in the RTS. The "Power Hardware" section models the hardware setup that is discussed in section II-A. The "PHIL Interface" models the interface between the RTS and the power hardware, which accounts for the signal amplification delays as well as the proposed compensation blocks that will ensure the accuracy and stability of the simulation.

C. Modeling of Major Loop Components

The *distribution feeder model* up to the PCC of the ESS is modeled using a simplified Thevenin equivalent circuit consisting of a series combination of a voltage source and an equivalent impedance of the network as seen by the PCC as shown in (3).

$$V_{ESS} = V_{Src} + Z_{Src} I_{ESS} \tag{3}$$

where $Z_{Src} = R_{Src} + sL_{Src}$ and s is the Laplace variable. Z_{Src} is the effective impedance seen by the ESS in the simulation distribution system model. In this paper, $Z_{Src} = 29.5e^{-3} + s78.2e^{-6}$ ohms.

The digital-to-analogue (DAC) and analogue-to-digital (ADC) converters of the RTS at the interface are assumed to have unity gain, but together they model the delay introduced by the RTS input/output (I/O) interface and solver. A total time delay equal to a single RTS time step ($T_{RTS} = 50\mu s$) is assumed for the RTS, and the delay is lumped into the ADC block. Therefore, $G_{DAC} = 1$ and $H_{ADC} = e^{-sT_{RTS}}$.

The *GS* converts the (low-voltage) reference signal at its input to a power voltage V_{GS}. A thorough analysis has been conducted in a previous project [10] to model and characterize the PHIL grid simulator, which determined that it can be modeled by a delay and a single pole filter:

$$G_{GS} = \frac{V_{out}}{V_{ref}} = \frac{1}{\frac{s}{2\pi f_{GS}} + 1} e^{-sT_{GS}} \tag{4}$$

where $f_{GS} = 1950$ Hz and $T_{GS} = 50\mu$sec.

The GS also has an output impedance, which results in a voltage rise proportional to load current and contributes to the difference between the measured V_{Pri} and the reference voltage signal sent to the grid simulator. We model the impedance as $Z_{GS} = R_{GS} + sL_{GS}$, where we empirically estimated $R_{GS} = 10\text{m}\Omega$ and $L_{GS} = 40\mu$H.

The *HUT transformer* is modeled as an ideal 480V Delta / 300V Wye transformer by the forward voltage (G_{Txfr}) and reverse current (H_{Txfr}) transfer functions:

$$G_{Txfr} = H_{Txfr} = \sqrt{3} N_{Txfr} \tag{5}$$

where $N_{Txfr} = 300/480$ is the transformer turns ratio.

Finally, the *HUT inverter* is modeled as a Norton equivalent composed of a current source I_{Inv} (representing the regulated inverter current) in parallel with an admittance (its three phase Wye-connected filter capacitance):

$$Y_{Inv} = \frac{2}{3} sC_{Inv}. \tag{6}$$

where $C_{Inv} = 500\mu$F.

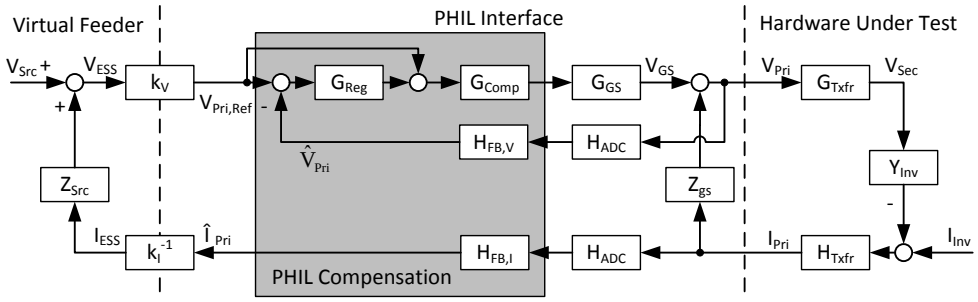

Fig. 2: Block diagram of the PHIL voltage and current loop model

D. Uncompensated Stability and Performance

The uncompensated interface is composed of only the current loop of Fig. 2 while setting $G_{Reg} = 0$ and $G_{Comp} = H_{FB,I} = 1$ where $H_{FB,I}$ is the current feedback compensation. This scheme is equivalent to the conventional voltage-type ideal transformer model (VITM) [2] that assumes that amplification time delay is the only source of error. An open-loop Bode diagram of both the VITM loop and the expanded uncompensated PHIL loop is shown in Fig. 3.

The open-loop transfer function of the conventional VITM (ignoring Z_{GS} and H_{ADC} is:

$$G_{OL,VITM} = \frac{k_V k_I^{-1} Z_{Src}}{Z_L} e^{-sT_{GS}} \tag{7}$$

where T_{GS} is the GS amplification delay and $Z_L = V_{Pri}/I_{Pri} = (G_{Txfr}Y_{Inv}H_{Txfr})^{-1}$ is the equivalent impedance of the HUT. It has been shown [2] that the ideal voltage-type ITM model with non-zero delay will be stable if $|k_V k_I^{-1} Z_{Src}(j\omega)/Z_L(j\omega)| < 1 \,\forall\, \omega$.

However, in contrast to the conventional VITM model, when Z_{GS} and delays are considered, the uncompensated ESS PHIL loop has the following open-loop transfer function:

$$G_{OL,Uncomp} = \frac{k_V k_I^{-1} Z_{Src}}{(\frac{s}{2\pi f_{GS}} + 1)(Z_L + Z_{GS})} e^{-s(T_{RTS}+T_{GS})} \tag{8}$$

In the case of the ESS PHIL loop, the phase delay $e^{-s(T_{RTS}+T_{GS})}$ drops off faster than the magnitude of $Z_L + Z_{GS}$. This leads to a negative gain margin (as shown in Fig. 3), resulting in the instability of the uncompensated ESS PHIL loop.

In addition, the instability of the PHIL loop is closely related to the presence of a parasitic impedance in the hardware. The equivalent impedance $Z_L + Z_{GS}$ causes a resonance due to the interaction between the inverter filter capacitance C_{Inv} on the secondary side and the grid simulator inductance L_{GS}. The peak frequency of this resonance can be calculated as follows:

$$f_{Resonance} \approx \frac{1}{2\pi N_{Txfr}\sqrt{2L_{GS}C_{Inv}}} \approx 1.27kHz \tag{9}$$

This resonance is parasitic because it is due to the grid simulator impedance Z_{GS}, which does not exist in the conventional

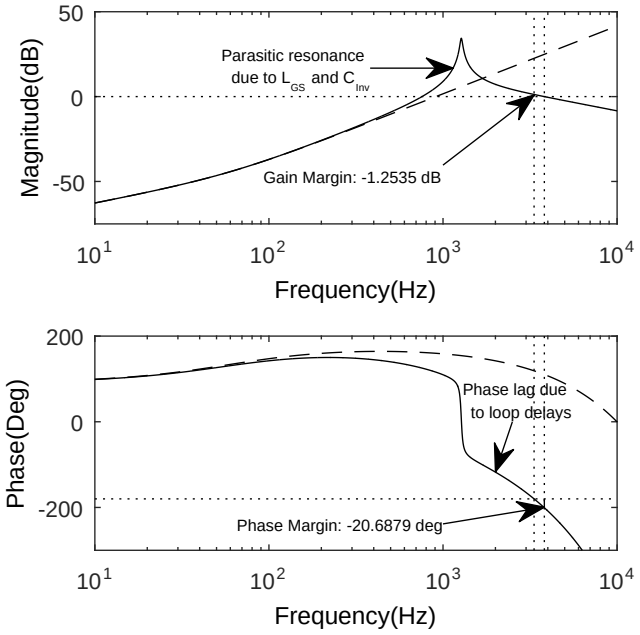

Fig. 3: Bode plot of PHIL current loop without compensation (8) (solid) vs. the conventional VITM model (7) (dashed)

VITM model. The resonance causes a high gain near the phase crossover of the uncompensated PHIL loop (at about 2.9 kHz) and contributes to the observed instability.

E. Voltage Tracking Error

In addition to the instability issue, the uncompensated ESS PHIL loop is found to have poor voltage tracking at the AC fundamental frequency $\omega_F = 2\pi 60$ rad/sec. The primary-side voltage V_{Pri} in hardware can exhibit significant error when compared to the scaled ESS voltage $V_{Pri,Ref} = k_V V_{ESS}$ due to the grid simulator delay and voltage drop across the grid simulator impedance Z_{GS}. The voltage tracking error is:

$$V_{Error} = \frac{1 + Z_{GS}H_{Txfr}Y_{Inv}G_{Txfr} - H_{ADC}G_{GS}}{1 + Z_{GS}H_{Txfr}Y_{Inv}G_{Txfr}} V_{Pri,Ref} - \frac{H_{ADC}Z_{GS}H_{Txfr}}{1 + Z_{GS}H_{Txfr}Y_{Inv}G_{Txfr}} I_{Inv} \tag{10}$$

This transfer function exhibits significant error ($\sim 7\%$) even under no-load conditions ($I_{Inv} = 0$). However, under loaded conditions the error can be as large as $\sim 11\%$ of the rated voltage. This voltage error on the HUT results in significant closed-loop error when modeling the ESS system as a whole. It is therefore desirable to compensate for the voltage error to ensure that V_{Pri} accurately tracks $V_{Pri,Ref}$.

F. Illusionary Real and Reactive Power Due to PHIL Loop Effects

Because the objective of the PHIL simulation is to assess the effect of real and reactive power injections from the ESS on the simulated feeder, any error introduced in the ESS real and reactive power measurement will directly produce PHIL simulation errors. It is observed that the uncompensated PHIL exhibits a significant loop delay from the model voltage command to the resulting measured current, which creates an "illusionary P and Q" effect as described below.

The complex power injection $\tilde{S}_{ESS}$ of the simulated ESS in the real-time model is calculated as follows:

$$\tilde{S}_{ESS} = P_{ESS} + jQ_{ESS} = \tilde{V}_{ESS}\tilde{I}^*_{ESS} \tag{11}$$

where $\tilde{V}_{ESS}$, $\tilde{I}_{ESS}$ are the complex-valued fundamental voltage and current phasors of the ESS, respectively, and * indicates the complex conjugate. The goal of the PHIL simulation is that

$$\tilde{S}_{ESS} \rightarrow k_V^{-1}k_I^{-1}\tilde{S}_{Pri} = k_V^{-1}k_I^{-1}(P_{Pri} + jQ_{Pri}), \tag{12}$$

that is, P_{ESS} and Q_{ESS} should track a scaled version of the actual primary-side inverter complex power.

It is observed from Fig. 2 that for the uncompensated PHIL loop, $\tilde{V}_{PCC} = k_V^{-1}G^{-1}_{Vff}(s)V_{Pri}$ and $\tilde{I}_{ESS} = k_I^{-1}H_I(s)I_{Pri}$, where $G_{Vff}(s)$ and $H_I(s) = H_{ADC}(s)H_{FB,I}$ are the transfer functions from $V_{Pri,Ref}$ to V_{Pri} and from I_{Pri} to $\hat{I}_{Pri}$ from Fig. 2, respectively. Substituting into (11) and simplifying:

$$\tilde{S}_{ESS} = k_V^{-1}k_I^{-1}G^{-1}_{Vff}(j\omega_F)H^*_I(j\omega_F)\tilde{S}_{Pri} \tag{13}$$

for the uncompensated PHIL loop. Assuming unity magnitude for G_{Vff} and H_I at the fundamental frequency and splitting (13) into its real and reactive components:

$$P_{ESS} = k_V^{-1}k_I^{-1}[P_{Pri}\cos\delta - Q_{Pri}\sin\delta] \tag{14}$$

$$Q_{ESS} = k_V^{-1}k_I^{-1}[Q_{Pri}\cos\delta + P_{Pri}\sin\delta] \tag{15}$$

where $\delta = -\angle G_{Vff}(j\omega_F) - \angle H_I(j\omega_F)$ is the delay angle due to the PHIL loop. Observe from (14) and (15) that the introduction of the phase shift δ by the PHIL loop at the fundamental frequency skews the values of P_{ESS} and Q_{ESS}. As a result, P_{ESS} and Q_{ESS} are not simply a scaled version of the desired P_{Pri} and Q_{Pri}. In particular, the second terms of (14) and (15) respectively represent an "illusionary real and reactive power," which is proportional to the sine of the phase delay δ. In the PHIL test system constructed in ESIF, the value of $\delta \approx 4.2\,\text{deg}$, yielding "illusionary" P and Q terms of nearly 8%. This will directly introduce errors in the PHIL simulation of the effects of the ESS on the feeder. Therefore, the PHIL phase shift δ should be compensated to eliminate this error.

III. Compensation Design

A. Identifying Design Requirements

This section will discuss the design process that is followed to ensure the stability and accuracy of the PHIL simulation. Section II showed the issues in the PHIL simulation if performed without compensation. The main issues that could affect the stability and accuracy of the simulation as shown from the uncompensated analysis in section II are summarized below:

1) Parasitic resonance that exists due to the interaction between the grid simulator inductance L_{GS} and the inverter filter capacitance C_{Inv}.
2) Instability of the PHIL current loop due to the resonance and the loop time delays.
3) Voltage difference between the measured primary voltage (V_{Pri}) and the commanded reference ($V_{Pri,Ref}$) due to the parasitic impedance Z_{GS}.
4) Illusionary effect in P and Q due to the time delays described in section II-F.

The above issues necessitate the addition of compensation to achieve stability and accuracy. The proposed compensation method consists of the following:

1) Forward compensator (G_{Comp}) that ensures the stability of the current loop and addresses the resonance issue.
2) Feedback filters, $H_{FB,I}$ and $H_{FB,V}$, which will account for the time delays in the interface and also eliminate the illusionary P and Q effect.
3) Addition of an inner voltage regulation loop and voltage compensator G_{reg}, which will use a voltage feedback signal to enhance the voltage tracking capability.

The described compensation design is illustrated in the shaded block in Fig. 2.

B. Design of the Compensator Blocks

1) Forward Compensator (G_{Comp}): The forward compensator G_{Comp} is a simple notch filter with moderate damping that is used to eliminate the parasitic resonance. While the resonance can't be physically eliminated from the setup because it is produced by the interaction in hardware, a notch filter in the forward voltage path will ensure that the PHIL model doesn't excite this resonance (or amplify such excitation). The notch frequency is equal to the parasitic resonance frequency, which can be calculated using (9).

2) Voltage Regulator Compensation (G_{Reg}): The voltage compensation G_{Reg} in the voltage loop regulates the error between the voltage feedback signal of the measured voltage V_{Pri} in hardware and the reference signal $V_{Pri,Ref} = k_V V_{ESS}$ produced by the software model. This compensator accounts for the voltage drop across the parasitic impedance Z_{GS}. G_{Reg} is a resonant controller at the fundamental frequency ω_F regulating the line-to-neutral voltage as described in [11]. The resonant compensator is chosen because the primary frequency of interest is the fundamental frequency.

The cutoff frequency ω_C of the resonant compensator should have a width equal to the maximum frequency deviation from the nominal AC frequency. In this case, ω_C is selected such that $\omega_C = 2\pi(0.5)$ rad/sec for a 0.5 Hz frequency deviation. The resonance gain k_R should be selected to ensure that the voltage open-loop gain is sufficient to achieve the target regulation at the fundamental frequency. In this model, $k_R = 150$ is selected in order to achieve a gain greater than 40dB at ω_F. This reduces the voltage error to $< 1\%$ of its uncompensated value.

3) Current Feedback Filtering ($H_{FB,I}$): The current feedback filter $H_{FB,I}$ stabilizes the PHIL current loop by attenuating unsafe frequencies from the PHIL current feedback. Because the PHIL loop introduces delays in the open-loop transfer function, it is necessary to introduce a gain rolloff at high frequencies to ensure that they do not result in a negative gain margin. Following [7], a low-pass filter $H_{FB,I}$ is introduced in the current feedback path to attenuate such frequencies. To ensure a satisfactory gain margin of the PHIL current loop, $H_{FB,I}$ is selected as a second order Butterworth filter at $\omega_{FB,I} = 2\pi 800$ rad/sec. While this limits the bandwidth of the PHIL simulation, it ensures that attenuation is achieved even at the hardware resonant frequency $f_{Resonant} \approx 1.27kHz$. This ensures that stability is achieved even if the notch filter G_{Comp} is not exactly aligned with the hardware resonance.

4) Voltage Feedback Filtering ($H_{FB,V}$): Finally, it is desired that the ESS emulated complex power $\tilde{S}_{ESS}$ tracks the scaled primary-side voltage as shown in (12). In particular, the PHIL loop must be compensated so as to eliminate the "illusionary power" that appears as a result of the PHIL loop delay as shown in (14) and (15). As shown below, this can be accomplished by ensuring that the voltage feedback path has the same delay as the current feedback path.

If the voltage regulation loop ensures good voltage tracking at the fundamental frequency, then $V_{Err} \approx 0$. This (from Fig. 2) implies that $\tilde{V}_{ESS} = k_V^{-1} H_V(j\omega_F)\tilde{V}_{Pri}$, where $H_V(s) = H_{FB,V}H_{ADC}$ is the transfer function of the path from V_{Pri} to $\hat{V_{Pri}}$. Substituting into (11):

$$\tilde{S}_{ESS} = k_V^{-1}k_I^{-1}H_V(j\omega_F)H_I^*(j\omega_F)\tilde{S}_{Pri} \qquad (16)$$

for the compensated PHIL loop. Assuming that the gain of the voltage and current feedback paths is unity at the fundamental frequency:

$$\tilde{S}_{ESS} = k_V^{-1}k_I^{-1}[\angle H_V(j\omega_F) - \angle H_I(j\omega_F)]\tilde{S}_{Pri}, \qquad (17)$$

where $\angle H_V(j\omega_F)$ and $\angle H_I(j\omega_F)$ are the phase shifts of the voltage and current feedback paths, respectively, at the fundamental frequency ω_F.

A selection of $H_{FB,V} = H_{FB,I}$ ensures that $\angle H_V(j\omega_F) = \angle H_I(j\omega_F)$, resulting in

$$\tilde{S}_{ESS} = k_V^{-1}k_I^{-1}\tilde{S}_{Pri}, \qquad (18)$$

that is, ideal tracking of ESS complex power to the actual primary-side power has been achieved. Conceptually, this is because V_{ESS} and I_{ESS}, while slightly delayed from the hardware V_{Pri} and I_{Pri}, nevertheless have the same phase relationship with each other as do V_{Pri} and I_{Pri} due to the equal delay of the voltage and current feedback paths. Thus, the selection $H_{FB,V} = H_{FB,I}$ ensures the desired complex power tracking capability in (12).

C. Performance of the Compensated PHIL Test System

Fig. 4 and Fig. 5 show the open-loop Bode diagrams of the voltage and PHIL (current) loops, respectively, with the above-designed compensators G_{Reg}, G_{Comp}, and $H_{FB,V} = H_{FB,I}$ in place. Notice that in both diagrams, the parasitic resonance due to the interaction of L_{GS} with C_{Inv} has been compensated by the notch filter G_{Comp}. In addition, both Bode diagrams show gain rolloff at frequencies above $\omega_{FB,V} = \omega_{FB,I}$ due to the low-pass filters $H_{FB,V}$ and $H_{FB,I}$, producing positive gain margin (and thus stability) for both loops. Finally, the resonant compensator G_{Reg} produces a gain > 40 dB at the fundamental frequency ω_F, resulting in a fundamental frequency tracking error of less than 1%.

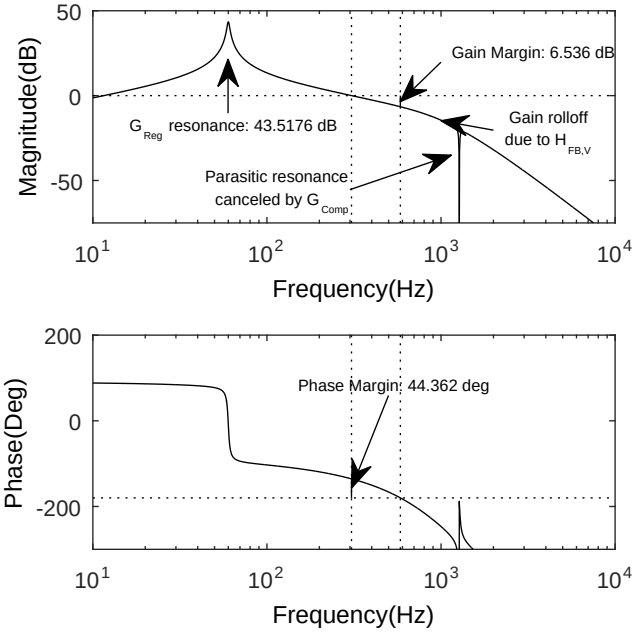

Fig. 4: Open-loop Bode plot of voltage tracking loop with compensation

IV. Experimental Results

To validate the stability and performance issues characterized in Section II and the compensation design in Section III, the PHIL simulation system in Fig. 1 was constructed and simulated both with and without compensation.

First, it was verified that the uncompensated PHIL system exhibits instability at the maximum $Z_{Src} = 29.5e^{-3} + j\omega_F 78.2e^{-6}$. When the uncompensated PHIL current loop was enabled, the measured voltage and frequency exhibited a strong high-frequency oscillation at 1414 Hz (near the unstable gain crossover predicted by the model). This tripped the inverter overcurrent protection after a few seconds of operation.

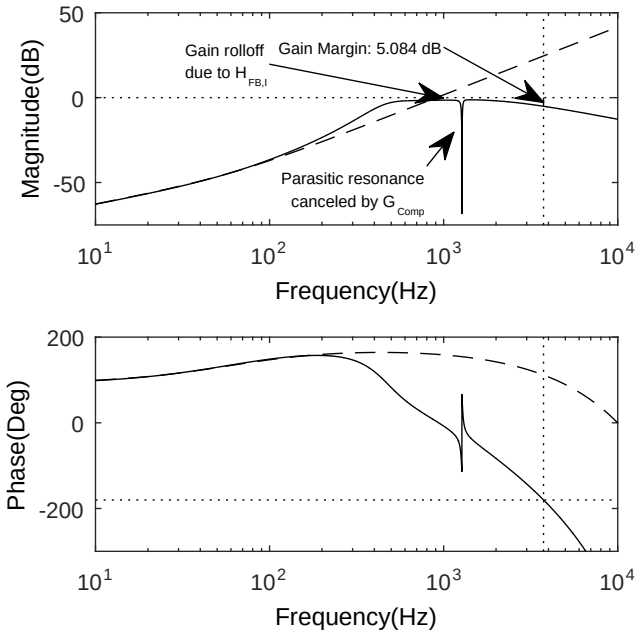

Fig. 5: Open-loop Bode plot of PHIL current loop with compensation (solid) vs. the conventional VITM model (7) (dashed).

Then, the addition of the forward compensator G_{Comp} and the current feedback filter $H_{FB,i}$ (while leaving $G_{Reg} = H_{FB,V} = 0$) is considered. This compensation of the PHIL current loop is sufficient to stabilize it, but does not correct the voltage tracking and illusory P/Q issues. The PHIL loop was activated and the ESS inverter stepped through several different values of inverter real power command, with the results shown in Table I below. Notice that while the PHIL loop has been stabilized, the voltage tracking is still poor and the illusory Q error is still significant.

TABLE I: Test Results for Compensated PHIL Current Loop w/o Voltage Regulation

$\mathbf{P_{Inv}}$	$\mathbf{Q_{Inv}}$	$\mathbf{k_V k_I}$ $\mathbf{Q_{ESS}}$	$\mathbf{V_{Pri,Ref}}$	$\mathbf{V_{Pri}}$	$\mathbf{V_{Err}}$	$\mathbf{Q_{Err}}$
kW	kVAr	kVAr	Vrms	Vrms	%	%
99.6	9.3	22.2	274.9	278.0	17.5	-13.4
199.8	11.0	40.5	275.0	279.3	18.3	-15.2
-102.8	-8.5	-16.2	274.7	275.6	18.8	-22.4
-205.5	-5.2	-30.6	274.6	274.0	19.2	-29.9

Finally, we apply the voltage regulator G_{Reg} and the voltage feedback filter $H_{FB,V}$, thus regulating the hardware voltage V_{Pri} to track the reference $V_{Pri,Ref}$ and repeat the previous test (results shown in Table II). Notice that with the application of the voltage regulation loop with $H_{FB,V} = H_{FB,I}$, then the voltage error is significantly reduced, achieving the target regulation of $< 1\%$ error. Finally, the illusory Q error has been reduced from as much as 25% of P to $< 8\%$, a reduction of a factor of 3. These results validate that not only did the proposed compensation stabilize the (previously unstable) PHIL loop, but it also significantly increased accuracy both in voltage and power tracking between the hardware and simulated subsystems.

TABLE II: Test Results for Compensated PHIL Current Loop w/ Voltage Regulation

$\mathbf{P_{Inv}}$	$\mathbf{Q_{Inv}}$	$\mathbf{k_V k_I}$ $\mathbf{Q_{ESS}}$	$\mathbf{V_{Pri,Ref}}$	$\mathbf{V_{Pri}}$	$\mathbf{V_{Err}}$	$\mathbf{Q_{Err}}$
kW	kVAr	kVAr	Vrms	Vrms	%	%
99.8	7.3	5.9	274.9	275.0	0.6	1.4
200.0	2.2	9.0	275.0	275.0	0.6	-3.4
-102.7	-5.6	-4.1	274.7	274.8	0.5	-3.3
-205.5	-5.0	-9.0	274.7	274.8	0.6	-7.8

V. Conclusions

In this paper, models for a PHIL test setup was developed for a hardware ESS inverter and simulated distribution system. The uncompensated PHIL loop exhibited instability under some operating conditions due to parasitic effects and loop delays. In addition, accuracy errors due to poor voltage tracking and loop delays were characterized. A compensation method based around a voltage regulation loop and forward and feedback compensators was presented, which was validated both analytically and experimentally to result in both stabilization of the PHIL system and improved accuracy with respect to voltage and power measurements.

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