Development of Application Function Blocks for Power-Hardware-in-the-Loop Testing of Grid-Connected Inverters

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Development of Application Function Blocks for Power-Hardware-in-the-Loop Testing of Grid-Connected Inverters

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***Abstract*—This paper presents standard Application Function Blocks (AFBs) for Power-Hardware-In-the-Loop (PHIL) testing of grid-connected inverters. The main objective is to develop standard AFBs that can be used as an interface between PHIL simulation and hardware. A critical feature of the AFBs is the ability to be reused and reconfigured with minimal effort for various PHIL tests. The PHIL interface includes five AFBs: power amplifier protection, PHIL interfacing compensation, analog output conditioning, analog input conditioning, and device under test (DUT) energy generation model. The design and development of each AFB is presented in detail for PHIL researchers. A test procedure is provided to aid in replicating the work and to guarantee safe operation. Experimental results of testing the battery and PV inverters demonstrate the effectiveness of the developed AFBs. A discussion on the reusability and reconfigurability of AFBs is presented, showing the value of using standard AFBs for accelerating the PHIL test.**

***Index Terms*—application function block, grid-connected inverter, power-hardware-in-the-loop (PHIL), test procedure.**

I. Introduction

Power-hardware-in-the-loop (PHIL) has been increasingly used as an important test and evaluation step for integrating inverters into electric grids prior to installation in the field [1], [2]. Extensive research regarding PHIL testing of grid-connected inverters has been reported in the literature, including the design and development of the PHIL test setup, the evaluation of grid-tied inverters' functionalities and impacts, and the development of interface algorithms for achieving stability and accuracy of the PHIL platform [3]–[6]. In particular, the stability and accuracy of the PHIL platform has been a common problem and challenging issue for a long time; thus, continuous efforts and research have been devoted to developing interface algorithms to improve upon this [7].

The works presented in the literature exhibit promising solutions to compensate for the errors in the PHIL platform caused by inherent nonidealities, such as time delays, sensing errors, nonlinearities, and hardware bandwidth limitations [8]; however, there is a need to harmonize various solutions into a standard framework that provides a general solution for various PHIL test beds and that can be reused with minimal modifications to avoid extra effort. A good way to do this is by using application function blocks (AFBs). AFBs are model-based and can be developed as a standard library component, thus achieving satisfactory reusability and reconfigurability for various platforms [9]. Because of the software flexibility of the PHIL simulation, appropriate functions can be easily implemented in the digital real-time simulator (DRTS) to preprocess the reference signal before sending it to the power amplifier [7]. Therefore, this paper aims to develop standard AFBs for use in DRTS for the PHIL interface to test grid-connected inverters. The PHIL AFB library is separated into five AFBs that will be presented in detail in this paper.

The contribution of this paper is to (1) develop and discuss standard AFBs for PHIL that can be used and reconfigured with minimum effort to test various devices; and (2) provide detailed test procedures for start-up, testing, and shutdown to aid in the replication of work and to guarantee safe operation and prevent hardware damage.

II. PHIL Interface AFBs Overview

The proposed AFBs for the PHIL can be divided into five categories, as shown in Fig. 1: AFB#1 Power Amplifier Protection, AFB#2 PHIL Interfacing Compensation, AFB#3 Analog Output Conditioning, AFB#4 Analog Input Conditioning, and AFB#5 DUT Energy Generation Model.

AFB#1 Power Amplifier Protection provides signal monitoring and protection as well as signal selection between simulated and zero reference signals. A manual selector switch is used to select between the measured point-of-common-coupling (PCC) voltage, *v1*, and the zero voltage reference, *v0*, as shown in Fig. 2. The root mean square (RMS) magnitude and frequency are measured for signals *v1*, *v4*, *v6*, and *i3* to verify system stability. For additional protection, instantaneous voltage magnitude is also measured for *v1*. If the measured signals are within acceptable limits, then *v1* will be selected by the control logic and output as signal *v2*. If any of the measured signals are not within the acceptable limits, then the zero voltage reference *v0* will override *v2* and be output as signal *v2*. AFB#1 is also used to switch between local current injection and the measured feedback current, *i2*. The selected current signal is then output from the AFB and injected into the model as signal *i3*.

The purpose of AFB#2 PHIL Interfacing Compensation is to enhance the measured PCC voltage *v2*. This is accomplished by applying a series of signal processing function blocks including, but not limited to, feedback control and notch

filtering. The feedback signal *v6* (measured PHIL grid voltage) is sent to the signal processing blocks to achieve closed-loop control. The modified and compensated voltage is then sent out of the AFB as signal *v3* for further processing.

AFB#3 Analog Output Conditioning accepts simulated power-line-level signals and scales them to appropriate low-voltage signals that are sent to the PHIL devices. These signals are also fine-tuned and attenuated using factors such as DC offset and rate limiters. Signal *v3*, the simulated PCC voltage, is scaled and fine-tuned in AFB#3 before being sent to the AC power amplifier as signal *v4*. Likewise, control reference signals *Voc* and *Idc* are scaled and calibrated before being sent to the controllable DC source.

AFB#4 Analog Input Conditioning accepts feedback signals from the field and scales and fine-tunes them for use within the simulation. These signals may be filtered using low-pass filters, or further signal processing functions may be applied before being output from the AFB. The measured DC voltage at the DUT terminals *Vdcin1* is processed in this block and output as *Vdcin*. The AC current and voltage feedback signals *i1* and *v5*, which are measured between the DUT and the power amplifiers, are processed in this block as well and output as *i2* and *v6*.

The purpose of AFB#5 DUT Energy Generation Model is to simulate and control the DC energy source connected to the terminals of the DUT. Control references for the DUT (e.g., active and reactive power references, P_{ref} and Q_{ref}) may also be generated in this block. In the case of a photovoltaic (PV) inverter, this AFB would simulate the PV array I-V characteristics; and for a battery energy storage inverter, this would simulate the dynamics of a battery system. These simulations are then used to control the DC source used for PHIL testing. For example, the open-circuit voltage *Voc* is calculated based on PV array circuit parameters and sent to the DC source. Additionally, the feedback signal *Vdcin* is used by AFB#5 to generate the commanded current *Idc* based on the I-V characteristics of the PV array. These signals are output by the AFB for further processing by AFB#3 and then sent to the controllable DC source.

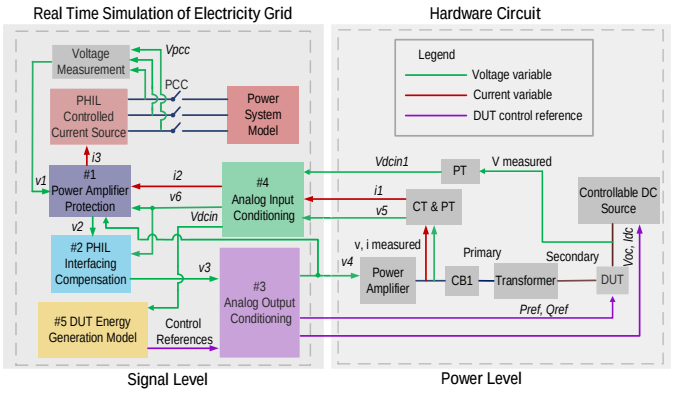

Fig. 1. Schematic diagram of the implemented PHIL simulation.

To test different devices, major changes need to be made in AFB#1 and AFB#5 because these relate to the dynamics/characteristics of the DUT. Small changes might be needed for the rest of AFBs. The standardized framework shown in Fig. 1 interfaces hardware and simulation using the ideal transformer method, but it can be adapted with some changes to other PHIL methods, such as damping impedance method. The advantage of this framework is that it can be reused extensively to test various devices. More importantly, this PHIL interface framework can achieve good stability and accuracy, as proved in [10].

III. Design and Development of AFBs for PHIL Interface

To develop the AFBs for the PHIL interface, specific requirements should be defined. As outlined in [7], the design requirements are categorized from the system point of view (including the control architecture, execution logic, and AFB dependencies) and from the point of view of individual AFBs (including the embedded algorithm, inputs and outputs, parameters and settings, and timescale). Because the AFBs for the PHIL interface support only a single purpose rather than complex industrial automation processes, and because all AFBs will be developed in a DRTS, the design requirements can be simplified, including the embedded algorithm, parameters, and settings.

A. AFB#1 Power Amplifier Protection

Even though the power amplifier has built-in protection functions, such as overcurrent and overvoltage protection, software protection in the DRTS is also necessary to prevent the amplification of harmful waveforms. Waveforms with high harmonic content or operating at incorrect frequencies can damage the power amplifiers and/or the DUT. The AFB for power amplifier protection is shown in Fig. 2. It includes two sub-AFBs: #1.1 Power Amplifier Protection and #1.2 Injection Current Generation.

Sub-AFB#1.1 generates the voltage reference *v2* based on the selection from the switch (controlled by signal *OK*). During start-up, we begin the test with "Switch 1" set low. This sets *v2* equal to the zero voltage reference, *v0*. The original simulated voltage at the PCC, *v1*, is scaled from the simulated voltage to the voltage of the DUT (*v1'*) using a scaling factor of *Kv*. Start-up protection is performed by checking the three-phase RMS value, the single-phase RMS value, and the three-phase frequency value. If the RMS values and frequency are okay, then *Push Button 1* is pressed to reset the flip-flop and *Switch 1* will be turned on. *StartOK* will now be high. During the start-up process, the selection signal *CloseLoop1* is low, so the signal *StartOK* is selected and the output logic signal *OK* is high. Thus, the simulated voltage reference *v1'* is selected and output as the voltage reference *v2*. At the end of the start-up process, we close the PHIL loop by turning on *Switch 2* (shown in sub-AFB#1.2), and the signal *CloseLoop* will then become high. After the defined delay, the selection signal *ClosedLoop1* is high as well, and the system stability status signal *SystemOK* is selected to choose the output voltage reference. The signal *SystemOK* is obtained by evaluating the RMS and frequency of interface variables (*v1'*, *v4*, *v6* and *i3*) and instantaneous voltage magnitude of *v1'*. If the system is stable without harmful transients, the *SystemOK* is high, and *v1'* will continue to be output as the voltage reference. Otherwise, the zero voltage reference, *v0*, will supersede the voltage reference *v1'*

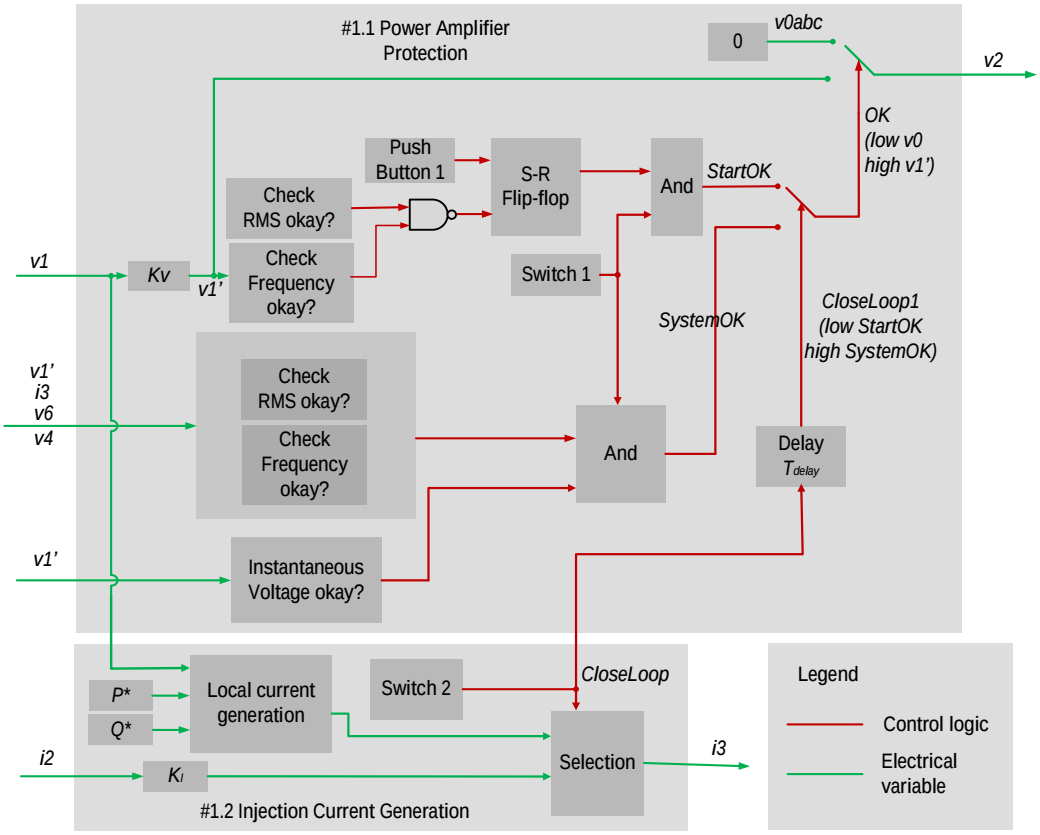

Fig. 2. Schematic diagram of AFB#1 Power Amplifier Protection.

Table 1. Settings and Parameters of AFB#1

<sub-function name>	Description	Symbol	<Value>
#1.1 Power amplifier protection	Scaling *v1* from high voltage/medium voltage to low voltage	Kv	$Kv = V_{DUT}/V_{pcc}$
	Lower limit of the RMS values of the interface voltage *v1', v4, v6*	V_{min}	0.9 p.u.
	Upper limit of the RMS values of the interface voltage *v1', v4, v6*	V_{max}	1.1 p.u.
	Lower limit of the frequency of the interface voltage *v1', v4, v6*	F_{min}	58 Hz
	Upper limit of the frequency of the interface voltage *v1', v4, v6*	F_{max}	62 Hz
	Upper limit of the interface current *i3*	I_{max}	1.8 p.u.
	Delay time	T_{delay}	2 s
	Threshold of the instantaneous voltage magnitude	-	1.1 p.u.
	Time limit of the instantaneous voltage over the threshold	-	2 time steps of real time simulation
#1.2 Local current generation	Active power reference	P^*	Adjustable
	Reactive power reference	Q^*	Adjustable
	Scaling *i2* to *i3* based on the power expansion	K_I	$(S_{power}/V_{grid})/(S_{DUT}/V_{DUT})$

to protect the power amplifier. The generated voltage reference signal *v2* is then sent to the AFB#2 for signal processing. During the shutoff process, we manually turn off *Switch 1* to switch from *v1'* to *v0*. Note that the frequency measurement requires high accuracy and fast response to capture the transient behavior of the interface variables when harmful transients caused by instability exist.

The sub-ABF#1.2, injected current generation, produces three-phase current for the controlled current source (CCS) based on the predefined power reference P^* and Q^* during the start-up process. This locally generated current is synchronized with the PCC voltage via a phase-locked-loop. The scaled feedback current (*i2*) is compared with the locally injected current in terms of magnitude, phase sequence, and waveform. If no errors are observed, the three-phase current injected to the CCS is switched from the locally injected current to the feedback current transducer (CT) current manually by turning on Switch 2. Note that the current from the CT is scaled by a factor K_I, which is used to adjust for different power ratings. For instance, if a DUT's rated power is 500 kW and the expected power in the simulation is 3 MW, then K_I is used to scale the DUT's power to that required in simulation.

The settings and parameters of AFB#1 are summarized in Table 1.

B. AFB#2 PHIL Interfacing Compensation

To guarantee the stability and accuracy of the PHIL platform, an interfacing compensation algorithm (#AFB2) is

added to augment the voltage reference *v2* before sending it to the analog output block. This AFB includes two sub-AFBs: #2.1 Tracking Error Cancellation and #2.2 Stability Improvement.

The voltage reference *v2* and the scaled feedback voltage from the potential transducer (PT) *v6* are sent to the sub-AFB#2.1 to cancel the tracking error between the scaled measured voltage *v6* and the reference voltage *v2*. A proportional resonance (*PR*) voltage regulator in the natural reference frame (*abc*) is used to cancel the tracking error in each phase. The transfer function of the *PR* control is shown in (1). The meaning and value of each parameter are shown in Table 2.

$$G_{Reg} = \frac{2K_r\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \quad (1)$$

Because of the potential instability associated with the resonance between the DUT output filter capacitance (C_{Inv}) and the power amplifier output filter inductance (L_{GS}), a notch filter (sub-AFB#2.2) is used to eliminate the parasitic resonance and to improve the stability of the PHIL system. The transfer function of the notch filter is shown in (2). The expression of the resonance frequency is shown in Table 2, with N_{Txfr} as the ratio of the transformer connected to the DUT.

$$G_{Notch} = \frac{s^2 + \omega_n^2}{(s + \omega_n)^2} \quad (2)$$

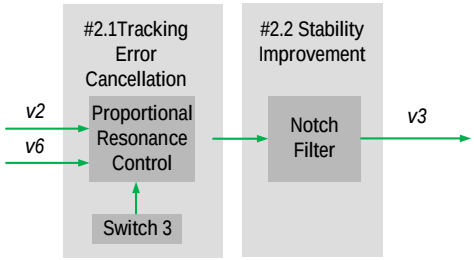

Fig. 3. Schematic diagram of AFB#2 PHIL Interfacing Compensation.

Sub-AFB#2.2 is not required for all DUTs and can be removed if unnecessary. The settings and parameters of AFB#2 are summarized in Table 2.

Table 2. Settings and parameters of AFB#2

<Sub-function name>	Description	Symbol	<Value>
#2.1 Tracking error cancellation	Gain of the PR control	K_r	150 but adjustable
	Cutoff frequency	ω_c	2π0.5 but adjustable
	Fundamental frequency	ω_0	2π60 rad/s
#2.2 Stability improvement	Resonance frequency [10]	ω_n	$\omega_n = \frac{1}{2\pi N_{Txfr}\sqrt{2L_{GS}C_{Inv}}}$

C. AFB#3 Analog Output Conditioning

The schematic diagram of AFB#3 is shown in Fig. 4. The generated voltage reference *v3* is sent to AFB#3 Analog Output Conditioning for processing prior to sending to the power amplifier. It is first adjusted by a gain K_1 and DC offset compensation D_V, then adjusted by a scale-down factor K_M, and finally passed through a limiter. The generated output *v4* is then sent to the power amplifier for signal reconstruction. The factor K_M is the ratio of the maximum input voltage and maximum output voltage of the power amplifier. The gain K_1 and compensation D_V are adjusted for each phase. Note that there are some coupling effects among the three-phase voltages, and K_1 and D_V need to be retuned after tuning each phase. The upper and lower limits V_{upper} and V_{lower} correspond to the maximum and minimum output voltage of the analog output card of the DRTS. The generated DC control signals (*Voc* and *Idc*) are scaled down by the ratio of the maximum input voltage and the maximum output of the DC supply. The power references (P_{ref} and Q_{ref}) are similarly converted to analog output signals based on the requirements of the DUT and DRTS hardware. The settings and parameters of AFB#3 are listed in Table 3. Note that the values for calibration in Table 3 are recommended values, and they are adjustable.

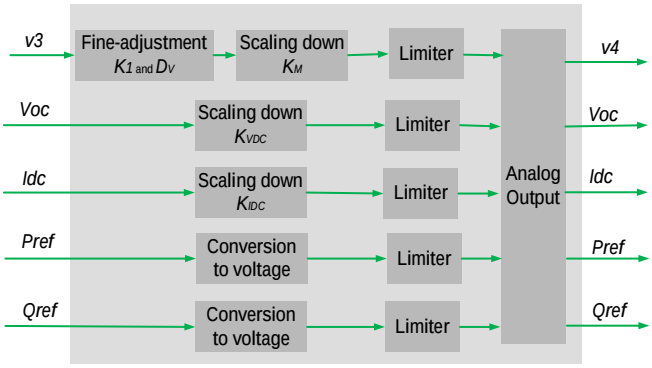

Fig. 4. Schematic diagram of AFB#3 Analog Output Conditioning.

Table 3. Settings and parameters of AFB#3

Description	Symbol	<Value>
Scale-down gain	K_M	V_{in}/V_{out} (Hardware specific)
Fine-adjustment gain	K_1	0.9~1.1
DC offset compensation	D_V	-0.1~0.1
Scale-down gain	K_{VDC}, K_{IDC}	V_{in}/V_{out} (Hardware specific)
Upper limit of analog voltage	V_{upper}	Hardware specific (e.g., RTDS is 10 V)
Lower limit of analog voltage	V_{lower}	Hardware specific (e.g., RTDS is -10 V)

D. AFB#4 Analog Input Conditioning

AFB#4 Analog Input Conditioning is shown in Fig. 5. This AFB receives the interface signals *v5* and *i1* from the measurement PT and CT and performs a series of signal processing—including coarse scaling, fine-adjustment scaling, and DC offset compensation and filtering—and then sends the "cleaned" signals to the related AFBs.

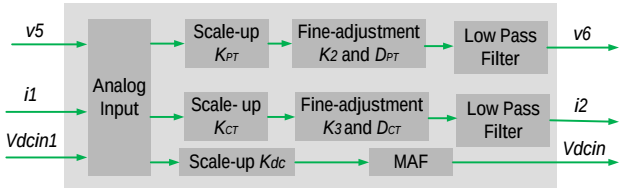

Fig. 5. Schematic diagram of AFB#4 Analog Input Conditioning.

The scale-up factor K_{PT} is the ratio of the PT input and output signals. The gain K_2 and compensation D_{PT} must be adjusted for each phase. Similarly, the factor K_{CT} is the ratio of

the CT input and output signals, and the gain K_3 and compensation D_{CT} must be adjusted for each phase as well. The low-pass filter is used to filter the harmonics from power electronic devices (power amplifier and the DUT) and measurement noises. The low-pass filter (LPF) applied to the current signal *i1* stabilizes the system by attenuating unsafe frequencies from the PHIL current feedback. The LPF applied to the voltage signal *v5* helps eliminate unwanted harmonics and improve voltage regulation. As the LPF introduces phase delay to the feedback current/voltage signals, affecting accuracy, a compromise must be made between stability and accuracy when applying the filter. Also, the same cutoff frequency should be used for both voltage and current LPFs to eliminate the angle difference between voltage and current, thus achieving improved power factor accuracy. The feedback DC voltage V_{dcin1} is scaled up by a factor K_{dc} and conditioned by a moving average filter (MAF). The settings and parameters of AFB#4 are listed in Table 4.

Table 4 Settings and parameters for AFB#4

Description	Symbol	<Value>
Scale-up gain	K_{PT}	Ratio of PT
Fine-adjustment gain	K_2	0.9~1.1
DC offset compensation	D_{PT}	-0.1~0.1
Scale-up gain	K_{CT}	Ratio of CT
Adjustment gain	K_3	0.9~1.1
DC offset compensation	D_{CT}	-0.1~0.1
Cut-off frequency	ω_c	1000 rad/s
Scale-up gain	K_{dc}	Ratio of PT

E. AFB#5 DUT Energy Generation Model

The AFB#5 generates the control/emulation reference for the DUT/DC source. This AFB is DUT specific. As shown in Fig. 6, #5.1 emulates the PV solar array I-V characteristics based on the mathematical model of the PV solar cell and array, considering PV module temperature, insolation, and PV array data. The open-circuit DC voltage *Voc* is sent from DRTS to the hardware DC source as a set point. The DUT perturbates the voltage at its terminals via a maximum power point tracking (MPPT) algorithm, and this DC voltage *Vdcin1* is measured and sent back to the DRTS (*Vdcin*). The simulated PV array follows the I-V curve, based on *Vdcin*, and generates the current *Idc*. This current *Idc* is then sent from the DRTS to the hardware DC source as a set point. In this scenario the DC source is operating in "current control" mode. The system will stabilize when the DUT's MPPT algorithm locates the maximum power point.

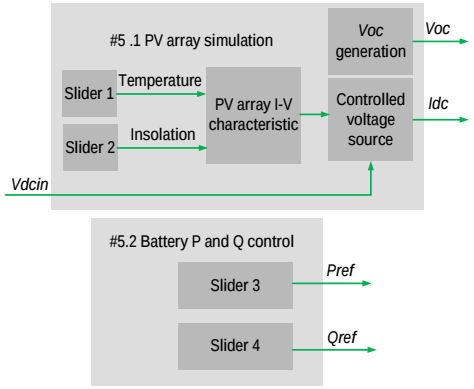

Fig. 6. Schematic diagram of AFB#5 DUT Energy Generation Model.

For the battery inverter, AFB#5.2 generates the control references P_{ref} and Q_{ref} and sends them to the AFB#3 for conditioning before being sent to the DUT. Battery's grid service (such as peak shaving, voltage support, etc.) can be simulated in this AFB and used to generate P_{ref} and Q_{ref}. Note that control references may be sent through communication links (e.g., TCP/IP DNP 3) or via analog output. Also, if a real-world controller is used to send power commands to the DUT, there is no need to have the sub-AFB#5.2. Battery state-of-charge (SOC) was ignored for this test, but this AFB could be used to simulate SOC or other battery system dynamics as required.

IV. Standard Test Procedure

After developing the standard AFBs for the PHIL interface, it is necessary to develop an operational test procedure for the PHIL experiment. This is to guarantee safe operation and protect hardware devices by following the correct sequence of actions to achieve closed-loop PHIL and to avoid harmful transients. Fig. 7 shows the schematic diagram of the test procedure, including the start-up process, normal testing, and shutdown process.

The start-up process starts from the PHIL with voltage reference *v2* equal to *v0* ("0"). If RMS values and frequency of simulated voltage reference v1' are okay, the *Push Button 1* will be pressed. After a few seconds, we can turn on *Switch 1* to set the voltage reference *v2* equal to v1'. Then check the analog output *v4* from the DRTS run time console and also by using an oscilloscope. If three-phase signals of *v4* are inspected to be sinusoidal waveforms with appropriate peak magnitude and phase sequence, we can turn on the power amplifier. Next, we can close the circuit breaker *CB1* between the power amplifier and the transformer. Check the reconstructed voltage (*v6*) from the power amplifier. If *v6* is okay, then turn on the voltage regulator. If the system continues to be stable, turn on the local current injection with zero power reference and then slightly increase the power reference (e.g., 10% of the rated power of the DUT) while ensuring the system remains stable. Next, enable the DUT (e.g., on/off switch), and set the power level equal to the local injection. If the scaled analog input *i2* (from CT) is okay, switch the current injection to the CT feedback current. Then the PHIL is closed-loop, and the start-up process ends.

The normal test process is DUT dependent and will change based on experimental needs. In this paper, we modified the control references for the battery inverter in AFB#5. For the PV inverter, we changed irradiation and temperature.

The shutdown process is designed to turn off the power hardware in an orderly fashion. As a first step, the power reference set points to the DUT are set to zero. This ensures that the current flow is close to zero in the hardware. The current injection in the DRTS model will also be minimal. Next, the DUT is disabled, effectively removing it from the circuit. The power amplifier is then turned off. The hardware is now in a safe condition, and "CB1" can be opened. The final step is to stop the PHIL model in the DRTS. Between actions, an appropriate time interval should be maintained to ensure system stability.

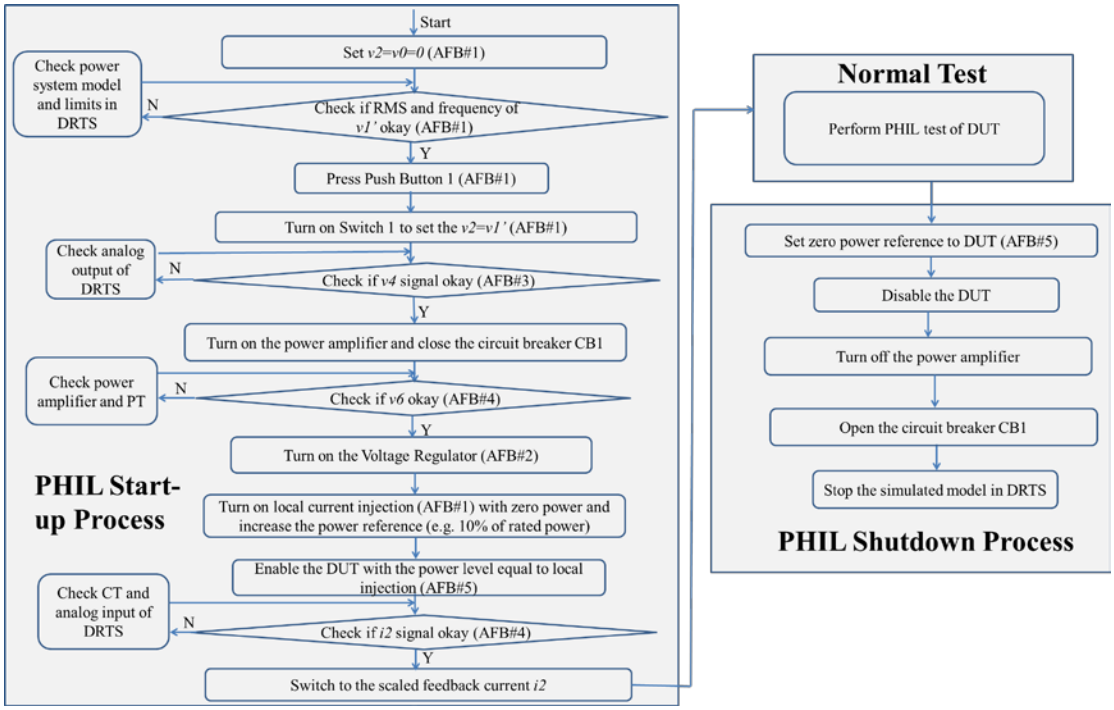

Fig. 7. Schematic diagram of the operation procedure of the PHIL test: start-up process, normal test, and shutdown process.

V. Sample Experimental Test Results and Discussion

To test and evaluate the developed AFBs for the PHIL interface algorithm, two commercially available grid-connected inverters were tested: (1) a 540-kVA battery inverter and (2) a 500-kW PV solar inverter. The configuration of the PHIL setup is shown in Fig. 1, which includes the DRTS, AC power amplifier, transformer, DC amplifier, and the DUT. There are two test purposes: (1) to prove that all AFBs for the PHIL interface work correctly and (2) to demonstrate the reconfigurability of the developed AFBs from testing one DUT to another. The sample results are shown in Fig. 8 and Fig. 9.

Fig. 8 shows the PHIL test results of a simulated medium-voltage network with the battery inverter connected. The DUT's rated power is 540 kVA, and the injected power in the DRTS is scaled up to 3 MW. The presented results follow the operation process shown in Fig. 7 (only partial results are presented here because of limited space): switching from "0" voltage reference *v0* to simulated voltage *v1'*, turning the voltage regulator on (*v2*, *v6*, and tracking error v_{error} (*v2*-*v6*)), switching from local (the first part of *i3*) to DUT current injection (the second part of *i3*) and the scaled measured current from CT (*i2*), the step change of the power references of the DUT and the output power (P_{ref}, P_{meas}, Q_{ref} and Q_{meas}), and the analog output *v4* and system stability indicator *SystemOK* when an overvoltage event is triggered. As shown in Fig. 8 (a), the voltage reference *v2* exhibits no transients when we manually switch from "0" voltage reference *v0* to simulated voltage *v1'*. Fig. 8 (b) shows that the reconstructed voltage in the power amplifier *v6* deviates from the voltage reference *v2* before turning on the voltage regulator. The voltage deviation is noticeably reduced after turning on the voltage regulator. The tracking errors during the period of turning on the voltage regulator are shown in Fig. 8 (c), and a significant reduction in tracking error (from 20.89% to 1.02%) can be observed. The steady-state tracking errors are presented, and the magnitudes are very small, around 2 V (RMS). Fig. 8 (d) shows the injected currents during the period of turning from the local injection to DUT feedback CT current *i2* injection. Note that *i2* is scaled from *i1* based on the factor K_I. Fig. 8 (e) shows the output power of the DUT when the reference power is step changed, which indicates the response of the battery inverter and also the interactive dynamics between active and reactive power. The voltage reference *v4* (analog output) and the system stability indicator *SystemOK* when an overvoltage event is triggered are shown in Fig. 8 (f), showing that the overvoltage condition is detected and the voltage reference *v4* becomes *v0* ("0") as designed. All results shown in Fig. 8 demonstrate the effectiveness of AFBs. The results also show the stability and accuracy of the PHIL platform for emulating DUT dynamics.

Fig. 9 shows the PHIL test results of the same simulated medium-voltage network with the PV inverter connected. The DUT's rated power is 500 kW, and the injected power in the DRTS is scaled up to 6 MW. The same grid simulator is used for the PV inverter. The PHIL interface algorithm AFBs for testing the battery inverter are reconfigured for testing the PV inverter. The following modifications are made: (1) AFB#1: the scaling factor K_I needs to be changed because the scaled power is different. (2) AFB#2: the notch filter needs to be redesigned because the capacitance of the output filter of the PV inverter is different; PR control needs to be retuned to have less tracking gain and larger phase margin if the stability is poor. (3) AFB#3: calculate the scaling factor K_{VDC} and K_{IDC}. (4) AFB#4: the scale-up factor K_{PT} needs to be calculated for the PV inverter; also, for the scale-up factor K_{CT}. If the stability

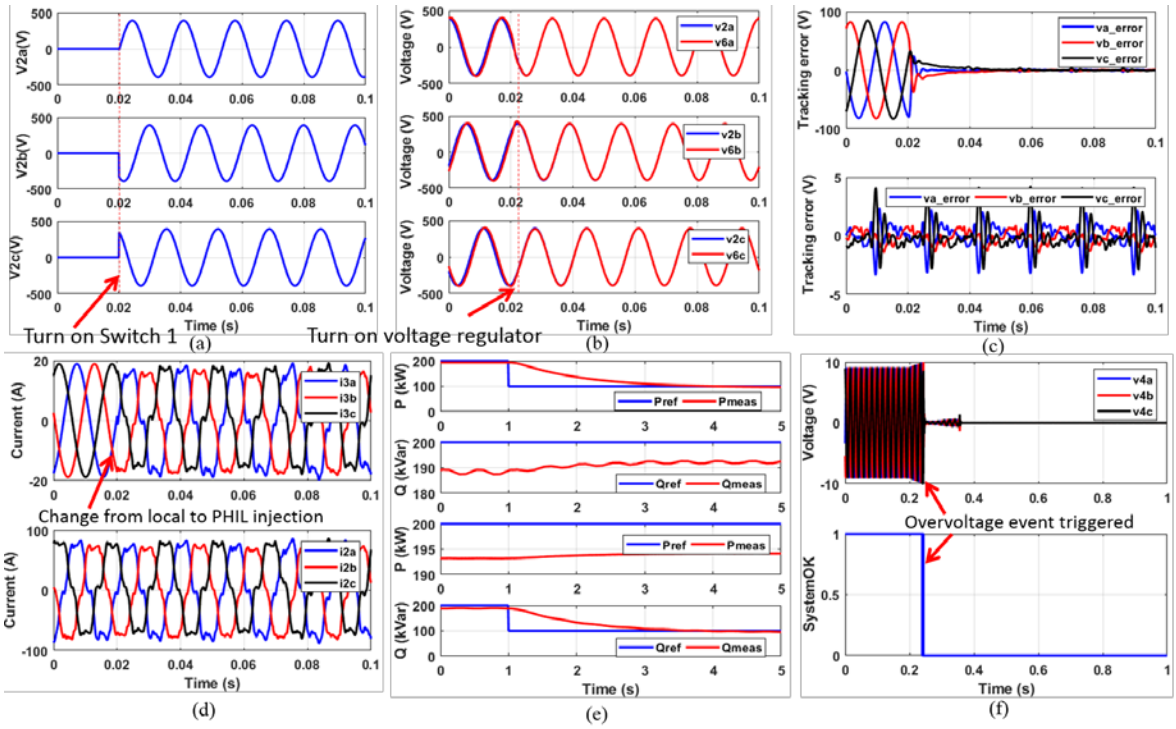

Fig. 8. PHIL simulaton of a medium-voltage network with battery connected: (a) turn on Switch 1; (b) and top figure of (c) turn on Switch 3; bottom figure of (c) tracking error in steady state; (d) switch from local to DUT current injection; (e) step change of active power and reactive power reference for the DUT; (f) analog output *v4* and system stability indicator *SystemOk* with overvoltage event triggered.

is poor, the cutoff frequency of the low-pass filter (both voltage and current) can be reduced. (5) AFB#5: the sub AFB#5.1 is used for emulating PV array dynamics for controlling the DC source. These are some of the modifications that may be required for testing a different DUT, in this case, the PV inverter.

The results shown in Fig. 9 demonstrate that the PHIL test for PV is successfully performed: the switch from "0" voltage reference *v0* to the simulated voltage *v1'* is smooth; turning on the voltage regulator is useful to reduce the tracking error and improve the accuracy of the PHIL; switching from the local current injection to the PHIL feedback CT current is a good precheck of the stability and avoids harmful transients when closing the PHIL loop; change in insolation and temperature impacts the PV output power and also the scaled power injected to the grid, and the response of the PV inverter (initial response and settling time) on those changes can be observed; the overvoltage event can be detected, and the voltage refence *v4* becomes *v0* ("0") to short-circuit the power amplifier for protection.

Based on our experiences, a few points to improve the PHIL interface AFBs in the future are: (1) the PCC voltage should not be high or medium voltage unless the DUT has high-voltage or medium-voltage output. Therefore, instead of scaling the high voltage/medium voltage to low voltage by using a scaling factor K_V, a transformer should be used inside the simulation model in DRTS to step down the voltage to the nominal voltage of the power amplifier. (2) The PHIL interface we developed is for nominal system tests; transient test scenarios such as low-voltage-ride-through (LVRT) or fault events are not considered. However, we can loosen the limits in the relevant AFBs to allow the transients in voltage to be sent to the power amplifier. For example, the lower limit of the voltage magnitude and RMS value in AFB#1.1 should be 0.5 p.u. based on the LVRT test requirements in IEEE P1547.7. Therefore, the simulated voltage reference *v1'* will be within the acceptable limits of AFB#1.1 and will not be overridden by *v0*. (3) In the most basic scenario, the DC source for a battery inverter can be configured to discharge/charge regardless of the SOC. Although this is unrealistic in practice, it can be useful if the SOC or other battery conditions are unimportant for the given experiment. The DC source can also be configured to receive control signals from the DRTS (similar to the PV inverter). In this scenario, a model within the DRTS will simulate the battery and values such as voltage, current, and resistance can be sent to the DC source as set points [11]. This way, features (SOC, charging/discharging) of batteries can be emulated to simulate the battery dynamics more realistically.

Results shown in Fig. 8 and Fig. 9 demonstrate the performance of the AFBs in terms of stability and accuracy. The capability of the AFBs to be reconfigured for a new DUT is presented from the PV inverter test results. The DUTs are unique in terms of output filter parameters, power rating, and voltage rating. The AFBs need to be modified to match the specifications of the DUT. These modifications can be scaling factors, filter parameters, etc. Even though every AFB needs to be modified for testing the new DUT, the effort for reengineering is kept to a minimum to accelerate the setup of a new PHIL test. Thus, using AFBs is time-saving, and its advantages will become more salient when more PHIL tests will be performed.

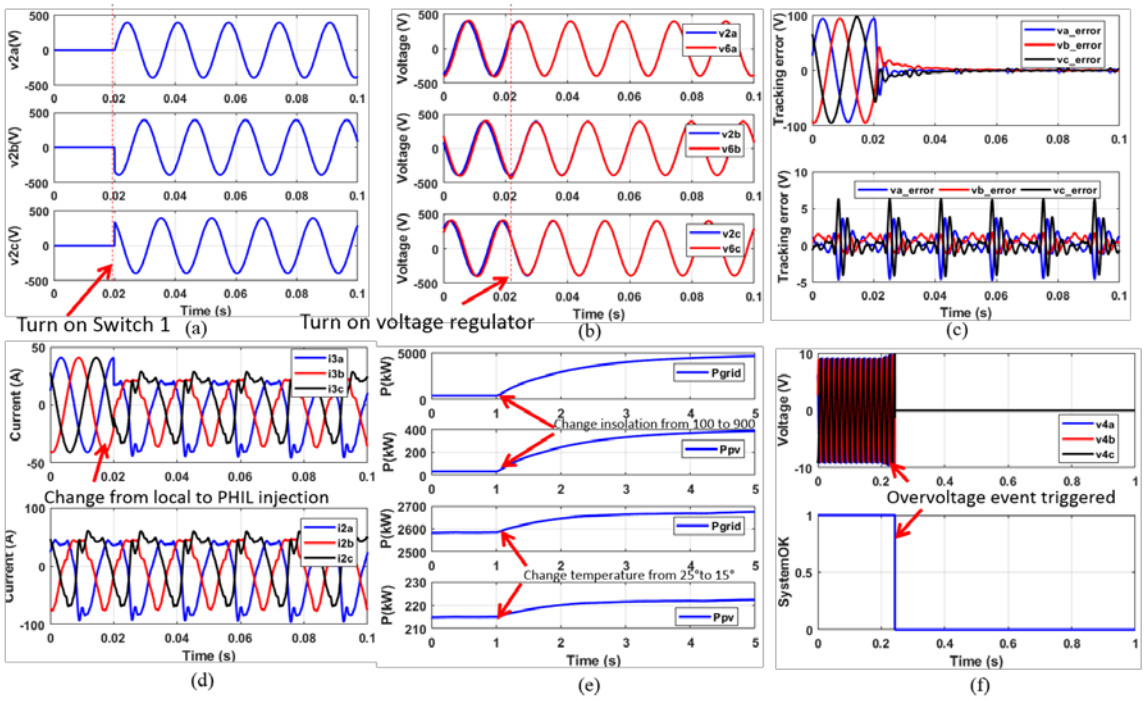

Fig. 9. PHIL simulaton of a medium-voltage network with PV connected: (a) turn on Switch 1; (b) and top figure of (c) turn on Switch 3; bottom figure of (c) tracking error in steady state; (d) switch from local to DUT current injection; (e) step change of isolation and temperature for the DUT; (f) analog output *v4* and system stability indicator *SystemOk* with overvoltage event triggered.

VI. Conclusion

This paper presented standard AFBs for use in the PHIL experimental setup for testing grid-connected inverters. The standard test procedure for PHIL experiments is also presented. This standard test procedure reduced transients and equipment damage during start-up and shutdown of the PHIL experiments. The AFBs and the standard test procedure are presented in detail for replication by researchers for PHIL experiments. Experimental results of testing battery and PV inverters demonstrated the effectiveness of the developed AFBs. The results improved tracking of the voltage and power set points with the use of AFBs and the proper test procedure. Finally, a discussion on the usability and reconfigurability of AFBs is presented, showing the value of using standard AFBs to accelerate the PHIL experiments.

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