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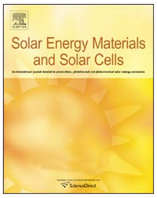

Charge carrier transport mechanisms of passivating contacts studied by temperature-dependent J-V measurements

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ABSTRACT

The charge carrier transport mechanism of passivating contacts which feature an ultra-thin oxide layer is investigated by studying temperature-dependent current-voltage characteristics. 4-Terminal dark *J-V* measurements at low temperatures reveal non-linear *J-V* characteristics of passivating contacts with a homogeneously grown silicon oxide, which result in an exponential increase in contact resistance towards lower temperature. The attempt to describe the *R(T)* characteristic solely by thermionic emission of charge carriers across an energy barrier leads to a significant underestimation of the resistance by several orders of magnitude. However, the data can be described properly with the metal-insulator-semiconductor (MIS) theory if tunneling of charge carriers through the silicon oxide layer is taken into account. Furthermore, temperature-dependent light *J-V* characteristics of solar cells featuring passivating contacts at the rear revealed a FF drop at $T < 205$ K, which is near the onset temperature of the exponential increase in contact resistivity.

1. Introduction

Passivating and carrier-selective contacts based on a thin silicon oxide layer and a heavily-doped Si layer (poly-Si or Si-rich SiC$_x$) have recently attracted attention for their low recombination current densities < 10 fA/cm^2 while maintaining contact resistivities sufficiently low for solar cell contacts [1–10]. Although solar cells with efficiencies above 25% have been realized [11], the underlying physical transport mechanism of these contacts is still not fully understood. In general, it should be noted that although the principal structure of the above-mentioned contacts is similar, the process steps differ quite significantly, especially the thickness of the oxide and the final thermal treatment which makes it difficult to generalize theories about the underlying physical transport mechanisms.

Soon after the advent of the poly-Si emitter for bipolar junction transistors (BJTs) in the 1970s, different models were proposed to explain the current gain enhancement by the poly-Si emitter. An excellent review paper can be found here [12]. Among those, the most famous was the "oxide tunneling" model which described very adequately the reduction of the base current and the increase of the emitter resistance of BJTs with deliberately grown interfacial oxide [13]. For the hole current of n$^+$-poly-Si/c-Si(p) junction it reads:

$$J_p \approx q\sqrt{\frac{k_B T}{2\pi m_h^*}}\frac{P_t}{N_{D,int}}n_{i,int}^2\exp\left(\frac{q}{k_B T}(V_j - \phi_s)\right). \tag{1}$$

In this expression $N_{D,int}$ and $n_{i,int}^2$ are the donor concentration and the intrinsic carrier concentration at the interface, respectively, V_j is the internal junction voltage, and ϕ_s is the surface band bending in the c-Si. The tunneling probability, P_t, is solved with the Wentzel-Kramers-Brillouin (WKB) approximation

$$P_t \approx \exp\left(-\frac{2}{\hbar}t_{ox}\sqrt{2m_h^* q\Delta\phi_h}\right). \tag{2}$$

According to Eq. (2), the tunneling probability decreases exponentially with the oxide thickness, t_{ox}, and the height, $\Delta\phi_h$, of the energy barrier. As one can readily see Eq. (2) is of the same form as the equation for the direct tunnel current in a metal-oxide-semiconductor (MOS) system, with the heavily-doped poly-Si showing metal-like behavior (degenerate doping). The assumption that tunneling is the dominant transport mechanism was further substantiated by the weak temperature dependence of these devices [12]. However, the model does not describe pnp BJTs well. In essence, the oxide poses a larger

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barrier to holes than to electrons which is reflected in the barrier heights $\Delta\phi_h = 1.0$ eV and $\Delta\phi_e = 0.3$eV determined with this model [12]. However, in the case of a pnp transistor this means that a slight current gain enhancement would come at the expense of a very high emitter resistance which does not reflect the experimental findings [14–16]. In addition, it should be noted that the reported values for $\Delta\phi_e$ and $\Delta\phi_h$ are much lower than the conduction (3.2 eV) and valence (4.7 eV) band offsets between c-Si and bulk SiO_2 [17]. Apart from tunneling over the oxide barrier, transport could also be realized through pinholes in the oxide, which are reported to be formed under certain experimental conditions. In view of the approach by Gan and Swanson [18] which capitalizes on deliberately formed pinholes in a thick oxide ($t_{ox} \geq 2$ nm), a model accounting only for transport through pinholes was recently published [19,20]. Furthermore, a technique not only capable of visualizing pinholes but also capable of quantifying the pinhole density has been published [21]. Yet it is still to be demonstrated that moderate annealing conditions ($T_{anneal} < 900$ °C) lead to a significant pinhole density. In addition, the pinhole model does not explain the *J-V* characteristics of non-annealed poly-Si/SiO_x/c-Si structures, which also yielded significant current gain enhancement factors [22].

In this manuscript, the transport mechanism is studied in detail by means of temperature dependent *J-V* measurements on test structures and solar cells. We compare three different TOPCon structures where oxide integrity ranges from fully intact to strongly disintegrated and show that their distinct *J-V* temperature-dependence can be explained with their structural differences. The TOPCon structure features an ultrathin oxide ($t_{ox} \approx 1.2$–1.4 nm) which should suffice the requirements for an efficient carrier flow via quantum mechanical tunneling [23].

2. Experimental details

2.1. Sample preparation

A range of TOPCon structures with varying oxide integrity and thus electronic quality with respect to surface passivation and contact resistivity was prepared. Both symmetric lifetime samples and unipolar test structures featuring an ohmic rear contact and a circular metal contact on the TOPCon structure at the front (c.f. Fig. 1) were realized on shiny-etched (100)-oriented, 200 µm thick, 1 Ω cm n-type wafers. The TOPCon structures were realized by growing a thin oxide in boiling nitric acid (68%), depositing 15 nm silicon-rich a-SiC_x:H(n) by PECVD, thermal annealing, and, finally, hydrogen passivation at 400 °C. Three different annealing conditions were chosen: (i) 800 °C, 60 min; (ii) 900 °C, 10 min; and (iii) 950 °C, 3 min. At $T_{anneal} = 800$ °C the a-SiC_x layer remains amorphous, while it becomes partially crystalline for $T_{anneal} \geq 900$ °C as evidenced by Raman spectroscopy shown in Ref. [4].

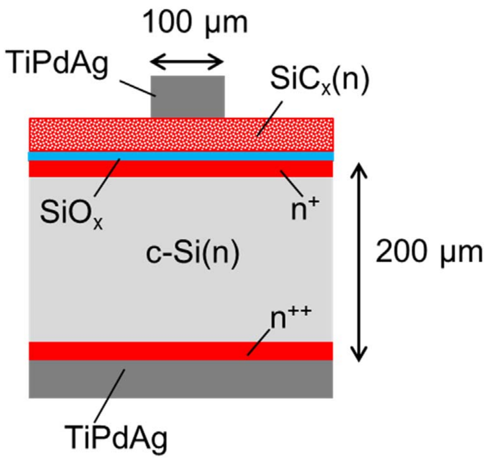

Fig. 1. Sketch of the unipolar test structure.

The unipolar test structures received a full-area metal contact at the rear and circular metal contacts with radius of ~ 53 µm (determined by optical microscopy) at the front as shown in Fig. 1. Metal was deposited by thermal evaporation of Ti, Pd, Ag. The electrodes were structured by the lift-off technique. The rear was fully metallized by thermal evaporation of Ti, Pd, Ag.

Solar cells featuring a boron-diffused emitter at the front and an n-type TOPCon contact at the rear were realized as described in Ref. [24]. The TOPCon structure was annealed at 800 °C, 60 min, and 900 °C, 10 min, respectively.

2.2. Characterization

The test structures were mounted onto a gold ceramic and the front electrode was contacted to a conductive pad by a bonded gold wire. The ceramic was then mounted into a cooling system and two probes made contact to the front pad and two contacted the chuck. The sample under investigation was cooled down to a temperature of about 114 K by liquid nitrogen. Before each *J-V* curve acquisition, the temperature was held for 2 min to establish thermal equilibrium. *J-V* data were taken in a temperature range of 114–350 K.

Temperature-dependent *J-V* data of the solar cells were taken by using a home-built hybrid light-emitting diode halogen lamp solar simulator with a temperature controllable chuck. More information on this setup can be found in Ref. [25].

3. Experimental results

3.1. Surface passivation and contact resistivity

The implied V_{oc} and contact resistivity (ρ_c) of the different TOPCon structures are displayed in Table 1. It can be seen that both the highest iV_{oc} and ρ_c were obtained for $T_{anneal} = 800$ °C. With increasing T_{anneal} both iV_{oc} and ρ_c decreased. At 950 °C virtually no surface passivation was obtained which can be ascribed to a complete disintegration of the tunnel oxide. In Fig. 2a TEM micrograph shows that for this annealing condition the oxide is completely "balled up", which leads to epitaxial regrowth of the Si layer on the c-Si wafer. Furthermore, diffusion of phosphorus from the SiC_x layer into c-Si is enhanced with temperature and instead of a very shallow diffused c-Si region (depth < 50 nm for $T_{anneal} = 800$ °C) a few 100 nm deep c-Si(n^+)-layer was formed which had a sheet resistance of about 850 ± 100 Ω/sq and 194 ± 5 Ω/sq in the case of 900 °C and 950 °C, respectively.

3.2. Dark J-V on test structures

The unipolar test structures featuring TOPCon at the front were measured in a temperature range from 114K to 350 K. Fig. 3a) shows the dark *J-V* characteristics of the sample structure featuring n-TOPCon annealed at 800 °C. At $T = 114$ K a non-linear *J-V* characteristic was observed showing a symmetric shape with respect to voltage. With increasing temperature, the current increased and at $T = 243$ K the *J-V* characteristic exhibited an almost linear shape. The latter denotes a transition from a Schottky contact to an ohmic contact. Fig. 3b) shows the *J-V* curves of the sample which was annealed at 900 °C. In the

Table 1
Sample description.

T_{anneal}	Oxide integrity[a]	iV_{oc} (mV)	ρ_c [mΩ cm^2]
800 °C	High	715.5	3.9 ± 0.4
900 °C	Medium	683.3	1.7 ± 0.3
950 °C	Low, many pinholes	624.7	0.5 ± 0.1

[a] Qualitative figure of merit.

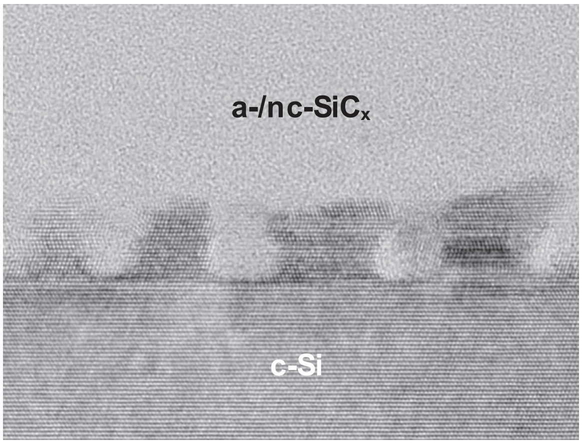

Fig. 2. TEM image of TOPCon structure annealed at 950 °C. The dark hatched regions reveal that epitaxial regrowth at the c-Si surface occurred.

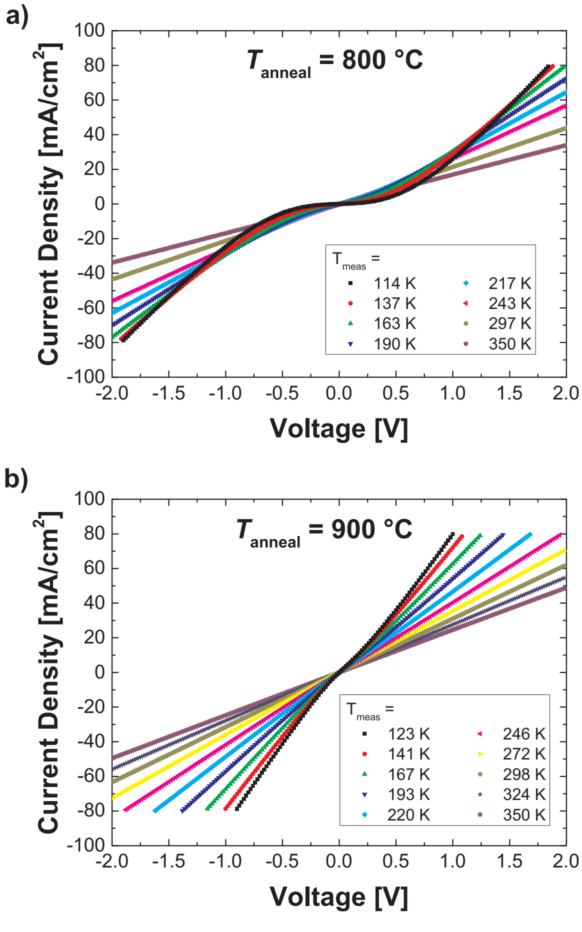

Fig. 3. Dark *J-V* characteristics of n-TOPCon annealed a) at 800 °C and b) at 900 °C.

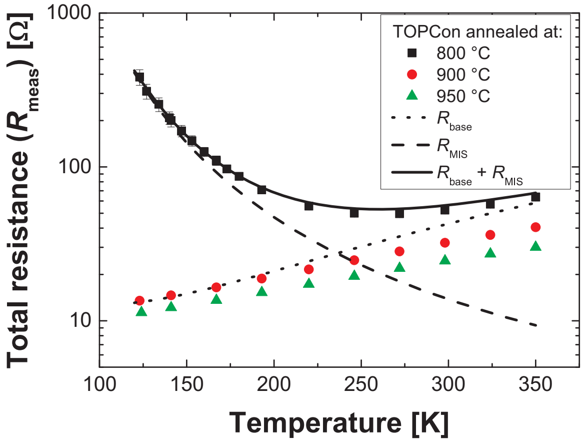

Fig. 4. Total resistance of the test structures plotted over measurement temperature. The resistance was extracted by linear fit around $V = 0$ V. In addition, the *R(T)* data was modelled by R_{MIS} and R_{base} as described in the text.

almost entire temperature range a linear *J-V* relationship is observed. Only at temperatures below 180 K a subtle non-linearity near 0 V can be observed.

Fig. 4 shows the total measured resistance (R_{meas}), which is the sum of the contact resistance and the wafer's spreading resistance (R_{base}), of the three different test structures over a wide temperature range. For the samples which were annealed at 900 °C and 950 °C the resistances were obtained by linear regression in the voltage range from −0.5 V to 0.5 V. Since the sample annealed at 800 °C exhibited non-linear *J-V* characteristics (c.f. Fig. 2a), the resistances were obtained by linear regression in four different voltage ranges close to zero bias ($V_{max} = -V_{min} = 50, 100, 160, 200$ mV) and by calculating the mean value. The error bars describe the uncertainty of the resistances of the 800 °C-sample.

The two samples which were annealed at 900 °C and 950 °C, respectively, exhibit monotonically decreasing resistances with decreasing temperature. The calculated wafer's spreading resistance (dotted line) shows a similar trend with temperature which is governed by the increase in electron mobility in the substrate with decreasing temperature. That both samples annealed at 900 °C and 950 °C yielded resistances lower than R_{base} can be ascribed to the diffused c-Si(n$^+$)-layer underneath TOPCon which mitigates current crowding effects. For instance, numerical simulation of this test structure yielded resistances of 32.6 Ω and 22.0 Ω for $R_{sh} = 800$ Ω/sq and 200 Ω/sq, respectively, which match $R_{meas,900\,°C} = 32.1$ Ω and $R_{meas,950\,°C} = 24.5$ Ω at $T = 298$ K well.

While the temperature dependence of the latter two samples was governed by the temperature dependence of R_{base}, the sample annealed at 800 °C shows quite the opposite behavior: at higher temperatures the resistance decreases as well with temperature but for $T < 250$ K the resistance starts to increase exponentially towards lower temperatures. The latter effect can possibly be attributed to an energy barrier which has to be overcome by thermionic emission. From the *J-V* characteristics of thermionic emission one obtains R_{TE} which depends exponentially on temperature and barrier height (surface band bending) [26]:

$$R_{TE} = \frac{k_B}{A^* Tq}\exp\left(\frac{q\phi_s}{k_B T}\right). \tag{3}$$

In order to gain a better understanding of the underlying transport phenomena, more data points were taken in the low temperature range of 120 K–180 K and R_{meas} was extracted as described above. After subtraction of R_{base} the barrier height was obtained from an Arrhenius plot in the temperature range from 120K to 180 K (see inset of Fig. 5). A barrier height of 42.6 meV was measured for the shown sample. On another sample a barrier height of 38.4 meV was obtained. A barrier height of 42.6 meV leads to R_{TE} values of 1.1 mΩ (180 K) to 6.3 mΩ (120 K) according to Eq. (3), which is significantly lower than the actually measured R_{meas}. The ratio $\ln((R_{meas}\text{-}R_{base})/\ R_{TE})$ is shown in Fig. 5. Interestingly, this ratio is constant over temperature and could be explained by tunneling, as tunneling adds a temperature-independent factor to Eq. (3) [27].

$$R_{MIS} = R_{TE}/P_t = R_{TE}\exp\left(\frac{2}{\hbar}t_{ox}\sqrt{2qm_e^{**}\phi_e}\right) \tag{4}$$

$1/P_t \approx \exp(11.1)$ was extracted from Fig. 5 and used to calculate

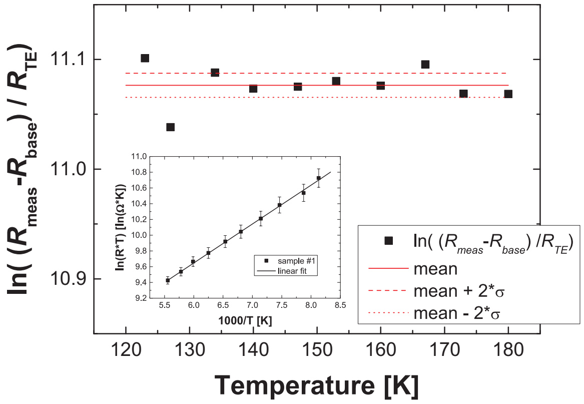

Fig. 5. Logarithmic ratio of (R_{meas}–R_{base}) to R_{TE} plotted over temperature. The inset shows the Arrhenius plot from which E_{act} was extracted.

R_{MIS} with $\phi_s = 42.6$ meV and the result is shown in Fig. 3 with dashed line. For $T < 225$ K R_{meas} is dominated by the resistance R_{MIS} while for $T > 250$ K the spreading resistance of the wafer (dotted line) contributes mainly to R_{meas}. The solid line refers to the total calculated resistance of this structure which describes the measured resistance well in the entire temperature range.

If one assumes that the barrier height for electron tunneling matches the Si-SiO$_2$ conduction band offset ($\phi_e = 3.2$ eV), one can determine an effective tunneling mass of 0.25 m_e for an oxide thickness of 1.2 nm. Although these values agree quite well with literature, it should be noted that the extraction of the barrier height and effective mass for electron tunneling is prone to error as the oxide thickness is not precisely known in this experiment.

3.3. Solar cell results

Solar cells featuring TOPCon rear contacts (either annealed at 800 °C or 900 °C) were measured as described above. Fig. 6 plots V_{oc} and FF as a function of temperature. The V_{oc} of the two different solar cells behaved similarly and increased towards lower temperature. The temperature coefficients of the different solar cells are displayed in Fig. 6 as well. Since the cell featuring TOPCon/800 °C at the rear had the highest V_{oc} it also showed the lowest temperature coefficient of −1.81 mV/K for $T > 275$ K. In this temperature regime the temperature coefficients of the V_{oc} can be well reproduced by applying [28]

$$\frac{dV_{oc}}{dT} = -\frac{\frac{nE_g}{mq} - V_{oc} + \frac{\gamma nkT}{q}}{T} \tag{5}$$

with n = 3, $m = \frac{E_g(T)}{E_g(0K)}*n \approx 2.88$, γ = 1. For $T < 250$ K the temperature coefficient of the V_{oc} changed and the measured V_{oc} deviates from theory [29] which can be attributed to a steeper decrease of the $J_{\mathrm{sc}}(T)$ characteristic with decreasing temperature (not shown here).

For $T > 275$ K the FF of both cells increased towards lower temperatures as it is expected from theory. Moreover, the FF(T) characteristics can be well described by [30]

$$FF = FF_0*(1-r_s) = \frac{v_{oc} - \ln(v_{oc}+0.72)}{v_{oc}+1}*(1-r_s), \quad \text{with } v_{oc} = \frac{q}{nkT}V_{oc} \tag{6}$$

where the ideality factor (n) and the normalized temperature-independent series resistance (r_s) were used as fitting parameters (dashed lines). The higher FF of the TOPCon/800 °C cell can be ascribed to both the cell's lower grid resistance and its higher FF$_0$. While Eq. (6) describes the FF(T) characteristic of the TOPCon/900 °C cell very well over the entire temperature range, the FF of the TOPCon/800 °C cell deviates markedly from the calculated FF characteristic for $T < 250$ K. More precisely, the FF peaked near 200 K and then rolled off towards lower temperatures. In an attempt to describe the data a temperature-dependent series resistance is added to Eq. (6):

$$FF = FF_0*(1-r_{s,1} - r_{s,2}(T)) = FF_0*\left(1-r_{s,1} - r_{s,2}*\exp\left(\frac{qE_A}{kT}\right)\right). \tag{7}$$

By using Eq. (7) and $r_{s,1}$, $r_{s,2}$, and E_A as fit parameter the measured FF(T) data can be reasonably well described over the entire temperature range. The extracted activation energy takes a value of 34.7 meV which is comparable to ϕ_s determined from the dark J-V measurements on test structures. Thus, the FF of the TOPCon/800 °C cell shows a signature of the exponential R_{meas} increase seen in Fig. 4.

Previously a strong FF drop at low temperatures was reported for standard silicon heterojunction (SHJ) solar cells [31]. This has been attributed to a pronounced transport barrier which hampers the rate of thermionic emission of charge carriers. In contrast, the FF drop observed here for the TOPCon cell annealed at 800 °C is much less pronounced likely due to a significantly smaller energy barrier compared to SHJ solar cells. Furthermore, the TOPCon cell annealed at 900 °C demonstrates that the transport barrier can be effectively reduced to values close to zero. One reason for this effect could be that the SiC$_x$(n) layer is partially crystalline after annealing at 900 °C and, thus, the electrically active carrier density is higher which leads to improved

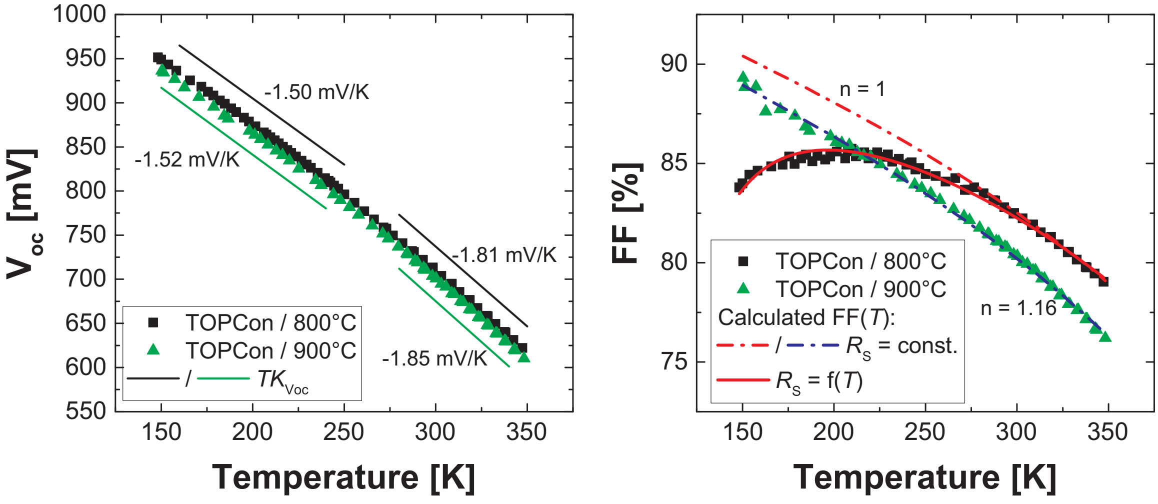

Fig. 6. V_{oc} and FF plotted over temperature. The solar cells featured a full-area passivating rear contact (TOPCon) which was annealed at 800 °C and 900 °C, respectively. Right graph: the dashed lines were calculated according to Eq. (6) using a temperature-independent series resistance. The solid red line was calculated according to Eq. (7) using an additional temperature-dependent series resistance. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article)

contact formation. However, the improved FF characteristic came at the expense of increased recombination at the rear contact and resulted in a lower efficiency compared to the TOPCon/800 °C cell in the relevant temperature range.

4. Summary

The charge carrier transport of passivating TOPCon contacts was investigated by means of temperature-dependent *J-V* measurements on dedicated test structures and solar cells. TOPCon contacts with an intact oxide layer showed an exponential increase of the contact resistance towards lower temperatures. The contact resistance could be properly described with the MIS theory with a temperature-independent resistance contribution due to tunneling. On the other hand, TOPCon contacts with probably partly disrupted tunnel oxides did not show an exponential increase in contact resistance towards low temperatures, and their *J-V* characteristics were governed by the temperature dependence of the wafer conductivity.

Moreover, the distinctive FF characteristics of the solar cells featuring TOPCon with HNO_3 oxide annealed at 800 °C or 900 °C can be qualitatively explained by the distinctive behavior of their contact resistances. Additionally, this shows that although the principal structure of different contact structures based on a thin silicon oxide layer and a heavily-doped Si layer might look similar, the physical transport mechanism strongly depends on the used processes (i.e. oxide thickness and annealing temperature). For other oxide types (e.g. ozone-based or thermally grown) the transition from an intact to a disintegrated oxide layer can occur at a higher temperature.

In summary, the *J-V* data support the notion that quantum mechanical tunneling is the dominant transport path for the TOPCon structure with intact oxide. In comparison to the TOPCon contact which was annealed at 900 °C, the TOPCon structure with intact oxide provides a better surface passivation quality and yields an at least 10 mV higher V_{oc} at device level. Hence, the application of the TOPCon contact with HNO_3 oxide (annealed at 800 °C) at the rear of an n-type Si solar cell featuring a selective boron-diffused front emitter yielded an efficiency of 25.3% [11].

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