Photovoltaic Cells Employing Group II-VI Compound Semiconductor Active Layers

Cooperative Research and Development Final Report

CRADA Number: CRD-09-325

NREL is a national laboratory of the U.S. Department of Energy
Office of Energy Efficiency & Renewable Energy
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Contract No. DE-AC36-08GO28308

Technical Report
NREL/TP-5K00-72467
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NOTICE

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Cooperative Research and Development Final Report

In accordance with Requirements set forth in the terms of the CRADA agreement, this document is the final CRADA report, to be forwarded to the DOE Office of Science and Technical Information as part of the commitment to the public to demonstrate results of federally funded research.

Parties to the Agreement: EPIR Technologies, Inc.

CRADA number: CRD-09-325

CRADA Title: Photovoltaic Cells Employing Group II-VI Compound Semiconductor Active Layers

Joint Work Statement Funding Table showing DOE commitment:

Estimated Costs	Funds in to NREL
2010	$ 38,000.00
2011	$ 32,871.00
2012	$ 15,000.00
2016	$ 5,000.0
TOTALS	$ 90,871.00

Abstract of CRADA Work:

Group II-VI compound semiconductors hold great promise for incorporation into low cost/watt solar photovoltaics. This CRADA will partner EPIR Technologies, Inc, a leading company in II-VI semiconductors and photovoltaics, with NREL to expedite the development of this novel class of solar cells.

Summary of Research Results:

EPIR provided NREL with samples including datasheets, necessary stack information, and at times optical and electrical characteristics. EPIR's layers/processes at times included metal back contact; monocrystalline Si as a substrate, and an active photovoltaic layer grown by molecular beam epitaxy. NREL provided samples with transparent conducting oxide (TCO) layers, polycrystalline II-VI thin films, $CdCl_2$ treatment, CdS (sputtered or CBD), buffer layer, TCO layer(s), grid metal layer(s), and anti-reflective layers, as well as measurements and characterization including SIMS and time-resolved photoluminescence measurements, capacitance voltage (CV) analysis of junction characteristics, surface analysis of heterojunction diffusion profiles and electron beam induced current. NREL and EPIR jointly explored processes to optimize solar cell performance.

Multiple polycrystalline CdS/CdTe solar cells with efficiencies greater than 15% were produced on buffered, commercially available Pilkington TEC Glass at EPIR Technologies, Inc. (EPIR, Bolingbrook, IL) and verified by the National Renewable Energy Laboratory (NREL). n-CdS and

p-CdTe were grown by chemical bath deposition (CBD) and close space sublimation, respectively. Samples with sputter-deposited CdS were also investigated. Initial results indicate that this is a viable dry process alternative to CBD for production- scale processing. Published results for polycrystalline CdS/CdTe solar cells with high efficiencies are typically based on cells using research-grade transparent conducting oxides (TCOs) requiring high-temperature processing inot conducive to low-cost manufacturing. EPIR's results for cells on commercial glass were obtained by implementing a high-resistivity SnO_2 buffer layer and by optimizing the CdS window layer thickness. The high-resistivity buffer layer prevents the formation of CdTe-TCO junctions, thereby maintaining a high open-circuit voltage and fill factor, whereas using a thin CdS layer reduces absorption losses and improves the short-circuit current density. EPIR's best device demonstrated an NREL-verified efficiency of 15.3%. The mean efficiency of hundreds of cells produced with a buffer in the first year of this effort is 14.4%. Quantum efficiency results are presented to demonstrate EPIR's progress toward NREL's best-published results.

Disparities in efficiencies between commercial modules and lab scale cells are prevalent throughout the solar industry. This gap is particularly pronounced in the thin-film CdTe market. The CdS/ CdTe solar cell has a maximum theoretical efficiency of approximately 30%, with a more conservative practical limit of around 20%. The industry leader in CdTe solar at the start of this CRADA reported record module efficiencies of 13.4% and a record lab cell efficiency of 17.3%.

EPIR's research to narrow the gap between lab and module efficiencies in this CRADA had two general aspects: (1) improving the cell efficiency while using materials and processes conducive to low-cost manufacturing, and (2) improving the reproducibility of high cell efficiencies. The focus of the research presented here is on improving the efficiency of cells fabricated on commercially available transparent conducting oxide (TCO) coated glass by optimizing the CdS material quality and using a high-resistivity buffer layer to allow the CdS layer to be made thinner. Thinning the CdS enhances the short-circuit current (J_{sc}) by increasing the amount of light reaching the junction. However, film uniformity can become a problem when thinning CdS, and pinholes or other areas of incomplete coverage can lead to localized shorts between the CdTe and the TCO. TCO roughness has to be considered for avoiding TCO/ CdTe shorts; e.g., a smooth TCO will require minimal CdS, whereas a rough TCO requires a certain thickness to cover the entire surface. Shunting paths between CdTe and the TCO greatly reduce the open-circuit voltage (V_{oc}). A thin buffer layer, with resistivity much higher than that of the TCO, can minimize the influence of these shunting paths on the cell performance by isolating the CdTe from the TCO. The use of a buffer layer to improve device performance with thin CdS was investigated as early as 1998. Significant work also was done in the mid-2000s. EPIR uses an undoped SnO_2 layer to serve this purpose. EPIR has seen not only a substantial efficiency gain through implementation of the buffer layer but also a great improvement in the yield of higher efficiency cells. This is particularly interesting considering the use of a commercially available glass/TCO and the potential for these relatively simple and scalable improvements to achieve such impressive gains.

Typically, EPIR uses chemical bath deposition (CBD) to grow CdS. This is a slow, batch-style process that generates a substantial amount of waste, making it more difficult to scale to production levels than alternative dry deposition methods. Although excellent results have been achieved with the CBD process, EPIR is exploring sputtered CdS as an alternative dry deposition

method that is more easily scalable and more conducive to in-line processing. Sputtered CdS has shown promising results elsewhere. Some of EPIR's results from this work are presented here.

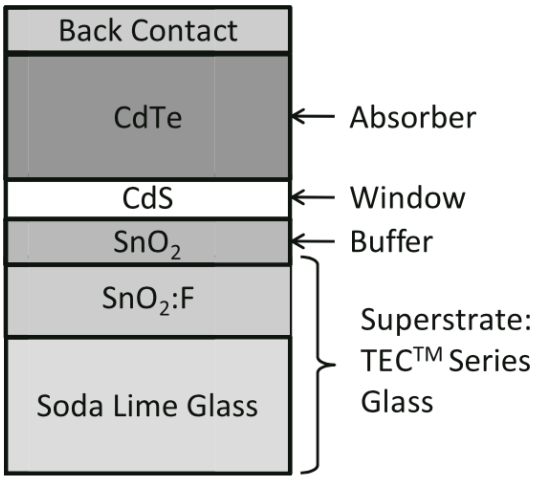

Fig. 1. Polycrystalline CdTe solar cell device structure.

EPIR used a typical polycrystalline CdS/CdTe device structure with commercially available Pilkington TEC Glass as a superstrate. This superstrate is a soda lime glass with fluorine doped SnO_2 (SnO_2:F) as a TCO. After a simple solvent clean, a thin SnO_2 buffer layer was grown by chemical vapor deposition (CVD) at the National Renewable Energy Laboratory (NREL). We chose to prepare the undoped SnO_2 layer for improved process control at the lab scale; however, the CVD process is highly scalable. Oxygenated CdS is then grown by CBD. The thickness, oxygen content, and quality of the CdS layer are optimized by controlling the deposition rate, the precursors, and the deposition time. Because CBD is a batch process, a witness sample with nearly identical CdS material properties can be analyzed alongside wafers that have undergone further processing. CdTe was grown by close space sublimation (CSS) in a helium and oxygen environment, where oxygen facilitates CdTe nucleation on the CdS surface. A second CSS chamber was then used for a dry $CdCl_2$ annealing process. Photolithography followed by a nitric phosphoric (NP) etch was then performed prior to a proprietary back-contact deposition and anneal. The NP etch creates a highly p-type region near the back contact for improved contact quality. Wafers comprise sixteen 0.5-cm x 0.5-cm cells. EPIR's sputtered CdS cells undergo identical processing steps except that the CdS is deposited in a sputtering chamber at NREL as opposed to being deposited by CBD at EPIR.

Current–voltage (I–V) characteristics were obtained from completed devices using EPIR's solar simulator (Newport Oriel), which is equipped with an AM1.5G spectral filter. Devices of particular interest were sent to NREL for certification. In addition to first and second [fill factor (FF), V_{oc}, J_{sc}] level metrics, additional device parameters are extracted through further modeling of I–V characteristics. The model developed at EPIR initially segments the I–V curve into regions where certain behaviors are expected to dominate. The model then iteratively fits the entire curve starting by weighting the parameters dominant in each region appropriately and fitting them all simultaneously through the Levenburg-Marquardt technique. However, when comparing results from cells sent to NREL, the relative difference between the NREL results and those obtained at

EPIR was less than 2%. Quantum efficiency (QE), capacitance–voltage (C–V), and time-resolved photoluminescence (TRPL) measurements were also performed at NREL for some devices to gain more detailed information about the device performances and the limitations on their performance. EPIR measured the transmittance and reflectance of the CdS witness films with a Perkin Elmer LAMBDA 950 spectrophotometer to gain insights into the CdS layer quality prior to Using the device architecture described previ- ously and a series of focused process optimizations, EPIR has produced multiple polycrystalline CdS/ CdTe solar cells on commercially available TCO coated glass with efficiencies above 15%. The best device without an antireflection coating (ARC) exhibited an NREL verified efficiency of 15.3%.

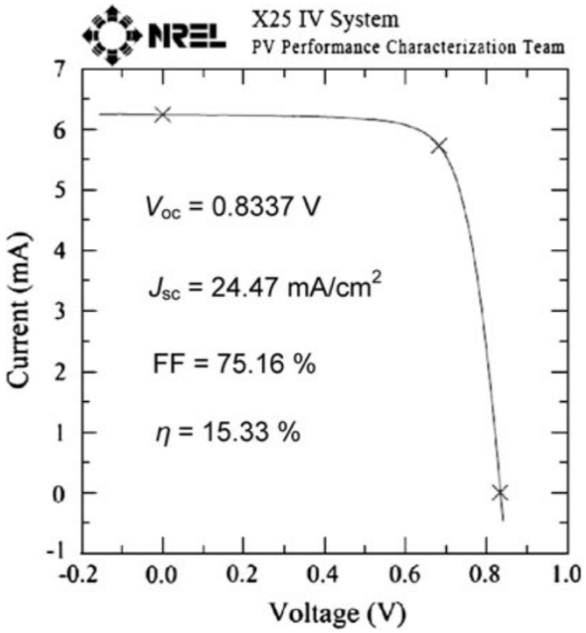

Figure 2. Illustration of certified NREL current voltage results for pX cell.

The implementation of a buffer layer has been crucial in achieving these results. The NREL deposited buffer layer was implemented after the 12.02% cell was tested. Within the next 6 months, the obtained cell efficiencies increased 3.2 absolute percentage points. The values obtained for J_{sc}, V_{oc}, and FF all increased. The J_{sc} increase was directly related to the thinning of the CdS, which reduced absorption losses in the window layer. The FF and V_{oc} values were maintained and even increased through implementation of the buffer layer.

QE data for a production module from a large-scale manufacturer, NREL's best lab cell, and EPIR's 15.3% cell were compared. In addition to an ARC, NREL's best lab cell used a high-quality, high-temperature, TCO. The overall lower QE of EPIR's cell compared with that of NREL is primarily an effect of decreased glass transmission, a lower quality TCO, and the absence of an ARC. The higher quality TCO and glass used in the NREL device have a lower light absorption over the entire spectral range of interest, so the NREL device shows a 5–10% higher QE across this entire range. The thinning of the CdS layer is significant predominantly in the short wavelength region, as light absorption in the CdS occurs primarily in that region. This effect is observed most significantly when comparing EPIR's cell with the production module. EPIR's cell has far better

QE in this short-wavelength region. This is an indication that the production module had a thick CdS layer. If a buffer layer was not implemented, thick CdS is a good way to improve repeatability. A buffer layer can account for this repeatability issue as well and is discussed below. Maintaining a high V_{oc} and FF with the devices using thin CdS deposited by CBD was only possible after the implementation of the resistive SnO_2 buffer layer. These results are among the best reported CdS/CdTe solar cell efficiencies using commercial TCO-coated soda lime glass. Previous publications have reported devices produced on TCO-coated soda lime glass with efficiencies on the order of 15%, but these have not been independently verified.

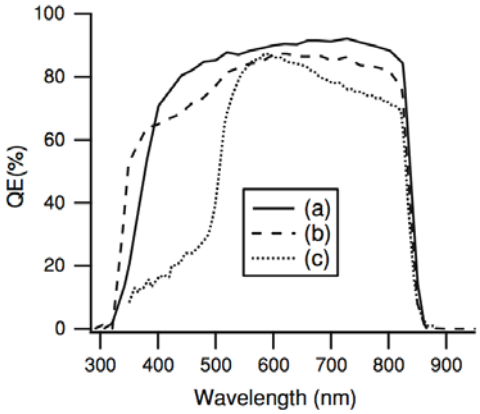

Fig. 3. QE comparing (a) NREL's best lab cell,[1] (b) a 15% cell produced at EPIR measured by NREL, and (c) a sample production cell (not produced by EPIR).[1]

Analysis of C–V measurements on the EPIR devices indicates an average loss of approximately 10 mV in the built-in voltage (V_{bi}) of the junction from thicker to thinner CdS samples with a buffer layer. This loss in V_{bi} is vastly outweighed by the enhanced J_{sc} of the device resulting in an improved overall efficiency of the cells with a thinner CdS layer and a buffer layer. Minority carrier recombination lifetimes derived from TRPL measurements were generally between 1 ns and 2 ns with no significant differences between devices with and without a thinner CdS layer and buffer layer.

Demonstrating good performance in a single cell is important as a proof of concept for the possibility of improving module efficiencies, but obtaining uniformly high-performance cells is also a primary concern. The mean efficiency of all of the hundreds of cells produced at EPIR with a buffer layer after this CRADA increased to 14.4%. The distribution of cell efficiencies is given in Fig. 4. The standard deviation for this distribution is 0.6 percentage points. This result indicates that the implementation of a buffer layer not only improved individual cell performances but also facilitated impressive reproducibility of that improved performance. This consistency is necessary for the manufacturing of solar modules.

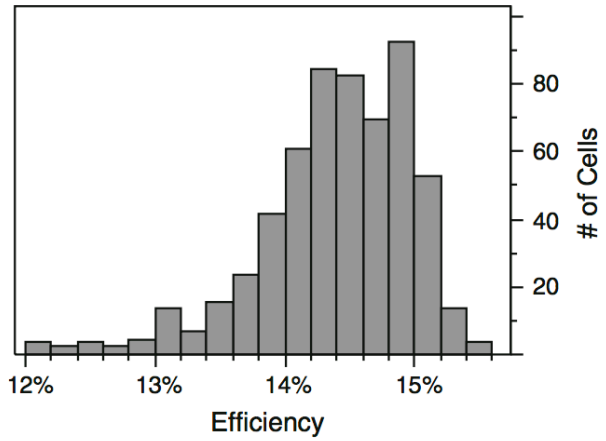

Fig. 4. Distribution histogram of devices with a buffer layer produced at EPIR between December 2010 and June 2011.

Table I. NREL-verified *I–V* characteristics parameters and certification dates

Month of Certification	η	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF
July 2010	12.02%	802	21.97	68.19%
December 2010	15.21%	815	24.03	77.64%
April 2011	15.08%	829	23.87	76.16%
April 2011	15.33%	834	24.47	75.16%

The device models developed at EPIR, as described above, were applied to hundreds of cells with and without buffer layers and the resulting fits were analyzed. The results indicate that increases in both the diffusion current in the bulk region of the CdTe layer (I_d) and the series resistance (R_S) correlate to the presence of the buffer layer. Assuming absorption and carrier generation occur predominantly in the depletion region, electrons and holes can quickly be swept out of the junction by the built-in potential. The electrons then quickly reach the buffer and back-contact considering comparatively thin CdS. The presence of a buffer layer will account for the increase in R_S. The potential loss in the FF as a result of an increased R_S can be compensated for by a vastly improved shunt resistance. The observed improvement in V_{oc} for cells with a buffer cannot come from the R_S improvement, but it can be attributed to the improved I_d seeing as the holes must traverse the bulk CdTe region to reach the back-contact. The observed increase in I_d may be a result of a higher quality CdTe associated with the buffered superstrate, but further investigation would be required. These results indicate that some improvements in our second-level metrics may also be attributed to this unexpected improvement in I_d.

In keeping with the goal of addressing the discrepancy between module and lab cell performance, EPIR investigated cells with CdS deposited by sputtering, as sputtering is a much more readily scalable process than CBD. In an initial experiment targeting sputtered CdS thickness, a 14.8% efficient cell was produced with a CdS thickness similar to that of the CBD-deposited CdS used for the 15.3% EPIR cell. This result was obtained without any process optimization specific to

sputtered CdS and, hence, is highly promising. The sputtered CdS grain size is believed to be strongly related to the oxygen level in the CdS. Oxygen also influences CdS-CdTe interdiffusion, which can greatly influence device performance. This means that the process optimization performed for CBD CdS could be largely irrelevant for sputtered CdS. These preliminary results in device performance indicate that using sputter-deposited CdS as an alternative to CBD CdS is a viable option and with further process optimization could yield cells with higher efficiencies. EPIR has produced high-efficiency polycrystalline CdS/CdTe solar cells on commercial TCO-coated soda lime glass through the implementation of a buffer layer between the TCO and the CdS and the optimization of the CdS material quality and thickness. Not only did the buffer lead to improved device performance, but it also greatly improved yield, reproducibility, and consistency. These results show progress in some of the typical problems that lead to the difference between module and lab-scale cell efficiencies. Finally, preliminary results for sputtered CdS indicate that it may well be a possible dry deposition alternative to CBD.

It is generally acknowledged that performance limitations are due to recombination of photo-generated carriers that limits open-circuit voltage (V_{oc}) and fill factor (FF). To investigate these limitations, NREL and EPIR have undertaken activities to develop what are sometimes called "model devices." In these model devices, the impact of likely recombination mechanisms in polycrystalline CdTe devices are limited and/or controlled. One important pathway toward these model materials and devices is synthesis of CdTe layers using molecular beam epitaxy (MBE). MBE can produce both single-crystal and polycrystalline CdTe layers with controlled stoichiometry, composition, impurities, and crystalline quality. This allows control of bandgap (i.e., alloy formation), doping (i.e., addition of donors and acceptors from either intrinsic or extrinsic defects), and ultimately, control of the bulk and surface recombination properties of the photo-generated carriers (i.e., addition of surface passivation layers and/or processes). Perhaps even more important-and in contrast with most present polycrystalline device-synthesis processes-MBE can allow control of these properties as a function of film thickness, thus (nominally) allowing one the ability to adjust material properties in each region of the device to facilitate optimum performance. For example, if the desired doping in a particular region of the device has a significant negative impact on recombination, then one can design devices that separate the regions of high doping from those of carrier generation.

At the time of the work, relatively few reports detailed the effects of critical synthesis processes that yield the type of high-quality material needed for CdTe-based PV model devices. For example, it is well known that careful incorporation of Group V impurities (e.g., primarily N, P, and As) should enable necessary substitutional acceptor doping on the Te site (i.e., the anion site). These reports also suggest that MBE films with Group V dopants can produce shallow net-acceptor concentrations (N_A) of ~mid 10^{17} cm^{-3}, with even higher N_A values demonstrated in certain dilute alloys, such as CdHgTe or CdZnTe. However, an added requirement for PV model devices is that these N_A concentrations must be achieved while also maintaining sufficient minority-carrier lifetime (MCL, targeting ~10-20 ns). Unfortunately, few reports detailed the limits and/or process functionality of these relationships. Available CdTe doping studies suggest that substitutional Group V doping generally benefits from increasing the relative concentration of the cation (i.e., Cd). This cation addition can be accomplished by adding an auxiliary Cd flux during MBE film growth, using a dopant source that contains an excess of the cation (e.g., $Cd_3 As_2$), or by post-deposition and/or contact anneals that contain a cation source (often Cd or Hg).

Perhaps not surprising, this work indicates that structural and optoelectronic properties of undoped CdTe crystalline films can also be sensitive to the environment during growth. This observation is important because understanding how the synthesis process affects undoped CdTe materials is likely to provide key guidance for the synthesis of doped CdTe and related alloys. Specifically, the studyies reported here show that careful addition of Te during MBE growth of undoped CdTe can have a significant and beneficial effect on the structural and optoelectronic quality of a CdTe heteroepitaxial film. This result may be somewhat unexpected, because evolving theoretical predictions and recent experimental observations may suggest a preference for Cd-rich growth conditions. However, because this study shows growth stoichiometry impacts both bulk and interfacial properties, these results help to remind us that it is generally prudent to view materials-development activities in a sufficiently broad context as device-fabrication studies commence.

The CdTe heteroepitaxial layers analyzed in this study were produced with a RIBER Opus 5-inch MBE system (using 3-inch Si wafers). The CdTe/Si heteroepitaxy techniques incorporated have been developed over the past 25 years and include the use of a double-side polished (211) 3-inch-diameter Si wafer that is boron doped to 30–70 ohm-cm. The wafer is cleaned ex situ using a modified RCA cleaning process, after which the substrates are loaded into the MBE system. Systems were pumped to pressures < 1 x10^{-9} torr, where the substrates undergo a dehydration bake at ~400°C, followed by a thermal oxide strip at >1000°C (note that all MBE temperatures quoted are uncorrected thermocouple values). Deposition of CdTe layers on Si begins with the fabrication of a multilayer, lattice-accommodating "template." Although the template layer can vary depending on intended application, the template produced for this study included a sub-monolayer of As followed by ~15 nm of ZnTe. In this template design, the As layer passivates dangling bonds at the Si, improving structural and adhesion integrity, whereas the ZnTe pseudomorphic layer maintains the (211)B orientation (i.e., the passivation layer is thinner than the critical thickness at which misfit dislocations occur). The ZnTe layer is deposited using migration-enhanced epitaxy, where beam flux from elemental sources of Zn and Te (99.99999% purity) are alternated with a short time between atomic layers to allow surface migration to improve two-dimensional growth. Following ZnTe deposition, the substrate temperature is reduced to the CdTe growth temperature of 325°C.

Although CdTe layers used for HgCdTe devices are generally about 10 microns (and are called CdTe buffer layers), this study included CdTe layers that were both thinner and thicker to allow correlation of the optoelectronic properties of the CdTe layer with structural properties. (CdTe thicknesses varied from 6 to 18 microns). All the CdTe films produced were undoped and deposited using co-deposition from nominally stoichiometric CdTe and Te effusion sources (99.99999%-purity). These two sources were controlled to produce a growth rate of 1 micron per hour.

Films were analyzed using a combination of techniques. Analyses included film-thickness uniformity using mapping infrared (IR) spectroscopy (~35-point maps, Fourier transform infrared spectroscopy [FTIR]) in the wavenumber range of 400–6000 cm^{-1} [using a Thermo Nicolet Nexus model 870 FTIR spectrometer with KBr beamsplitter and DTGS-TEC detector]. Surface-quality uniformity was performed using a combination of multi-point Nomarski optical imaging (5-point), whole-wafer optical image capture of low-angle scattered white light. Crystalline uniformity was assessed using mapping X-ray diffraction double-crystal rocking curve (DCRC, std. dev. calculated from ~35-point maps of the full width at half maximum [FWHM] of the CdTe <422>

peak [Bruker AXS Diffraktometer D8 with a high-resolution X-ray diffraction system employing a Ge(200) four-bounce beam filter for the Cu $K\alpha$ source]).

Analysis at NREL included electron backscatter diffraction (EBSD) to assess if the films demonstrated any polycrystalline artifacts (EDAX Pegasus system with Hikari EBSD detector, housed in a field-emission scanning electron microscope FEI Nova 630). Cross sections of "cleaved" films for EBSD were ion-beam milled for 5–10 h using a JEOL ion-beam cross-section polisher operated at 4 kV. Room-temperature 2-photon excitation time-resolved photoluminescence (2PE-TRPL) was performed at an analysis wavelength of 820 nm, using an excitation wavelength of 1120 nm, a laser repetition rate of 1.1 MHz, and 0.3-ps laser pulses. Because the two-photon absorption coefficient is much lower than a one-photon absorption coefficient, carriers are generated nearly uniformly throughout the volume defined by the excitation beam size and the 6 to 18 film thickness.

ID	Thickness (µm)	Te Over-pressure (%)	DCRC (arcsec)	DCRC St.Dev. (arcsec)	2PE-TRPL (ns)
W13009	10.7	20	74	2.8	1.8
W13007	10.0	0	102	80.7	1.2
W13010	6.3	12	109	11.4	1.1
W13008	18.0	0	67	40.2	1.7
W13028	14.8	33	73	2.5	1.7
W13029	14.4	12	71	3.1	2.3

Table II. Structural and electro-optical analysis of undoped CDTE layers grown heteroepitaxially on (211) SI substrates. Top three samples are "thin" for this study, whereas bottom three samples are "thick."

The table shows representative sets of samples that have been produced. In these sets, both CdTe thickness and Te overpressure have been varied in an attempt to determine which, if either, of these parameters may be dominating the structural and/or optoelectronic properties of the CdTe layers. For the purpose of this analysis, "thin" CdTe layers are roughly less than 10 microns (top three samples in Table), whereas "thick" layers are > 12 microns (bottom three samples). Although inspection of the measured results of this table suggests some systematic trends, the next figure shows a plot of these same data-where both optoelectronic quality (2PE-TRPL, left axis) and the structural quality (DCRC, right axis) are plotted as a function of Te overpressure.

The results demonstrate the following trends: 1) Regarding structural quality, if the films are "thick", then DCRC analysis generally reveals a "low value" of ~67-73 arcsec. This value is considered consistent for the eventual needs of the CdTe absorber for use in high-performance PV devices. However, if the films are "thin", then resulting DCRC values are generally higher, ranging between 74 and 109 arcsec. It is noteworthy that for these thinner films, the film with higher structural quality (i.e., 74 arcsec) is observed when the Te overpressure is higher. Further, as noted in the Table, the standard deviation (std. dev.) of the DCRC data for films deposited without Te

overpressure is very large, indicating that the variation of film structural quality across the 3-inch wafer is very significant if Te overpressure is not incorporated during growth.

Regarding optoelectronic quality, as assessed with 2PE-TRPL analysis, the figure below shows that the "thick" CdTe films demonstrate what are considered here to be "good" minority-carrier lifetime for unpassivated CdTe layers, with values of 1.7 to 2.3 ns. In contrast, the "thin" films show a lower value of 1.1-1.2 ns. Results in the range of 1.1-1.2 ns might be expected for unpassivated layers (i.e., because photo-produced carriers in the thicker film will be, on average, generated farther from the surfaces of potential recombination). However, it is again noteworthy that the minority-carrier lifetime for the thinner layers increased to the range of the thicker films-when a Te overpressure is added during deposition.

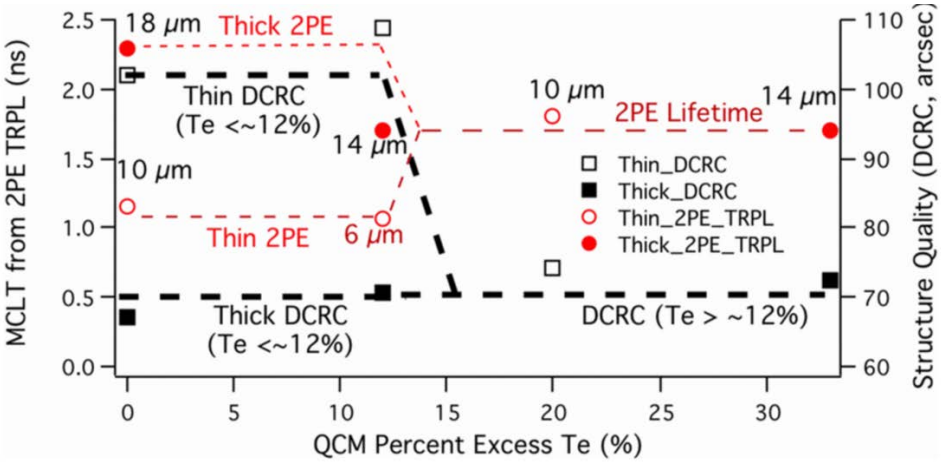

Fig. 5. Change in both structural properties (measured by dcrc) and minority-carrier lifetime (measured by 2pe-trpl) for undoped CdTe layers grown by MBE as a function of Te overpressure as measured as percent excess Te condensed onto a quartz-crystal microbalance relative to the deposition rate of CdTe. note that, the std. dev. for the structural data for samples with Te overpressure is approximately the size of the data points, however, for the two samples without Te overpressure, the std. dev. is too large to show on the figure.

Taken together, the results shown in Fig. 5 suggest that careful incorporation of Te overpressure can increase the structural and optoelectronic quality of CdTe films grown by MBE, as well as significantly improve the uniformity of these parameters across the wafer surface. This appears to be especially true if the films are deposited at a thickness less than 10 um.

The correlation of structural and optoelectronic analyses (DCRC and 2PE-TRPL) described above suggests that the Te overpressure improves both structural and optoelectronic quality, especially of thin CdTe films. However, it must be considered that both the DCRC and 2PE-TRPL analysis techniques probe relatively deeply into the bulk of the CdTe heteroepitaxial films; thus, details of the effect of Te overpressure, especially as a function of depth, remain uncertain. To investigate this, EBSD cross sections were analyzed near the Si/CdTe interface for several undoped heteroepitaxial CdTe films. Although initial plan-view EBSD analysis confirmed that Te overpressure during growth improved structural quality, the surfaces formed during the cleaving of the CdTe films were too rough for optimum EBSD. For this reason, several of these samples

were subjected to further sample preparation using cross-sectional ion-beam milling to reduce surface roughness and to suppress any cleave-induced structural artifacts.

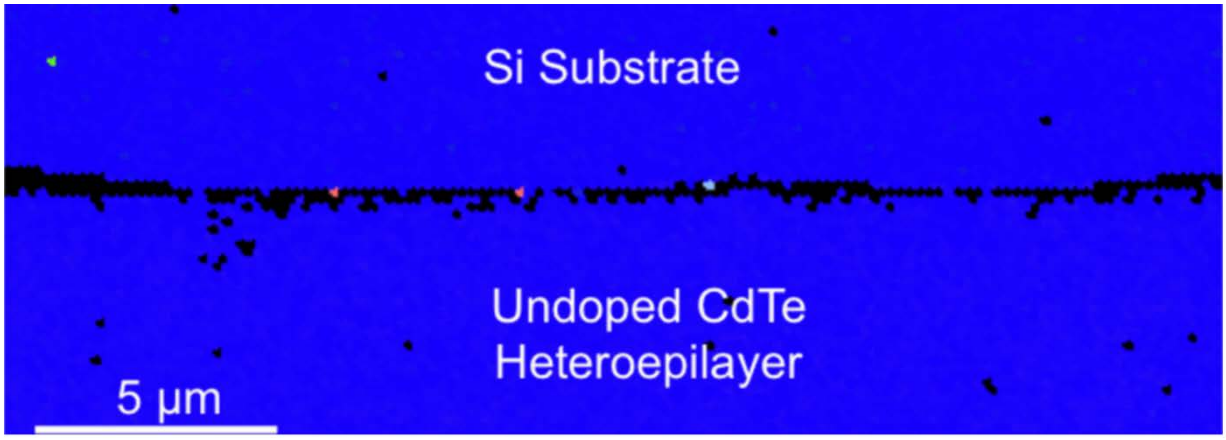

Fig. 6. Si/cdte heterointerface region for MBE-grown undoped CdTe layer without Cd or Te overpressure (sample w13026). Total undoped CdTe film thickness for this sample is 11 microns.

Figure 6 shows EBSD analysis of an ion-beam-milled cross-section of the initial 5 microns of undoped CdTe grown heteroepitaxially on Si (total undoped CdTe film thickness for this sample was 11 um. The figure shows that the EBSD software was able to correlate the resulting EBSD Kikuchi patterns to known crystalline orientations for the majority of the Si and CdTe layer. However, as indicated by the dark artifacts in the image, some regions of the bulk CdTe could not be correlated, especially near the interface between the CdTe film and Si substrate. Further, because the width of this interface region generally contains 3- 5 EBSD pixels, it is likely this represents actual structural disruption at the CdTe and Si interface, rather than an EBSD analysis artifact. This observation is not unexpected, because the lattice difference between (211) Si and CdTe is significant. Specifically, although the As and ZnTe accommodation "template" layers are known to produce CdTe films with sufficiently high quality for IR detectors, the EBSD-measured misorientation between the surface normal directions for the Si and CdTe layers remains at ~3°-4°. Although EBSD analysis of undoped CdTe films grown under Cd-rich conditions has not yet been performed, analysis of CdTe films that were doped lightly with $Cd_3 As_2$ (i.e., As content at mid 10^{15} cm^{-3}) shows very similar results to that shown in Fig. 6. Initial high-resolution EBSD analysis of this disordered region has not yet revealed significant additional insight.

Within the context of the results discussed above for Fig. 6, Fig. 7 shows a relatively surprising result. First, for similarly prepared Si/CdTe cross-sections, if the CdTe was deposited with a Te overpressure, EBSD analysis reveals significantly fewer regions in the CdTe film where the Kukuchi pattern could not be correlated (i.e., the crystal quality of the entire CdTe films appears higher than for film shown in Fig. 6). Second, the interface region between the Si and CdTe contains significantly less structural disruption. This is true even though the EBSD-measured misorientation in the samples produced with Te overpressure (Fig. 7) is the same as for the sample shown in Fig. 2 (i.e., ~3°-4° for both samples). It should also be noted that the undoped film shown in Fig. 6 is significantly thicker than the film shown in Fig. 7 (i.e., ~11 µm vs. 5.5 microns, respectively). Because the thinner film (Fig. 7) demonstrates higher structural quality than the thicker film (Fig. 6), this supports the trends identified by DCRC analysis of Fig. 5 that Te overpressure facilitates higher structural quality, especially for CdTe heteroepitaxial films.

Based on previous technology to obtain high- quality CdTe and CdZnTe epitaxial buffer layers on silicon substrates for infrared (IR) applications, there is a potential for II–VI monolithic multijunction solar cells based on a Si bottom cell with the promise of a conversion efficiency as high as, if not higher than, that of their III–V-based counter- parts. Compared with Ge or GaAs, Si has a more ideal band gap (E_g) for the bottom junction of a two-junction (tandem, 2J) or three-junction (3J) cell configuration. Theoretical values of both the Shockley–Queisser and ‘‘standard model’’ efficiency, assuming a fixed ideality factor, for III–V- based multijunction cells have been shown to be lower than those of II–VI-based 2J or 3J cells. Additionally, concentrator photovoltaic systems on the ground could become a viable possibility, especially with a low-cost crystal Si solar cell market.

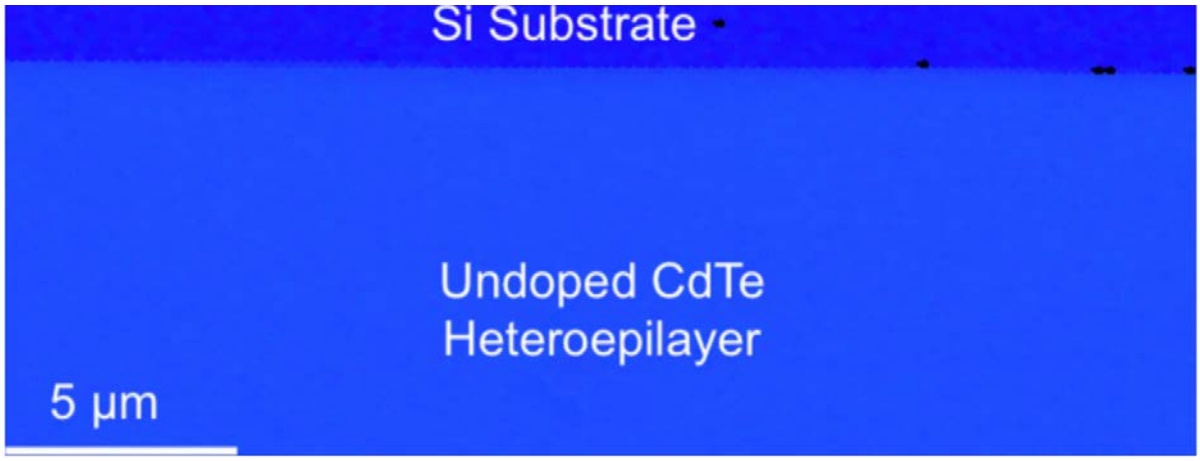

Fig. 7. Si/CdTe heterointerface region for MBE-grown undoped CdTe layer with 14% Te overpressure (sample w13042). Total undoped CdTe film thickness for this sample is 5.5 microns.

A possible II–VI-based triple-junction device con- figuration is shown in Fig. 8. Here, $Cd_{1-x}Zn_xTe$ with a high x-value would be used for the large-gap top cell, $Cd_{1-x}Zn_xTe$ with a low x-value would be used for the middle-gap center cell, and Si would be used as the small-gap bottom cell. To achieve such a device, high-quality CdZnTe grown on single-crystal Si needs to be fully understood. The improved efficiency of a multijunction photovoltaic device, compared with a single-junction device, relies on the voltage addition of the monolithic junctions. As such, high doping in the absorbers is desired to establish a high open-circuit voltage. Current management in a monolithic multijunction device is also critical. High-quality tunnel junctions to connect the monolithic devices would be used to ensure limited charge buildup. This would also require a high level of both doping and layer thickness control. A molecular beam epitaxy (MBE) system offers

a high level of layer and material quality control, but in situ doping techniques need to be developed to minimize the number of post- growth high-temperature anneal or activation steps that may adversely affect previously grown layers.

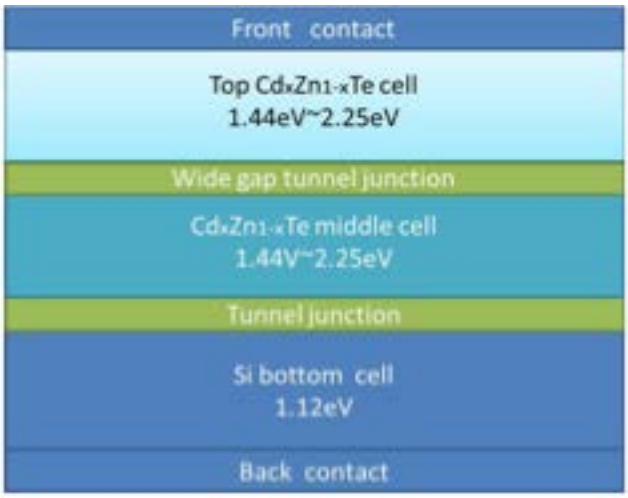

Fig. 8. Example CZT/Si-based multijunction device structure.

Previous work showed that p-type doping of CdZnTe using a nitrogen direct current (DC)-plasma source could be an effective method for in situ stable doping without activation anneals. Here N has to occupy V_{Te} (vacancy at Te site) to form a shallow acceptor. Additionally, previous experimental results indicate that the doping efficiency varies for various II–VI compounds. Cd overpressure is often used in Cd-based alloys such as CdZnTe to promote the formation of V during Te growth and therefore improve the probability that the N will occupy a Te site. To optimize CdZnTe/Si-based monolithic devices, we investigated the p-type doping of MBE- grown CdZnTe films on Si(211) substrates using an RF-nitrogen plasma source without Cd overpressure. CdZnTe(211):N/Si(211) samples were grown in a RIBER Compact 21 system with an RF-plasma nitrogen source. Before growth, the substrates were prepared by a standard RCA cleaning process. Then the substrates were heated up to 850°C in the growth chamber to remove the surface oxide. After exposure to As flux at high temperature for As passivation, a thin ZnTe buffer layer was deposited and in situ annealed to compensate lattice mismatch and preserve the (211) orientation. Single crystal $Cd_{1-x}Zn_xTe$ films were deposited with various thicknesses and Zn concentrations by changing the source flux ratio (CdTe/ZnTe) and deposition time. Growth rates were on the order of 0.8 um/h with a substrate temperature of about 250°C. These conditions correspond to a total beam equivalent pressure of 10^{-6} Torr (sum of CdTe and ZnTe). Typically, an undoped, high-resistivity, layer was grown first, followed by a nitrogen-doped layer. Subsequent electrical characterization of the CdZnTe can then be more directly associated with the doped layer on top rather than the underlying substrate layers.

The nitrogen flux was produced by a model RF4.5 plasma source supplied by SVT Associates, Inc. We could stably operate within a range of 0.01 sccm to 3.00 sccm flow rates using a custom, low-conductance nozzle. The ion content of the beam was reduced by electrostatic deflector plates across the nozzle exit. This deflection voltage reduces the beam pressure by about one order of magnitude, which indicates a high ion content in the native beam. The total amount of nitrogen incorporated into the CdZnTe epitaxial layer was adjusted by Ar gas dilution from 1% to 100%. The typical background pressure during this process was 10^{-6} Torr.

The CdZnTe structural quality was characterized by the full-width at half-maximum (FWHM) of x-ray double-crystal diffraction rocking curves. The Zn compositions of the CdZnTe layers were determined by the peak position of the $2h_{(422)}$ angle based on Vegard's law. The thickness of the CdZnTe layers was measured by a Fourier-trans- form IR spectrometer. Nitrogen doping and atomic concentration were characterized through room- temperature Hall measurements in the van der Pauw configuration and secondary-ion mass spectrometry (SIMS).

Here, the CdZnTe structural quality varies drastically as a result of process optimization. Better structural quality of the low- and high-Zn- concentration samples was expected considering the significantly more uniform lattice spacing in the binary system compared with the ternary system. The correlation of film thickness to structural quality was also expected considering the improved lattice relaxation as the layer grows away from the highly stressed heteroepitaxial junction region.

We compared the Hall measurement results of CdZnTe:N/Si heteroepitaxial layers with previous results of Baron's study of CdZnTe:N/CdZnTe homoepitaxial layers. Relatively higher carrier concentrations and mobilities were obtained. Unlike III–V compound solar cells, the electrical properties of CdTe-related materials are less sensitive to dislocations and other defects because of its more ionic and less covalent bonding nature. The maximum carrier concentration of 5×10^{19} cm^{-3} with a mobility of 22 cm^2 /Vs was reached for $Cd_{0.48}Zn_{0.52}Te$/Si. Meanwhile a gradual doping level decrease associated with the Zn content was observed.

To further understand the N-doping efficiency, the SIMS depth profile of a typical CdZnTe:N sample was obtained. Two different doped layers using 1% N/Ar and 100% N/Ar nitrogen diluted plasma were grown on undoped CdZnTe, as shown in Fig. 9. Unlike nitrogen RF-plasma doped CdTe, our doped layers were more uniform without nitrogen accumulation at the interface between doped and undoped layers. However, there was only a ten times nitrogen concentration difference between the diluted N-plasma (about 1% N) and the pure N-plasma grown layers. Pure N-plasma indicates an apparently low dopant solubility of N from N–N compensation or interstitial defects.

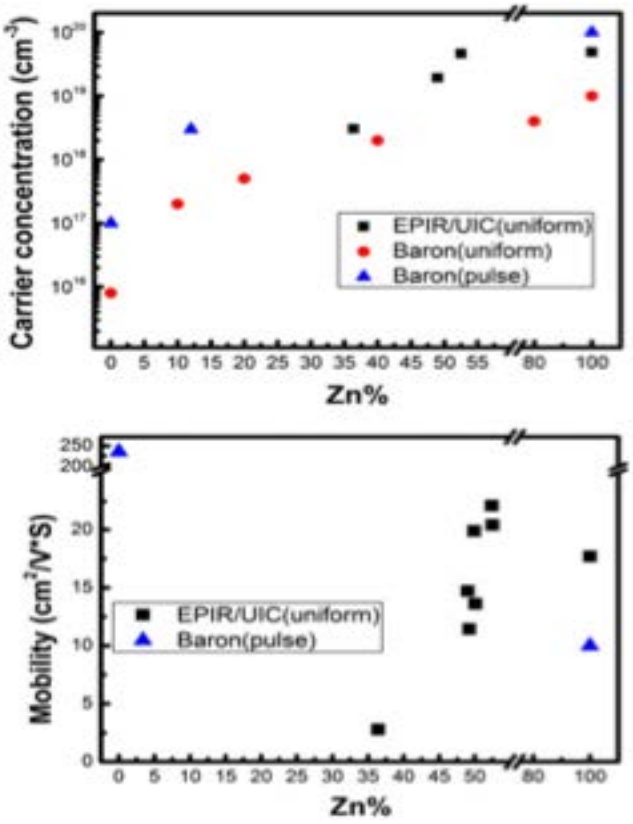

Fig. 9. Hole concentration (top) and mobility (bottom) versus Zn concentration. Results from Baron et al. are plotted from Refs. 6–8. Baron compared both uniform and pulse doping techniques. UIC/ EPIR have only investigated uniform doping.

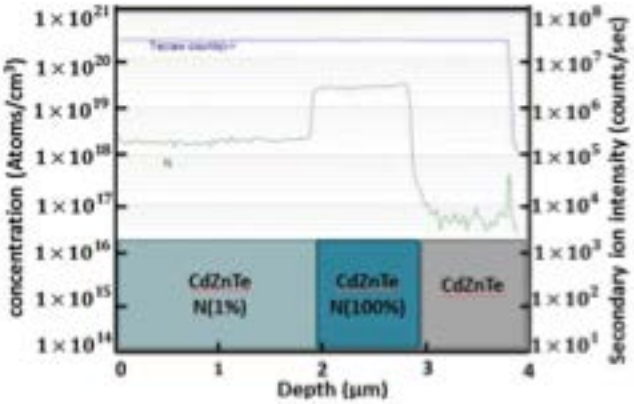

Fig. 10. SIMS profile for sample grown to examine nitrogen incorpo- ration. The incorporation difference between the regions with 1% nitrogen versus 100% nitrogen is only a factor of 10, indicating a saturation effect.

Further optimization of the doping processes was required to improve doping levels in CdZnTe. Because of the role of Zn in CdZnTe, increasing the Zn content could increase the doping level in

CdZnTe. With an increase of only a few percent of Zn, the carrier concentration can increase by an order of magnitude. Meanwhile, because the formation energy of N–N complex defects and interstitial N_2 is higher than that of N_{Te}, the doping level could possibly be enhanced through optimization of the dilution level of N-plasma.

P-type doping of molecular beam epitaxy-grown CdZnTe:N/Si using an RF-plasma source indicated that high-quality heteroepitaxial layers were obtained for both high and low Zn concentration levels. Results from room-temperature Hall measurements indicated good electric characteristics, even better than previous results.

In summary, the work has demonstrated paths towards efficiency polycrystalline solar cells at EPIR, along with developments in understanding of stoichiometry and N doping effects for pX materials and tandem applications being pursued at EPIR.

Subject Inventions:

None

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