Advanced Photovoltaic Inverter Control Development and Validation in a Controller-Hardware-in-the-Loop Test Bed

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Advanced Photovoltaic Inverter Control Development and Validation in a Controller-Hardware-in-the-Loop Test Bed

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***Abstract*—Penetration levels of solar photovoltaic (PV) generation on the electric grid have increased in recent years. In the past, most PV installations have not included grid-support functionalities. But today, standards such as the upcoming revisions to IEEE 1547 recommend grid support and anti-islanding functions-including volt-var, frequency-watt, volt-watt, frequency/voltage ride-through, and other inverter functions. These functions allow for the standardized interconnection of distributed energy resources into the grid. This paper develops and tests low-level inverter current control and high-level grid support functions. The controller was developed to integrate advanced inverter functions in a systematic approach, thus avoiding conflict among the different control objectives. The algorithms were then programmed on an off-the-shelf, embedded controller with a dual-core computer processing unit and field-programmable gate array (FPGA). This programmed controller was tested using a controller-hardware-in-the-loop (CHIL) test bed setup using an FPGA-based real-time simulator. The CHIL was run at a time step of 500 ns to accommodate the 20-kHz switching frequency of the developed controller. The details of the advanced control function and CHIL test bed provided here will aide future researchers when designing, implementing, and testing advanced functions of PV inverters.**

Keywords—controller-hardware-in-the-loop, advanced inverter control functions, inverter testbed.

I. INTRODUCTION

The integration of distributed photovoltaic (PV) generation into the distribution system is on the rise. Because of high penetration levels, grid operators and interconnection standards encourage the use of advanced grid support functions to operate inverters. Test cases in the literature consider the impacts of these functions on the stability and operation of distribution system [1]-[2]. Recently, PV standards have supported the notion of voltage and frequency control at the point of common coupling to provide grid support during power system disturbances [3]-[4]. The literature [5]-[6] also support the use of ramp-rate limits on the rate of change of the real and reactive power injected into the grid. PV inverters should also ride through grid disturbances for a period of time specified by the standards. In [7]-[9], dedicated controls are added to the low-level current controller to enable such ride through capabilities. Finally, in case of a grid blackout, PV inverters should identify the event, island themselves, and stop supplying load. The authors of [10] discussed the compatibility between the ride-through controls and anti-islanding methods and proposed a compatible control approach. The current literature tackles two of the many advanced inverter functions and proposes controls that work with each other, however, there is a lack of understanding in the literature of all of the different advanced inverter functions working in harmony. In this research, we develop an inverter controller that is capable of integrating the different grid support functions in a coordinated manner, and we test it in a simulation using a controller-hardware-in-the-loop (CHIL) test bed setup. This is the first contribution from this research.

This research also addresses another challenge in the development of inverter controllers: testing inverter controls that switches at high frequencies. The authors of [11] proposed a microgrid testbed. In this testbed, inverter control could be tested, but it could handle switching frequencies within the range of only a few kHz. The second contribution from this research is the CHIL test bed setup that runs at time step of 500 ns, thus enabling testing of inverters that switch at higher rates. The proposed current control-based lower level switching controller runs at 20 kHz.

In the research presented here, voltage/frequency control, ramp rate control, and anti-islanding functions were developed and tested in simulations. The algorithms were programmed using an off-the-shelf embedded controller that includes a dual-core computer processing unit (CPU) and field-programmable gate array (FPGA). Because the proposed CHIL test bed runs at a time step of 500ns, users can test inverter controllers with switching frequencies up to tens of kHz. Controls based on a look-up table for volt volt-ampere reactive (VVAR), volt-watt (VW), and frequency-watt (FW) are developed to provide voltage/frequency support. In addition, ramp-rate control, ride-through for voltage and frequency, and anti-islanding control were also developed.

In this paper, the block diagram of the grid support controller functions will be explained first. The lower level switching controller will also be explained. It is then followed by the description of CHIL testbed used to test both the low-level current control and the high-level grid support functions.

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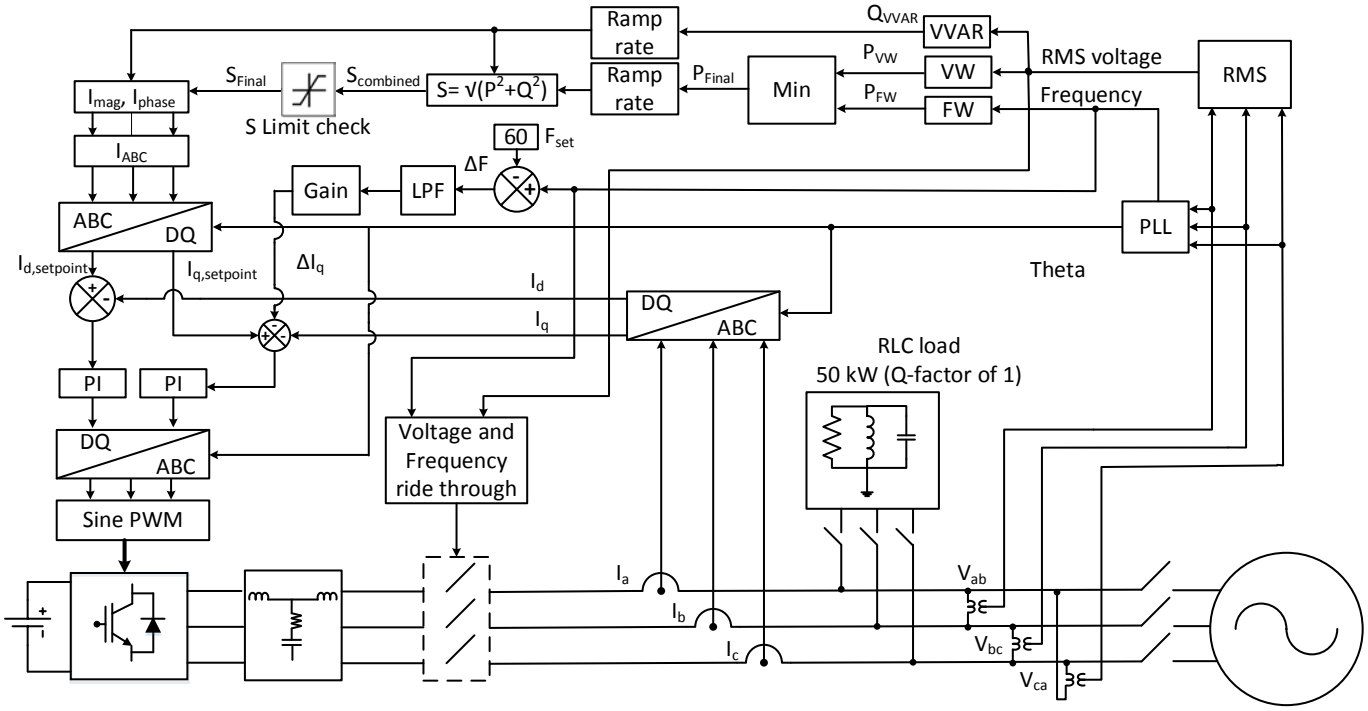


Fig. 1. Control block diagram of the advanced inverter functions developed and tested

Testing the controller in a CHIL testbed is helpful for transitioning the controller from a software model to a prototype and eventually a tested product.

Cases were developed to test the advanced inverter control functions. The results of selected cases from testing the controller in simulations are compared to results from the CHIL testbed. For ease of understanding and consistency, in this paper the term "simulation" indicates experiments performed in pure software simulation and does not involve any real-time simulation.

II. Inverter Controller Description

In this section, a detailed description of the advanced inverter controller will be provided. The controller proposed here work in a coordinated manner to ensure that the control functions of a single inverter with conflicting objectives work harmoniously. This becomes crucial when there is a high level of PV penetration, and a need for tight control of PQ injection/absorption for maintaining dynamic stability. In this paper, the term "coordinated controller" indicates the harmonious operation of different advanced inverter control functions in a controller embedded in a single PV inverter. The term should not be confused with coordination among multiple inverters on a distribution system, which is not the focus of this paper. Fig. 1 shows the block diagram of the advanced inverter controller with the lower level current controller.

A. Lower Level Current Control

The low-level current control algorithms are programmed on the sbRIO FPGA [12] and to regulate current at user-specified magnitude and phase angle. The three-phase inverter control is performed in the rotating synchronous frame, i.e., the dq-frame. The three-phase reference current and voltage

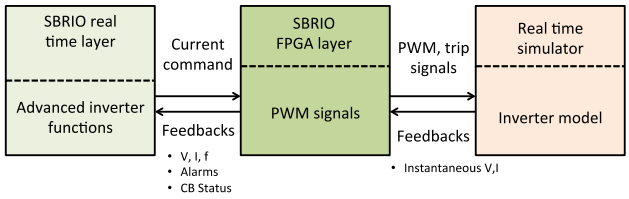
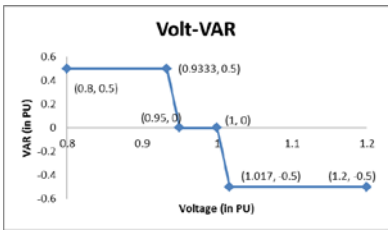


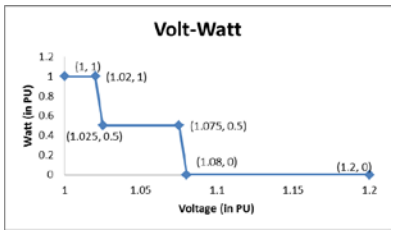
Fig. 2. Controller hardware-in-the-loop setup block diagram

waveforms are converted from the abc-frame to the dq-frame using the Clarke and Park transformations. The reference abc-frame current waveforms are generated relative to the instantaneous angle of the voltage measured on the line-side of the AC contactor, with magnitude and phase angle as set by the user or supervisory controller. A phase-lock loop (PLL) is used to measure the instantaneous angle of the voltage on the line side of the AC contactor, required for the reference waveform generation as well as the Park and Inverse Park transformations. The reference waveform generation algorithms, including the PLLs, execute at 100 kS/s.

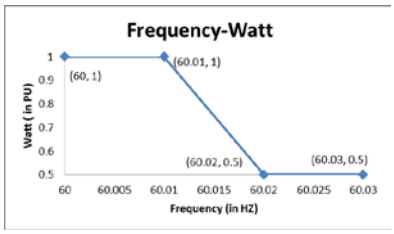
The three-phase sensed current and voltage waveforms are similarly converted from the abc-frame to the dq-frame. The reference and sensed dq quantities are then input to separate d and q PID feedback loops. The PID dq outputs are converted back to the abc-frame using the Inverse Park and Clarke transformations for sinusoidal pulse-width modulation (PWM) output. The control loops execute once per switching period. The control loops are synchronized with the PWM output algorithms to ensure the converter ripple is not aliased into the feedback loop. The control diagram of the lower level current control is included in Fig. 1. In addition to control, the FPGA controller computes the root mean square and real and reactive



(a) Volt-VAR curve used



(b) Volt-Watt curve used



(c) Frequency-Watt curve used

Fig. 3. Curves used in the voltage and frequency control functions

power quantities from the sampled waveforms. These are passed to the real-time controller, as shown in Fig. 2. Fig. 2 shows the location of the different control functions in the sbRIO platform and the data exchange among these layers. This is crucial because the PWM switching signals and other emergency trip signals need to live in the layer which can run at small time step (FPGA layer).

B. Advanced inverter controller function description

The advanced inverter controller function programmed in the sbRIO are VVAR, VW, FW, voltage /frequency ride-through, ramp-rate control and anti-islanding controls. VVAR, VW and FW use the voltage and frequency information to generate real and reactive power reference for the inverter. There are three components in these autonomous frequency- and voltage-based advanced inverter control functions: the input, control decision, and the control signal.

For both voltage-based functions (i.e., VVAR and VW), the input is the grid-side voltage. The control decision is the reactive power set point for the VVAR control and the real power set point for the VW control. These set points are obtained from the curves programmed in the look-up tables for each of these functions. The curves programmed in the look-up tables are shown in Fig. 3 (a) for the VVAR control and Fig. 3 (b) for the VW control. The VW and VVAR curves are designed so that the VW is activated when the VVAR control is exhausted.

For the frequency-based function (i.e., FW), the input is the grid-side frequency. The control decision is the real power set point for the FW control. These set points are obtained from the curves programmed in the look-up tables for the FW function. The curve programmed in the look-up table are shown in Fig. 3 (c) for the FW control. The curves shown in Fig. 3 are for CHIL testing purposes only and to understand the behavior of different curves at test scenario.

Under certain operating conditions, VW and FW might provide conflicting Watt set points. For example, as shown by the curves in Fig. 3, when the voltage is more than 1.026 per unit (p.u.), the VW control provides a set point of 0.5 p.u. In this same scenario, if the frequency is 60 Hz, the watt set point would be 1 p.u. These set points are conflicting in nature. To avoid this conflict, the minimum of the two set points is taken as the reference. This decision is made to reduce the impact of the more extreme event.

The real and reactive power reference values generated by these look-up tables will be used to generate current references for both the magnitude and phase angle. Before these values are used to calculate the current reference, their rates of change are limited by a ramp rate controller. This ramp-rate controller is programmable and depends on the standards and the needs of the utility, which can be modified. After the ramp-rate controller, the real and reactive power references are used to calculate the apparent power value at that reference set point. For example, consider the apparent power rating of the inverter to be 50 kVA. When the voltage is at 0.93 p.u., VVAR will request a reactive power of 25 kVAR (from Fig. 3) and VW will request a real power set point of 50 kW. At this value, the apparent power becomes 55 kVA. During this condition, the controller will give preference to the reactive power support and provide 25 kVAR and 43 kW to keep the apparent power within the 50 kVA limit.

When the reference set points are finalized, the three-phase reference current magnitude and phase angles are generated and converted to the dq axis as shown in Fig. 1. These current signals are the control signal component explained earlier. The d-axis current reference is compared to the actual value and sent to a PI controller. For the q-axis current reference, an additional component is added to the actual q-axis current value for anti-islanding control.

TABLE 1 VOLTAGE RIDE THROUGH SETTING FROM HAWAIIAN ELECTRIC COMPANY'S INTERCONNECTION REQUIREMENTS

Operating region	Voltage setting (in %)	Ride-through until (in secs)
Over Voltage 2 (OVR2)	V > 120	No ride through
Over Voltage 1 (OVR1)	V > 110	0.92 s
Under Voltage 1 (UVR1)	V < 88	20 s
Under Voltage 2 (UVR2)	V < 70	20 s
Under Voltage 3 (UVR3)	V < 50	No ride through

The next advanced inverter control function is the island-detection algorithm. The island-detection algorithms used in this controller is based on an anti-islanding scheme developed by General Electric under a subcontract with NREL [13]. The method incorporates positive feedback of frequency compared to the reactive-axis current command and it will drive the frequency out of bounds during islanded conditions. The signal generated by this algorithm is added to the original q-axis reference current before the actual measured q-axis current is subtracted and the error is sent to PI controller to generate the PWM signal. The current variation (ΔIq) value generated by this algorithm is small during normal operation, but it will continually grow and push the frequency out of nominal operating bounds during an islanded condition. This algorithm is able to detect an island under all real/reactive power flow

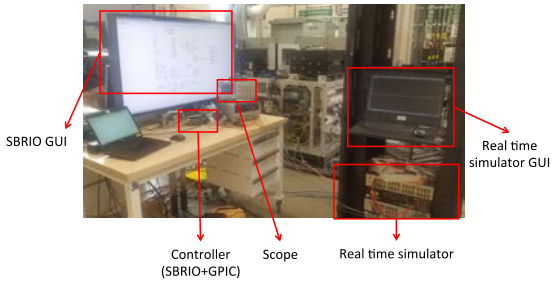


Fig. 4. Controller hardware-in-the-loop lab setup.

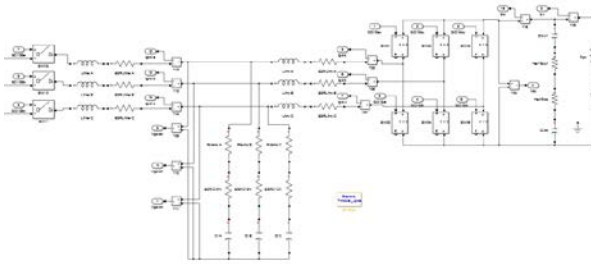
conditions, has minimal impact on power quality, and is robust to grid disturbances.

Finally, ride-through controls are programmed to disconnect the inverter in case of a voltage or frequency disturbance. In the past, standards prescribed disconnect requirements. Currently, standards have "must remain connected" and "must disconnect" requirements. This complicates the development of a coordinated advanced inverter controller. The voltage and frequency ride through controller disconnects or connects the inverter from/to the grid. Examples of the ride-through settings for the advanced inverter control functions are shown in Table 1.

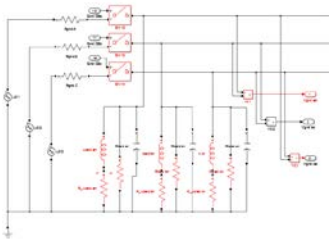
The values used for the ride through controls are adapted from Hawaiian Electric Company's interconnection requirements [14]. There are two set points in both the voltage and frequency ride-through (OVR2, UVR3, OFR2, and UFR2) controls at which the inverter will be tripped. The inverter is programmed to ride through at other operating points (OVR1, UVR1, UVR2, and OFR1, UFR1) as mentioned in Table 1. Ride-through settings from other standards-such as California Rule 21 and the revised IEEE 1547-can also be easily programmed in the controller presented here.

III. Controller-Hardware-in-the-Loop (CHIL) Setup

The sbRIO/GPIC controller was tested using CHIL to verify performance of both the low-level current control algorithms coded on the FPGA and the advanced inverter control algorithms coded on the real-time (RT) controller. The CHIL platform consisted of an Opal-RT OP5600 Simulator plus OP5607 FPGA expansion unit. The OP5607 with embedded Xilinx Virtex7 FPGA allows for the co-simulation of power electronic converters down to time steps 200 ns, with fiber-optic communications back to the power system model running at slower time steps on the OP5600 processor(s). The inverter model is developed using a subset of SimPowerSystems blocks—including power electronic switches, circuit breakers, voltage and current sources and measurements—passive components, and with specific naming conventions as described in [15]. The Opal-RT eHS solver facilitates the compilation and downloading of the model onto the Virtex7 without requiring time-consuming generation of a new bitstream file. Instead, a fixed bitstream file can be used that includes a state-space matrix structure whose entries are populated with model-specific parameters by the eHS solver. The model is then inserted into the parent SimPowerSystems model using eHS interface blocks, in addition to linking to the actual model file, they allow for specifying the model time step



(a) Inverter plus DC input

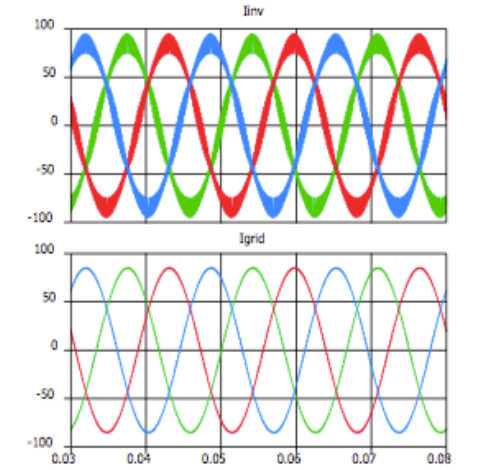


(b) Grid connection

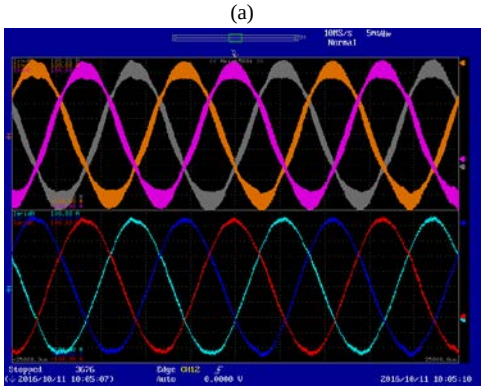
Fig. 5. SimPowerSystems model for field-programmable gate array simulation.

and configuring the model inputs and outputs. In particular, the user can specify whether gate drive inputs (as well as any other inputs) will come from the parent power system model (for pure software simulation) or from the OP5607 digital inputs (for CHIL), and, similarly, whether voltage and current measurements will be output to the parent power system model (for pure software simulation) or to the OP5607 analog outputs (for CHIL). For CHIL simulations, the OP5607 IO update at the model time step. Compilation and execution of the power converter model on the OP5607 and the power system model on the OP5600 is handled via Opal-RT's RT-LAB simulation software. Fig. 2 shows the CHIL block diagram, and Fig. 4 shows a photograph of the CHIL setup.

Fig. 5 shows the inverter model as developed in SimPowerSystems for implementation on the OP5607 FPGA. The figure is split into two parts for better display. Fig. 5 (a) shows the DC input and the inverter, and Fig. 5 (b) shows the grid connection. For this work, the DC input and a Thevenin equivalent grid connection were also included in the FPGA model because the models were sufficiently simple to execute in the fast FPGA time step. More complex feeder models would typically be implemented in a SimPowerSystem model running on the OP5600 processor(s). For the CHIL testing, the eHS block was configured for CHIL with the sbRIO gate drive outputs connected to the OP5607 digital inputs and the sbRIO voltage and current sense inputs connected to the OP5607 analog outputs. The sbRIO trip signal for the circuit breaker was also connected to an OP5607 digital input. Additional measurements were output to the OP5607 analog outputs to allow for the connection of an oscilloscope for troubleshooting and to display the waveform results. The model was run at a time step 500 ns (1% of the switching period), although it is likely that elimination the nonessential IO would have allowed for the simulation at a time step 250 ns.



(a)



(b)

Fig. 6. Comparison of inverter output current waveforms, top: inverter side, bottom: grid side for (a) pure simulation, and (b) CHIL results.

IV. Test Cases and Results

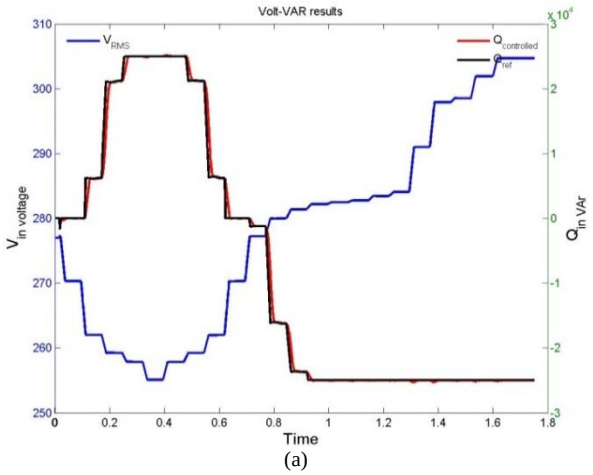
Four test results are shown here to validate the performance of the control blocks. Results from the pure simulation and CHIL are compared where applicable.

A. *Constant Current Control Test:*

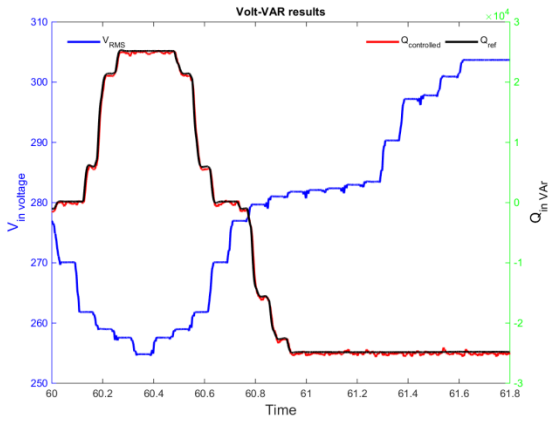
First, in the constant current control test, the inverter is operated at a constant current reference to demonstrate steady-state operation. A constant current reference of 60 A, 0° phase angle is set as the set point. The results comparing the simulation test to the CHIL test are shown in Fig 6 (a) and (b). The results from the constant current control test in the CHIL setup match the simulation result. This result shows that the lower level SPWM based current control works well in both the software simulation and in the CHIL testbed setup.

B. *Volt-VAR control test case*

In the previous case, the lower level current control was tested. In this test case, higher level voltage control is tested. Basically, the higher level control will generate the current magnitude and phase angle set point. The VVAR curves used in this setup is shown in Fig. 2 (a). Ideally, the VVAR control changes the VAR set point and thus the current set point. In most typical VVAR curves, when the voltage is high, the curve tends to absorb VAR to pull the voltage down, and when the voltage is low, the curve injects VAR into the system to push the voltage higher. To reduce the computational time for this test case, the ramp rate was set to a really high value, thus, making it seem disabled.



(a)



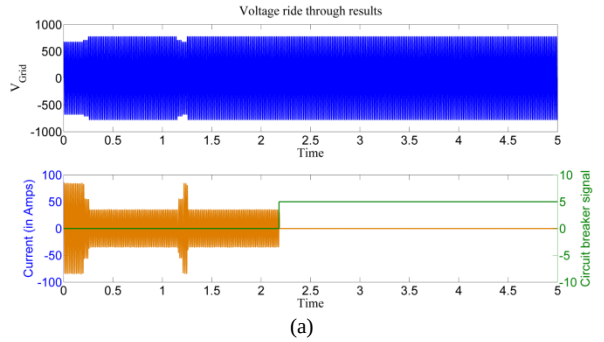
(b)

Fig. 7. Comparison of inverter output for Volt-VAR control in (a) pure simulation, and (b) CHIL results, (Blue = V_{rms}, Black = Q_{ref}, and Red = $Q_{controlled}$ for both cases).

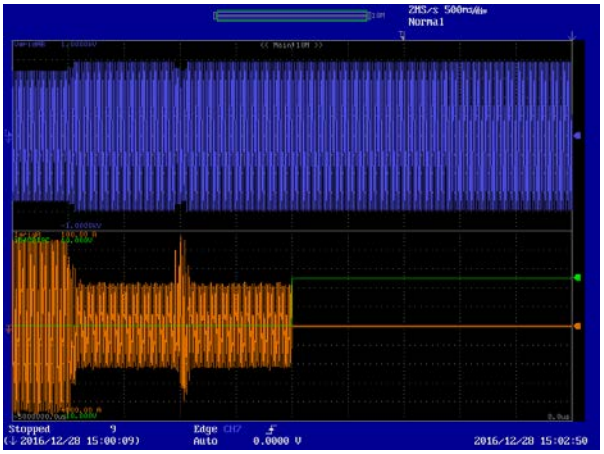
Fig. 7 (a) and (b) shows the VVAR operation compared to the CHIL. Initially, the voltage was stepped down from 1.0 p.u. to a low value, and then it was increased to a high value, until it reaches the maximum VAR injection and absorption, respectively. For this test, the grid side voltage is controlled in steps. The reactive power reference generation from VVAR control and the actual generation/absorption of the reactive power by the inverter is shown in black and red respectively. The reactive power reference generated follows the set points from the VVAR curve shown in Fig. 2 (a). This indicates the proper operation of VVAR controller.

C. *Ride-Through Test Case*

The third case tested the capability of the inverter controls to properly isolate from an unsafe voltage event. For this case, ride-through control was tested by applying a high voltage using the controlled voltage source. Table 1 shows the voltage ride-through values used for this test, and Fig. 8 shows the results.



(a)



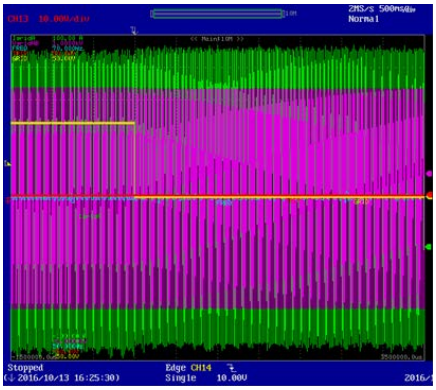
(b)

Fig. 8. Comparison of ride through functions (a) pure simulation, (b) CHIL results (Orange = Ia (20 A/div), Blue = Vab (100 V/div), Green = trip signal).

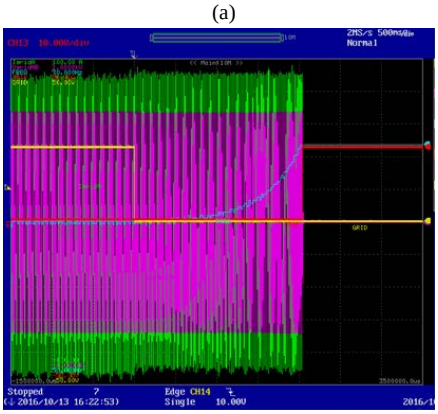
Two sequential high voltage events were programmed: the first required the inverter to remain connected (a high voltage sustained for a short duration), and the second required the inverter to disconnect (a high voltage sustained for a long duration). Initially, the voltage reached 1.15 p.u. and stayed at this level for less than 0.92 s. Table 1 shows that if the voltage is more than 1.1 p.u. and less than 1.2 p.u., the inverter can ride through and will disconnect only if the voltage stays between theses limits for more than 0.92 s. At the beginning of the test, the voltage was kept at 1.15 p.u. for less than 0.92 s. The ride-through controls appropriately did not trip the inverter. This can be observed in Fig. 8. After 1.25 s, the voltage was programmed again to reach 1.15 p.u. During the second event, the high voltage is sustained for more than 0.92 s. At 0.92 s after the occurrence of the high voltage event, the ride-through control tripped the inverter. The results are shown in Fig. 8 (a) and (b). The comparisons between the simulation and CHIL shown in Fig. 8 indicate the proper implementation of the ride-through controller in the hardware.

D. Anti-islanding test case

Finally, Fig. 9 shows the CHIL results with and without the island detection algorithms. This case tests the operation of the island-detection algorithms in the sbRIO. This case follows the test setup and procedures recommended by IEEE 1547.1 [16]. The modeled inverter is operated at a current command of 60 A, phase angle of 0°, and a 50-kW resonant load with Q-factor of 1 was connected to the inverter terminals. The grid was disconnected from the inverter output, and the waveforms were



(a)



(b)

Fig. 9. Anti-islanding testing (a) without active islanding detection, (b) with active islanding detection (Green = Ia (20 A/div), Pink = Vab (100 V/div), Blue = Frequency (2 Hz/div), Red = SBRIO trip signal, Yellow = Grid circuit breaker status).

captured. The plots in Fig. 9 include inverter AB line-to-line output voltage, Phase A output current, frequency as measured by the DL750 oscilloscope, the sbRIO trip signal, and the status of the grid circuit breaker. Fig. 9 (a) shows the case when the island-detection algorithms are disabled, and Fig. 9 (b) shows the case when the algorithms were enabled. All advanced functions were disabled for this test; instead, the sbRIO was configured to trip the inverter offline immediately if the frequency reached 60±5 Hz. Fig. 9 (a) shows that with the island-detection algorithms disabled, the frequency remained constant at 60 Hz and the controller could not detect the loss of grid. Fig. 9 (b) shows that the island-detection algorithm pushed the frequency out of bounds in the event of a grid black out, thus triggering a frequency trip.

V. Conclusion

In this paper, a coordinated advanced inverter controller was proposed, and its working was explained in detail. All the different control functions in the proposed controller work in unison. The controller algorithms were developed and programmed using an off-the shelf controller including a real-time CPU and FPGA. Detailed explanations of the high-level inverter controls programmed on the CPU and lower level inverter current controls programmed on the FPGA were provided. The developed controls were tested using both simulation and a CHIL platform. Four test cases were used to validate the approach: constant current set point, VVAR control, ride-through, and anti-islanding. The results from the

test cases indicate satisfactory performance, and the results from the simulation and the CHIL tests match perfectly.

For the CHIL test bed, the inverter power stage, DC input, and grid connection were modeled on an FPGA, and the model was run at a time step of 500 ns. This allowed the users to test controllers switching at 20 kHz. The comparison between the simulation and the CHIL testbed indicates the proper simulation of the inverter model at very small time step in real time, thus allowing the evaluation of advanced inverter control functions. The details provided in this paper for the testbed setup and the advanced inverter control functions can be used by other researchers to repeat this work to evaluate the impact of advanced inverter control functions in the distribution system operation.

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REFERENCES

[1] D. T. Rizy, H. Li, F. Li, Y. Xu, S. Adhikari, P. Irminger, "Impacts of varying penetration of distributed resources with & without volt/var control: case study of varying load types", Power and Energy Society General Meeting 2011 IEEE, 2011.

[2] J. W. Smith, W. Sunderman, R. Dugan and B. Seal, "Smart inverter volt/var control functions for high penetration of PV on distribution systems," 2011 IEEE/PES Power Systems Conference and Exposition, Phoenix, AZ, 2011, pp. 1-6.

[3] "IEEE Std 1547 – Standard for Interconnecting Distributed Resources with Electric Power Systems" in , May 2014, IEEE Press.

[4] EPRI, 2012, Common Functions for Smart Inverters, Version 2. EPRI, Palo Alto, USA, Report ID:1026809.

[5] A. Sangwongwanich, Y. Yang and F. Blaabjerg, "A cost-effective power ramp-rate control strategy for single-phase two-stage grid-connected photovoltaic systems," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-7.

[6] V. Salehi and B. Radibratovic, "Ramp rate control of photovoltaic power plant output using energy storage devices," 2014 IEEE PES General Meeting | Conference & Exposition, National Harbor, MD, 2014, pp. 1-5.

[7] P. Piya, M. Karimi-Ghartemani and S. A. Khajehoddin, "Fault ride-through capability for grid-supporting inverters," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8.

[8] D. Iioka and H. Saitoh, "Enhancement of fault ride through capability using constant current control of photovoltaic inverters," 2016 IEEE Innovative Smart Grid Technologies - Asia (ISGT-Asia), Melbourne, VIC, 2016, pp. 1083-1088.

[9] Y. Zhang, D. Cao, Z. Yang, Y. Wang and H. Xu, "Research on the control technique of low voltage ride-through for grid-connected photovoltaic inverter," 2016 China International Conference on Electricity Distribution (CICED), Xi'an, 2016, pp. 1-5.

[10] M. Dietmannsberger and D. Schulz, "Compatibility of fault-ride-through capability and anti-islanding-detection in inverters connected to low voltage distribution grids," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 7010-7015.

[11] Bailu Xiao et al., "Development of hardware-in-the-loop microgrid testbed," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 1196-1202.

[12] B. MacCleery et al., "A new platform and methodology for system-level design of next-generation FPGA-based digital SMPS", Proc. IEEE ECCE, pp. 1599-1606, 2012.

[13] Z. Ye, R. Walling, N. Miller, P. Du, K. Nelson, L. Li, R. Zhou, L. Garces, and M. Dame, Reliable, Low-Cost Distributed Generator/Utility System Interconnect, Final Subcontract Report, November 2001 – March 2004, NREL Subcontractor Report, NREL/SR-560-38017, March 2006.

[14] Hawaiian Electric Rule No. 14, Paragraph H: Interconnection of Distributed Generating Facilities with the Company's Distribution System (Rule 14H), The Hawaiian Electric Companies.

[15] eHS User Guide, 2016, http://www.opal-rt.com/wp-content/themes/enfold-opal/pdf/L00161_0407.pdf, accessed 28-JUN-2017.

[16] IEEE 1547.1-2005: IEEE Standard Conformance Test Procedures for Equipment interconnecting Distributed Resources with Electric Power Systems, IEEE Std. 1547.1-2005, Jul. 2005.