CEMAC Clean Energy Manufacturing Analysis Center

Established in 2015 by the U.S. Department of Energy's Clean Energy Manufacturing Initiative, CEMAC engages the DOE national lab complex, DOE offices, U.S. federal agencies, universities, and industry to promote economic growth and competitiveness in the transition to a clean energy economy. CEMAC is operated by the Joint Institute for Strategic Energy Analysis at the DOE's National Renewable Energy Laboratory.

SiC Power Electronics in Medium Voltage Motor Drives
Trade and Manufacturing Analysis

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SiC Simplified Value Chain for Medium Voltage Variable Frequency Drive & Regional Cost and Manufacturing Analysis

Raw and Processed Materials → Ingots → Wafers → Chips/Bare Die → Power Modules → Variable Frequency Drive

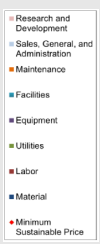




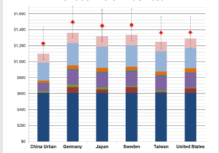

Bottoms-up Regional Manufacturing Costs and Modeling Assumptions

- Regional costs are computed for each manufacturing process based on input data from materials and equipment suppliers and manufacturers
- **MSP** is the minimum sustainable price that a company must sell its product for in order to pay back the capital and operating expenses during the plant lifetime

- Manufacturing cost modeling base case
  - Models the effect of core country factors:
    - Labor rates
    - Electricity prices
    - Effective corporate tax rates
  - In this early-stage industry — particularly for upstream components — manufacturing competitiveness is less driven by core country factors, but this may change over time
- Economic modeling assumptions for all countries:
  - Same cost of debt and equity, D/E ratio
  - Same production volumes, yields, and wafer diameter
  - No subsidies
  - Assumes the same knowledge/capability of firms
  - Assigns the same risk associated with firms regardless of country
  - Wafer model assumes 100% capacity utilization

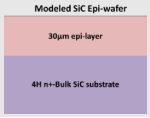


SiC Epi-Wafers
Substrates and Epi-Layer
For use in 3.3kV devices

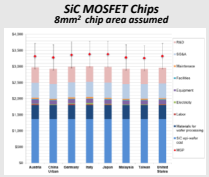


MSP per wafer: $1228-$1496/unit

Modeled SiC Epi-wafer

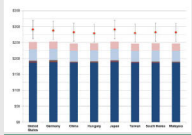


SiC MOSFET Chips
8mm² chip area assumed



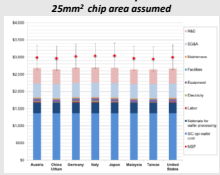
- *MSP per chip: $1.67-$1.73/unit*
- *Calculated wafer processing cost for MOSFET chips: $320-$380/6" wafer*

SiC Power Modules



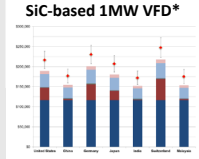
MSP per module: $279-$291/unit

SiC SBD Chips
25mm² chip area assumed



- *MSP per chip: $4.86-$5.03/unit*
- *Calculated wafer processing cost for SBD chips: $190-$230/6" wafer*

SiC-based 1MW VFD*

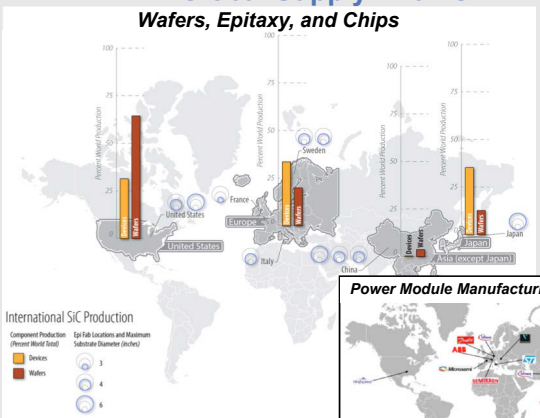


MSP per drive: $170K-$200K/unit

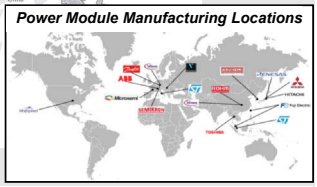
***Hypothetical, no known products available on the market**

Global Supply Chains

Wafers, Epitaxy, and Chips



Power Module Manufacturing Locations

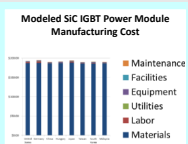


- Wafers, Epitaxy, and Chips:
  - *US currently one of the top 3 countries manufacturing these upstream components*
    - *Particularly strong in wafer fabrication: good quality, yields*
  - *For devices:*
    - *Trend is towards large, multi-national incumbent power electronics players in Power Electronics*
  - *Industry is moving towards vertical integration globally (acquisitions)*
- *For Modules:*
  - *Locations indicated are known to be capable of assembling IGBT sized modules.*
  - *Additional contract manufacturing not shown on this map is often used for high-volume production. These contract manufacturing facilities are located primarily in Southeast Asia and China*

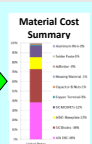
Sources : Yole Développement. (2016). Power SiC 2016: Materials, Devices, and Applications., System Plus Consulting. (2015, July 7). POWER COSIM+: Semiconductor Manufacturing and Cost Simulation Tool., NREL primary research

Techno-economic Modeling Can Help Inform Research and Investment

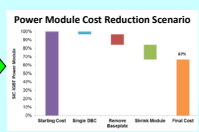
Modeled SiC IGBT Power Module Manufacturing Cost



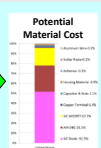
Material Cost Summary



Power Module Cost Reduction Scenario

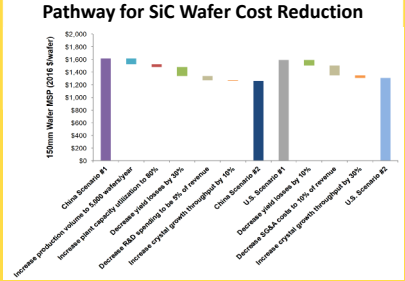


Potential Material Cost



- ***Majority of SiC Power Module manufacturing cost is material cost***
  - ***Currently SiC Devices are 46% of the material cost***
  - ***Potential cost reduction scenario reduces manufacturing cost 33%***
    - ***SiC Device become 69% of cost***

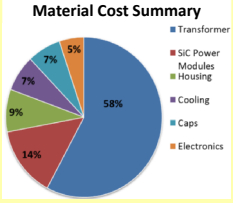
Pathway for SiC Wafer Cost Reduction



- Regional cost driver understanding allows specific regional cost reduction modeling

- Analytically model costs instead of using antidotal references
- Help guide research and manufacturing advancements
- Understand impact before committing development resources

SiC-based 1MW VFD Material Cost Summary



- Quantify specifically what material is driving cost
  - Can identify unexpected cost drivers

For more detailed information on our assumptions, see our accompanying technical report:
"Global Cost and Competitiveness Issues in Manufacturing SiC Power Electronics for Medium Voltage Motor Drives," NREL/TP-6A20-67694 (Feb. 2017)
http://www.nrel.gov/docs/fy17osti/67694.pdf

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