Controller-Hardware-in-the-Loop Test Bed for Fast-Switching SiC-Based 50-kW PV Inverter

Preprint

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National Renewable Energy Laboratory

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Controller-Hardware-in-the-Loop Testbed for Fast-Switching SiC-Based 50-kW PV Inverter

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***Abstract*— The recent advent of wide bandgap power semiconductor devices will lay the path for future power converters. These devices provide the advantage of high switching speed and lower losses. The high cost and high switching speeds of these devices provide a challenge in the development and validation of the fast-switching inverter controls with accuracy comparable to that of a hardware setup. In this paper, a field programmable gate array (FPGA) real-time simulator-based controller-hardware-in-the-loop (CHIL) testbed is used to verify the low-level and advanced inverter controls for fast-switching wide bandgap-based photovoltaic string inverter. The paper also includes development of the CHIL testbed, which is run at a time step of 500 ns in order to implement 20-kHz switching frequency. The developed CHIL testbed is validated through experimental results from a three-phase, 50-kW, 480-V_{LLrms} SiC device-based inverter.**

Keywords— advanced grid-support functions, controller hardware-in-the-loop, high switching frequency, power electronics converters, SiC devices.

I. INTRODUCTION

The large-scale integration of renewable energy such as solar and wind will result in increasing levels of distributed power generation. The future power grid will involve increasing numbers of power converters while increasing the complexity of the associated control systems. The future of the power converters is driven by advancements in the wide bandgap semiconductor devices [1]. These devices can provide very high switching speeds, lower switching losses, and they can reduce the size of the associated filter [2]. In the current market, these devices are two to three times more expensive than silicon (Si) devices with similar ratings but recent studies have shown that the economic parameter (cost/power) for wide bandgap devices will approach that of Si devices in the next decade because the cost reductions are accelerating [3]. The fast-switching characteristics of these devices and requirement of faster controls have posed a challenge of accurately validating the developed controls without risking the damage of the power hardware. The controller-hardware-in-the-loop (CHIL) methodology has gained recognition in the recent years because it bridges the gap between pure simulation and power hardware experiment. The CHIL methodology serves as an approach for engineering design because of its advantages, including low cost, low risk, fast implementation, and design flexibility, which reduce the design development cycle for any new power converter significantly [4], [5]. Research that used CHIL tests as a basis for converter design have also been reported for slow-switching power converters [6], [7]. Multiple papers have been published on CHIL application for power converters in power systems [8], [9]. These studies either do not implement a switching-level model for the power converter or have a slow real-time simulation for the system, which prevents accurate modeling of the fast-switching dynamics realized by the advent of wide bandgap device-based power converters. A microgrid testbed was proposed in [10] that can test the developed controls, but it is limited to switching frequencies up to a few kHz. A hardware-in-the-loop testbed was developed in [11] for validation of the developed inverter controls, but this testbed validates higher level SunSpec compliance controls such as Volt-VAr (VVAR), Volt-Watt (VWATT), etc. In this paper, a field programmable gate array (FPGA) real-time simulator-based CHIL testbed is demonstrated that is capable of validating controls with device switching frequencies as high as 20 kHz. Furthermore, the testbed can be used to validate switching control so-called low-level controls and advanced inverter functions (VVAR, VWATT, etc.), which are called higher level controls. Following the introduction, the inverter controls and the developed CHIL testbed are explained in detail in Section II. Section III presents the CHIL test results for different inverter controls. The CHIL testbed validation through experimental results from a 50-kW, SiC-based three-phase photovoltaic (PV) inverter are also presented in Section III. The conclusions and main findings are summarized in Section IV.

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II. INVERTER CONTROLS AND CHIL TESTBED

In this section, the inverter controls are first discussed, followed by CHIL testbed development details. The controller used for implementing the control algorithms is an off-the-shelf, embedded controller with a dual-core computer processing unit and FPGA.

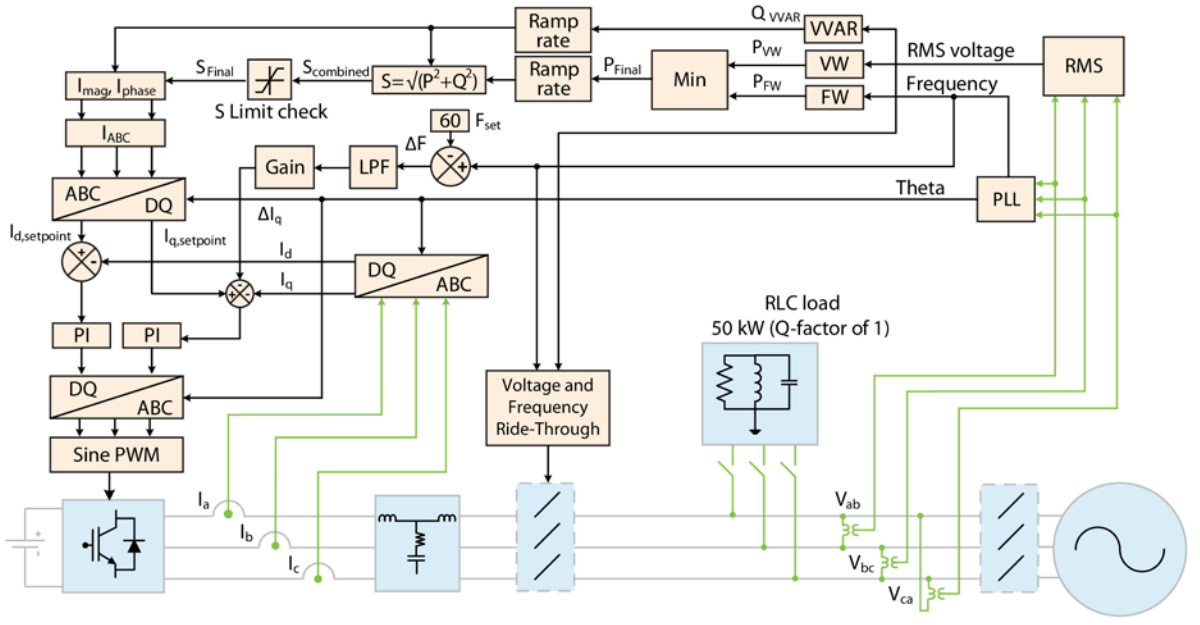
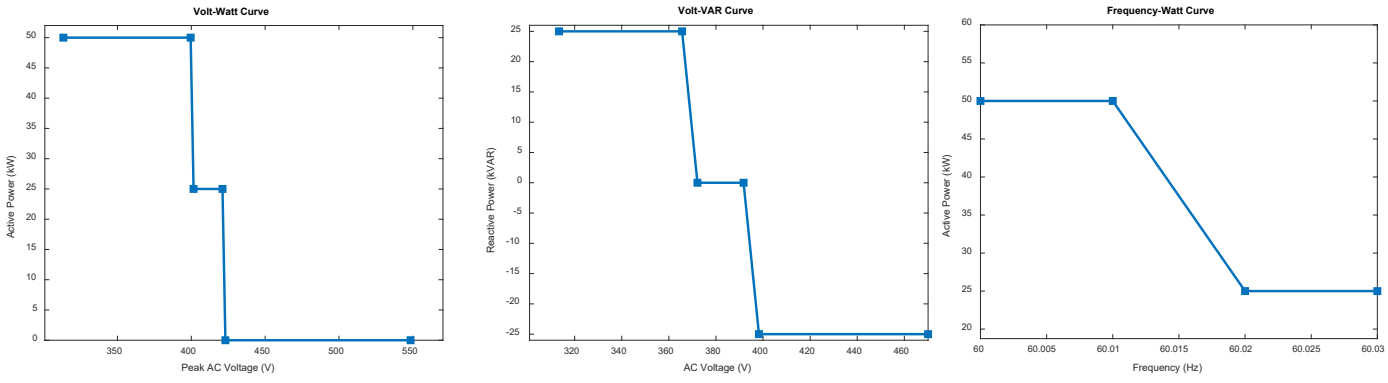


Fig. 1. Block diagram of the inverter control.

A. *Inverter Controls*

The PV inverter is switched using the traditional sine pulse width modulation. The power injected into the grid is controlled using current control. The reference current waveforms are generated relative to the instantaneous angle of the three-phase voltages measured at the point of common coupling (PCC). The instantaneous angle of the voltages is measured using a phase-lock loop (PLL), which is executed at 100 kS/s. These low-level controls are programmed on the single-board RIO (SBRIO) FPGA [12]. The details of the control algorithm are shown in Fig. 1. In addition to the low-level inverter control, advanced inverter functions are included in the control algorithm. These functions include grid-support application in accordance with the revised IEEE 1547 guidelines, which include VVAR, VWATT, frequency-watt (FWATT), voltage/frequency ride-through, anti-islanding, and other inverter functions [13]. For voltage regulation, VVAR and VWATT controllers generate active and reactive power references, respectively to control the voltage. The three-phase RMS voltage values are calculated and then to the controller sent to compute the reference active and reactive power for VWATT and VVAR control using the pre-programmed grid-support curves shown in Fig. 2. Because only the VVAR control sets the reactive power reference, it is directly used to calculate the reference current phase angle. The curve used for VVAR was designed for testing purposes, but it closely resembles the curve from IEEE 1547 [13]. The VVAR-enabled inverter injects or absorbs reactive power autonomously to the grid in order to mitigate grid voltage fluctuations. The VWATT parameters were selected such that after the VVAR control reaches its reactive power absorption limit, the VWATT curve would start curtailing active power generation. The goal of FWATT is to work along with the VWATT to generate the active power reference. After two active power references are generated, priority is given to the controller that curtails more. Similarly, the other advanced inverter functions – such as ride-through, anti-islanding, ramp rate control, etc. – are also implemented in the controller. The implementation of the control algorithm on the controller is shown in Fig. 3 and is explained in [14]. In the next subsection, the CHIL testbed is



(a) (b) (c)

Fig. 2. Grid-support function curves used for voltage and frequency regulation.

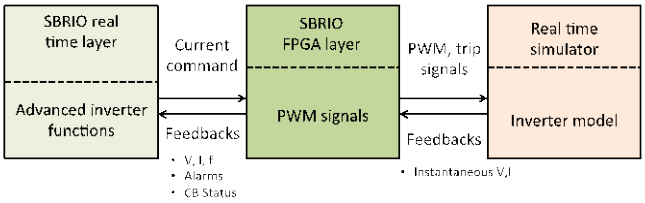


Fig. 3. Block diagram of the CHIL setup.

explained.

B. CHIL Testbed Implementation

The inverter controller hardware and the control algorithms are tested using CHIL to verify the performance of both the switching-level current control algorithms coded on the FPGA layer and the grid-support functions coded on the real-time layer of the controller. The firmware implementation of the control algorithms was done through the National Instrument's (NI) SBRIO (NI 9607). The control algorithms were implemented in both real-time processors and in FPGAs. The location of different control functions on the SBRIO platform and the data exchange between these layers is also shown in Fig 3. Advanced inverter control functions VVAR, VWATT, FWATT, voltage ride-through, and frequency ride-through were programmed in the real-time layer. The FPGA controller was coded in LabVIEW FPGA, and it implements all the high-speed inverter control functions, including ac current and dc voltage feedback control loops, PLL, and unintentional island-detection algorithms. The FPGA code is modular and consists of a top-level virtual instrument that provides the interface to the real-time controller, and multiple sub-virtual instruments that implement the actual control functions. The top-level virtual instrument receives control parameters from the real-time controller including current magnitude and phase angle set points as well as connect/disconnect commands, it and transmits variables to the real-time controller, including status and alarm annunciators, frequency, RMS voltage and current, and active and reactive power. The sub-virtual instruments include the analog input scaling and filtering algorithms, the RMS and power computations, the reference waveform generation algorithms, the actual PID control loops, the PWM gate drive output control algorithms, and the active island-detection algorithms.

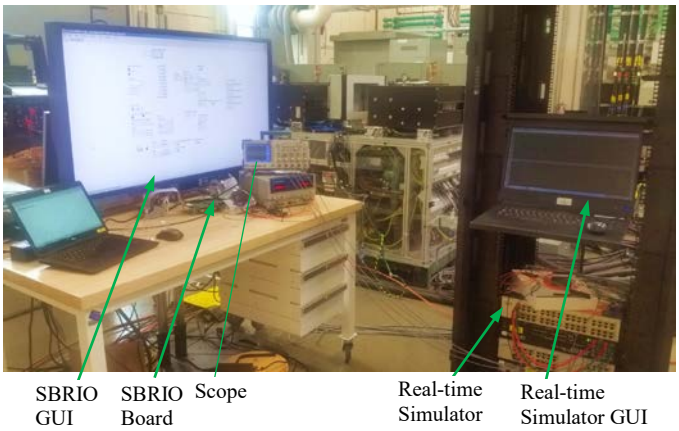


Fig. 4. Laboratory setup of the CHIL testbed.

The developed inverter controls were tested using the CHIL setup. For the testing, a switching-level model of the three-phase inverter was implemented on the Opal-RT OP5607 FPGA expansion unit. The OP5607 includes a Xilinx Virtex VII FPGA that can be programmed using the Opal-RT eHS Gen3 real-time power electronics simulation toolbox. The Xilink Virtex VII FPGA allows a time step of 200 ns for the co-simulation of power electronics converters, with fiber-optic communications back to the power system model running at slower rate on the OP5600 processors. The Opal-RT eHS Gen3 real-time power electronics simulation toolbox allows using subset of the MATLAB/Simulink SimPowerSystems block to develop the inverter model. This toolbox also enables compilation and downloading of the developed inverter model on the Virtex VII without the need of a new bitstream file. For the setup shown in Fig. 4, the inverter, as well as the dc input and ac grid connection, were simulated on the OP5607 at a 500-ns time step, or 1% of the 20-kHz switching period. The developed CHIL testbed is capable of testing fast-switching controls up to a switching frequency of 50-kHz, which is easily achievable with the advent of wide bandgap devices. The modeled inverter voltage and current waveforms were connected to the SBRIO analog input channels via the OP5607 analog output channels. Similarly, the SBRIO PWM and trip outputs were connected to the modeled inverter inputs via the OP5607 digital input channels. The results from the CHIL testbed and validation of the testbed through experimental results are presented in the next section.

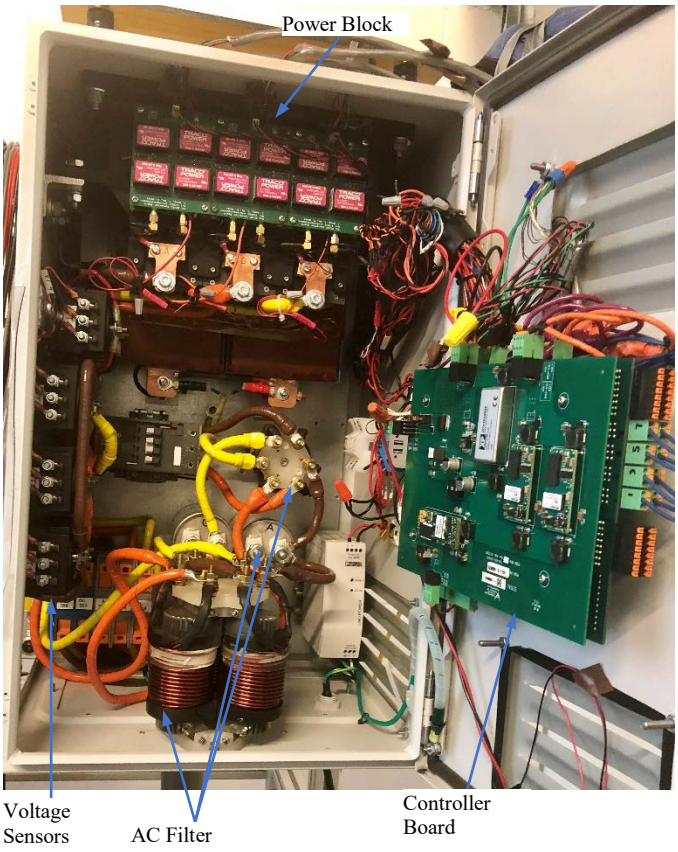
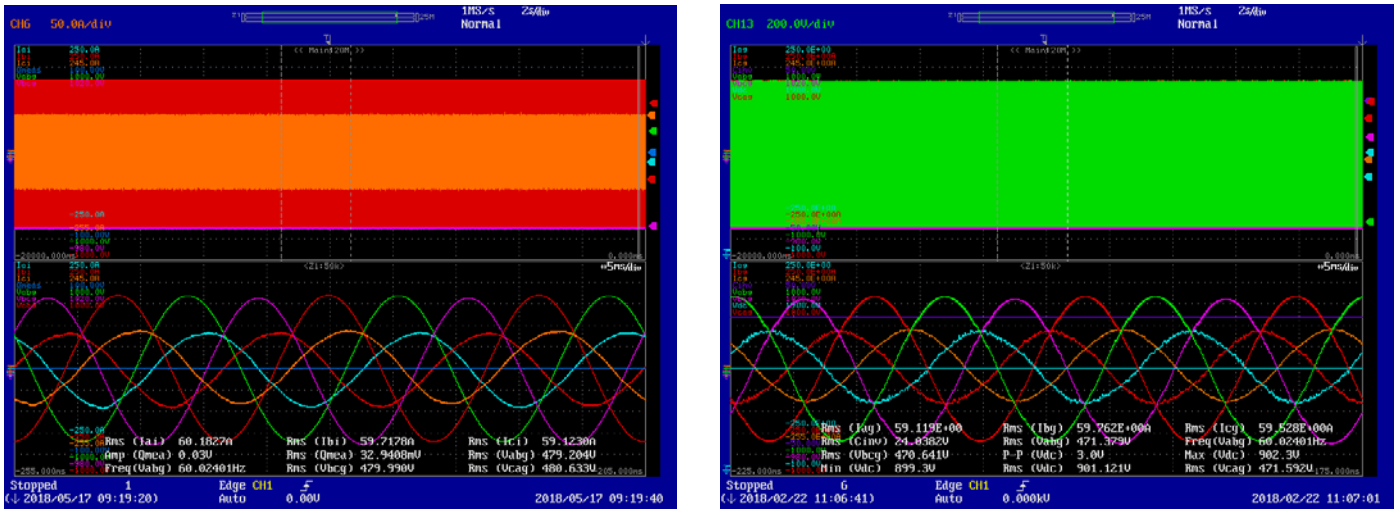


Fig. 5. Experimental setup of a three-phase 50-kW, 480-V, SiC-based string PV inverter.



(a) (b)

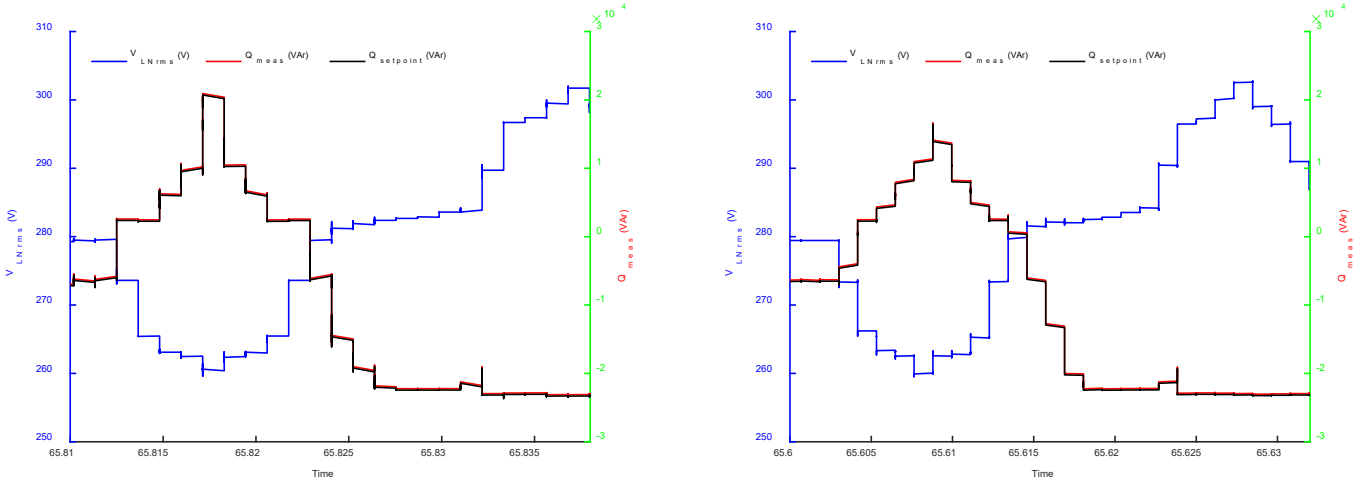
Fig. 6. Three-phase inverter output current waveforms from (a) CHIL test setup, and (b) experimental setup when injecting 50-kW into the grid at unity power factor. V scale: 200 V/div, I scale: 50 A/div

III. CHIL TESTBED VALIDATION

In this section, inverter controls verification using the developed CHIL testbed are presented. Additionally, the inverter control verifications are duplicated using the experimental setup to validate the developed CHIL testbed. The CHIL setup used for the verifications is shown in Fig. 4. Multiple test cases are presented for the verification of the inverter controls and CHIL testbed. Fig. 5 shows the experimental setup of the three-phase 50-kW, 480-V_{LLrms}, SiC-based string PV inverter used for the validation of the CHIL results.

The inverter output current waveforms when operating in closed-loop, current-control mode and injecting 50 kW of active power into the grid at unity power factor are shown in Fig. 6. The total harmonic distortion of the load currents for the CHIL and experimental results are measured to be about 2.11% and 2.14%, respectively. Inverter current RMS measured in the CHIL results was 59.98 A. The inverter current RMS measured in the experimental results was between 59.12 A and 59.76 A. Therefore, maximum error for the current was around 1.5%. The peak efficiency of the inverter using the CHIL setup is computed to be about 99%, and that measured experimentally is 98.2%. This discrepancy is because of the inaccurate loss models of the ac filter. The ac filter inductors are modelled as inductors with resistive loss associated with them (through equivalent resistive elements) and do not include the core loss which changes with frequency. Furthermore, the inverter model in the CHIL setup does not include the losses associated with the other physical parts, such as the thermal management system (cooling fans), and power consumed by the controller boards.

The next set of tests were done to verify the advanced inverter controls through CHIL and actual experimental results. The first test case verified is VVAR implementation on the CHIL setup and actual hardware. The VVAR controls allows the inverter to help maintain the grid voltage by injecting or absorbing reactive power during any voltage event. Fig. 2(a)



(a) (b)

Fig. 7. Test results showing voltage steps, set point, and measured reactive power injected into the grid using the (a) CHIL setup and (b) experimental setup for grid voltage variation.

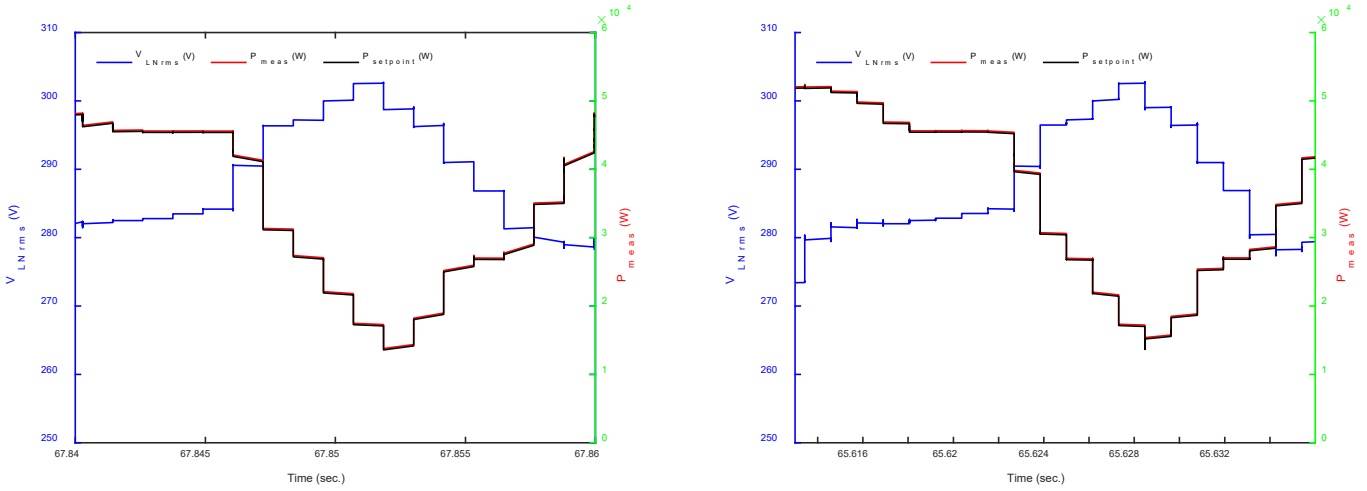


Fig. 8. Test results showing voltage steps, set point, and measured active power injected into the grid using the (a) CHIL setup and (b) experimental setup for grid voltage variations.

shows the VVAR curve used for the verification. For the CHIL setup, the simulated grid on OP5607 is programmed to have time steps to verify the VVAR control. Ametek's RS90 is used as the grid simulator for the experimental setup. RS90 was coded to provide voltage steps similar to that programmed in the CHIL setup. The CHIL test results and the experimental test results for similar voltage steps are presented in Fig 7 (a) and (b), respectively. It should be noted that the voltage for the CHIL and experimental results in Fig. 7 is the peak voltage measured at the PCC.

Fig. 8 presents the verification of the VWATT grid-support function through the CHIL testbed and experimental setup. The VWATT and FWATT controls work together to regulate the grid voltage and frequency depending on the severity of the event. An active power reference is generated from both VWATT and FWATT curves corresponding to the voltage and frequency at the PCC. The minimum of the two is used to generate the final active power reference. For the case of this test, the frequency of the grid voltage is maintained constant at 60 Hz for both the CHIL and experimental results. This results in a constant 50-kW reference from the FWATT curve (see Fig. 2(c)). The grid voltage is stepped, and the corresponding active power reference is generated using the VWATT curve (see Fig. 2(b)). Fig. 8 shows that the measured active power injected into the grid follows the reference, and they are same for both the CHIL and experimental results. It should be noted that the voltage presented in Fig. 8 is the peak voltage at the PCC. The experimental results for the dynamic response of the inverter are presented in Fig. 9. At t = 0.48 sec, the grid voltage is stepped from 277 V (1 p.u.) to 291 V (1.05 p.u.). It can be observed from Fig. 9 that the reactive power into the grid changes from 0 to -0.5 p.u., and the active power injected into the grid changes from 1 p.u. to 0.5 p.u. (following the VVAR and VW curves). Note that the active and reactive power shown in Fig. 9 are measured at the PCC.

TABLE I
VOLTAGE RIDE-THROUGH SETTING FROM HAWAIIN ELECTRIC COMPANY'S INTERCONNECTION REQUIREMENTS

Operating Region	Voltage Boundary (%)	Ride-Through Time (sec.)
Overvoltage 2 (OVR2)	V > 120	No ride-through
Overvoltage 1 (OVR1)	V > 110	0.92
Undervoltage 1 (UVR1)	V < 88	10
Undervoltage 2 (UVR2)	V < 70	20
Undervoltage3 (UVR3)	V < 50	No ride-through

The next advanced grid-support function tested using the CHIL setup and then verified using the experimental setup is voltage ride-through. Table I presents the voltage ride-through settings used in the test. The value used for the ride through controls are adapted from Hawaiian Electric Company's interconnection requirements [15]. When the voltage exceeds the limit, an elapsed timer will be triggered. This timer will be compared with the time setting provided in the table. When the elapsed timer exceeds this time setting, a trip signal will be sent to trip the inverter. Fig. 10 provides the CHIL and experimental result from a sample voltage ride-through testing.

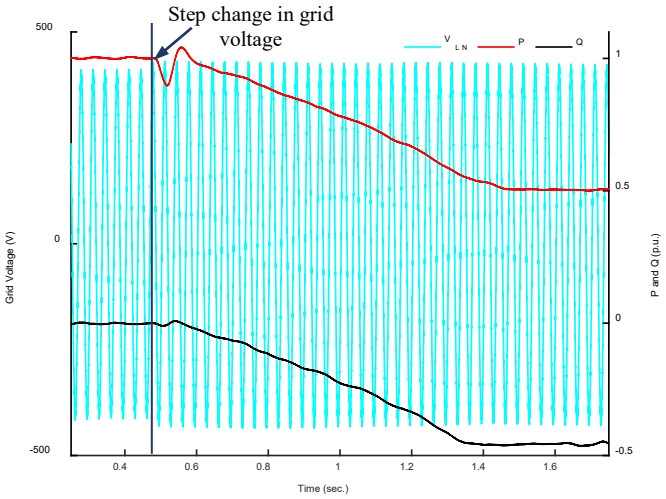
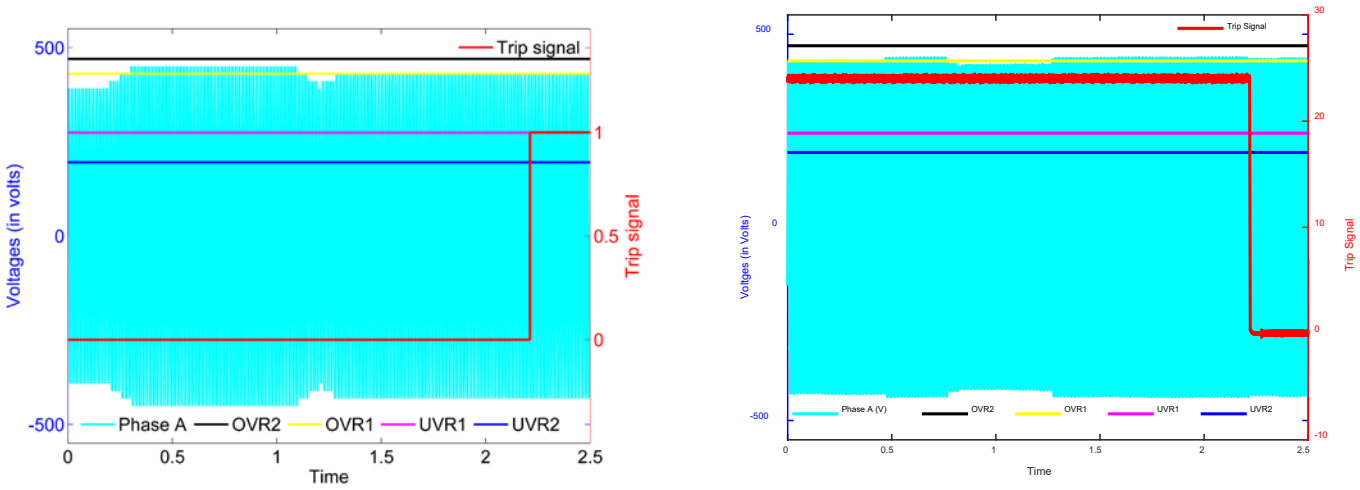


Fig. 9. Experimental result for dynamic change in P and Q following the corresponding curves, when a step change to grid voltage is applied.



(a) (b)

Fig. 10. Test results showing voltage ride-through settings, Phase A voltage, and the grid circuit-breaker trip signal using the (a) CHIL setup and (b) experimental setup for grid voltage variations.

In this verification, the overvoltage 1 (OVR1) setting was tested. This particular OVR1 setting gets activated when the grid voltage is more than 110% but less than 120% of the nominal voltage (see Table I). For that operating region, the inverter is required to ride-through until 0.92 second. If the voltage does not return to the normal range by that time, the inverter should trip. Fig. 10(a) shows that the voltage exceeds 1.1 p.u. (431 $V_{ph,peak}$) at about 1.30 seconds, and it stayed at this voltage level. The trip signal was triggered after 0.92 seconds as expected and required. The trip signal shown in Fig. 10(a) is the control signal in the simulated model of the inverter to open the circuit breaker. Fig. 10(b) shows a similar test case for the experimental setup. The grid voltage exceeds 1.1 p.u. (431 $V_{ph,peak}$) at about 1.30 seconds, and it stays at that level. The trip signal is activated after 0.92 second. Note that the trip signal shown in Fig. 10(b)is the actual 24-V signal being sent to the three-phase AC contactor by the SBRIO. It can be seen from Fig. 10(b) that during normal operation and ride-through periods, the trip signal is at 24 V i.e., the contactor is ON. When the ride-though limit is reached at about 2.22 seconds, the controller sends 0 V to the contactor coil to trip it.

The agreement between the CHIL results and the experimental results demonstrate that the developed CHIL testbed provides accurate results as that through the experimental results for both low-level and high-level inverter controls. This can result in a more robust method for development of complex controls and to test them before implementing them on actual hardware, thereby resulting in a more risk-free debugging of the algorithm while eliminating the possibility of damaging the hardware.

IV. Conclusion

In this paper, a controller-hardware-in-the-loop testbed has been presented and validated. The CHIL testbed was developed using by interfacing NI 9607 SBRIO with Opal-RT OP5607 FPGA expansion unit. The dc input source, inverter, ac filter, and grid have been modelled on the OP5607's Xilinx Virtex VII FPGA with a time step of 500 ns for implementing 20-kHz switching frequency. Lower-level switching, and higher-level grid-support functions – such as VVAR control, VWATT control, and voltage ride-through – have been implemented on the controller and tested using the CHIL testbed, in this paper. Furthermore, these tests have been repeated on an experimental setup formed using a three-phase 50-kW, 480-$V_{LL,rms}$ SiC-based PV inverter. It has been shown that the results obtained using the CHIL setup closely match the experimental results and that the developed CHIL testbed provides a reliable platform for debugging and verifying complex controls without the risk of damaging the hardware. The comparison between the CHIL testbed and experimental setup results indicate proper simulation of the inverter model at a very small time step in real time, thus allowing for the accurate evaluation of inverter controls for complex inverter architecture. The details provided in this paper for the testbed setup can be used by other researchers to evaluate complex control algorithms for fast-switching converters with switching frequencies up to 50 kHz.

Acknowledgment

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