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Modeling and Analysis of Gallium Oxide Vertical Transistors

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Gallium oxide (Ga_2O_3) based semiconductor devices are expected to disrupt power electronic applications in the near future. Due to the wide bandgap of Ga_2O_3, it should be possible to fabricate power devices with higher breakdown voltages and lower on-state resistances compared to incumbent Silicon (Si) and Silicon Carbide (SiC) technologies. In particular, vertical metal-oxide field effect transistor (MOSFETs) and vertical Fin Field Effect Transistor (FinFETs) devices based on Ga_2O_3 have been recently reported. Here, we present a comparative modelling study of such vertical Ga_2O_3 power transistors using use Technology Computer Aided Design (TCAD) and analyze their electro-thermal performance under static and dynamic operating conditions. We find that the MOSFETs show a trade-off between the current gains and threshold voltages, as a function of device geometry and acceptor concentrations in the body region. In contrast, in the FinFETs structures it is possible to achieve normally-off operation by proper design of the fin width and its donor concentration, without p-type doping. Overall, the modeling and analysis results presented here can be used as a guide for experimental improvement of the vertical Ga_2O_3 device performance for future power electronic applications.
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Gallium Oxide (Ga_2O_3) material has recently gained significant attention as an attractive candidate for the fabrication of power electronic devices. The attractive properties of β-Ga_2O_3 are wide band-gap (E_g) of 4.85 eV, high breakdown field in the range of 8 MV/cm, and the resulting excellent figures of merit.[1–5] The high figures of merit of Ga_2O_3 result in a possibility to fabricate the transistor with low on-resistance (low conduction losses), high breakdown voltage (good reliability), and high switching speeds (broad range of applications). In addition, inexpensive and high-quality Ga_2O_3 wafers[6] are expected to lead to low-cost and high-reliability transistors,[5–8] addressing concerns related to the higher cost and lower quality of silicon carbide (SiC) and gallium nitride (GaN) wafers. The main drawbacks of Ga_2O_3 compared to SiC and GaN are its much lower thermal conductivity and somewhat lower bulk carrier mobility.

Recently, various transistor devices based on Ga_2O_3 material have been reported,[8–13] including many lateral depletion- and enhancement-mode device structures, as well as several vertical device structures. The lateral device structures are generally not suitable for applications requiring breakdown voltages greater than 600 V, and result in significant drift resistance at reverse voltages exceeding 200 V.[7] In contrast, the vertical device architectures do not have these limitations, offering a wider range of potential applications including grid-tied power electronics, inverters for photovoltaics and motor drives, high-voltage DC and modular converter/inverter topologies.[5] The two recently reported Ga_2O_3 vertical device architectures (Fig. 1) are the planar metal-oxide field effect transistors (MOSFETs), and Fin Field Effect Transistors (FinFETs), both fabricated on β-Ga_2O_3 wafers.[11–13]

Here, we report on the modeling and analysis of Ga_2O_3 vertical transistors for future applications in power electronic devices. Technology Computer Aided Design (TCAD) physics-based models are presented for Ga_2O_3 based vertical planar MOSFET structure and vertical FinFET structure, in a form of comparative study. Various mixed-mode analyses are performed to assess the electro-thermal performance of the device, and the results for the static and dynamic behavior are presented. The effects of p-type doping on the vertical planar MOSFET device, and the influence of the fin geometry on the vertical FinFET device, are assessed in terms of the threshold voltage and the current gain. Finally, the results are summarized, and conclusions are derived based on these modeling and analysis results.

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Methods

The modeled transistor structures shown in Fig. 1, including layer thicknesses and doping profiles, were defined within the Sentaurus Synposys TCAD environment. For each material, including the semiconductor, gate oxide, and other materials, material properties were defined in a parameter file. As an example, the material properties for Ga_2O_3, including electron mobility, thermal conductivity, bandgap value, electron density and masses, are summarized in Table I. Device performance was modeled by simultaneously solving in 2-dimensions (2D) the electron and hole continuity equations, Poisson equation, and thermodynamic equations, using finite-difference time domain analysis.[14]

To assess the feasibility of Ga_2O_3 devices for power electronic applications, Direct Current (DC), Alternating Current (AC), transient, and electrothermal characteristics for different transistor architectures were analyzed. For the characterization of device transfer curves and output characteristics, DC analysis was performed as a function of voltage at the gate and drain terminals of the transistor. For the characterization of device C-V (capacitance vs. voltage) characteristics, small-signal AC analysis was performed. Short-circuit transient behavior of the device was assessed at a DC bus voltage of 1 kV.

Results and Discussion

Vertical planar MOSFET.—Fig. 1a shows the cross-section of the modeled vertical planar MOSFET device structure, that employs a p-type current blocking layer in the body of the transistor and a Si-doped n^--Ga_2O_3 drift layer. The structure of this device is similar to the one for shielded-planar vertical MOS device structures that has a Mg-doped p-type shielding region that extends under the N^+ source and N-base regions. The extension of the body region beyond the N^+ source region edge defines the transistor channel region. The transistor threshold voltage is determined by the thickness and the doping concentration of the N- base region, such that the PN junction formed between the body region and the N-base is fully depleted.[15]

For current conduction, an external bias is applied at the gate terminal. This forms an electron accumulation region below the oxide (Al_2O_3) region at the surface of the N- base region, which enables current conduction. The shielding region at the body of the terminal also protects the oxide region from high reverse electric fields formed in

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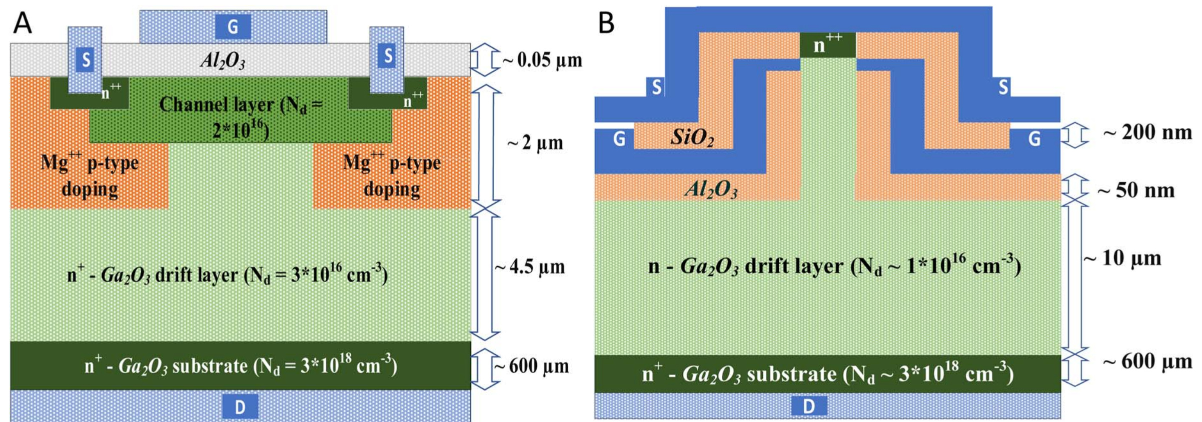

Figure 1. Two vertical transistor structures modeled here, including (a) vertical planar MOSFET, and (b) vertical FinFET.

Table I. Important material properties of Ga_2O_3.

Property	Symbol	Value	Units
Band Gap[#]	E_g	4.85	eV
Dielectric Constant	$\varepsilon_s/\varepsilon_0$	10.2	n/a
Electron Mass[#]	m_e/m_0	0.28	n/a
Intrinsic Concentration	η_i	1.79	10^{-22} cm^{-3}
Electron Affinity	E_a	4.0	eV
Low-field Mobility	μ_{min},	118	cm^{2}V^{-1}S^{-1}
High-field Mobility	μ_{max},	50	cm^{2}V^{-1}S^{-1}
Thermal Conductivity	κ	10.9	W/mK
Specific Heat	c	0.56	Jg^{-1}K^{-1}

[#]= temperature dependence.

the drift region. In the blocking mode of the transistor, a high reverse voltage can be supported at the depletion region formed between the P^+ body region and the N- drift region. The drift-region resistance and maximum breakdown voltage that can be supported by the transistor form an important trade-off in the transistor design.

The first reported vertical Ga_2O_3 MOSFET had a threshold voltage between to −50 to −60 V.[12] Similar modeling results were obtained with an acceptor concentration of 5 × 10^{17} cm^{-3} using the TCAD model developed in this article (black dashed curve in Fig. 2a). These device threshold voltages were far from the desired transistor performance when used in switching applications. Based on the TCAD modeling results, the V_{th} becomes more positive with higher acceptor concentration and lower thickness of N- base region, which is desirable for power electronics. Consequently, the doping concentration and the thickness of the N- base region were adjusted to achieve the desired threshold voltage.

The transfer (Fig. 2a) and output (Fig. 2b) characteristics of a transistor that yielded good performance are shown in Fig. 2 The Mg^{++} acceptor concentration in the body region is 10^{17}–10^{19} cm^{-3}, the donor concentration in the N- base region is 3 × 10^{16} cm^{-3}, and the N-base region thickness is 0.45 µm. This device yielded a threshold voltage of −0.2 V which is significantly higher than the one published in Ref. 12. However, it was also observed that the current gain decreases with increasing the acceptor concentration. Together, these two trends lead to an unfavorable trade-off for the vertical planar MOSFET structure. Also, it can be observed that with the increasing applied gate-source voltage, the drift resistance increases resulting in a drop in the drain current and higher conduction losses.

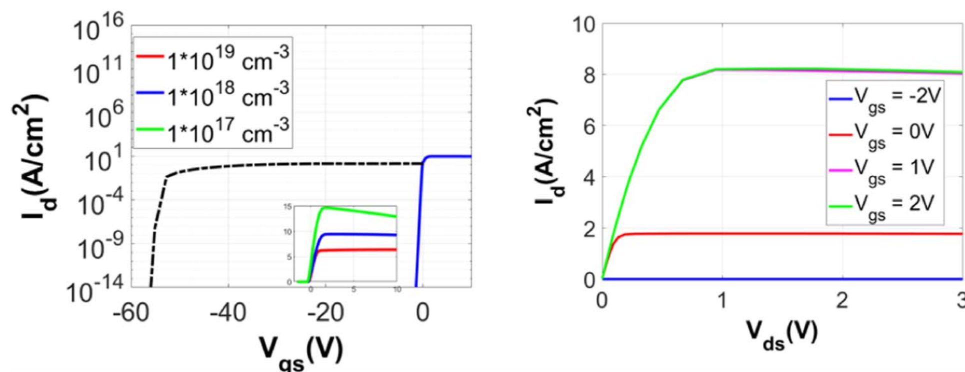

Figure 2. Modeling results for the vertical planar power MOSFET device, including (a) transfer characteristics for different Mg doping levels, including published experimental work (black curve), with linear plot in inset, and (b) output characteristics for different gate voltages with Mg doping of 10^{19} cm^{-3}.

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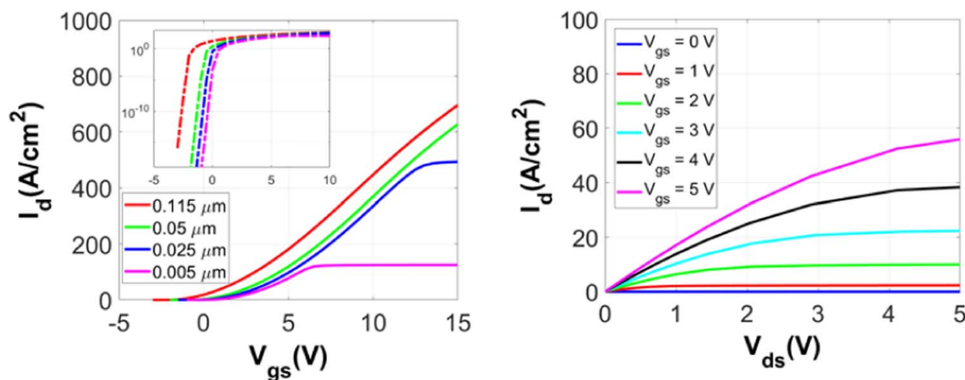

Figure 3. Modeling results for the Vertical FinFET device, including (a) transfer characteristics for different fin widths, with logarithmic plot in inset, and (b) output characteristics for different gate voltages.

Vertical FinFET device.—Another important device structure that has recently gained attention for *GaN* as well as Ga_2O_3 devices is the vertical FinFET configuration shown in Fig. 1b.[11] This FinFET is expected to circumvent the difficulty of achieving the necessary p-type acceptor concentration for the vertical planar MOSFET. Lateral FinFET structures have already captured a market space in the advanced Si-nodes for various CMOS analog integrated circuits. The doping concentrations of different fabrication layers and the device 2-D dimensions are shown in Fig. 1b. An n-drift layer with a donor concentration of 10^{16} cm^{-3} is grown on top of the n-type Ga_2O_3 substrate that is unintentionally doped with a donor concentration of 10^{18} cm^{-3}.

The on-state channel current is modulated through a vertical Ga_2O_3 fin-shaped region wrapped under the gate metal and oxide regions. In the absence of any external bias at the gate, the electrons in the fin-shaped channel region are fully depleted due to the metal-semiconductor work function difference. The fin width is designed so that the depletion regions formed on either side of the cross-section meet in its middle, resulting in a normally-off transistor operation that is essential for power electronics applications. The N-drift region grown on the β-Ga_2O_3 wafers supports the high reverse voltage applied across the transistor. The width and the doping concentration of the drift region can be designed to achieve the desired maximum reverse breakdown voltage.

Fig. 3 shows the DC *I-V* characteristics of the gallium oxide FinFET structure. Based on the transfer characteristics (Fig. 3a), the threshold voltage of the device is close to 1.25 V for a fin width of 0.005 μm resulting in a normally-off device operation, but strong saturation in current. Increase the fin width from 0.005 to 0.115 μm increases the current gain but makes the threshold voltage more negative. The output characteristics for a fin width of 0.005 μm (Fig. 3b) suggests that the drift resistance is quite low. Based on the modeled C-V characteristics, it was also concluded that the internal capacitances were quite low.

The static and dynamic electro-thermal characteristics of vertical FinFET devices are shown in Fig. 4. As expected, with the increase in junction temperature, the static current decreases for every bias condition due to an increase in the device on-resistance (Fig. 4a). The power dissipation and the transient junction temperature rise for short-circuit condition, which is one of the most sever in power electronics, are shown in Fig. 4b. The power dissipation goes up to 3,500 W/cm^2 and the junction temperature rises to 1,120 K when the device is short-circuited with a DC bus voltage of 1 kV. Thus, it appears that dynamic electro-thermal stability must be addressed through proper design solutions in fabrication and/or at the system level, just like for other wide band-gap devices. Other important future research directions include modeling of the switching characteristics of these semiconductor devices, which is of great importance for their power electronic applications.

Conclusions

This paper presented comparative TCAD modeling results for two recently reported vertical Ga_2O_3 structures: MOSFET and FinFET. It was reported that the vertical planar MOSFET architecture has low threshold voltage and depletion mode operation, which must be addressed before this structure can be adopted for power electronics applications. Our modeling results show that the device threshold voltage can be improved by increasing the acceptor concentration and by adjusting the N-base region thickness, but at the expense of current gain. On the other hand, our model shows that the FinFET structure eliminates the need for p-type doping and provides a pathway to develop normally-off transistors through proper combination of fin widths and channel doping, in agreement with published experimental literature. The modeled steady-state and dynamic performance characteristics of

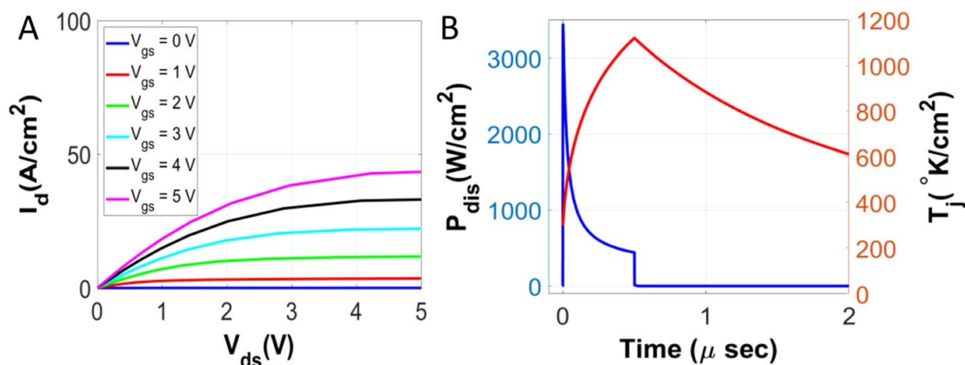

Figure 4. Modeling results for electro-thermal performance for vertical finFET device, including (a) self-heating in output characteristics for different gate voltages, and (b) transient thermal behavior for junction temperature and power dissipation.

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the FinFET structure demonstrate that it should be possible to fabricate high-performance Ga_2O_3 based power electronic devices in the future.

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