A Novel Decentralized PWM Interleaving Technique for Ripple Minimization in Series-Stacked DC-DC Converters

Preprint

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A Novel Decentralized PWM Interleaving Technique for Ripple Minimization in Series-stacked DC-DC Converters

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***Abstract*—Cascaded dc-dc converters are commonly used in applications where distributed energy sources or loads are connected to elevated voltage levels for power transfer. In such systems, it is advantageous to minimize the ripple on the bus current and voltage by proper phase shifting of the pulse-width modulation (PWM) pulses among the converters via a method known as interleaving. Existing approaches use either a centralized controller or separate communication lines among the stacked converters to control their relative PWM switch transitions. The key drawbacks are that these methods entail significant wiring, the central controller acts as a single point of failure, and implementation on very large numbers of units is impractical. In this paper, we introduce a decentralized interleaving control (DIC) strategy that acts on local current measurements at every converter and achieves communication-free PWM interleaving among the series-stacked converters. The proposed controller is simple in structure and is shown to converge asymptotically to the interleaved state irrespective of clock drifts among the digital signal processors. Experimental results are provided for a system of five series-connected converters showing a $10\times$ reduction in the current ripple compared to normal operation.**

I. Introduction

Series stacking of power converters has become essential in scenarios where distributed energy sources or loads need to be connected to elevated voltage levels for power transfer. Use of series-stacked dc-dc power converters for two such emerging applications are shown in Figure 1. In Fig. 1(a), local maximum power point tracking (MPPT) at the PV module or sub-moudule level is achieved by individual dc-dc converters which are cascaded across a central string inverter. Figure 1(b) shows a state-of-the-art dc distribution architecture adopted in data centers [1], [2]. In this architecture, servers are interfaced to the 380 V dc bus using series connected power supply units (PSUs) that generate the 12 V server input. Cascaded architectures not only enable the use of low voltage devices, but also offers benefits such as localized control, modularity, and improved power conversion efficiency [2]–[4]. Moreover, such a system possesses the advantage of minimizing total harmonic distortion (THD) of the common bus current (i_{bus}) with switch interleaving [4]. This translates to relaxed filtering requirements, and, hence, increased efficiency with reduced volume. In this work, we focus on leveraging this property of series connected dc-dc systems to minimize current distortion and associated filtering requirement, by using a simple localized PWM phase shift control strategy.

THD minimization via a central controller that manages relative pulse-width modulation (PWM) phase shifts has been studied in both parallel- and series-connected setups [4]–[7]. However, as the number of converter units in those systems grow, a centralized controller becomes impractical due to limited PWM resources, finite channel counts, and processor speed bottlenecks. Centralized controllers also act as a single point of failure and compromise reliability. Hence, local digital signal processors (DSP) are usually employed to manage each converter and decentralize the control effort [8]–[11]. However, doing so makes it difficult to manage the relative PWM pulse positions as any two DSP clock edges typically drift at a rate of 5-10 μs per 1 s due to very small mismatches in their clock frequencies [12]. As a result, the harmonic distortion envelope in i_{bus} exhibits beat frequencies which require further filtering. In this work, we propose a method to overcome the aforementioned clock drift issue to obtain symmetric interleaving where converter PWM pulses are equally phase shifted by $360°/N$ where N is the total number of units. This results in minimum THD when the power processed by the converters are equal.

To overcome drift among DSP clocks, one straightforward approach entails the use of communication signals between converters to restore and maintain desired PWM phase shifts. That not only entails significant wiring complexity, but is also vulnerable to communication failures and implementation

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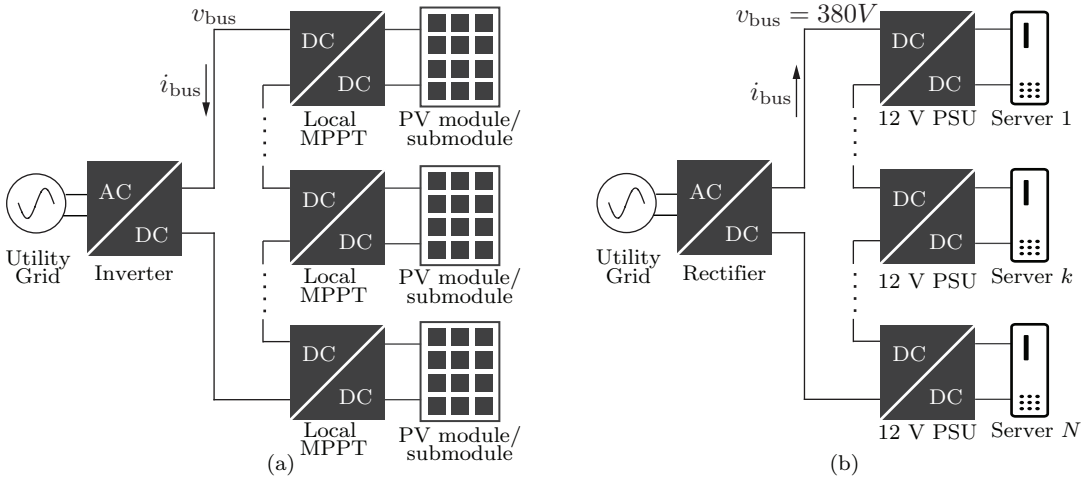

Fig. 1. Application of cascaded dc-dc converters: (a) Local MPPT at PV module/sub-module level, (b) DC distribution in data centers.

on larger numbers of units separated by long distances is impractical. To overcome these challenges, in this paper, we present a simple, decentralized, communication-free control scheme where each converter uses its locally sensed current to achieve the desired minimum THD state or symmetric interleaved state. The controllers require no communication with neighbouring controllers and are able to converge to the the symmetric interleaved state from any initial condition irrespective of DSP clock drifts. The resulting system is independent of the number of converters in the stack and can be applicable for a number of dc–dc converter topologies such as buck, boost, buck-boost, flyback, Ćuk, and SEPIC converters.

The remaining part of this paper is organized as follows- Section-II presents a detailed Fourier analysis of the common output current of the series stacked system and provides the expression of the sampled version of the output current. In Section-III, we lay out the theoretical formulation of the proposed decentralized interleaving controller and derive the practically-implementable form of the controller as well as the required sampling point of the current in a switch cycle. Section-IV demonstrates the effective performance of the proposed controller in experiments with 5 series stacked dc-dc converters and finally, Section-V concludes the paper.

II. Fourier Analysis of Bus Current

Consider N dc-dc converters connected in series and collectively delivering power to a resistive load R_{load} via a output filter inductance L_{f} as shown in Fig. 4. The set $\mathcal{N}$ is defined as $\mathcal{N} := \{1, 2, \cdots, N\}$. Let, $i_k(t)$ be the time domain expression of the current flowing in the system if the k^{th} converter in the stack was operating alone and all others were shorted out. A generic waveform for $i_k(t)$ is shown in Fig. 2 where, the peak-to-peak ripple is Δi_k corresponding to a duty period of d_k. Now, the ac ripple component of $i_k(t)$, denoted as $\widetilde{i}_k(t)$, can be expressed as the Fourier series

$$\widetilde{i}_k(t) = \sum_{m=1}^{\infty} b_{k,m} \sin\left(m(\omega_{\text{sw}} t - \phi_k - \pi d_k)\right), \tag{1}$$

where ϕ_k is the phase shift of the k^{th} converter PWM carrier with respect to a frame synchronously rotating at angular velocity $\omega_{\text{sw,nom}}$ and m is the harmonic index. The Fourier coefficient $b_{k,m}$ of the above waveform is

$$b_{k,m} = -\frac{\Delta i_k (-1)^m \sin\left(m(1-d_k)\pi\right)}{m^2 d_k (1-d_k)\pi^2}. \tag{2}$$

Now considering the case where every module delivers equal amount of power and operates at equal duty ratio d such that

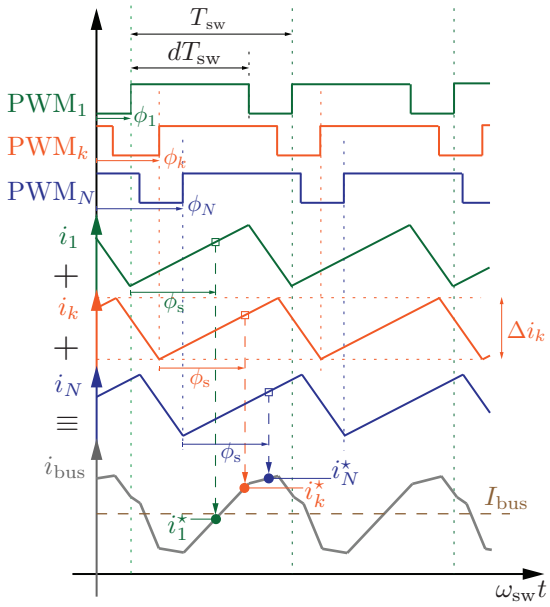

Fig. 2. Illustration of component current waveforms produced by the 1st, k^{th} and N^{th} converter in the stack if they operate individually. Superposition of these N components produce the net bus current i_{bus}.

$b_{k,m} = b_m,\ \forall k \in \mathcal{N}$, then (1) can be expressed as

$$\widetilde{i}_k(t) = \sum_{m=1}^{\infty} b_m \sin\left[m(\omega_{\text{sw}} t - \phi_k - \pi d)\right]. \tag{3}$$

Since all N inverters operate simultaneously, the total ripple in the bus current, $\widetilde{i}_{\text{bus}}(t)$, is the obtained via superposition of all N waveforms as below:

$$\widetilde{i}_{\text{bus}}(t) = \sum_{k=1}^{N} \widetilde{i}_k(t) = \sum_{k=1}^{N} \sum_{m=1}^{\infty} b_m \sin\left(m(\omega_{\text{sw}} t - \phi_k - \pi d)\right).$$

This net current is passed through a sensor and low-pass filter which naturally imparts attenuation and phase shift of the current harmonics. The output of the sensor and filter can be written in the form

$$\widetilde{i}_{\text{bus}}(t) = \sum_{k=1}^{N} \sum_{m=1}^{\infty} G_m b_m \sin\left(m(\omega_{\text{sw}} t - \phi_k - \pi d) - \Omega_m\right), \tag{4}$$

where G_m and Ω_m are the gain and phase lag, respectively, introduced by the sensor and filter network at the frequency $m\omega_{\text{sw}}$. (4) can also be written in phasor form as

$$\widetilde{i}_{\text{bus}}(t) = \sum_{k=1}^{N} \sum_{m=1}^{\infty} A_m e^{-\text{j}m\theta_{k,m}} \tag{5}$$

$$= \sum_{k=1}^{N} \sum_{m=1}^{\infty} A_m \sin\left[m(\omega_{\text{sw}} t - \theta_{k,m})\right], \tag{6}$$

where A_m is the amplitude and $-m\theta_{k,m}$ is the phase angle of the phasor corresponding to the m^{th} harmonic generated by the k^{th} converter. These are given by

$$A_m = G_m |b_m|, \tag{7}$$

$$\theta_{k,m} = \phi_k + \pi d + (\Omega_m - \psi_m)/m, \tag{8}$$

where $|\cdot|$ denotes the absolute value and ψ_m is

$$\psi_m = \begin{cases} 0 & \text{if } b_m \geq 0 \\ \pi & \text{if } b_m < 0 \end{cases}. \tag{9}$$

To facilitate digital implementation in each switch cycle, all the converters sample the common bus current at a specific instant in their switching cycle given by $\phi_{\text{s}} = 2\pi d_{\text{s}}$ (see Fig. 2). For the k^{th} converter, this instant corresponds to a phase angle of $\omega_{\text{sw}} t = \phi_{\text{s}} + \phi_k$, on the i_{bus} waveform. As a result, from (6), the sampled current value observed by the k^{th} converter in the n^{th} switching cycle, denoted as $\widetilde{i}_k^{\star}[\text{n}]$, is

$$\widetilde{i}_k^{\star}[\text{n}] \approx \sum_{l=1}^{N} \sum_{m=1}^{\infty} A_m \sin\left(m(\phi_{\text{s}} + \phi_k) - m(\phi_l + \pi d) - \Omega_m + \psi_m\right) \tag{10}$$

$$\approx \sum_{l=1}^{N} \sum_{m=1}^{\infty} A_m \sin\left(m(\phi_{kl} + \phi^{\star})\right), \tag{11}$$

where $\phi^{\star} = \phi_{\text{s}} - \pi d + (\psi_m - \Omega_m)/m$. Note that in each switch cycle the k^{th} converter will adjust it's PWM carrier phase shift, ϕ_k, according to the control law outlined in the following section.

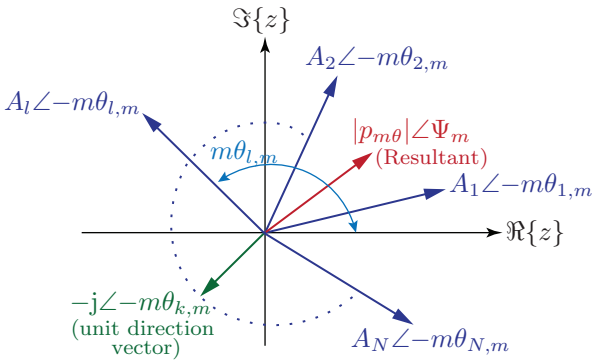

Fig. 3. Current phasors corresponding to the m^{th} harmonic.

III. Proposed Decentralized Interleaving Control (DIC) Method

As formulated in (5) and pictorially shown in Fig. 3, the m^{th} harmonic of the current component $\widetilde{i}_l(t)$ generated by the l^{th} converter, can be represented as a phasor, $A_m e^{-\text{j}m\theta_{l,m}}$, with amplitude A_m and phase $-m\theta_{l,m}$, defined relative to the synchronously rotating frame with angle $m\omega_{\text{sw}} t$. Summing m^{th} harmonic contributions from all N converters yields the net m^{th} harmonic component present in the bus current. This net m^{th} harmonic component is defined as

$$p_{m\theta} := \sum_{l=1}^{N} A_m e^{-\text{j}m\theta_{l,m}} = |p_{m\theta}| e^{\text{j}\Psi_m}. \tag{12}$$

The resultant magnitude $|p_{m\theta}|$ quantifies the extent of synchronism among the units. In particular, $|p_{m\theta}|$ is maximum with value NA_m when all phasors are phase-synchronized and minimized to 0 when they are positioned for vector cancellation. Given the notion of harmonic phasors, we construct the potential function

$$U(\theta) = \sum_{m=1}^{\lfloor \frac{N}{2} \rfloor} \cos\left(m\phi^{\star}\right) |p_{m\theta}|^2 = \sum_{m=1}^{\lfloor \frac{N}{2} \rfloor} \kappa_m |p_{m\theta}|^2, \tag{13}$$

where $\phi^{\star}$ is chosen such that $\kappa_m = \cos\left(m\phi^{\star}\right) > 0$ for all $m = 1, \cdots, \lfloor \frac{N}{2} \rfloor$ and $\lfloor \cdot \rfloor$ denotes the floor function. In essence, the potential $U(\theta)$ captures the sum of the RMS values of the ripple content upto the $\lfloor \frac{N}{2} \rfloor^{\text{th}}$ harmonic. As shown in [13], a necessary and sufficient condition for the symmetric interleaved state is

$$|p_{\theta}| = |p_{2\theta}| = \cdots = |p_{\lfloor \frac{N}{2} \rfloor \theta}| = 0. \tag{14}$$

(14) reveals key properties on the uniqueness of the interleaved state. Namely, i) the interleaved state is the only configuration where the first $\lfloor N/2 \rfloor$ harmonics of the current vanish, and hence, ii) the potential function, $U(\theta)$, in (13) reaches its global minimum of zero only at the interleaved condition.

Now we seek a controller that drives the converters towards the interleaved state from any initial condition. We do this by constructing a gradient-based control law that asymptotically drives the constructed $U(\theta)$ towards its minimum. In

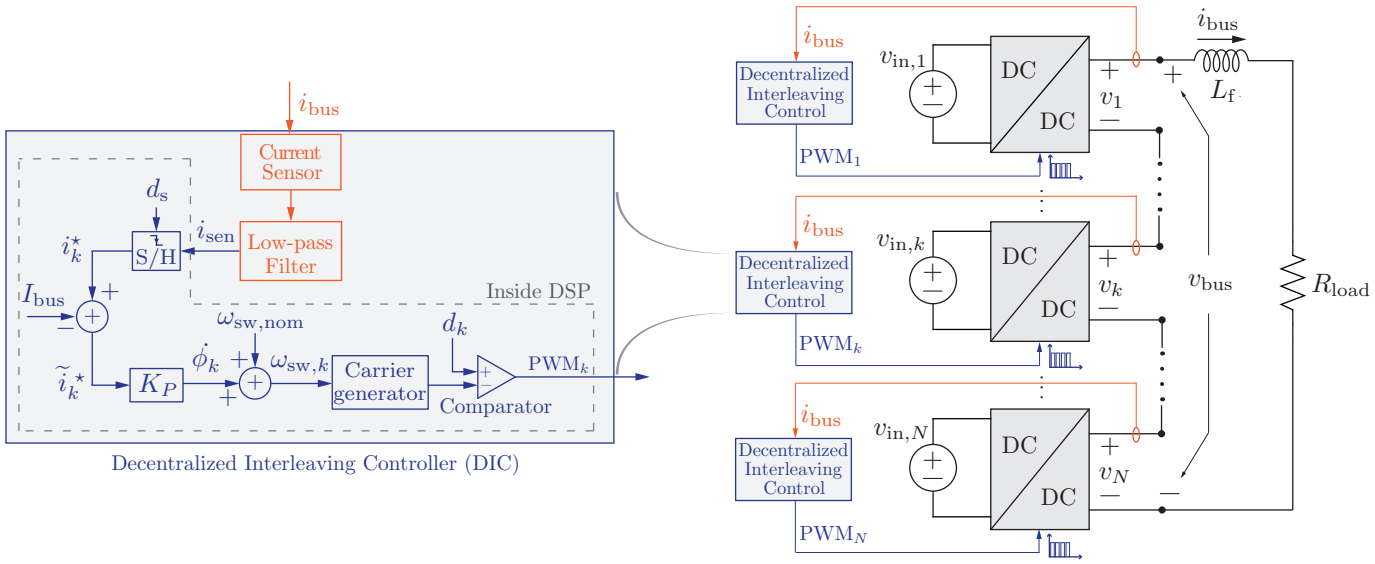

Fig. 4. Proposed method for decentralized interleaving control of N series-connected dc-dc converters.

particular, the phase of the k^{th} converter PWM is dynamically changed according to the negative of the potential gradient given by

$$\dot{\phi}_k = -K\frac{\partial U(\theta)}{\partial \theta_{k,m}}, \quad \forall\, k \in \mathcal{N}, \tag{15}$$

where K is a static control gain. This control law results in asymptotic convergence of the system to the critical points of $U(\theta)$. The critical points of $U(\theta)$ appear in the form of symmetric M-patterns which have M equally spaced clusters of N/M harmonic phasors. The symmetric interleaved state is the case when $M = N$. Out of these critical points of $U(\theta)$, the symmetric interleaved state is the only stable point subject to the control action given in (15). The proof of this statement can be found in [14], [15].

A. Controller Implementation

Now we derive the practically-implementable form of the control law proposed above for the system of cascaded dc-dc converters. The partial derivative in (15) captures the gradient of $U(\theta)$ in the direction of $\theta_{k,m}$ changes. For the m^{th} harmonic, the gradient is

$$\begin{aligned}\frac{\partial\left(\cos m\phi^\star |p_{m\theta}|^2\right)}{\partial\theta_{k,m}} &= \frac{\partial\left\langle p_{m\theta}, p_{m\theta}e^{-\mathrm{j}m\phi^\star}\right\rangle}{\partial\theta_{k,m}} \\ &= 2\left\langle p_{m\theta}, \hat{\theta}_{k,m}e^{-\mathrm{j}m\phi^\star}\right\rangle \\ &= 2\left\langle \sum_{l=1}^{N} A_m e^{-\mathrm{j}m\theta_{l,m}}, -\mathrm{j}e^{-\mathrm{j}m(\theta_{k,m}+\phi^\star)}\right\rangle \\ &= -2\sum_{l=1}^{N} A_m \sin\left(m(\phi_{kl}+\phi^\star)\right), \end{aligned} \tag{16}$$

where $\langle ;\cdot\rangle$ indicates the inner product and $\hat{\theta}_{k,m}$ is the unit vector along the direction of $\theta_{k,m}$ and is given by $\hat{\theta}_{k,m} = -\mathrm{j}e^{-\mathrm{j}m\theta_{k,m}}$. Application of (16) to each term in $U(\theta)$ gives

$$\dot{\phi}_k = -K\sum_{m=1}^{\lfloor \frac{N}{2}\rfloor}\frac{\partial \kappa_m |p_{m\theta}|^2}{\partial\theta_{k,m}} \tag{17}$$

$$= 2K\sum_{m=1}^{\lfloor \frac{N}{2}\rfloor}\sum_{l=1}^{N} A_m \sin\left(m(\phi_{kl}+\phi^\star)\right) \tag{18}$$

$$= K_P \times (\text{Sampled value of first } \lfloor N/2\rfloor \text{ harmonics of } \widetilde{i}_{\text{bus}} \text{ as formulated in (11)}). \tag{19}$$

Above, the effective gain is $K_P = 2K$. As shown in Fig. 4, (19) is implemented using a low-pass-filtered version of measured current at each converter and varying the switching frequency slightly to in turn adjust the phase of the converter switching action. Note that it may not be necessary to build the low-pass filter discussed above since any current sensor and accompanying analog circuitry possess an inherent low-pass characteristic. Having said that, harmonics above the $\lfloor N/2\rfloor$ component in i_{bus} should attenuated such that their magnitudes are small and have a negligible effect on dynamic performance.

For each converter, the analog-to-digital converter samples a signal denoted as i_{sen} in each switch cycle. Sampling occurs at the instant parameterized by d_{s} (see Fig. 2). Selection of d_{s} is discussed in the next subsection. After the sampled current is obtained, the dc component of the bus current, denoted I_{bus}, is subtracted to extract the ripple magnitude, $\widetilde{i}_k^\star$, which is subsequently multiplied by K_P to adjust the the switching frequency from its nominal value $\omega_{\text{sw,nom}}$.

B. Selection of Measurement Sampling Point

For the above controller to function, it follows that the coefficients in the potential function (13) must satisfy $\kappa_m > 0$,

$\forall\, m = 1, \ldots, \lfloor N/2 \rfloor$. It follows that we need $\cos(m\phi^\star) > 0$, which implies $-\pi/2 < m\phi^\star < \pi/2$, and ultimately gives the following inequality:

$$-\frac{\pi}{2} < m\left(\phi_s - \pi d + \frac{(\psi_m - \Omega_m)}{m}\right) < \frac{\pi}{2} \tag{20}$$

Since $\phi_s = 2\pi d_s$, we obtain

$$\frac{d}{2} - \frac{\left(\psi_m - \Omega_m + \frac{\pi}{2}\right)}{2\pi m} < d_s < \frac{d}{2} - \frac{\left(\psi_m - \Omega_m - \frac{\pi}{2}\right)}{2\pi m} \tag{21}$$

The above inequality needs to be satisfied for all $m = 1, \ldots, \lfloor N/2 \rfloor$. In theory, the available range for selecting d_s that satisfy these constraints for any case should be, $\Delta d_s = 1/\max(m) = 1/\left(2\lfloor N/2 \rfloor\right)$. However, the low pass filter bandwidth plays a significant role in determining this available selection range. As an example, for a system having $N = 5$ converters operating at a duty ratio of $d = 0.7$ and with parameters listed in Table-I, $\max(m) = 2$. The low pass filter bandwidth is chosen to be at 20 kHz so that it provides sufficient attenuation to frequency components higher than the 2$^{\text{nd}}$ harmonic. Hence, for this case, $\Omega_1 = -3\pi/20$, $\Omega_2 = -\pi/4$ and from (9), $\psi_1 = 0$, $\psi_2 = \pi$. Applying (21), for $m = 1, 2$, in this case, gives

$$d_s \in (0.18, 0.68) \cap (0.04, 0.29)$$

The above implies that we need to choose d_s in the interval, $d_s \in (0.18, 0.29)$ in order to guarantee asymptotic convergence to the interleaved state. It should be noted here that, the bandwidth of the current sensor does not play a significant role in determining the controller performance as typical sensor -3dB bandwidth are an order of magnitude higher that the considered switching frequency of the power converter. Even for higher switching frequencies, the phase lag introduced by comparatively low bandwidth sensors need to be taken into account in a similar way as outlined in this subsection. Hence, any off-the-shelf current sensor can be used for this purpose.

IV. Experimental Results

TABLE I
System and Controller Parameters.

Symbol	Description	Value	Units
V_{in}	DAB input voltage	25	V
n	DAB turns ratio	2	
V_{dc}	Buck Converter input voltage	50	V
f_{nom}	Nominal buck switching frequency	10	kHz
R_{load}	Load resistance	33	Ω
L_{load}	Load inductance	5	mH
K_P	DIC Controller gain	0.32	kHz/A

Hardware validation was carried out on series-connected dc-dc converters comprised of an buck output stage preceded by a dual-active bridge (DAB) (see Fig. 5). Note that the DAB input stage is not needed for the proposed method and was mainly used to streamline our particular experiment and provide isolation among the converters. A common power supply with voltage V_{in} fed all DAB inputs and there are $N = 5$ cascaded units across an RL load. System parameters are given in Table-I and a photo of the experimental setup is shown in Fig. 6.

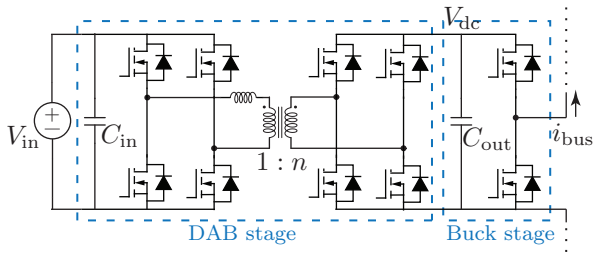

Fig. 5. Converter topology used in series-connected experiment.

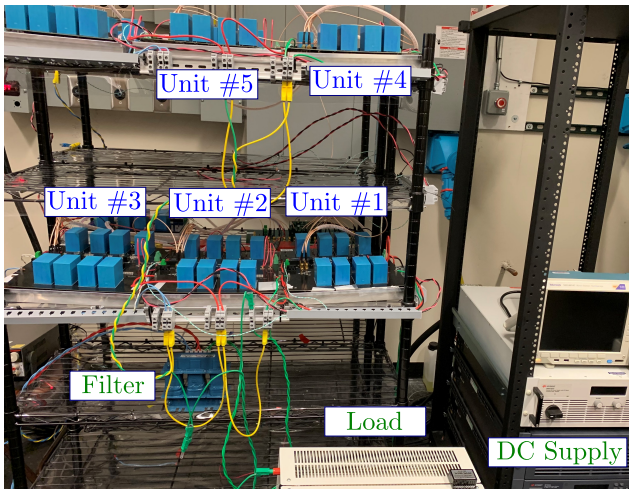

Fig. 6. Experimental system with 5 dc-dc converters connected in series.

Experimental results are shown for 3 different duty ratios to demonstrate the effective performance of the proposed controller in achieving the symmetric interleaved state across the entire range of duties. A summary of the obtained results is provided in Table II.

TABLE II
Summary of Experimental Results

Duty ratio	Sampling instant (d_s)	Convergence time	$\Delta i_{\text{pk-pk}}$ (DIC ON)	Ripple reduction
0.15	0.1	10 ms	0.2 A	6×
0.45	0.18	40 ms	0.2 A	10×
0.7	0.25	50 ms	0.2 A	6×

Figure 7 shows the measured waveforms when the converters are operating at a low duty ratio of $d = 0.15$. The average bus voltage and output power in this condition are $V_{\text{bus}} = 37$ V, $I_{\text{bus}} = 1.1$ A and $P_{\text{out}} = 43$ W, respectively. Figure 7(a) shows the transient in the bus current ripple, $\tilde{i}_{\text{bus}}$, and bus voltage, v_{bus}, at the instant the control loops are turned on. The convergence time to the interleaved state is around

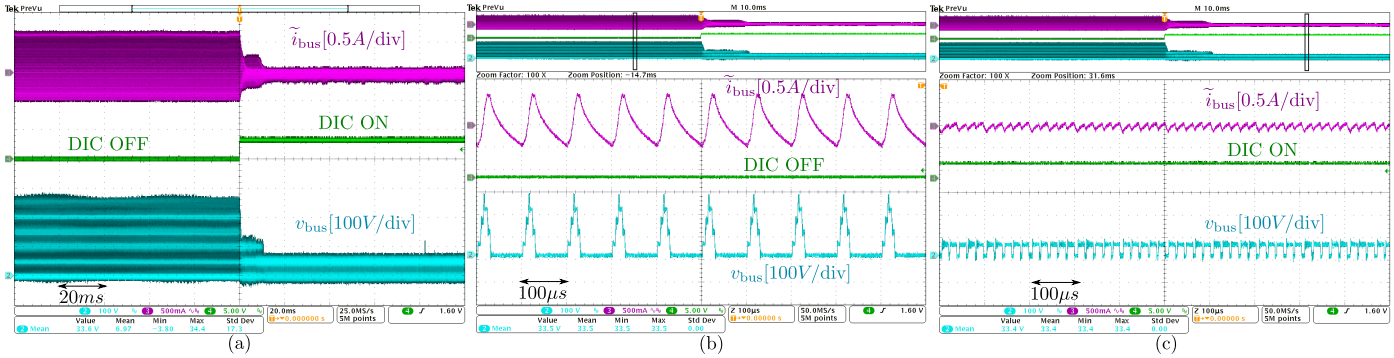

Fig. 7. Experimental validation of the performance of proposed DIC method. (a) Transient response of $\widetilde{i}_{\text{bus}}$ and v_{bus} for $d = 0.15$ and convergence to the symmetric interleaved state in 10 ms. Zoomed view of $\widetilde{i}_{\text{bus}}$ and v_{bus}: (b) before DIC controller is engaged, and, (c) after DIC is turned on. A $6\times$ reduction in ripple is obtained compared to the uncontrolled state.

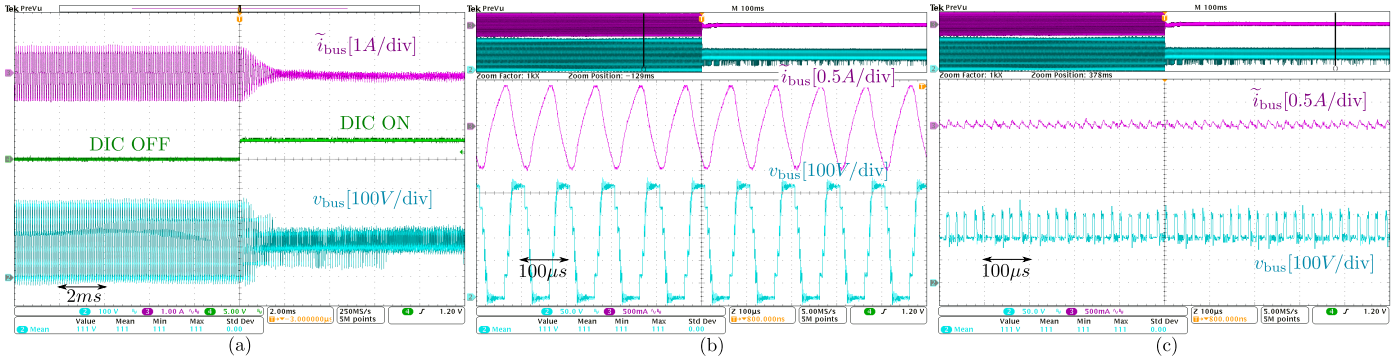

Fig. 8. Operation with $d = 0.45$: (a) transient response of $\widetilde{i}_{\text{bus}}$ and v_{bus} shows convergence to the symmetric interleaved state in 7 ms. Zoomed view of $\widetilde{i}_{\text{bus}}$ and v_{bus}: (b) before DIC controller is turned on, and, (c) after DIC is turned on. A $10\times$ reduction in ripple is obtained.

10 ms. Figure 7(b)-(c) shows enlarged views of $\widetilde{i}_{\text{bus}}$ and v_{bus} before and after the control is initiated. Evidently, the peak-to-peak value of $\widetilde{i}_{\text{bus}}$ reduces from 1.2 A to 0.2 A to give a $6\times$ reduction in ripple. The worst case current ripple appears when the PWMs of the converters become phase synchronized due to drifts in their DSP clocks. This worst case current is higher than 1.2 A. Hence, the ripple reduction in that case would be higher.

Figure 8 shows the results when the converters are operating at a medium duty ratio of, $d = 0.45$. In this condition, $V_{\text{bus}} = 113$ V, $I_{\text{bus}} = 3.4$ A and $P_{\text{out}} = 385$ W. Figure 8(a) shows the transient in $\widetilde{i}_{\text{bus}}$ and v_{bus} when control is initiated. As shown in Fig. 8(b)-(c), the bus current ripple falls from 2 A to 0.2 A resulting in a $10\times$ reduction in peak-to-peak current.

Figure 9 shows similar results when the converters are operating at a high duty ratio of, $d = 0.7$. In this condition, $V_{\text{bus}} = 175$ V, $I_{\text{bus}} = 1.8$ A and $P_{\text{out}} = 310$ W. In this case R_{load} was 66 Ω. Figure 9(a) shows the transient in $\widetilde{i}_{\text{bus}}$ and v_{bus} when control is initiated. As can be seen from Fig. 9(b)-(c), the bus current peak-to-peak ripple falls from 1.2 A to 0.2 A resulting in a $6\times$ reduction in peak-to-peak current.

Due to symmetric PWM phase shifts of $360°/5 = 72°$ among the converters, frequency components from fundamental to 4^{th} harmonic in the bus current gets eliminated and the dominant frequency component in $\widetilde{i}_{\text{bus}}$ now becomes $5 \times f_{\text{nom}}$ or 50 kHz, which leads to relaxed filtering needs.

V. Conclusion

In this paper, we validated a novel method to achieve decentralized switch interleaving for current ripple minimization in series-connected dc-dc converters. The proposed controller only requires a measurement of the locally-sensed current and functions by perturbing the switching frequency of each converter around the nominal value in proportion to the sensed ripple content. As each converter in the series-connected system carries out this routine independently, their collective interactions drive the system asymptotically to the switch interleaved state. After delineating an analytical model and design approach, the proposed method was validated on a series connected setup consisting of 5 series-connected buck converters.

Compared to other existing methods, this method of decentralized interleaving is simple to implement as it does not require over-sampling of the current waveform and very high bandwidth sophisticated current sensor to measure the current. The bandwidth of the current sensor does not play a significant role in determining the controller performance. Hence, any off-the-shelf current sensor can be used for this purpose.

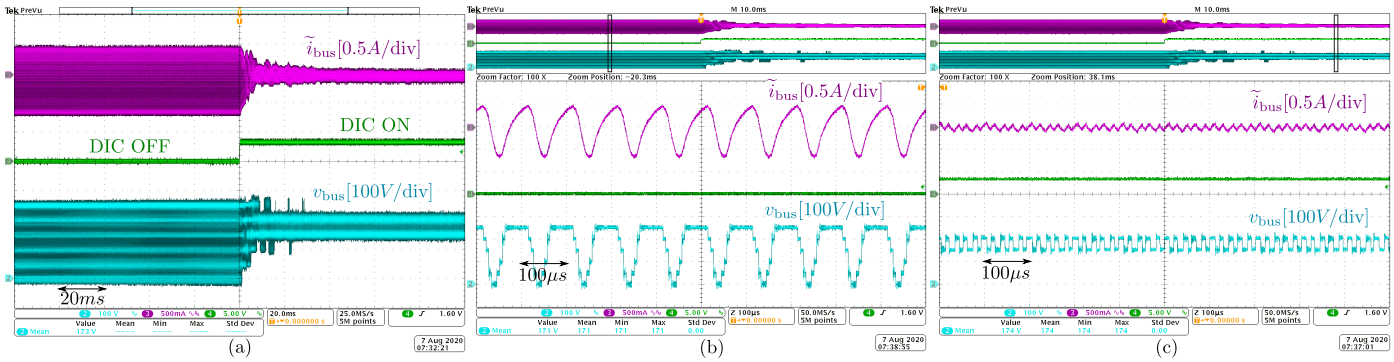

Fig. 9. Operation with $d = 0.7$: (a) transient response of $\widetilde{i}_{\text{bus}}$ and v_{bus} shows convergence to the symmetric interleaved state in 7 ms. Zoomed view of $\widetilde{i}_{\text{bus}}$ and v_{bus}, (b) before the interleaving controllers are turned on, and, (c) after control loops are turned on. A $10\times$ reduction in ripple is obtained.

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