

A High-Frequency Planar Transformer with Medium-Voltage Isolation

Preprint

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A High-Frequency Planar Transformer with Medium-Voltage Isolation

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Abstract—This paper presents the design of a low-loss, highfrequency planar transformer having medium-voltage (10's of kV) isolation capability while transformer primary and secondary windings are interleaved to reduce losses. Mediumvoltage isolation between adjacent printed circuit board (PCB) layers is extremely challenging using traditional PCB dielectrics. The isolation requirement is met using PCB with 7 kV/mil polyimide (Panasonic Felios RF775) as the dielectric, and by an appropriate layout of the windings and the inter-winding vias. The transformer is used to implement a dual active bridge (DAB) converter in a stackable dc-ac architecture where the dc port is connected to a photovoltaic (PV) string and ac outputs are connected in series to achieve direct PV string-to-medium voltage conversion without the need for low-voltage collection or a bulky line frequency transformer. Since each DAB transformer processes time-varying power, a design methodology is developed to minimize line-cycle-averaged losses. Experimental results are presented for a 1:1 planar transformer in a 7.5 kW SiC-based dc-to-ac module operating at 200 kHz. Isolation of 26 kV between the primary and secondary layers and between the windings and the core is verified using a hipot tester.

I. INTRODUCTION

Medium-voltage (MV) transformers are gaining attention in emerging power electronics applications such as solid-state transformers (SST). Such systems feature direct low-voltage-to-MV conversion or vice versa, which eliminates intermediate power conversion stages and improves efficiency [1]–[3]. To

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increase power density, to reduce height, to improve reliability, and to simplify manufacturing, planar transformers with printed circuit board (PCB) windings are commonly utilized in various power electronics applications [4]–[7]. However, the use of planar transformers to achieve high-frequency MV isolation in 10's of kV has not been explored. A challenge is that standard PCB dielectrics such as FR4 do not offer adequate isolation between layers. This challenge is magnified by the fact that interleaving between the primary and the secondary layers is necessary to reduce ac winding losses in high-frequency transformers. To overcome the challenges brought on by the need to sustain elevated inter-layer voltages while maintaining high efficiency, this paper introduces a novel PCB technology and an accompanying design approach for high-frequency MV planar transformers.

To illustrate a MV planar transformer application, this paper is focused on a modular photovoltaic (PV) dc-to-ac architecture shown in Fig. 1(a) [8], where dc-to-ac modules are connected in series to interface PV string voltages $V_{pv,i}$ to a MV ac grid without the need for low-voltage collection and bulky line frequency transformers. Since PV strings are typically grounded, ac-side cascaded interconnections necessitate MV isolation between each dc input and the three phase ac output in each converter module. Fig. 1(b) reveals that each isolated converter consists of a quadruple active bridge (QAB) dc-dc stage followed by H-bridge inverters. The QAB stage generates three electrically isolated copies of the dc input voltage, each acting as the dc bus for the corresponding Hbridge inverter. The ac line voltage appears across the primary and the secondary of the high-frequency transformers, which must therefore meet MV isolation requirements. The planar transformer described in this paper is designed for the QAB stages in the stacked architecture of Fig. 1.

The paper is organized as follows. Section II introduces the planar transformer technology with MV isolation capability, and points to the design issues related to the winding layout and inter-winding vias. The proposed design approach mini-

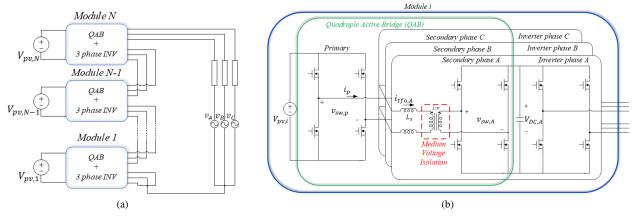


Figure 1: (a) Stackable architecture for PV string to medium voltage ac conversion [8], (b) Module schematic. In a target system, the nominal operating conditions are: 1 kV dc string voltage, and 13.2 kV MVAC grid voltage.

mizes losses in the transformer while respecting MV isolation requirements. Experimental results, including isolation testing up to 26 kV, are presented in Section III for a prototype transformer, and for a prototype converter module operating with 1 kV dc input and three-phase ac output voltages, with 7.5 kW of power delivery, and a 200 kHz switching frequency. Section IV concludes this paper.

II. ANALYSIS AND DESIGN OF MEDIUM-VOLTAGE PLANAR TRANSFORMERS

A. MV Isolation Requirements in a Planar Transformer

There are three major challenges for planar windings with MV isolation between layers. First, the dielectric between two adjacent layers must have a sufficiently high breakdown voltage. Second, the vias interconnecting primary or secondary layers must be spaced sufficiently far from the windings since the vias and the windings act as two adjacent conductors with high potential difference between them. Third, the fringing electric fields at the edge of the PCB winding may result in voltage breakdown and arcing to the ferrite core or to an adjacent layer.

With a breakdown voltage rating of $7 \, \text{kV/mil}$ (276 kV/mm), polyimide (Panasonic Felios RF775) is an attractive and low-cost dielectric option [9], [10]. Having a dielectric with 5 mil (0.13 mm) of RF775 enables potential difference of $\approx 35 \, \text{kV}$ between two adjacent PCB layers. In contrast, using standard

FR4 material as dielectric (breakdown voltage 500V/mil) would require a 70 mil (1.8 mm) thick dielectric in order to withstand the same voltage of 35 kV, leading to an impractical PCB design.

Fig. 2(a) shows an example planar transformer modeled using Ansys Maxwell 3D finite element model (FEM) simulation tool with RF775 as the dielectric. The locations of the vias and their distances from windings are highlighted in Fig. 2(b). The dielectric strength of dry air ($\approx 3 \,\mathrm{kV/mm}$) can inform the spacing of these vias from adjacent windings.

Finally, to model the effects of fringing electric fields from the windings to the core and to the adjacent layer, Fig. 2(c) shows a simplified 2D electrostatic finite element model capturing only two layers of the transformer with the RF775 dielectric in between. Two design options are considered as a trade-off between losses and the complexity of assembly: i) placing the windings sufficiently away from the core, and ii) encapsulating the core with an epoxy material.

Fig. 2(c) illustrates the second option. In order to better utilize the core window and to avoid arcing from the winding edge to the core, the core is encapsulated with an epoxy material (Sylgard 164) which has a breakdown voltage of 19 kV/mm. This material is also modeled in the 2D simulation model.

It is clear that the farther the windings are from the core, the electric field strength in the air is weaker. Given that air

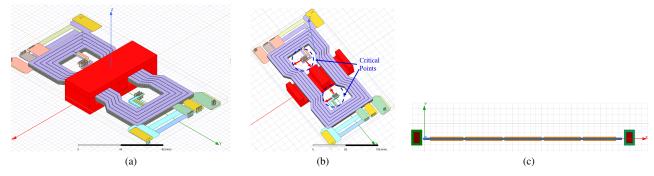


Figure 2: 3D model of the planar transformer in Ansys Maxwell: (a) isometric view; (b) vias for interconnection of layers and their spacing relative to the windings; (c) simplified 2D model to estimate the effect of fringing electric field originating from high potential difference between two adjacent layers.

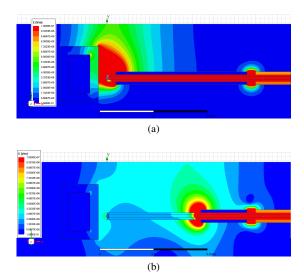


Figure 3: 2D field simulations showing fringing electric fields for (a) windings 1.2 mm away from the core and (b) windings 5.2 mm away from the core for a potential difference of 20 kV between two layers.

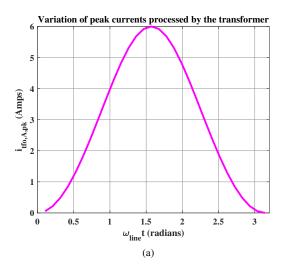
breaks down at approximately $3\,kV/mm$, 2D FEM simulations can verify a safe distance between the core and the windings. Fig. 3(a) shows how moving the windings closer to the core and the edge of the board causes high fringing fields that may cause breakdown. Fig. 3(b) shows a particular design with sufficient spacing leading to a field strength in the air of $\approx 3\,kV/mm$ with $20\,kV$ between the high voltage windings and the core.

B. MV Planar Transformer Design

While preserving the constraints due to MV isolation requirements discussed in the previous section, the core geometry and the PCB windings can be selected to minimize the loss of the transformer under application-specific operating conditions. In the module shown in Fig. 1, the specifications include the dc bus voltages on the primary and the secondary side, and the average power P processed by each of the three phases.

Fig. 4(a) shows the peak value of the transformer current varying over line cycle, as time-varying power is being processed by the transformer at twice the line frequency. Fig. 4(b) shows the trapezoidal nature of the transformer current at various points of the line cycle, with the phase shift between the active bridges adjusted to regulate the secondary-side dc link voltages [8].

Assuming quasi steady-state operation at each point along the line cycle, the core loss is estimated following the iGSE method [11], and the ac winding losses are computed using Dowell's equations [12] for up to the 11th harmonic of the transformer currents. Finally, the overall loss is obtained by averaging the losses over a line cycle. The process is repeated for various core sizes and winding arrangements to arrive at



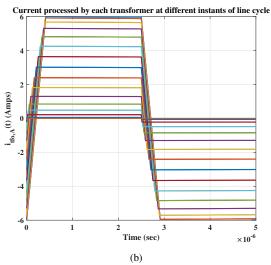


Figure 4: (a) Peak value of the transformer current during one half of the line cycle and (b) high-frequency trapezoidal current at $V_{pv,i}=1000\,\mathrm{V}$ and $P=7.5\,\mathrm{kW}$

a design where the total average loss is minimized subject to meeting the isolation constraints.

For the application in the module shown in Fig. 1(b), the planar transformer design is summarized in Table I together with the prototype system specifications.

C. Loss Estimation using 3D Finite Element Simulations

Using the 3D geometry of the optimized transformer shown in Fig. 2(a), eddy current simulations using Ansys Maxwell tool were carried out to characterize the frequency-dependent impedance matrices [13], [14] of the MV transformer. A 3D finite element eddy current simulation model of the MV transformer solved at 200 kHz is shown in Fig. 5(a). Using

Table I: Experimental prototype parameters

\overline{P}	$V_{DC,link}$	n	f_{sw}	Core geometry	Number of primary turns	Copper thickness	Number of layers
7.5 kW	1000 V	1	$200\mathrm{kHz}$	EILP 102	30	2 oz	12 (5 Turns/L)

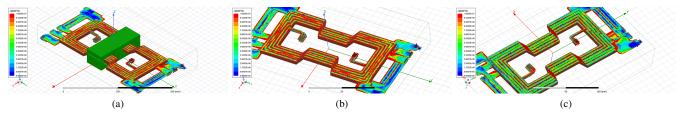


Figure 5: 3D FEM eddy current simulation of the MV transformer: (a) simulation model with an airgap; (b) current density distribution in the top layer; (c) current density distribution in the bottom layer. This simulation was performed at a particular point of the line cycle with $\hat{I}_1 = 6.85 \angle - 65^{\circ}$ and $\hat{I}_2 = 7.5 \angle - 80^{\circ}$.

this model, at 200 kHz the impedance matrix is found as:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 4.15 + j6787 & -3.16 - j6786 \\ -3.16 - j6786 & 4.15 + j6787 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$
 (1)

It should be further noted that to achieve soft switching over the entire line cycle, the transformer can be used as an energy storage device by reducing the magnetizing inductance and circulating some reactive currents [15]. Adding an airgap changes the impedance matrix and increases the winding losses. An estimate of the modified impedance matrix is obtained using the same 3D simulation model in Fig. 5(a):

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 4.44 + j456 & -3.25 - j455 \\ -3.25 - j455 & 4.44 + j457 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$
 (2)

The magnetizing inductance is reduced from (1) to (2) by the use of an airgap. The difference of current density distribution between the top and the bottom layer of the transformer can be observed from Fig. 5(b) and Fig 5(c). Due to the imbalance in primary and secondary currents the transformer fails to achieve perfect interleaving, resulting in larger proximity losses on the top winding layer. Finally, from the impedance matrices the winding loss can be calculated for all the harmonics present in the winding currents, using [13]:

$$P_{winding} = \sum_{\omega} \frac{1}{2} R_1(\omega) \hat{i}_1 \hat{i}_1^* + \frac{1}{2} R_2(\omega) \hat{i}_2 \hat{i}_2^* + \frac{1}{2} R_{12}(\omega) \left(\hat{i}_1 \hat{i}_2^* + \hat{i}_2 \hat{i}_1^* \right)$$
(3)

This results in an accurate estimate of the winding losses while, as mentioned earlier, the iGSE method can provide relatively accurate core loss estimates.

III. EXPERIMENTAL RESULTS

A MV transformer is built with 5 mils of Panasonic Felios RF 775 as the dielectric, according to the specifications in Table I. The isolation capability is tested using the setup described in Section III-A, while Section III-B presents experimental results for the converter prototype shown in Fig. 1(b) using the MV transformer.

A. MV Isolation

Fig. 6(a) shows a fully assembled transformer with the dielectric between two copper layers capable of withstanding $\approx 35\,\mathrm{kV}$ using a sheet of 5 mil polyimide (Felios RF775). A high-voltage test setup using PTS-75 hipot tester [16] is utilized to test the isolation capability of the MV transformer at Energy Systems Integration Facility of National Renewable Energy Laboratory at an elevation of 5,675 ft. from the sea level. Using the hipot tester, medium voltage is applied between the primary and the secondary windings of the prototype transformer. The core of the transformer is connected to the low voltage side, which is referred to as the system ground. In accordance to the hipot tester recommended procedure [17], a guarded return connection was used to accurately measure the leakage current between the transformer windings as well as between the high voltage windings and the grounded ferrite

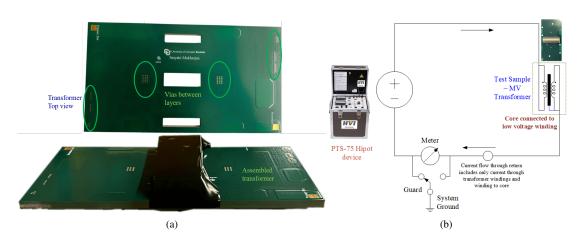


Figure 6: MV transformer and hipot test setup: (a) Fabricated planar MV transformer: PCB winding top view and assembly, and (b) circuit diagram of the guarded hipot test setup used to verify the isolation capability of the MV transformer.

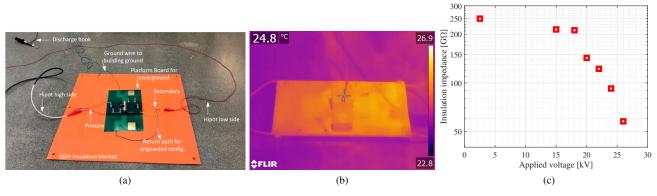


Figure 7: Hipot test setup and result data: (a) Photograph of the hipot testing setup with the device under test and connections from the PTS-75 hipot tester marked, (b) thermal image of the MV transformer with $26 \, \text{kV}$ applied between it's primary and secondary terminals with grounded core segments, and (c) measurements of insulation impedances reported using the hipot tester across a wide range of applied voltages. Operating conditions: Ambient temperature: $21.9^{\circ}C$, Relative humidity: 10.10%, elevation from sea level: $5,675 \, \text{ft}$.

core. The connection diagram of the hipot test setup is shown in Fig. 6(b).

The insulation impedance is measured using the applied voltage and the hipot built-in high precision current meter. Fig. 7(a) shows a photograph of the MV transformer undergoing the hipot test procedure with all the connections labeled appropriately. Fig. 7(b) shows a thermal image of the transformer under hipot testing, with 26 kV applied between the primary and the secondary terminals demonstrating operation unaffected by the applied voltage. In Fig. 7(c), the insulation impedance measured using the PTS-75 hipot tester is plotted against a wide range of applied voltages. The device under test, i.e. the prototype transformer, is capable of maintaining $> 50 G\Omega$ impedance up to 26 kV across the transformer terminals, indicating no breakdown. Testing up to 26 kV allows for almost 140% margin on the isolation requirement given by the peak line-to-neutral voltage of 10.8 kV at the nominal system operating point in the 13.2 kV line-to-line MV ac (MVAC) grid, thus meeting the ANSI NETA ATS 2017 standard for isolation requirements. The insulation on the MV transformer

was found to be most prone to breakdown between the high voltage winding and the grounded core. A separate experiment with only the planar PCB excluding grounded ferrite core segments demonstrated $152\,G\Omega$ insulation impedance at $26\,\mathrm{kV}$ applied across the windings.

B. Prototype Module with the High-Frequency MV Planar Transformer

Fig. 8 shows a completely assembled module utilizing three MV transformers of Fig. 6(a). A primary board with a full bridge inverter of the QAB stage and three secondary boards each consisting of a full bridge rectifier for the QAB stage and a low frequency full bridge inverter, all utilizing 1700 V SiC devices with distributed controllers are shown in Fig. 8.

Fig. 9(a) demonstrates switch-node voltages with zero voltage switching of the high-frequency SiC MOSFETs. High-frequency primary and secondary current waveforms of all three DAB modules in the QAB stage are shown in Fig. 9(b), utilizing the MV transformer at $V_{pv,i} = V_{DC,link} = 1000 \, \text{V}$, $L_s = 60 \mu \, \text{H}$ and processing 7.5 kW power with 97% overall

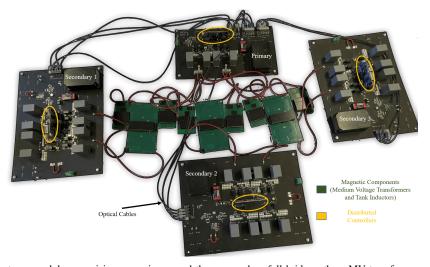


Figure 8: Photograph of the dc-to-ac module comprising one primary and three secondary full bridges, three MV transformers, and six power-transfer series inductors. Distributed controllers are marked on each of the primary and secondary boards.

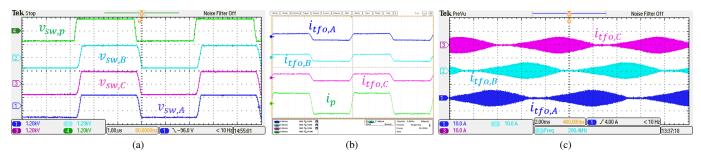


Figure 9: (a) Switch-node voltage waveforms in the dc-to-ac module illustrating generation of three isolated dc bus voltages from the primary input dc voltage of 1000 V, (b) zoomed-in high-frequency flat-top current waveforms processed by the MV transformers, and (c) secondary currents of the three module transformers with twice line-frequency components illustrating three-phase operation of the module delivering a total of 7.5 kW.

efficiency. Additionally, Fig. 9(c) shows pulsating currents processed by the three MV transformers over the line cycle for dc-to-3 phase ac operation of the module. Predicted transformer loss of approximately 55 W per transformer, with 7.5 kW three phase power processed by the converter module, is consistent with the experimental results. Out of a total loss of 55 W, 15 W is the core loss and 40 W is the conduction loss. The conduction losses are largely attributed to two factors: 1) presence of an airgap, in order to ensure zero voltage switching of the secondary SiC MOSFETs, which degrades interleaving of the high-frequency windings and results in a higher current density in the top winding layer, and 2) to maintain proper isolation, the length of the transformer windings are increased resulting in a larger dc resistance. The transformer losses are related to the choice of the planar core (EILP 102), which is the largest standard planar core available. If a larger core was available, a design with fewer turns would result in a more efficient planar MV transformer.

IV. CONCLUSIONS

Design of a high-frequency planar transformer suitable for direct low-voltage to MV conversion has been presented in this paper. Design challenges associated with PCB windings withstanding MV isolation are identified and addressed in detail, including the use of 7 kV/mil polyimide (Panasonic Felios RF775) as the PCB dielectric between layers, as well as the layout of the windings and the vias to achieve MV isolation. Using a hipot tester, it is shown how a 12-layer, 30:30 turn, 2 oz planar transformer withstands 26 kV between the primary and the secondary and between the windings and the grounded core. The high-frequency operation of the transformer is experimentally demonstrated in a prototype dc to three-phase ac module processing 7.5 kW power with 97% efficiency. The module is intended for a stackable photovoltaic (PV) system architecture with 1 kVdc string to 13.2 kV MVAC conversion.

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