High-Efficiency, Low-Cost III-V Solar Cells by Dynamic Hydride Vapor Phase Epitaxy Coupled with Rapid, Polishing-Free Wafer Reuse through Orientation-Optimized (110) Spalling

Kevin Schulte

National Renewable Energy Laboratory

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Technical Report
NREL/TP-5900-80411
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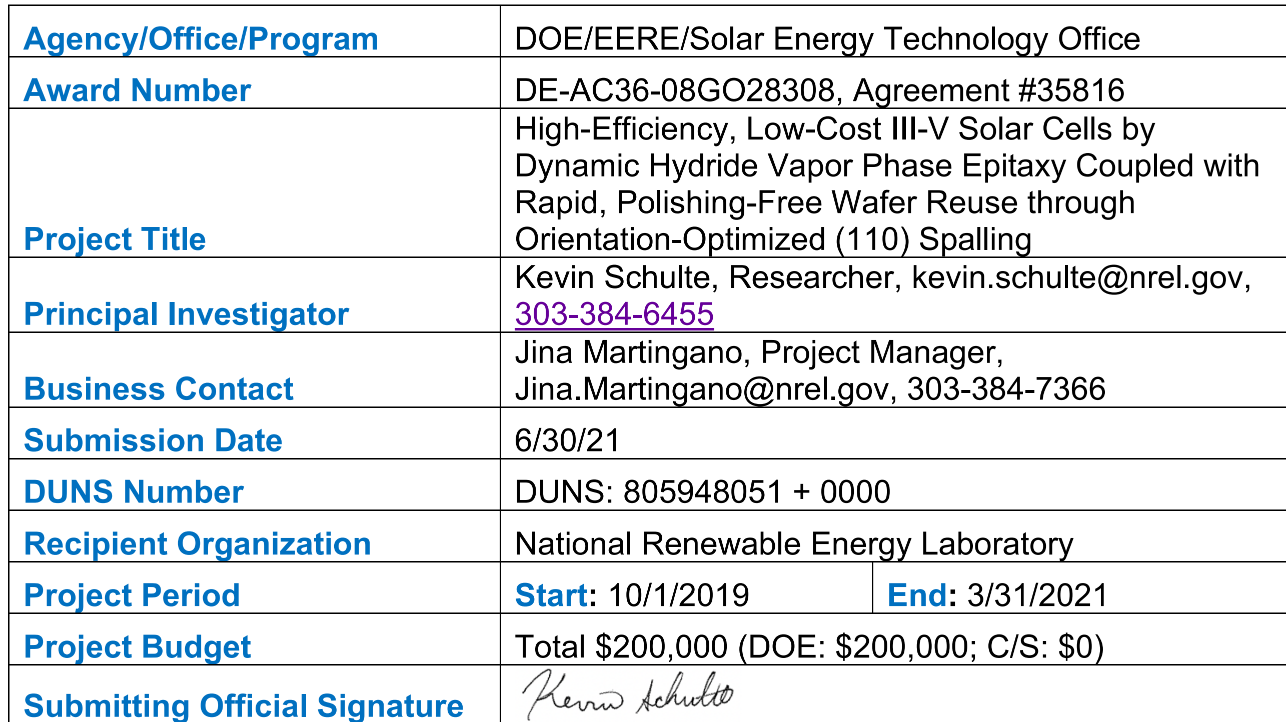
Final Technical Report



Agency/Office/Program	DOE/EERE/Solar Energy Technology Office	
Award Number	DE-AC36-08GO28308, Agreement #35816	
Project Title	High-Efficiency, Low-Cost III-V Solar Cells by Dynamic Hydride Vapor Phase Epitaxy Coupled with Rapid, Polishing-Free Wafer Reuse through Orientation-Optimized (110) Spalling	
Principal Investigator	Kevin Schulte, Researcher, kevin.schulte@nrel.gov, 303-384-6455	
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DUNS Number	DUNS: 805948051 + 0000	
Recipient Organization	National Renewable Energy Laboratory	
Project Period	**Start**: 10/1/2019	**End**: 3/31/2021
Project Budget	Total $200,000 (DOE: $200,000; C/S: $0)	
Submitting Official Signature	Kevin Schulte	

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3 Executive Summary:

III-V solar cells enable the highest demonstrated efficiencies of any photovoltaic technology with a proven track record of performance and stability. Their light weight and flexibility make them ideal for numerous terrestrial applications, including transportation and portable power. The US maintains leadership in the manufacture of III-V devices, especially for aerospace PV, making III-V photovoltaics important to the national interest. Deployment of III-V solar cells is presently limited by their cost of manufacture, which includes significant costs due to epitaxy of device materials and epitaxial growth substrates. This project investigated ways to reduce these costs by studying the growth of III-V solar cells on the (110) GaAs substrate orientation as well as controlled spalling of (110)-oriented GaAs substrates.

Controlled spalling is a method by which epitaxial III-V devices can be exfoliated from the parent substrate, enabling reuse of the substrate with potentially minimal surface re-preparation. This provides improved economics over state-of-the-art substrate recovery techniques such as epitaxial liftoff (ELO) [1]. Spalling of the most common GaAs substrate orientation, (100), results in the formation of 10-15 µm-scale surface facets which require polishing or epitaxial smoothing before devices can be re-grown on the substrate, limiting the viability of this technology [2]. On the other hand, spalling from (110)-oriented substrates yielded facet-free spalls in preliminary demonstrations. However, epitaxy of (110)-oriented III-V devices is significantly less mature than epitaxy on the near-ubiquitous (100) orientation. Therefore, in this project we investigated spalling of substrates with (110) orientation and the growth and regrowth of devices on previously spalled (110) substrates by dynamic hydride vapor phase epitaxy (D-HVPE), a growth technology with the potential for cost savings.

We demonstrated (110) GaAs solar cells grown by D-HVPE with equivalent performance and material quality relative to (100) devices. Also, we developed a procedure for repeatable wafer-scale spalling of (110) GaAs. Spalled surfaces were free of the facets founds in (100) GaAs spalling, the large arrest lines found in (100) Ge spalling, and surface features greater than 3 µm in peak-to-valley height, which can otherwise degrade the efficiency of regrown III-V devices. A sub-µm step-terrace morphology was discovered on the post-spall wafer surface, resulting from the restricted cleavage system of GaAs, but we developed understanding of the factors that determine the resulting morphology, enabling ample opportunity for optimization of morphologies suitable for device growth and spall depth waste minimization on (110) GaAs. Lastly, we demonstrated a device grown on a previously spalled surface with only 8% relative efficiency difference to a cell grown on a new unspalled wafer. Significant optimization of the substrate regrowth conditions are required to enable higher efficiency, but these results highlight the promise of (110)-oriented devices coupled with substrate reuse by spalling as a pathway for low-cost III-V photovoltaics.

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4 Background:

The cost of III-V materials and devices must be reduced to facilitate their cost competitiveness and enable their benefits, such as high efficiency and low weight, to impact society in terrestrial applications. NREL is working on D-HVPE as a means to reduce the cost of III-V epitaxy [3], because this technique uses lower cost inputs and has potentially higher throughput than incumbent technology. NREL's D-HVPE GaAs solar cell efficiency is rapidly approaching that of industry-standard metalorganic vapor phase epitaxy (MOVPE), providing a path to lower cost epitaxy without sacrificing performance [3]. With growth rates of >5 µm/min using elemental precursors, D-HVPE offers a path to ~$0.25/W epitaxy costs vs. current costs of ~$12/W [4]. However, substrate costs are high and fixed, with GaAs or Ge substrates costing ~$100 per 6" diameter wafer in high volume (or ~$32/W); this is far too high to reach SunShot 2030 LCOE targets without dramatic changes to substrate use [4].

Epitaxial liftoff (ELO) with substrate reuse is the industry-standard substrate cost-reduction method. ELO uses a selectively-etched sacrificial layer between the substrate and the solar cell to release the substrate for reuse. While ELO is proven industrially, its cost competitiveness is limited by low throughput and the need for a chemical mechanical polishing (CMP) step to clear insoluble etch products. Cost reductions using ELO are ultimately pinned by the frequency and cost of CMP. Current estimates of CMP costs are $10-$25 per wafer, too high for terrestrial applications [1, 4], even if multiple reuses are obtained between CMP cycle.

Controlled spalling, illustrated in Fig.1, utilizes brittle fracture to separate a thin layer of material from a parent substrate. Spalling, combined with direct regrowth without CMP, potentially offers cost savings compared to ELO, making it an attractive choice as a path-to-market for III-V substrate reuse [1]. Controlled spalling works by applying a metal stressor layer to the device or substrate surface with a residual tensile stress to bring the system close-to but just below the critical fracture toughness, K_{Ic}, of the bulk substrate. An externally applied force is then applied to the stressor layer to initiate and propagate a horizontal crack parallel to the substrate surface at a depth controlled primarily by the thickness of the stressor layer [5, 6]. Wafer-scale spalling usually employs an edge-exclusion zone on the surface of the wafer to create a defined stress concentration at the edge of the electroplated region to initiate fracture [7, 8]. Wafer-scale spalling and direct regrowth of PV devices has been demonstrated on Ge wafers, but not GaAs [9]. Crystallography severely constrains the available cleavage systems for GaAs compared to Ge, resulting in highly faceted surfaces for controlled spalling of (100) GaAs. (110)-oriented GaAs wafers have a favorably oriented cleavage plane parallel to the wafer surface and have been reported to produce facet-free spall surfaces [2, 10].

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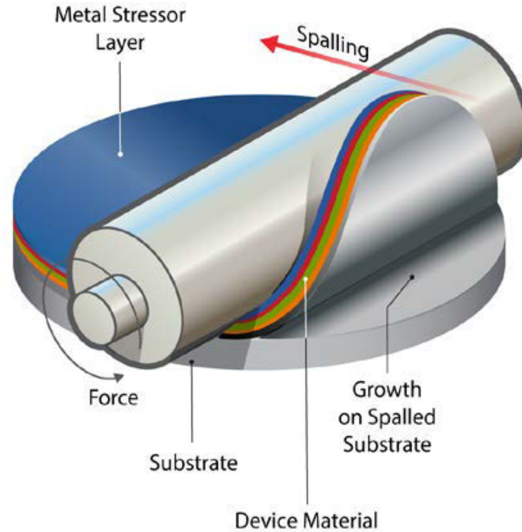

Fig.1. Exfoliation of an epitaxial device from a parent substrate via controlled spalling.

High-performance (110) D-HVPE-GaAs devices must be developed to fully leverage the benefits of (110) spalling. In current production, III-V devices are almost exclusively grown on (100)-oriented substrates, and comparatively little is understood about (110) GaAs epitaxy or devices. Historically, 21.5% efficient (110) GaAs solar cells with AlGaAs passivation were demonstrated by MOVPE [11], roughly equivalent to the best (100) MOVPE efficiencies of the time [12], but only 17% efficiency was reached in a (110) HVPE [13] device in 1981. That HVPE device lacked heterobarrier passivation of modern III-V cell designs, a challenge that D-HVPE was developed and proven to overcome.

5 Project Objectives:

The objective of this project was to preliminarily validate (110) device growth by HVPE coupled with substrate reuse by (110) spalling as a viable path to low cost III-V devices by demonstrating three components: 1*) HVPE growth of III-V materials and devices on new (110) substrates 2) Wafer scale spalling of (110) GaAs substrates 3) Growth of a device by HVPE on a previously spalled (110) substrate*. Current III-V roadmaps [3, 4] estimate that III-V manufacturing costs can compete with Si if a lower-cost, high-throughput growth technique like D-HVPE can be combined with a substrate reuse technique that achieves a high number of reuses *without invoking CMP*. Completion of the above objectives was intended to show a cost-competitive path for the terrestrial implementation of III-V devices. As III-V manufacturing costs approach Si, their higher efficiency, light weight, and higher energy yield give them advantages in some terrestrial markets, especially in space constrained applications such as residential or building integrated PV, as well as transportation.

The target audience for this work is solar cell manufacturers, space power, transportation/UAV manufacturers, building-integrated PV manufacturers. III-Vs are one of the few areas in PV where the US maintains a leadership role in manufacturing, and NREL's leadership in D-HVPE could lead to significant expansion of this manufacturing sector, resulting in job creation in the areas listed above. There are multiple potential U.S.-based companies and organizations interested in commercialization of a low-cost III-V PV product, including and Microlink Devices, Spectrolab, SolAero, the Air Force Research Laboratory Space Directorate, and the

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Department of Defense. This project was intended to de-risk this technology for these groups, enabling the U.S. to advance its lead in this important technology.

A summary of the tasks related to these objectives is given below:

Task 1.1: Development of (110) epitaxy and solar cells by D-HVPE

Task Description:

This task will develop growth recipes for GaAs solar cells on (110) GaAs substrates, including n- and p-type doping and GaInP passivation, and then measure device efficiency, targeting at least 15% conversion. Devices on as-spalled surfaces with minimal degradation will also be demonstrated.

Subtasks:

1.1.1: Achieve a (110) GaAs epilayer doped n-type with >$1x10^{18}$ cm^{-3} and an RMS roughness of <5 nm in a 10 µm x 10 µm scan area. Verify that the threading dislocation density has not increased relative to the initial substrate density.

1.1.2: Achieve > $1x10^{18}$ cm^{-3} doping level in at least 200 nm thick p- and n-doped (110) GaInP with a lattice-matched composition between $Ga_{0.50}In_{0.50}P$ and $Ga_{0.52}In_{0.48}P$.

1.1.3: Grow a passivated, anti-reflection coated GaAs device with at least 15% (absolute) solar conversion efficiency on an epi-ready (110) wafer, as well as a witness device grown on a previously spalled (110) wafer with efficiency within 15% (relative) of the epi-ready device.

Task 1.2: Develop wafer-scale controlled spalling of (110) GaAs substrates with minimal waste.

Task Description:

Effort in this area will focus on adapting established conditions for (100) GaAs spalling for (110) oriented wafers and on developing edge release methods for wafer-scale spalling. Spalled surfaces will be characterized, and the process will be optimized to limit roughness and development of arrest lines.

Subtasks:

1.2.1: Demonstrate wafer scale spalling, removing 14 cm^2 of area using varying edge release methods and down-select to the more reliable.

1.2.2: Demonstrate control of spall depth at wafer-scale, removing 14 cm^2 of area with removed thickness between 3 and 10 µm. Verify that any arrest line defects do not exceed 5 µm in peak to valley height.

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6 Project Results and Discussion:

Project results are broken out by subtask:

Subtask 1.1.1: Achieve a (110) GaAs epilayer doped n-type with >1x10^{18} cm^{-3} and an RMS roughness of <5 nm in a 10 µm x 10 µm scan area. Verify that the threading dislocation density has not increased relative to the initial substrate density.

Our initial work focused on the development GaAs epilayers which serve as the building blocks of the GaAs solar cells we intended to grow. Rear heterojunction GaAs devices require n-type GaAs with sufficient doping above 1x10^{18} cm^{-3} for the contact layer, and relatively smooth surface quality to obtain high efficiency devices. III-Vs grown by MOVPE on exact (110) substrates facet, and so a small offcut is used to obtain a smooth surface.

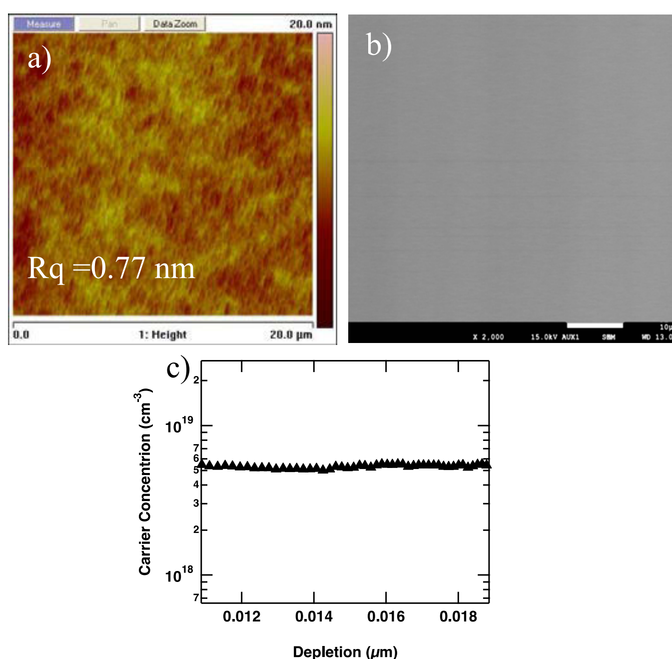

Fig. 2. a) Atomic force microscopy of a D-HVPE grown GaAs layer on a (110) GaAs substrate with 3 degree offcut. b) Cathodoluminescence image of a D-HVPE grown (110) GaAs layer, showing no recombinative defects. c) Carrier concentration vs. depletion depth in a (110) GaAs epilayer, as determined by a capacitance-voltage measurement.

Fig. 2(a) shows atomic force microscopy of a D-HVPE-grown GaAs layer on a (110) GaAs substrate offcut 3° towards (111)A with low roughness below 1 nm, satisfying the milestone metric. Fig. 2(b) shows a cathodoluminescence image of a (110) D-HVPE GaAs layer, with no recombination at defects observed, indicating high quality material suitable for solar cells. Fig. 2(c) shows the results of capacitance-voltage measurement on a n-doped GaAs layer, which yields a carrier concentration vs. depletion depth profile. The doping is well above the 1x10^{18} cm^{-3} target defined in the milestone. These three pieces of data demonstrate that we can grow the necessary (110) GaAs layers for devices by HVPE, satisfying the milestone.

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1.1.2: Achieve > $1x10^{18}$ cm^{-3} doping level in at least 200 nm thick p- and n-doped (110) GaInP with a lattice-matched composition between $Ga_{0.50}In_{0.50}P$ and $Ga_{0.52}In_{0.48}P$.

GaInP is a critical layer in III-V solar cells because it is used to passivate GaAs junctions and serve as an etch stop for inverted devices, but it must be lattice-matched, otherwise dislocation formation will degrade device performance. The thickest GaInP layer required for a GaAs device is ~200 nm, meaning that a composition of $Ga_{0.51}In_{0.49}P$ with $x_{Ga} \pm 0.01$ should be sufficient to prevent relaxation based on critical thickness calculations. High efficiency devices require the incorporation of front and rear GaInP passivation layers with n- and p-type doping of > $1x10^{18}$ cm^{-3}, respectively. Development of these GaInP epilayers gives us the building blocks to make a GaAs solar cell.

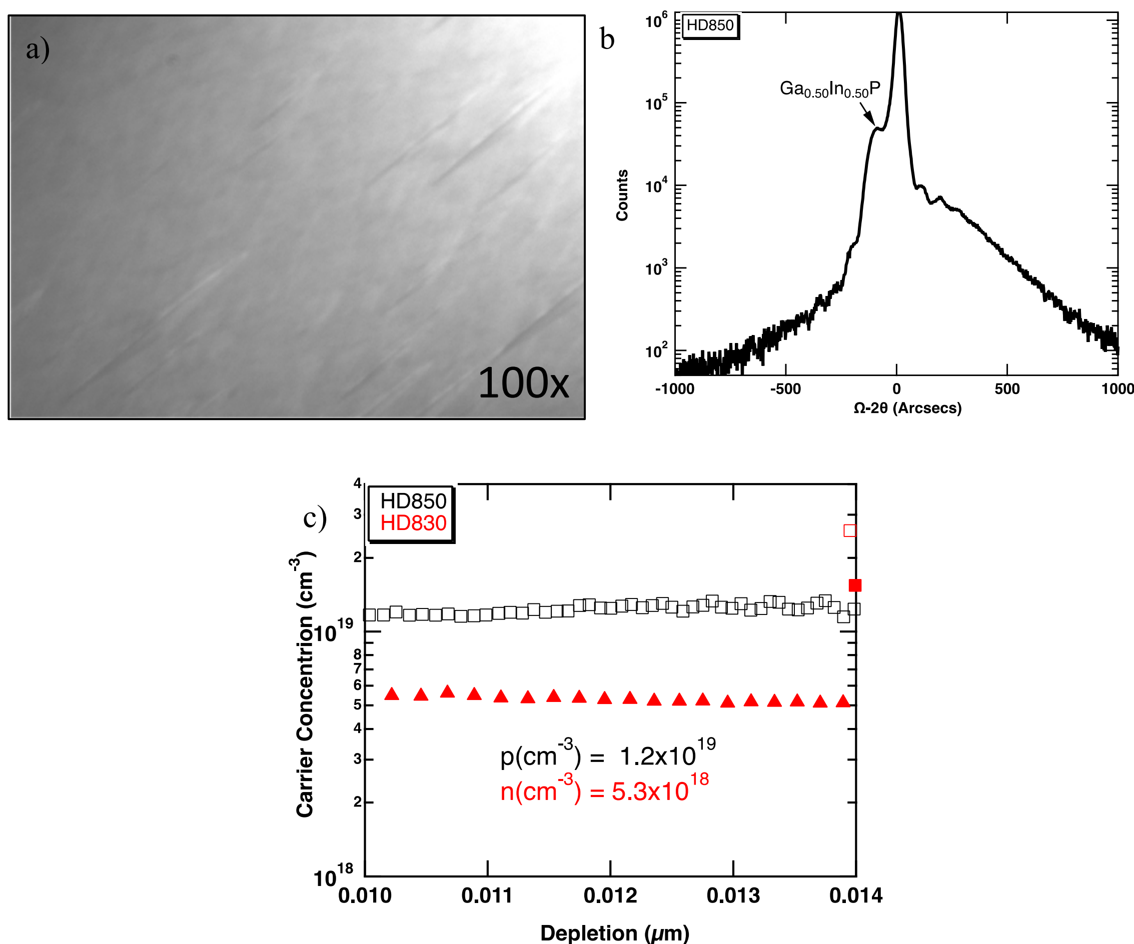

Fig. 3. a) 100x optical micrograph of a (110) GaInP epilayer grown by HVPE. b) X-ray diffraction measurement of the (220) reflection of a (110) GaInP epilayer. The GaInP peak and GaAs substrate peak are pointed out in the figure. c) Carrier concentration vs. depletion depth of p- and n-doped (110) GaInP epilayers grown by HVPE.

Fig. 3(a) shows a Nomarski optical microscopy image of an HVPE (110) GaInP epilayer with a very smooth surface, without the cross-hatch indicative of relaxation. We performed X-ray diffraction (XRD) to measure the lattice constant and composition of the GaInP layer. Fig. 3(b) shows a (220) XRD scan of a GaInP epilayer, showing close lattice match between the GaInP

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epilayer and the GaAs substrate. The composition is $Ga_{0.50}In_{0.50}P$, within the tolerance specified by the metric. Fig. 3(c) shows the results of capacitance-voltage measurements on p- and n-doped GaInP epilayers. The doping is well above the $1x10^{18}$ cm^{-3} target for both dopant types as defined in the milestone. The data in Fig. 2 demonstrate that we can grow the necessary solar cell layers of (110) GaInP by HVPE, satisfying the milestone.

1.1.3: Grow a passivated, anti-reflection coated GaAs device with at least 15% (absolute) solar conversion efficiency on an epi-ready (110) wafer, as well as a witness device grown on a previously spalled (110) wafer with efficiency within 15% (relative) of the epi-ready device.

Device efficiency is the most direct way to evaluate whether the quality of material grown on epi-ready and as-spalled surfaces can sustain high quality devices. The 15% efficiency baseline in the proposed device structure represents the development of GaAs and GaInP with requisite doping, as well as their integration into a complete device with suitable quality. This efficiency represents significant progress after only one year of development, and a path forward for future work. Demonstration of efficiency within 15% (relative) in at least one device on spalled (110) GaAs shows that major hurdles to regrowth on spalled surfaces do not exist, with the understanding that future optimization of spalling and re-growth may still be required. Overall, the milestone validates the potential for both high-efficiency (110) devices as well as a viable low-cost pathway for substrate reuse on this platform.

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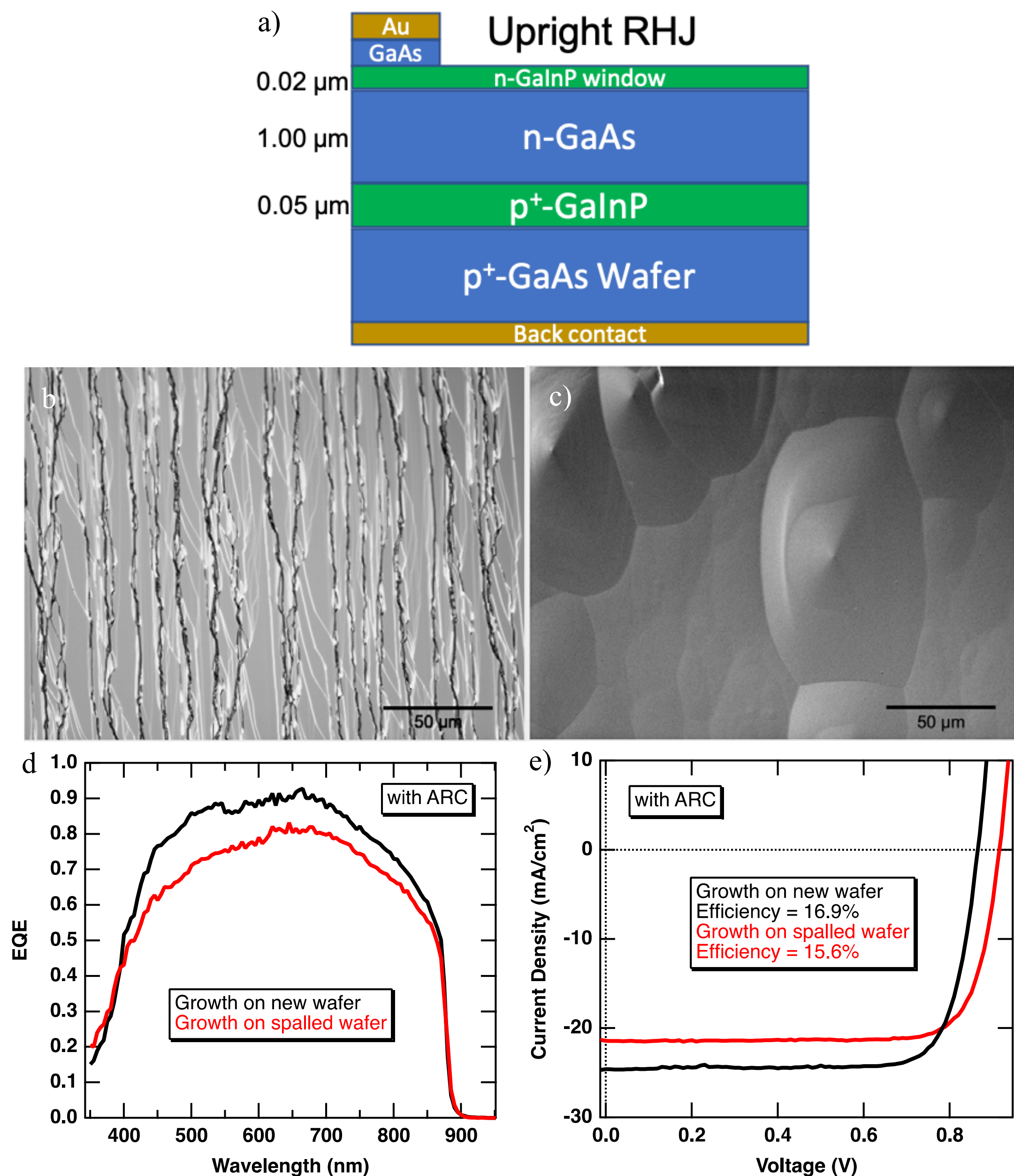

Fig. 4. a) Upright device structure used in this study. b) Nomarski micrograph of the post spall surface morphology of a (110) GaAs wafer. c) Nomarski micrograph of the surface after growth of the upright device structure on the previously spalled wafer. d) External quantum efficiency of upright devices grown on new and previously spalled (110) wafers. e) AM1.5G light current-density voltage measurements of these devices.

We initially attempted an inverted device growth but faced challenges with processing the cells regrown on the spalled surfaces because the etch stop layer was insufficiently flat due to the spall surface morphology. We believe that inverted growth and processing will be possible with spalling surface optimization as well as nucleation and regrowth optimization, but did not have the resources to perform that development work in this agreement. Instead, we used the upright device structure shown in Fig. 4(a). Fig. 4(b) shows the surface of the (110) wafer used for the regrowth after spalling, and Fig. 4(c) shows the surface after regrowth. We see the presence of surface hillocks that

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we did not observe in growth on a new, non-spalled wafer. This result suggests that learning how to nucleate and grow on spalled surfaces is key to future development of this technology. We note that the spalled wafer underwent no processing before re-growth, except for being dipped in a Ni-selective etchant to remove residual Ni left over from the spalling process. The etchant does not chemically etch the GaAs. Fig. 4(d) shows the external quantum efficiency of upright devices grown on a previously spalled wafer and a control device grown on brand new non-spalled wafer. The device grown on the spalled wafer exhibits a reduced EQE relative to the control implying a reduced carrier diffusion length in the spalled wafer device. Thus, this device has a lower short-circuit current density than the control device. However, comparing the current density-voltage curves of each device [Fig. 4(e)], both devices have an efficiency above the 15% threshold, and the spalled wafer device is within ~7% relative efficiency of the control device, satisfying the milestone.

1.2.1: Demonstrate wafer scale spalling, removing 14 cm^2 of area using varying edge release methods and down-select to the more reliable method.

In order for spalling to provide an economical substrate re-use solution, wafer-scale spalls must be demonstrated without significant edge effects that increase roughness and limit the number of achievable spalls per wafer. (110)-oriented GaAs wafers with 50-mm diameter were prepared for spalling by electroplating a stressed Ni layer on the surface, defined by an edge-adhesion demoter coated on the outer 4 mm of the wafer radius. Three methods for applying the edge-adhesion demoter were investigated: manual application of colloidal Ag paint, lithography of photoresist (PR) edge-demoter with a sputtered Ni seed layer, and lithography of photoresist edge-demoter with no sputtered Ni seed layer. An area of 14 cm^2 was spalled from wafers using an automated spalling apparatus. We down-selected to lithography of photoresist edge-demoter with no sputtered Ni seed layer as the most suitable method for controlled spalling, based on good spall reliability, decreased presence of edge effects and surface features such as arrest lines, and good process compatibility for repeatable spalling. Fig. 5 illustrates the down-selected spalling procedure and a representative spalled film and wafer.

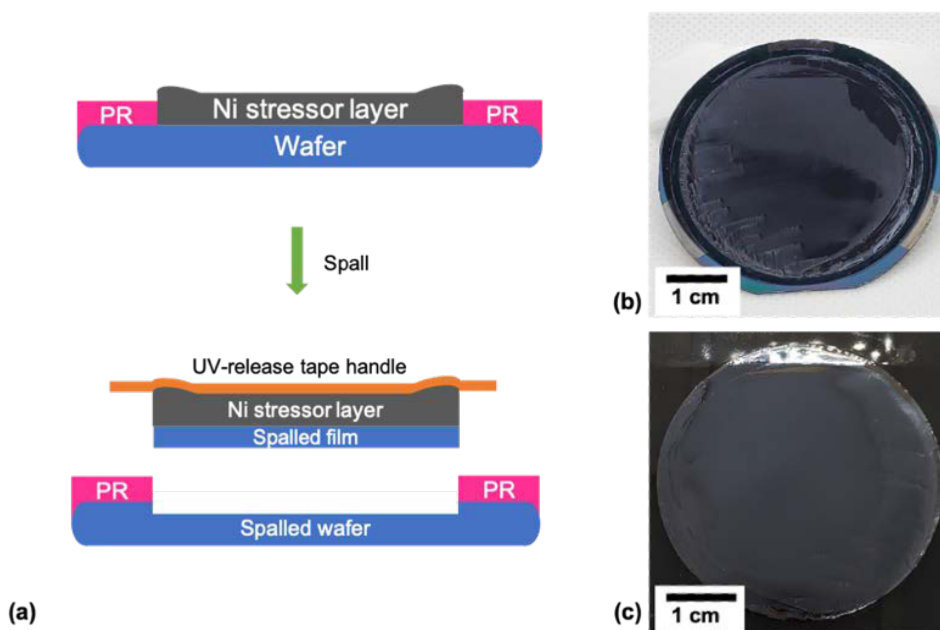

Fig. 5. (a) Diagram of spalling process for (110) GaAs wafers, (b) spalled (110) GaAs wafer, (c) spalled (110) GaAs film

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1.2.2: Demonstrate control of spall depth at wafer-scale, removing 14 cm^2 of area with removed thickness between 3 and 10 µm. Verify that any arrest line defects do not exceed 5 µm in peak to valley height.

A selective etching procedure was developed to measure the spalled GaAs depth of films. A gridded PR mask was applied using photolithography and exposed GaAs was etched. The spall depth was measured by contact profilometry of the etched grid points and mapped over the wafer surface. Measurements showed that the average spalled GaAs depth was within the milestone limits, however local deviations outside the target depth were observed. Wafers were evaluated using laser profilometry, confocal microscopy, and atomic force microscopy (AFM) for surface roughness and topographical features. Arrest lines exceeding 5 µm in peak-to-valley height were observed on spontaneously spalled samples but were absent on samples that underwent controlled spalling. Crystallographic steps and terraces (features distinct from arrest lines and other fracture morphologies previous observed in Ge and (100)-GaAs) were observed on spalled samples with average peak-to-valley height of 0.1-1 µm, with slightly larger steps observed on samples with high wafer offcut angle (1.5° ±0.5°, 3° ±0.5°). No steps exceeded 3 µm in height, satisfying the milestone target. Steps were separated by smooth terraces consisting of {110} planes with sub-nm roughness. The size of terraces is dependent on the offcut angle of the substrate and the spall direction. Substrates with high offcut angle (1.5° ±0.5°, 3° ±0.5°) produced small terraces from a few microns to 10s of micrometers in width. Substrates cut on-axis within ±0.5° and ±0.05° tolerance produced large terraces tens to hundreds of micrometers in width. Spall direction impacted terrace width on substrates with high offcut angles, producing wide parallel terraces in [1-10] spalling and small irregular terraces in [00-1] spalling. Fig. 6 compares the morphology of spalled (110) GaAs surfaces by offcut angle and spall direction.

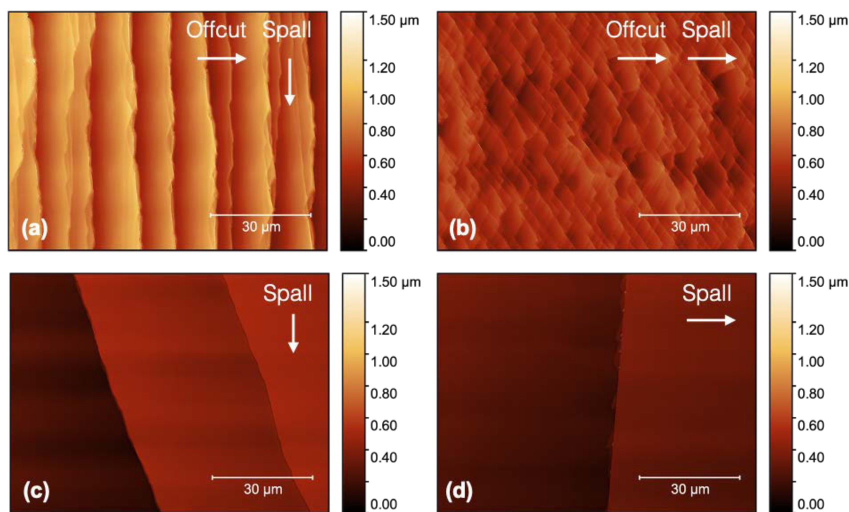

Fig. 6. Confocal micrographs of spall morphologies in (110) GaAs by offcut angle and spall direction. (a) 3°B, [1-10] spall (b) 3°B, [00-1] spall (c) On-axis, [1-10] spall (d) On-axis, [00-1] spall

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7 Significant Accomplishments and Conclusions:

This project demonstrated the first HVPE-grown GaInP with a (110) orientation, as well as the first direct growth of a GaAs solar cell device on a previously spalled GaAs wafer, of any orientation. We developed significant understanding of how to control the growth morphology of HVPE growth on (110) surfaces, which is significant because this is a traditionally challenging orientation on which to grow. We see no barriers to the achievement of similar efficiencies and material quality on (110) vs. (100) substrates. In order to increase demonstrated efficiencies, development of understanding about how to control nucleation on spalled surfaces will be key.

A procedure for repeatable, wafer-scale spalling of (110) GaAs was developed. We demonstrated high-quality spalls at least 14 cm^2 in area from 50-mm diameter wafers and controlled the average spall depth to be within 3-10 µm needed for economical spalling of devices with minimal excess substrate loss. Some variability in spall depth outside the target range was observed. Spalled surfaces were free of large arrest lines and surface features greater than 3 µm in peak-to-valley height, which can degrade the efficiency of regrown III-V devices [9]. A sub-µm step-terrace morphology was discovered on the post-spall wafer surface, resulting from the restricted cleavage system of GaAs. The size and shape of steps and terraces can be adjusted by the substrate offcut angle and spall direction, enabling ample opportunity for optimization of morphologies suitable for device growth and spall depth waste minimization on (110) GaAs.

8 Budget and Schedule:

The budget and spending is summarized in the following table:

Spending Summary by Budget Category						
	Approved Budget per SF-424A				Actual Expenses	
Budget Categories per SF-424a	**BP 1**	**BP 2**	**BP 3**	**Total**	**Cumulative**	**%**
a. Personnel	$115,499			$115,499	$114,748	99%
b. Fringe Benefits	$0			$0	$0	
c. Travel	$1,977			$1,977	-$377	-19%
d. Equipment	$0			$0	$0	
e. Supplies	$16,704			$16,704	$23,412	140%
f. Contractual	$52,320			$52,320	$51,100	98%
g. Construction	$0			$0	$0	
h. Other	$13,500			$13,500	$10,430	77%
i. Total Direct Charges	**$200,000**	**$0**	**$0**	**$200,000**	**$199,313**	**100%**
j. Indirect Charges	$0				$0	
k. Total Charges	**$200,000**	**$0**	**$0**	**$200,000**	**$199,313**	**100%**
DOE Share	$200,000	$0	$0	$200,000	$199,313	
Cost Share				$0		
Cost Share Percentage	0.0%			0.0%	0.0%	

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The project spent more than originally budgeted on supplies because we learned early during the project that the substrate offcut has a dramatic effect on the spalled surface morphology. To study this effect, we acquired (110) GaAs substrates with many different offcut directions and magnitudes, increasing the total substrate cost. This extra cost was made up by funds originally budgeted for travel that were not used due to the COVID-19 pandemic, as well as slightly reduced spending on personnel and other costs.

The project had one budget period, originally 10/1/2019-9/30/2020, but a two-quarter no-cost extension was granted, extending the project end date to 3/31/2020 to accommodate delays due to the COVID-19 pandemic.

9 Path Forward:

Future growth development should focus on understanding nucleation and growth on spalled surfaces in the initial stages. Depending on the spalling conditions and wafer offcut, the surface can have different morphology. It will be key to understand how to promote flat growth over steps, and coalescence without creating threading dislocations which will harm performance. Further down the road, development of GaInP and tandem devices will be key to boosting efficiency.

Future development of controlled spalling should focus on improving spall depth uniformity to eliminate device-depth deviations and exploration of edge-to-edge electroplating and spalling techniques. Controlled spalling of (110) GaAs can provide a variety of surface morphologies based on offcut and spall direction. Future work should seek to better understand the formation of the step-terrace morphology and the impact of these variations on device regrowth and planarization.

If these development challenges can be overcome, there would be significant potential to transfer this technology to companies PV for space and unmanned aerial vehicles (Microlink Devices, Spectrolab, SolAero). The spalled devices will be lightweight, ideal for these applications, and the reductions in substrate costs will enable them to reach more markets.

10 Inventions, Patents, Publications, and Other Results:

Publications

1. Metaferia, W., Braun, A.K., Simon, J., Packard, C.E., Ptak, A.J. and Schulte, K.L. "Control of Surface Morphology during the Growth of (110)-Oriented GaAs by Hydride Vapor Phase Epitaxy," Crystal Growth & Design, 2021. https://doi.org/10.1021/acs.cgd.1c00235
2. Metaferia, W., Chenenko, J., Packard, C.E., Ptak, A.J. and Schulte, K.L. "(110)-Oriented GaAs Devices and Spalling as a Platform for Low-Cost III-V Photovoltaics," *48th Photovoltaics Specialists Conference,* 2021.
3. Chenenko, J., "The Role of Offcut and Spall Direction in Surface Morphology of Spalled (110) GaAs", MS Thesis, Colorado School of Mines, 2021

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Patents

1. Metaferia, W., Braun, A.K., Simon, J., Packard, C.E., Ptak, A.J. and Schulte, K.L. "Control of Surface Morphology during the Growth of (110)-Oriented GaAs by Hydride Vapor Phase Epitaxy," US Provisional Application No. 63/196,897.

Students Trained

1. Wondwosen Metaferia, post-doc, now employed at SolAero Technologies
2. Jason Chenenko, Colorado School of Mines, M.S. in Materials Science, graduating July 2021.
3. Jie Chen, Colorado School of Mines, post-doc, now employed at Applied Optoelectronics, Inc.

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