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High Mobility Cd₃As₂(112) on GaAs(001) Substrates Grown via Molecular Beam Epitaxy

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ABSTRACT: The three-dimensional Dirac semimetal Cd₃As₂ exhibits ultrahigh electron mobilities that are attractive for optoelectronic devices. However, its strong propensity to grow in the (112) orientation limits the feasibility to epitaxially integrate it into semiconductor structures that are conventionally grown in the (001) orientation. Here, we demonstrate a route to epitaxially growing high mobility Cd₃As₂(112) layers on GaAs(001) substrates, opening up possibilities for device design. The (001) crystallographic orientation of the GaAs substrate is switched to the (111) orientation through a strain-driven process at a CdTe/ GaAs interface, resulting in a CdTe(111) buffer layer on top of which Cd₃As₂ can be grown. Although the CdTe(111) buffer layer

Thin CdTe interlayers permit Cd₃As₂ (112) growth on GaAs (001)

templates Cd₃As₂ in the (112) orientation, it is not sufficient for producing Cd₃As₂ with high electron mobility. We therefore demonstrate additional buffer layer design principles for realizing Cd₃As₂(112) epilayers with similar electron mobilities to those grown on lattice-mismatched III−V (111) substrates. Finally, we outline a pathway to use this approach to grow Cd₃As₂(112) epilayers on Si(001) substrates, further expanding the potential to integrate Cd₃As₂ into electronic devices.

KEYWORDS: molecular beam epitaxy, topological semi-metals, Cd₃As₂, thin films, heterostructures
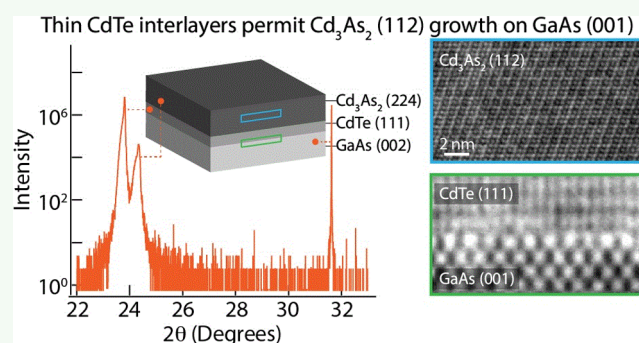
1. INTRODUCTION

Three-dimensional (3D) topological semimetals, characterized by the presence of bulk and surface band touching nodes, offer ultrahigh carrier mobilities and strong broadband optical absorption that are advantageous for optoelectronic applications. To exploit these properties, effective strategies for integrating them into semiconductor heterostructures must be developed. Dirac semimetal Cd₃As₂ is among the most studied topological semimetals and is an excellent candidate for integration, as it is air stable and has already been epitaxially grown on a variety of conventional semiconductor substrates.[1−8] A challenge to realizing high performance and scalable devices will be to control integration such that both Cd₃As₂ and semiconductor layers can be grown in their preferred crystallographic orientations to improve their properties, reduce defects, and enhance surface smoothness necessary for heteroepitaxy.

The easiest growth surface to achieve smooth, high quality epilayers on most zinc blende semiconductors is the (001) orientation.[9] Growing on this surface permits the widest range of deposition conditions to be used without producing rough surfaces or high native defect populations, and manufacturing is most commonly configured to utilize large area GaAs(001) substrates. However, the (112) surface of Cd₃As₂ is the primary cleave plane,[10] and its low energy commonly

determines the facet formation during bulk single crystal growth and the crystallographic orientation during epitaxy.[11] Owing to its tetragonal structure and a c/a ratio of ~2, the atomic arrangement across this surface is similar to that of the zinc blende (111) unit cell,[4] allowing high quality growth of Cd₃As₂(112) on CdTe(111)[5,6] and GaAs(111)[12] substrates. As-grown bulk epilayers (>100 nm) in this orientation in these studies exhibit room temperature electron mobilities above 15,000 cm²/V s. Recently, growth of Cd₃As₂ along its higher energy (001) surface was demonstrated on a GaSb(001) substrate,[13] using an InAs wetting layer to improve nucleation. These layers have similar electron mobilities to (112) oriented films, but their surfaces form an undesirable 3D morphology. The conductivity of GaSb substrates and low band gaps of InAs can also form alternate conduction channels that are not practical for device applications.

One route to epitaxially grow Cd₃As₂ in the lower energy (112) orientation on technologically relevant GaAs(001)
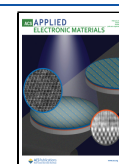
substrates is to change the crystallographic orientation in an intermediate buffer layer. Past work has shown that controlling the growth initiation conditions of CdTe on GaAs(001) can force it into the (111) orientation, with the removal of the surface oxide being critical to driving the (111) orientation.[14,15] In particular, higher temperature annealing without As was shown to create the highest quality crystals and was suggested to correspond to the changes in the As and Ga termination.[15] Creating a Ga−Te bonding interface allows the enormous lattice mismatch (14.6%) to be immediately relaxed across 3 monolayers by forming the pseudoepitaxial relationship shown in Figure 1, which was confirmed with careful
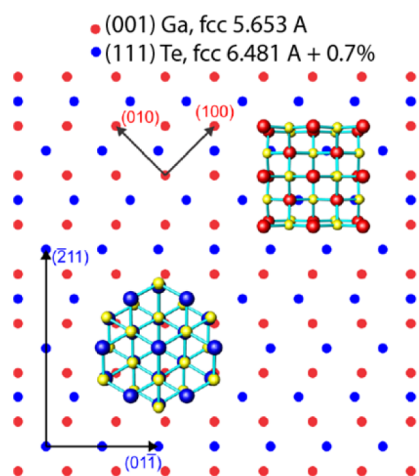
Figure 1. GaAs(001) and CdTe(111) unit cells. During growth, [1−10] directions are aligned in a coincident-site lattice, while [−211] and [110] directions are aligned with 0.7% mismatch. The red circles represent Ga, the blue circles represent Te, and the yellow circles represent the As and Cd atoms in the GaAs and CdTe crystals, respectively.

diffraction experiments.[16] While the dislocation density is high, relaxation occurs in only one principal direction, lowering the density relative to what is typically expected for this level of mismatch. Such a CdTe(111) buffer would be advantageous for growing Cd_3As_2 in its preferred (112) orientation on GaAs(001) substrates, but this approach must be adapted to implement broader strategies for controlling defects within the Cd_3As_2 epilayer and realizing the high mobilities expected for this material.[7]

Here, we demonstrate the epitaxy of Cd_3As_2(112) layers on II-Te(111)/GaAs(001) structures with electron mobilities comparable to Cd_3As_2(112) grown on GaAs(111) substrates. High electron mobilities are only possible by initiating the orientation change on a miscut GaAs(001) substrate to suppress the formation of twin defects and then designing the II-Te buffer structure to include a lattice-matched $Zn_xCd_{1−x}Te$ buffer to remove relaxation-related defects in the Cd_3As_2 epilayer. The insights detailed here now enable new optoelectronic device structures that take advantage of the respective preferred orientations of the Cd_3As_2 epilayer and semiconductor substrate without sacrificing the properties of the Cd_3As_2 epilayer.

2. EXPERIMENTAL METHODS

GaAs(001) buffers were grown on on-axis GaAs(001) substrates as well as substrates with a 2 or 4° miscut toward (111)A in a dedicated III−V molecular beam epitaxy chamber and then capped with

amorphous As_2. These GaAs(001) structures were then loaded into a II−VI chamber, where II-Te and Cd_3As_2 epilayers were grown using elemental sources and conditions similar to previous reports.[7] CdTe buffer layers were grown to 125 nm in instances where single layer buffer structures were implemented and to 25 nm in instances where an additional 125 nm $Zn_xCd_{1−x}Te$ buffer was inserted before Cd_3As_2 growth. X-ray diffraction (XRD) was performed in a Rigaku SmartLab system using a 4-bounce Ge(220) monochromator. Room temperature Hall measurements were performed on Van der Pauw geometries with indium contacts and an applied voltage of 5 mV. Variable temperature magneto-transport measurements were performed on Hall bar structures in a Quantum Design physical properties measurement system using a ±0.1 T field for Hall measurements. Hall bars were fabricated using standard photolithography, wet chemical etching, and Au electroplating methods. A $2NH_4OH/1H_2O_2/10H_2O$ etchant, commonly used for other arsenide compounds, was found to etch Cd_3As_2 at a rate of approximately 20 nm/s and is highly selective with respect to the telluride buffer layers. Transmission electron microscopy (TEM) was performed on a FEI Tecnai F20 UltraTwin field emitting gun scanning TEM operated at 200 kV and a FEI Tecnai ST30 TEM operated at 300 kV. Samples for TEM analysis were prepared by a standard lift-out technique using an FEI Nova NanoLab 200 dual beam focused ion beam (FIB) workstation. The sample surface was first protected by deposition of a Pt protective layer, and ion milling was carried out with Ga^+ ions with a 30 kV acceleration voltage and finished <5 kV. Ga^+ ion FIB damage was removed using low energy (<1 kV) Ar^+ ion milling in a Fischione NanoMill with the samples cooled using liquid nitrogen.

3. EXPERIMENTAL RESULTS

The CdTe(111)/GaAs(001) interface was formed by methods similar to those previously reported.[16] Following removal of the As cap at 350 °C, the on-axis GaAs(001) structure was briefly annealed at 500 °C to remove As from the surface, creating a Ga-rich, $c(8 \times 2)$ reconstruction measured by reflection high energy electron diffraction (RHEED). Upon cooldown to growth temperatures, signs of the (6 × 6) reconstruction are visible (see Figure 2a).[17] These Ga-rich reconstructions are critical for forming the Ga−Te bonding arrangement that will mediate the orientation change. We note that many previous studies used compound CdTe sources to allow for growth of thick layers, which limits the ability to intentionally promote Te bonding. By using elemental sources here, the Ga-rich GaA surface can be briefly exposed to elemental Te flux prior to the initiation of CdTe growth to further promote the Ga−Te arrangement. RHEED measurements performed during CdTe epitaxy exhibit streaky (1 × 1) patterns, indicating smooth two-dimensional growth.

XRD (Figure 2b) confirms that the CdTe epilayer nucleated on the Ga-terminated GaAs(001) surface is indeed in the (111) orientation. The presence of interference fringes further indicates that the interface is abrupt. To highlight the importance of the initial Ga−Te bonding at the CdTe (111)/GaAs(001) interface on the resulting CdTe(111) material, $2\theta−\omega$ curves were measured on epilayers grown after GaAs(001) surface preparations that reduced the degree of Ga−Te bonding. CdTe(111) epilayers grown directly on As-decapped $c(4 \times 4)$ GaAs(001) surfaces exhibited a double XRD peak, while partial removal of the As surface termination using UV photon irradiation[18] produced a sharper XRD peak but no interference fringes (Figure 2b). Rocking curves of the same peaks show that the full width half max (FWHM) decreases significantly when fully promoting Ga−Te bonding at the interface, going from 506 arc seconds without annealing to 226 arcseconds following the optimum surface treatment. This FWHM improvement results in values similar to using an initial ZnTe layer to then nucleate CdTe(111) on GaAs(111) substrates (202 arcseconds) as a high-quality buffer for Cd_3As_2(112) growth (Figure 2c).[7]

TEM images of the CdTe(111)/GaAs(001) interface prepared by maximizing Ga−Te bonding further confirms the sharp interface and orientation change. FFTs taken in the interface region demonstrate the expected epitaxial relationship shown in Figure 1. Furthermore,
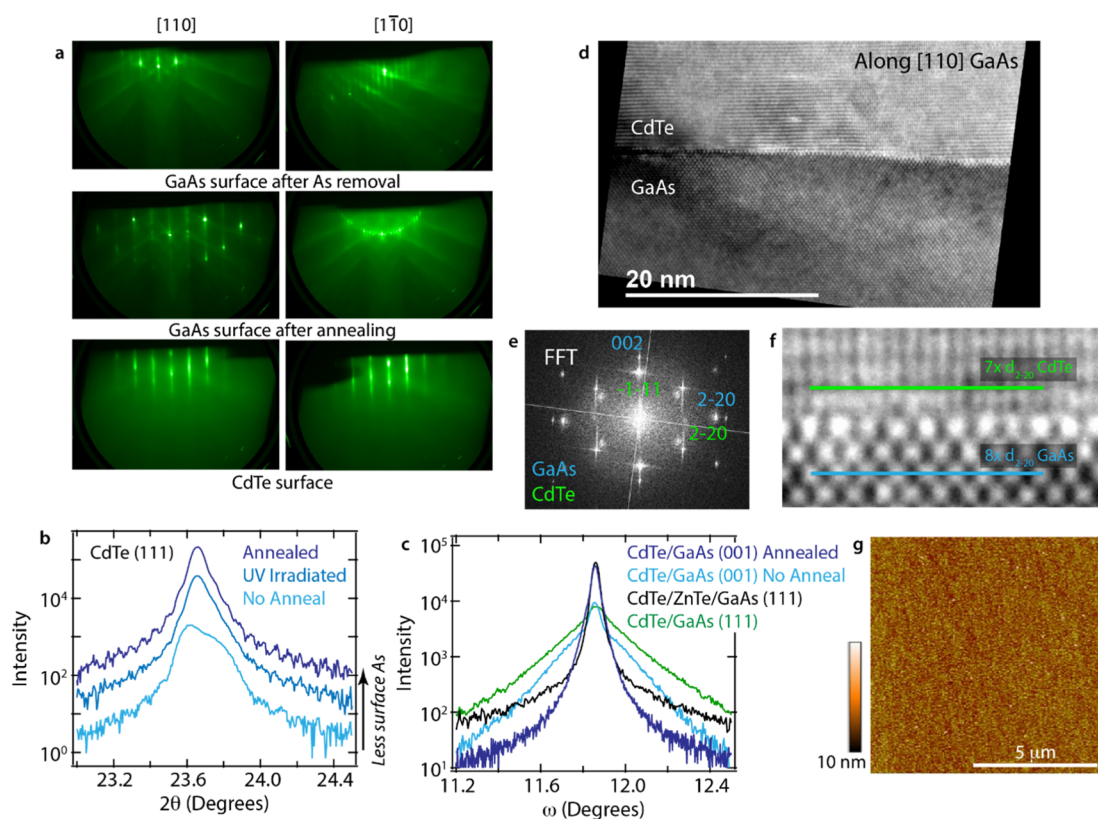
Figure 2. (a) RHEED patterns observed during growth after amorphous As removal (top) and annealing of the GaAs(001) buffer to produce a Ga-rich surface (middle) and CdTe growth (bottom). (b) XRD patterns of CdTe(111) grown on GaAs(001) following pre-treatments that produced surfaces with varying As content. (c) XRD patterns of CdTe (111) layers grown on GaAs(001) and (111) substrates using various interface treatments. (d) TEM image of the CdTe(111)/GaAs(001) interface. (e) Fast Fourier transform (FFT) of the GaAs/CdTe interface confirming the epitaxial relationship. (f) TEM imaging showing a 7:8 coincident site lattice across the interface, as well as the sharp interface transition. (g) Atomic force microscopy (AFM) image of a CdTe(111) layer grown on a GaAs(001) substrate.
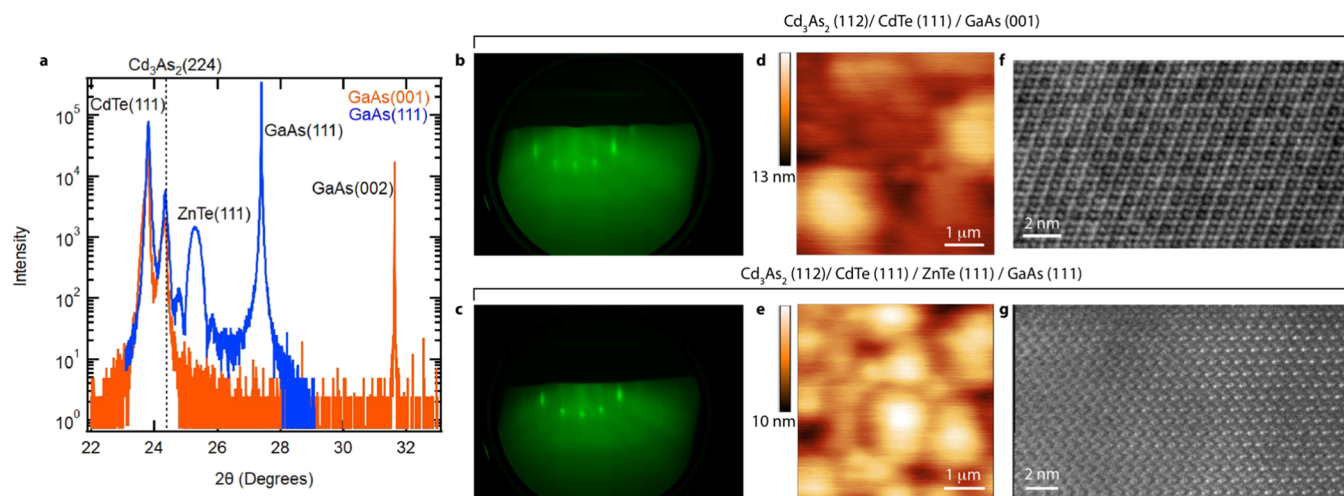

Figure 3. (a) XRD patterns of Cd_3As_2(112) epilayers grown on CdTe(111)/GaAs(001) and CdTe(111)/ZnTe(111)/GaAs(111) structures. (b) RHEED, (d) AFM, and (f) TEM images of Cd_3As_2(112) grown on CdTe(111)/GaAs(001) structures. (c) RHEED, (e) AFM, and (g) TEM images of Cd_3As_2(112) grown on CdTe(111)/ZnTe(111)/GaAs(111) structures.

the image in Figure 2f shows the expected 7:8 coincident site lattice expected in this direction. Finally, while the exact interface region cannot be determined by a single image, it is consistent with previous reports which observed the transition to occur over a 3 monolayer As/Ga/Te region.[16] Even after 125 nm of CdTe(111) growth, the surface remains smooth (Figure 2e) with a root mean square (RMS) roughness of 0.92 nm, which is key to promoting 2D epitaxy of the

subsequent layers and avoid extended defect formation that is more common with 3D growth.

Cd_3As_2 epitaxy on the on-axis CdTe(111)/GaAs(001) structure is remarkably similar to that on a CdTe/ZnTe/GaAs(111) structure. Figure 3 summarizes the results from both growths. The $2\theta-\omega$ curves (Figure 3a) are nearly identical in the region of interest, with similar peak shapes and positions. The RHEED patterns (Figure 3b,c) are likewise identical, with similar 4× surface reconstructions and
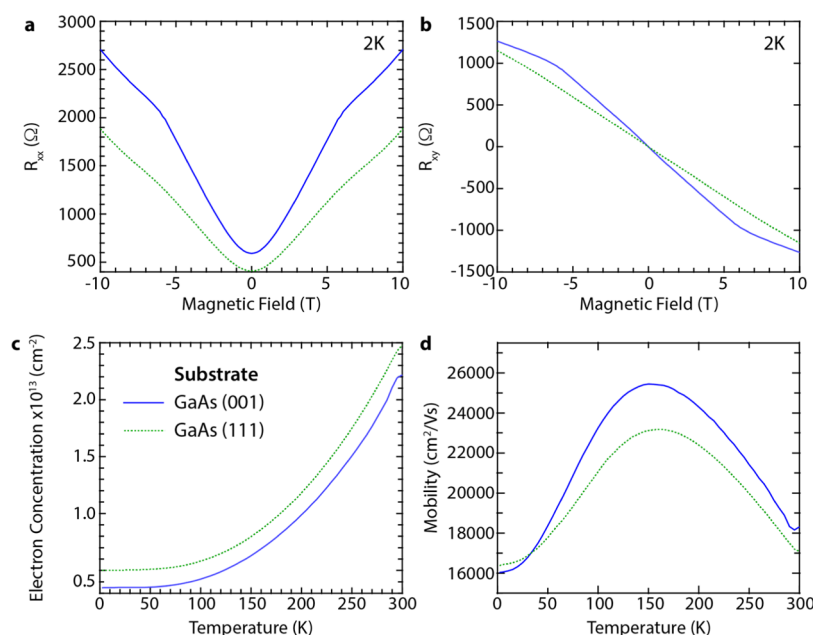
Figure 4. Magneto-transport measurements of $Cd_3As_2(112)$ epilayers grown on $ZnCdTe(111)/CdTe(111)/GaAs(001)$ (blue solid line) structures compared with the epilayers on $ZnCdTe/ZnTe/GaAs(111)$ (green dashed line). (a) Longitudinal magnetoresistance, R_{xx}. (b) Transverse magnetoresistance, R_{xy}. (c) Electron concentration as a function of temperature. (d) Electron mobility as a function of temperature.

intensities, and the surface morphologies (Figure 3d,e) are comparable, with RMS roughnesses of 1.37 and 1.27 nm, respectively. The high resolution TEM micrographs in Figure 3f,g verify that both Cd_3As_2 layers are single crystal epilayers in the (112) orientation. However, the room temperature electron mobilities are both around 4800 cm^2/V s and are unacceptably low for bulk Cd_3As_2 epilayers. This result highlights the fact that these designed CdTe(111) buffers are not sufficient for growing $Cd_3As_2(112)$ on GaAs(001).

Extended defects are known to impact the room temperature electron mobility. Previous studies of Cd_3As_2 epitaxy on (111) zinc blende substrates showed that implementing the combination of a single lattice-matched $Zn_{0.42}Cd_{0.58}Te$ buffer layer following a ZnTe nucleation layer to minimize strain relaxation-induced dislocation formation in Cd_3As_2, and a miscut substrate to suppress twinning in the Cd_3As_2 epilayers is required to reach high mobilities.[7] Adding Zn to the initial CdTe layer on GaAs(001) was unsuccessful in nucleating a coherent layer and resulted in a film with both (111) and (001) domains and poor epitaxial registry, as observed in XRD diffraction patterns. Therefore, a thin CdTe nucleation layer is still required for switching the orientation from (001) to (111). We have found that a 25 nm CdTe nucleation layer is sufficient for this purpose, at which point Zn can then be added to further relax the lattice constant to that of Cd_3As_2. Twin defects were previously suppressed in the II−VI buffer and Cd_3As_2 epilayers grown on GaAs(111) substrates by growing on a substrate with a 2° miscut.[7] However, using just a 2° miscut on GaAs(001) only raised the electron mobilities to 8000− 10,000 cm^2/V s when combined with a $Zn_{0.42}Cd_{0.58}Te$ buffer layer. We find here that a larger 4° miscut is needed to reach electron mobilities exceeding 15,000 cm^2/V s. It is possible a lower offcut may be sufficient if oriented in a different way, for example, toward (111)B or this simply may be required to fully suppress twin domain formation in these CdTe(111) layers, since they predominantly relax in one direction.

Magneto-transport measurements, as shown in Figure 4, were used to further confirm that $Cd_3As_2(112)$ epilayers grown on GaAs(001) substrates behave similarly to $Cd_3As_2(112)$ epilayers grown on the GaAs(111) substrate. Both exhibit nearly identical magnetic field-dependent R_{xx} and R_{xy} values as well as temperature-dependent electron concentrations and mobilities. In fact, the epilayer grown on GaAs(001) has slightly higher mobilities and lower carrier concentrations than this reference sample grown on GaAs(111),

though both are typical of the highest mobility as-grown Cd_3As_2 samples on GaAs(111),[4,20] and these differences between the two films are not beyond typical run-to-run variations. Their comparable behavior is also evident in the variable field measurements at 2 K. Similar curve shapes were reported in both R_{xx} and R_{xy} on thinner films (∼130 nm)[19] and were attributed to Hall plateaus that were also explored with angle-dependent measurements. These features may be less prominent in our epilayers due to the increased film thickness. The roll over in the mobilities at low temperature, observed in both Cd_3As_2 epilayers, has been previously observed and was attributed to the contributions from unpassivated surfaces.[20] The high threading dislocation densities that are present in both Cd_3As_2 epilayers arising from the relaxation in the II−VI buffer layers[7] could also contribute to the mobility reduction at lower temperatures and is addressable with the inclusion of buffer layers to reduce threading components.[21] For temperatures relevant to nearly all device applications, however, these films are comparable to the highest thin film values published to date.

4. DISCUSSION

The known technique of manipulating the surface of a GaAs(001) substrate to abruptly nucleate a CdTe(111) epilayer template provides an opportune pathway for incorporating $Cd_3As_2(112)$ into conventional semiconductor structures. However, we have shown here that this template alone is not sufficient to grow Cd_3As_2 epilayers with high electron mobilities. Additional methods of reducing extended defects in the Cd_3As_2 epilayer must be applied to produce a >3× increase in the electron mobility that is now commensurate with the best $Cd_3As_2(112)$ epilayers grown on GaAs(111) substrates. We highlight two important aspects of our results. First, the established approach of using a miscut substrate to reduce twin formation in II-Te epilayers also works when simultaneously changing the crystallographic orientation of the II-Te layer relative to the substrate using a Ga−Te-rich interface. The effect of the miscut angle on the room temperature Hall mobility is summarized in Table 1. Second, the two-step $Zn_xCd_{1-x}Te$ (125 nm)/CdTe (25 nm) buffer structure used here is a very effective template for

Table 1. Summary of the Highest Observed Cd_3As_2 in Room Temperature Hall Mobilities as a Function of Substrate Miscut and Buffer Structure Grown on Two Different GaAs Substrate Orientations

substrate and buffer	mobilities on GaAs(001) [cm^2/V s]	mobilities on GaAs(111) [cm^2/V s]
on-axis, CdTe	>4800	>4800
2° miscut, ZnCdTe	>8000	>18,000
4° miscut, ZnCdTe	>18,000	N/A

Cd_3As_2 growth, even though it is much thinner than the >1 μm CdTe(111) layers examined in previous studies to reduce dislocations.[8,22,23] These two aspects improve the ability to integrate high mobility Cd_3As_2 epilayers into (001)-oriented semiconductor devices by substantially reducing the total buffer thickness. We finally note that Te pretreatment of Si(001) surfaces has previously been shown to abruptly nucleate the CdTe(111) epilayer.[23] Similar buffer design approaches to the one presented here could correspondingly allow the growth of high-mobility Cd_3As_2 on Si(001) substrates, unlocking entirely new device design options.

5. CONCLUSIONS

High quality Cd_3As_2(112) epitaxy is demonstrated on GaAs(001) substrates using a two-step Zn_xCd_{1-x}Te/CdTe-(111) buffer. By designing the buffer structure to control extended defects in the Cd_3As_2 epilayers, the epilayer structure and electron mobility are shown to be identical to those grown on GaAs(111) substrates, despite the use of only 20 nm thick CdTe nucleation layers. The primary advantage of this approach is that the growth of Cd_3As_2 in its preferred (112) orientation produces smoother surfaces than growth in the (001) orientation and allows the use of a wider range of growth conditions. Ultimately, this work sets the foundation for combining Cd_3As_2 epilayers with existing III−V devices.

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Notes

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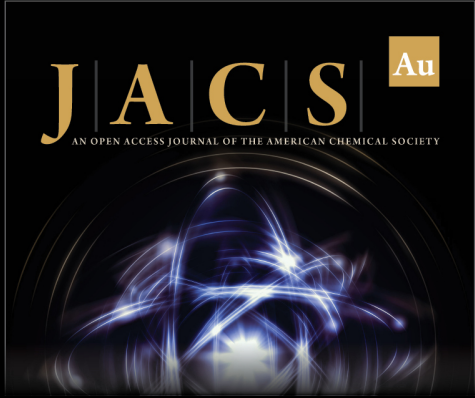
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