



# Enabling New Approaches to Low-Cost Dopant Patterning for Interdigitated Back Contact Crystalline Silicon Solar Cells

Cooperative Research and Development Final Report

CRADA Number: CRD-17-00665

NREL Technical Contact: Paul Stradins

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Contract No. DE-AC36-08GO28308

Technical Report  
NREL/TP-5900-81769  
January 2022



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## **Suggested Citation**

Stradins, Paul. 2022. *Enabling New Approaches to Low-Cost Dopant Patterning for Interdigitated Back Contact Crystalline Silicon Solar Cells: Cooperative Research and Development Final Report, CRADA Number CRD-17-00665*. Golden, CO: National Renewable Energy Laboratory. NREL/TP-5900-81769. <https://www.nrel.gov/docs/fy22osti/81769.pdf>.

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**Cooperative Research and Development Final Report**

**Report Date:** December 17, 2021

In accordance with requirements set forth in the terms of the CRADA agreement, this document is the CRADA final report, including a list of subject inventions, to be forwarded to the DOE Office of Scientific and Technical Information as part of the commitment to the public to demonstrate results of federally funded research.

**Parties to the Agreement:** Colorado School of Mines (CSM)

**CRADA Number:** CRD-17-00665

**CRADA Title:** Enabling New Approaches to Low-Cost Dopant Patterning for Interdigitated Back Contact Crystalline Silicon Solar Cells

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**Sponsoring DOE Program Office(s):**

Office of Energy Efficiency and Renewable Energy (EERE), Solar Energy Technologies Office (SETO)

**Joint Work Statement Funding Table showing DOE commitment:**

| <b>Estimated Costs</b> | <b>NREL Shared Resources<br/>a/k/a Government In-Kind</b> |
|------------------------|---|
| Year 1                 | \$0.00  |
| TOTALS                 | \$0.00  |

**Executive Summary of CRADA Work:**

NREL is sub to the Department of Energy (DOE) Photovoltaic Research & Development (PVRD) project, titled “New Approaches to Low-Cost Scalable Doping for Interdigitated Back Contact Crystalline Silicon Solar Cells”, awarded to Colorado School of Mines.

The goal of this project was to develop an industrially relevant dopant patterning technique that enable high performing, cost efficient Interdigitated Back Contact (IBC) solar cells based on n-Cz silicon wafer. Several possibilities were explored at the beginning of the project and the masked plasma deposition was deselected as the most promising and industrially relevant. This method was thoroughly explored ion the course of the project, its limitations revealed and mitigated. NREL

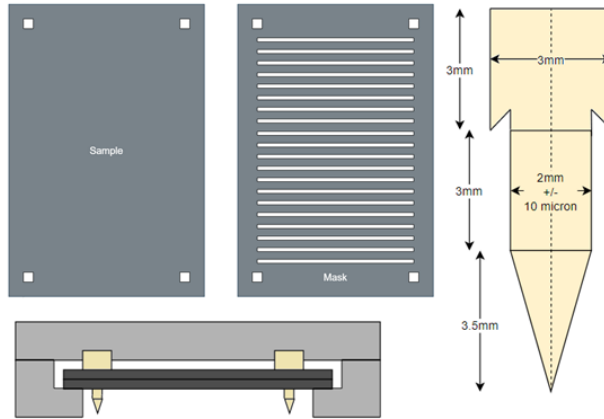
successfully the masked deposition integrated into the cell's process flow and produced the cells, alongside with numerous process development steps and application of in-house advanced characterization techniques. The report describes these developments by the task and in detail.

### **Summary of Research Results:**

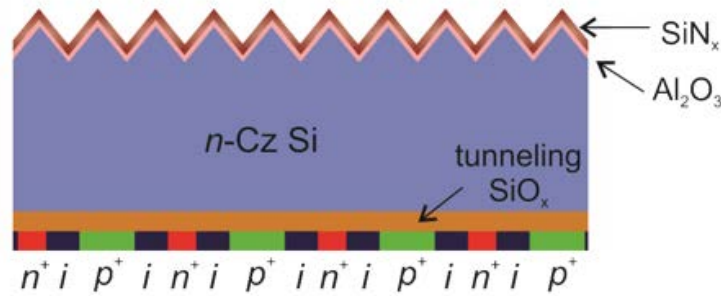
**Summary Introduction.** The goal of the main project and this CRADA was to develop an industrially relevant novel dopant patterning process to produce IBC cells. In the original plan, the patterning with UV light during doped film growth was proposed, but early on in the project the technique was replaced by masked dopant deposition and thermal drive-in (see Task 1 explanation for details), as it was deemed much more industrially relevant and cost effective. The revised SOPO was agreed upon between our main DOE and Mines sponsors, and followed. The cell development was centered around all aspects of the masked technique and its integration into the cell's process flow. After masked deposition development, dopant spreading investigations (and the mitigation technique development) with numerous electronic, optical, and atomic characterizations, we produced IBC cells. The IBC cells were then optimized to meet the main project's milestone of a 21% efficient 2×2 cm<sup>2</sup> IBC cell based on n-type Czochralski (Cz) Si. Below we describe the progress according to its consecutive tasks.

**Task 1 (Year 1, NREL FY17). Qualify NREL CVD tool(s) for the ultraviolet (UV)-assisted dopant patterning.** This will be done jointly by NREL scientific and engineering staff, and the Mines postdoc working onsite at NREL. Qualification includes modifying chambers for UV optical access, enabling in-situ ellipsometry, connecting reactive gases, designing and certifying safe operation, writing a standard operating procedure (SOP), and approval for safe chamber operation. This task will also include training, guiding, and advising the Mines postdoc to become a qualified operator of the tool(s).

**Explanation:** Early on the PVRD (main) project, it was determined, after some literature study and experimentation at Mines, that UV-assisted patterning would require very high (vacuum UV like) photon energies to enable the dopant patterning in the form it was originally proposed. Original PVRD proposal involved using UV inside the a-Si deposition chamber to modify the Si growth sticking/not sticking to the growth surface. Very high UV photon energies would require expensive UV sources (lasers) and special hard UV transparent windows, as well as extensive safety precaution. These processes would be poorly suited for the targeted inexpensive, high throughput industrial production of the interdigitated back contact (IBC) solar cells, the principal goal of this project. Therefore, early on the project, alternate approaches were proposed to the DOE sponsor and agreed upon in a modified SOPO. The most industrially relevant approach was chosen to be the dopant patterning by PECVD growth via a laser-scribed, mechanical mask. These masks were prepared in-house at NREL using NREL resources: LabView program for the laser code, laser scribe, KOH laser damage removal etch chemistry. The project postdoc Noemi Leick started to work at NREL under guidance of NREL PI Paul Stradins, but she soon choose another job. After this, Alex Lidiak, a PhD student from Mines worked on this project for 7 months, but decided to join another group. Finally, a PhD student, Matthew Hartenstein, was assigned by the Mines PI to this project and started his research work at NREL. He received all the needed training, guidance, and became qualified operator on laser scribe and etch chemistries needed for the project work. He was trained by the NREL CRADA funded staff members Paul Stradins and Bill Nemeth. NREL scientist Steven Harvey performed numerous ToFSIMS measurements needed for this project.



**Fig. 1. Laser scribed Si mask designs for dopant patterning instead of the UV. Left: ceramic alignment pin with dimensions, used to align the mask and substrate to 10 micron precision.**

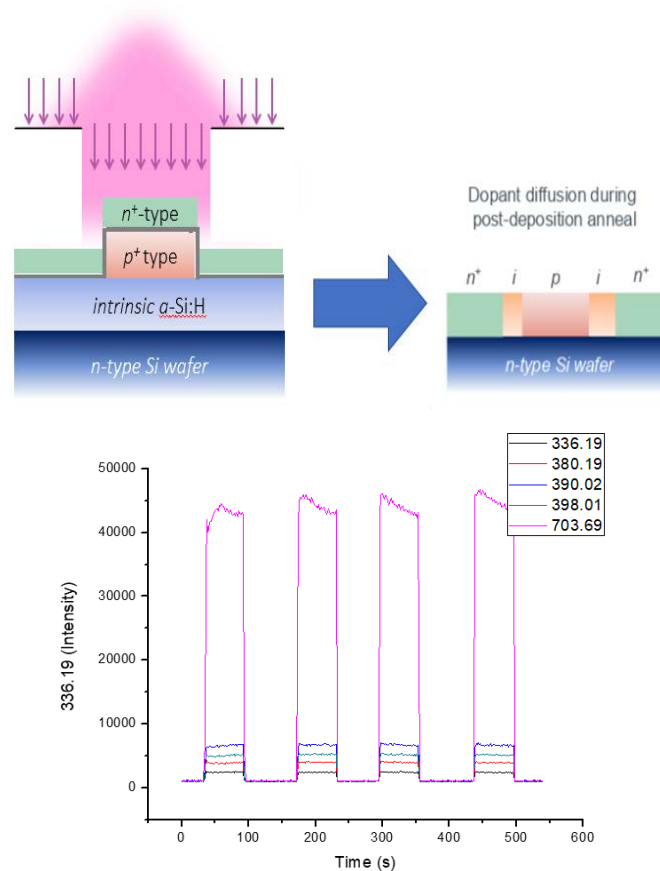


**Fig. 2. Target IBC solar cell structure for this project.**

NREL first developed of the deposition mask designs. The masks were laser scribed on Si wafers, then KOH-etched to remove the laser damage of the molten Si edges and trenches, and to allow mask fragments to separate. Fig. 1 shows the laser scribed mask designs that we developed in this work for the dopant patterning instead of UV-assisted process. They involve precision molded ceramic pins, masks, and sample substrates. The ceramic pins were ordered from an outside custom ceramic parts vendor, while all the other work (laser scribing of Si wafers with code optimization, etching, alignment optimization) was done in house at NREL. Both masks and the substrates are laser scribed to exact same size. Matching alignment holes are scribed into the masks and the substrates. Ceramic pins in the matching holes align the masks to the substrate (which eventually becomes an IBC solar cell). Our target IBC solar cell (Fig. 2) is based on poly-Si/SiO<sub>2</sub> passivated contact fingers (n and p-type) separated by a gap of intrinsic poly-Si. To achieve the desired dopant patterning, n-type P-doped a-Si:H is PECVD-deposited on the unmasked areas of the cell, that is uniformly coated with intrinsic a-Si:H. Then the n-type mask is replaced by the p-type mask that deposits B-doped a-Si:H on p-type fingers. Finally, the structure is annealed at 850 C to crystallize the a-Si:H into poly-Si, and to drive the dopants into the whole depth of poly-Si layer. Therefore, the procedure that NREL developed for this project, was the following:

1. Clean processing of the initial wafer and oxidizing it to create 1.5nm tunneling SiO<sub>2</sub> layer
2. Deposition of intrinsic a-Si:H on the backside (blanket)
3. Masked deposition of P-doped a-Si:H on the backside (with pins)

4. Masked deposition of B-doped Si (with pins)
5. Thermal anneal at 850C in a quartz diffusion furnace inside a cleanroom
6. Deposition of Al<sub>2</sub>O<sub>3</sub> H-source layer by ALD
7. Activating the Al<sub>2</sub>O<sub>3</sub> layer at 400C to release the H from it that passivates the contact interfaces
8. Etching off the Al<sub>2</sub>O<sub>3</sub> from the backside
9. Deposition of an optimized ARC coating (silicon nitride) by PECVD on the front
10. HF-cleaning of the back, and masked deposition of the metal fingers and busbars on the back.



**Fig. 3. An alternative dopant patterning technique – masked etching with SF<sub>6</sub> plasma. Top: the concept applied to the IBC cell; Bottom: Plasma emission lines (nm) evolution for 4 etch cycles.**

Before the processing sequence above was fully decided upon, we were exploring a parallel possibility of masked etching by SF<sub>6</sub> plasma. In this process, we would deposit the B-doped layer with masked process, then deposit blanket P-doped Si layer, then etch it using the same mask as before (Fig. 3). To plasma-etch the layers to the desired thickness, we planned to use a feedback signal – either B or P – by plasma emission spectroscopy or by gas mass spectroscopy. Samples were prepared for these experiments at NREL and the etching with monitoring was done at Mines. However, no detectable signal from B or P was measured, apparently due to the very low (<1%) dopant concentrations in the etch layers and small sample area. To boost the signals, it was decided

to use a thin SiN<sub>x</sub> interlayer between P- and B- doped layers as a marker. NREL deposited nitride films were tested for this purpose. However, even in this case, the detectable plasma emission lines were not changing, even though we confirmed that SiN<sub>x</sub> layer was etched off after the 1<sup>st</sup> etch cycle (Fig. 3, right panel). These experiments lead to the down-selection of only one dopant patterning technique for this project: the masked depositions of doped a-Si:H layers, a 10-step process outlined above. The rest of this report concentrates on this down-selected technique.

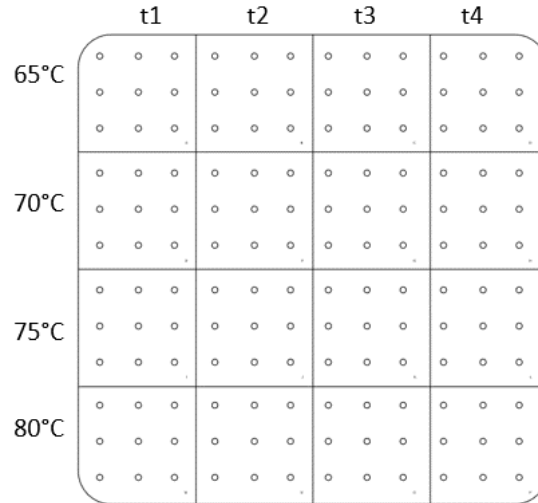
**Task 2 (Year 2, NREL FY18). Integrate the photo-CVD process with thin film processing for IBC cells in the film Si growth CVD tool at NREL.**

*Subtask 2.1:* Direct the Mines postdoc in design and integration of a UV light source in one of the CVD chambers within the film Si processing cluster tool and/or stand-alone CVD tool with doping capability. *Subtask 2.2.* Implement and test the photo-CVD process in the NREL cluster tool or/and stand-alone CVD tool (both with doping capability) and reproduce results from the Mines test chamber used in Year 1 on silane CVD (no dopants). This will be done collaboratively by the Mines postdoc and NREL staff. *Subtask 2.3.* Establish if photo-CVD can be used for area-selective growth of doped hydrogenated amorphous silicon (a-Si:H). Advise on electronic characterization. Grow n-Cz Si wafer/tunneling SiO<sub>2</sub>/poly-Si test structures for experiments at NREL and Mines. To enable this subtask goal, NREL will train the Mines postdoc in cleanroom procedures for high lifetime Si wafer handling, cleaning, oxidation, and poly-Si crystallization in a clean tube furnace. *Subtask 2.4.* Provide guidance to optimize the dopant activation parameters. NREL will train the Mines postdoc in carrier lifetime and implied Voc measurements, and data interpretation on both symmetric and device-type structures.

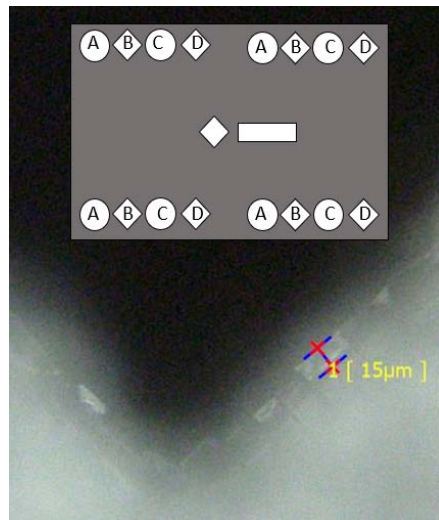
**Explanation.** Work on this task and numerous subtasks at NREL involved realizing the masked dopant deposition technique down selected in Task 1, to prepare for the actual IBC cell process at NREL. This involved training the student on the 10-step process above, and most importantly, establishing and mitigating the bottlenecks of the mechanical masking technique. Those bottlenecks directly affect cell efficiency and were focus of this task:

1. Mask alignment precision need to be ~ 10 micron, because the gap between P- and B-doped fingers can be as narrow as 30-50 micron. If the oppositely doped fingers contact, the cell is shorted
2. The mask touching the substrate, that is covered with just ~ 30 nm thick SiO<sub>2</sub>/a-Si:H layer protective stack, can cause loss of surface passivation by mechanical scratching. NREL has observed this effect before. Therefore, this effects needs to me checked and mitigated
3. With pts 1-2 satisfied, the dopants can penetrate under the mask and form long “tails” extending from one finger to another. In this case, cell can get shunted, which leads to loss of FF and efficiency.





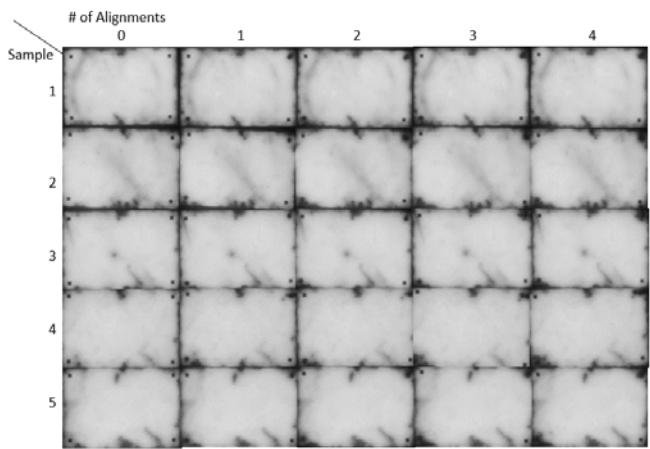
**Fig. 4. Test platform to develop precision mechanical mask alignment.**



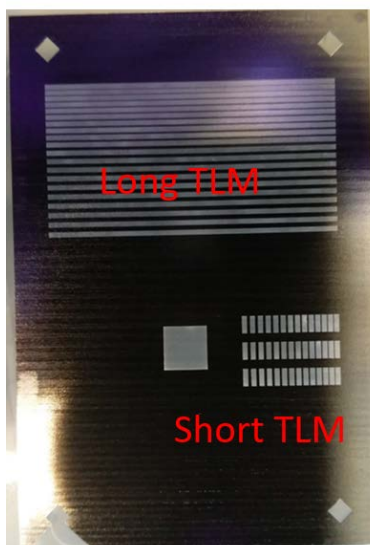
**Fig. 5. Tested shapes of alignment holes and the 15 μm fit achieved with the square hole shape (micrograph).**

*Mask alignment.* Making the alignment pin openings to precisely match the ceramic pins and align masks to substrate started with designing a test platform (Fig.4). Each small square on the test wafer (156x156 mm<sup>2</sup>) has 9 laser scribed openings, ranging from 1.95 to 1.99 mm to match the ceramic pin diameter of 2mm. Four different 22.5% KOH etch times and temperatures were tested for each square, because the etching widens the final hole diameter as it approaches or slightly exceeds 2 mm. Scribing was done at 21 Amps laser current, 50 kHz repetition, 1 mm/s scan speed. In this experiment, it was found that with round holes, the alignment is only within 20 microns due to hole to hole variability (the hole edges were not smooth, so even a single deviation could cause an obstruction). We then designed square holes (see the new test structure on Fig. 5) where the round pins have only four contact points, and found the alignment at or better than 15 microns, which was eventually optimized to about 10 microns. The alignment quantity was tested by inserting the pin i and the substrate, then observing the edges of both in a microscope as seen if Fig. 5.

*Evaluation of passivation damage by mechanical masking.* To evaluate possible damage to surface passivation, we prepared passivated contact samples and passivated them additionally with ALD  $\text{Al}_2\text{O}_3$  followed by the forming gas anneal (FGA). Five samples were mechanically aligned using pins, then alignment disassembled, then aligned again. The results are shown in Fig. 6. The brightness of the photoluminescence (PL) is a sensitive measure of surface passivation. Fig. 6 demonstrates that with careful handling, the mechanical alignment procedure does not deteriorate the surface passivation.



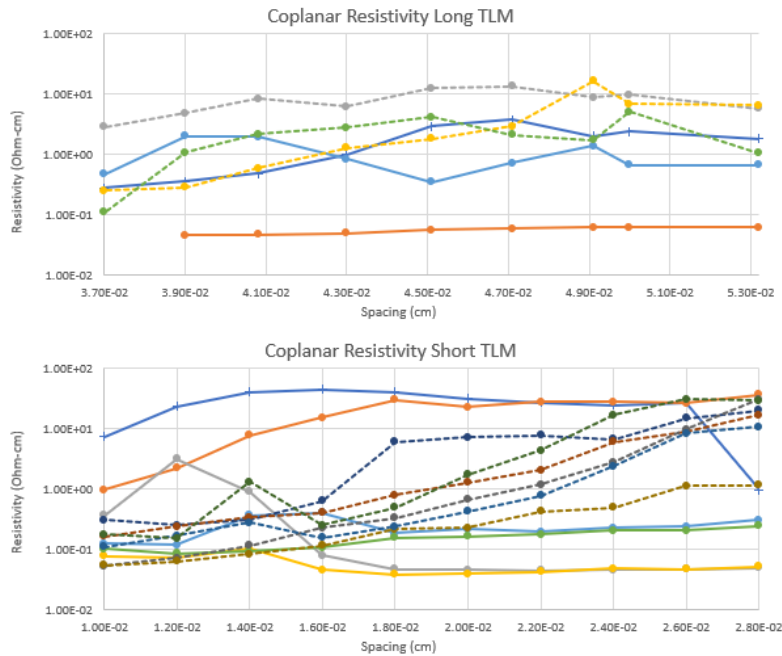
**Fig. 6. PL brightness of 5 samples as function of times the mechanical alignment was performed (mask touching the passivated substrate multiple times indicated).**



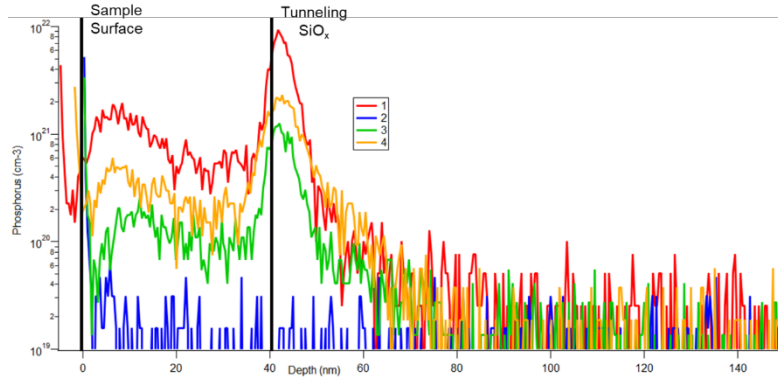
**Fig. 7. Si mask with two TLM patterns and alignment holes.**

Using the optimized laser code and etch recipes, we produced first mechanical masks and Si wafer substrates matched to them. The first masks were for TLM (transmission line method) metal pattern to enable conductivity measurements (Fig. 7). The openings resemble the IBC cell fingers, but the distance between them gets varied, and the dopant is the same type (B or P) for all fingers. These masks with  $\sim 10$  micron alignment precision allowed to prepare for the next Task, which was to integrate the dopant patterning process with thin film processing for the IBC cells.

*Possibility of shunting due to long dopant tails.* Dopant patterning with masks (or any method) inevitably leads to some dopant tails spreading out of the desired pattern. It can be caused by the imperfect optical imaging (for the case of UV patterning), ion scattering (for the case of the ion implantation) or, in our case, predominantly by the dopant penetration underneath the edges of the mechanical mask. Gas phase dopant transfer also contributes during the high T crystallization step (850C). These dopant tails can cause shunting of the cell; thus, they were investigated in detail to mitigate them. The first measurements to test this effect were performed on the TLM samples produced using masks of Fig. 7. The resistivity between two neighboring pads were measured for poly-Si films Si wafers with thick oxide. These samples underwent the same process flow as planned for the IBC cells (10-steps outlined in Task 1), but without using opposite dopant (we used only P-doped poly-Si). The measured resistivity was then converted into average conductivity of the (i)poly-Si film between the two neighboring fingers. Fig. 8 shows those results. We had previously estimated that in order for the IBC cell to function properly (FF loss < 1%), the average poly-Si gap film’s resistivity should be above 10 Ohm-cm. It is clearly not the case for our films: the results are scattered, but for both long and short TLM patterns the average resistivity of the gap is below the “non-shunted” limit.



**Fig. 8. Average poly-Si film resistivity values between two adjacent P-doped poly-Si fingers.**



**Fig. 9. Dynamic SIMS profiles. Red: doped finger, Blue: intrinsic region outside the fingers, Orange and green: intrinsic poly-Si between two adjacent P-doped fingers.**

In order to mitigate the dopant spreading into the gap, we investigated the possible causes of this using SIMS at NREL.

Dynamic SIMS measurements shown here were applied to different regions of a sample of phosphorus-doped *a*-Si:H deposited through a contact mask onto intrinsic *a*-Si:H. Dopant depth profiles were measured with dynamic secondary ion mass spectrometry (SIMS) (Cameca IMS 7f) with an oxygen primary ion beam at 3.5 kV and a sample potential of 2 kV. Depth profiles of four regions are shown in Fig. 9. The red curve shows the dopant concentration as a function of depth through an intentionally doped region of *a*-Si:H, while the blue curve shows the dopant concentration as a function of depth through an intrinsic region of *a*-Si:H. The green and orange curves show the dopant concentrations as a function of depth through regions meant to be intrinsic, but between doped regions separated by 280  $\mu\text{m}$  and 100  $\mu\text{m}$ , respectively. Depth profiling of dopants obtained by dynamic SIMS shows the level of dopant diffusion from the surface of the sample into the bulk *c*-Si. With this information, we showed that dopants spread into the regions covered by masks during PECVD. Understanding and mitigating of this phenomenon was deemed important to successfully use our selected dopant profiling technique for efficient IBC cells. This was done within the next Task.

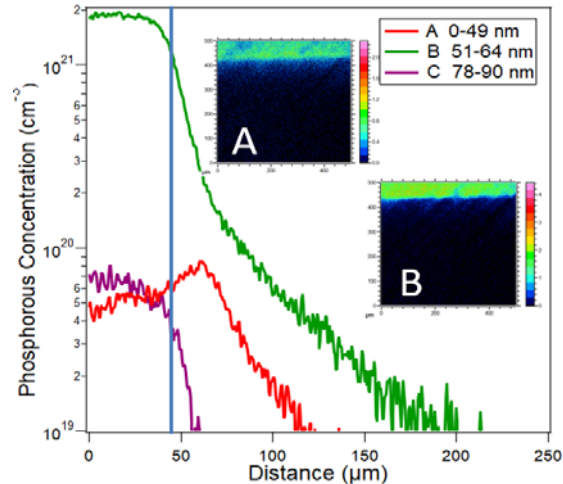
**Task 3 (Year 3, NREL FY19). Address the scientific and engineering challenges in process integration of proposed UV-assisted dopant patterning approach**, using beamline doping results (obtained within an independent project at NREL) as baseline. This includes: a) spatial limitations in dopant patterning posed by this technique; and b) electronic quality of the patterned contacts. Produce the first IBC cells based on the knowledge obtained. *Subtask 3.1.*

Collaboratively, NREL and the Mines postdoc will optimize the process conditions during photo-CVD. *Subtask 3.2.* Establish the process conditions during photo-CVD and post-processing.

Provide support to Mines postdoc in accurate characterizations to meet the project milestones.

*Subtask 3.3.* Using photo-CVD, create patterned contacts. This is a collaborative task.

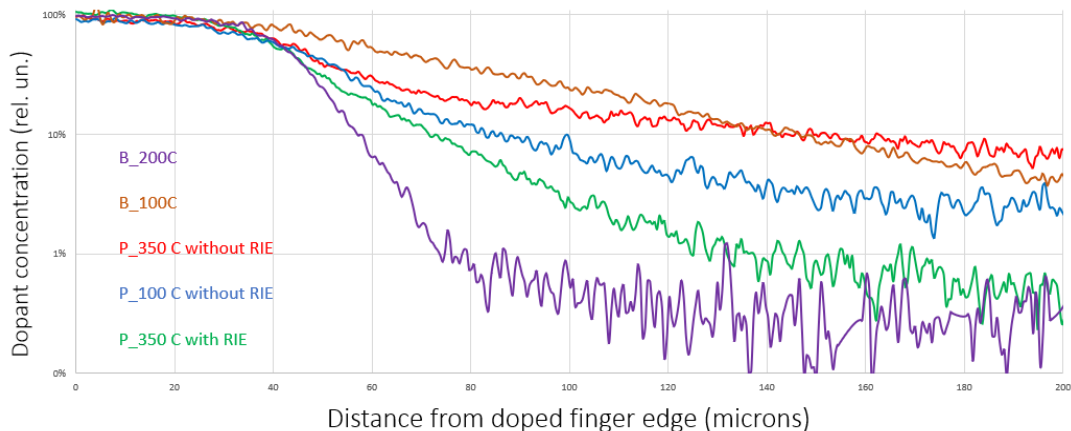
**Explanation:** This task with all its subtasks is aimed on developing and transferring the previously optimized, masked dopant patterning techniques to real IBC cells. As in Tasks 1-2, the UV patterning was replaced by the mechanical masking. Once the masks were made and optimized alignment procedure found, we focused on minimization of dopant spreading between the n- and p-type IBC cell fingers, mask design and fabrication for the IBC cells, and made the first cells with our technique.



**Fig. 10. ToFSIMS line scans extracted from the 3D maps, showing the P concentration at depth intervals shown, past the edge of the doped finger and extending into intrinsic gap. Insets A and B show 2D P-dopant maps in XY plane.**

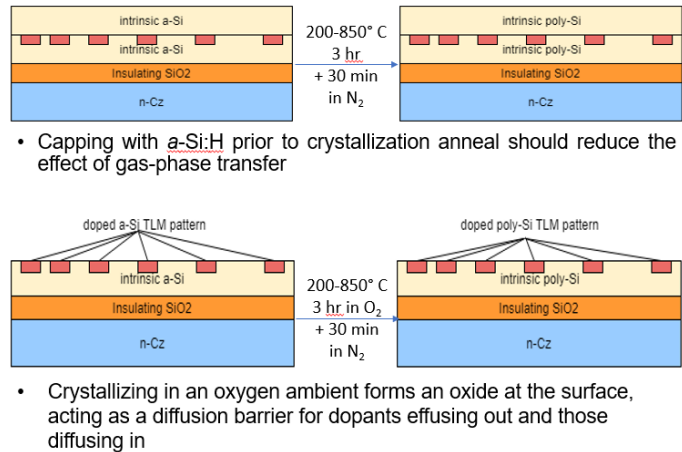
*Dopant spreading characterization and minimization.* We used time of flight SIMS (ToFSIMS) with lateral resolution to map the residual dopant concentrations within the (nominally intrinsic) poly-Si gap. We used the same TLM patterns than in Task 2. Time-of-flight SIMS measurements are shown on Fig. 10. The lateral resolution allows to map dopant concentrations for a  $500 \times 500 \mu\text{m}^2$  area at the edge of a phosphorus-doped IBC finger. Dopant concentration on top of the intrinsic a-Si:H layer was mapped prior to crystallization and metallization using time-of-flight SIMS (ION-TOF TOF-SIMS V). The primary ion beam was a 30 keV BiMn source, with a pulsed beam current of 1 pA. Measurements were performed in negative polarity utilizing a Cs+ gun for sputtering, operating at 3 kV at a current of 25 nA. ToFSIMS results are in the form of 3D map (z-depth profile for any point in x,y plane). Once concentration maps are obtained, 1D linescans in x-direction (perpendicular to the finger edge) are extracted to show lateral profiles of dopant concentration extending away from the intentionally doped finger edge, past the defined mask area. It over seen that particularly for the profile B at  $\sim 50$  nm depth, P-dopant profile extends over 100 micron from the P-doped finger edge. This can cause undesired shunting of the IBC cell.

To see the effect of substrate temperature on dopant spreading during deposition, boron- and phosphorus-doped a-Si:H films were deposited through contact masks at different substrate temperatures with all other conditions (gas flow rates, plasma power, chamber pressure) held constant.

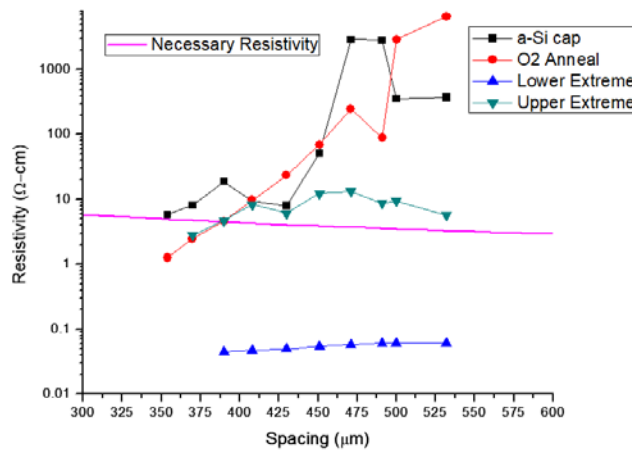


**Fig. 11. Lateral ToFSIMS profiles obtained for PECVD deposited, doped (both by P and B dopants) a-Si:H films, at different conditions and exposed to different processing, including reactive ion etching (RIE) post-deposition.**

In addition to substrate temperature during deposition, some films were subjected to 2-5 s of SF<sub>6</sub> plasma etching. Plasma etching was introduced at NREL to eliminate expected ~ 5nm of the residual P-doped a-Si:H films spreading below the mask finger. Once films were deposited, lateral SIMS profiles were obtained with TOF-SIMS as described above, and the relative changes in concentration of each profile as a function of distance are compared (Fig. 11). These results show that the PECVD deposition T appears not to affect P spreading, while for B, higher T of 200C produces a much sharper profile than 100C. Reactive ion etching (RIE) sharpens the profiles noticeably and was adopted as a future tool to prevent possible shunting effects in cells. We also found that besides dopant spreading during deposition, some P contamination results from the gas phase P atom transfer from the doped fingers to the intrinsic gap region. This is evidenced from the very flat dependences of average resistivity on the finger distance (see Fig. 8), whereas the decaying dopant tails are expected to give increasing resistance with distance. Two mitigation strategies were developed for this effect: 1) capping the dopant-patterned a-Si:H film with intrinsic a-Si:H film, to prevent dopant outdiffusion; 2) crystallizing the doped a-Si:H in an oxidizing ambient, to create a protective oxide that “locks in” the dopants near the surface (Fig. 12). Both strategies worked as shown by the red and black resistance curves in Fig. 13. The magenta curve represents the allowed minimum resistivity, while the green and blue curves show upper and lower limits of our results without mitigation applied. Finally, we found that the RIE etching off the ~ 5 nm a-Si:H off the deposited doped film is the best shunt mitigation technique: the average resistivities measured by TLM increased to ~ 10<sup>5</sup> Ohm-cm<sup>2</sup> (see our paper M. Hartenstein et al., J. of Photovoltaics Vol. 10, NO. 6, 2020).

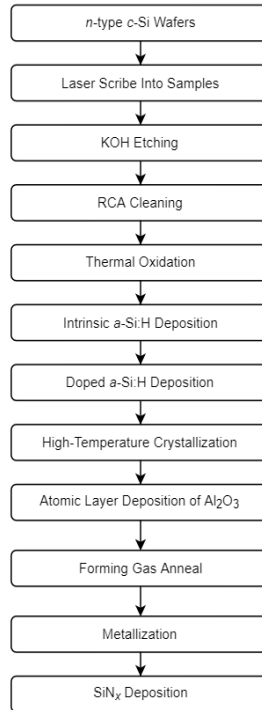


**Fig. 12. Two mitigation strategies for gas phase dopant diffusion: capping a-Si:H film and annealing in oxidizing ambient.**

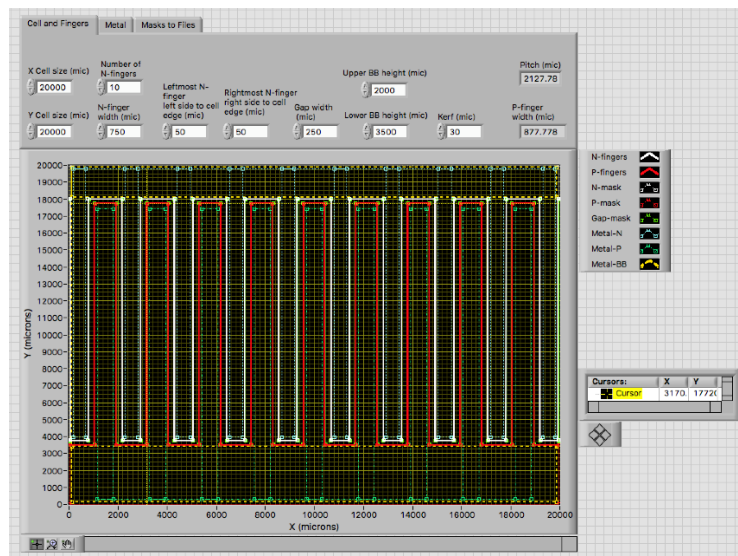


**Fig. 13. Gap resistivity without mitigation (blue and green curves), and with two mitigation strategies of Fig. 12 applied (red and black).**

With the dopant patterning technique verified and shunting minimized, we then applied it to the IBC cell processing. The cell process flow used in this project is shown in Fig. 14. It resembles the 10 process steps outlined in Task 1 above, but with more detailed description of wet chemistries applied. The laser scribing involves both the substrate (pin alignment holes) and patterned masks: 1) n-type fingers and busbar; 2) p-type fingers and busbar; 3) metallization: a metal finger mask and a busbars mask (these cannot be unified into one mask due to mechanical incompatibility). Fig. 15 shows the graphical interface of a previously NREL-developed Labview code that was modified for this project. The code produces a set of instructions and coordinates for the laser scribe to make all the above masks self-consistently. Alignment holes are added to the code as well, also the perimeter scribe of the sample (e.g., 3 cm x 4 cm).



**Fig. 14. IBC cell process flow at NREL.**



**Fig. 15. The mask scribing Labview code graphical interface for IBC cells.**

With the scribed wafer samples and masks, the first cells were produced using NREL tools, facilities, and process recipes. The PL images with associated implied open circuit voltages ( $iV_{oc}$ ) of the first IBC cell batch are shown in the top Fig. 16. The crystallization anneal was performed either in  $N_2$  or  $O_2$  ambient. The latter resulted in higher  $iV_{oc}$ s, but when metallized, the cells actual  $V_{oc}$ s were lower than for  $N_2$  (see the bottom Fig. 16). This is because the oxidation provides better passivation, but after the HF dip before the metallization the protective oxide layer including in grain boundaries and pinholes is removed. Their first cell efficiencies were low primarily because these wafers were not textured and no proper ARC coating. In addition, their



Vocs are relatively mediocre  $\sim 670$  mV, and fill-factors (FF) are topping at 74%. The fill-factor analysis showed that the low FF is mostly due to high series resistance, not shunting of the cells. This was further investigated in Task 4.

To summarize, in Task 3 we established the masked deposition technique and process flow to successfully produce IBC cells. We established the possible mechanisms for cell shunting and developed mitigation techniques. Finally, we produced first unoptimized IBC cell batches to show the validity of our approach in process integration. The student was trained in cell processing and characterization as well as cell analysis.

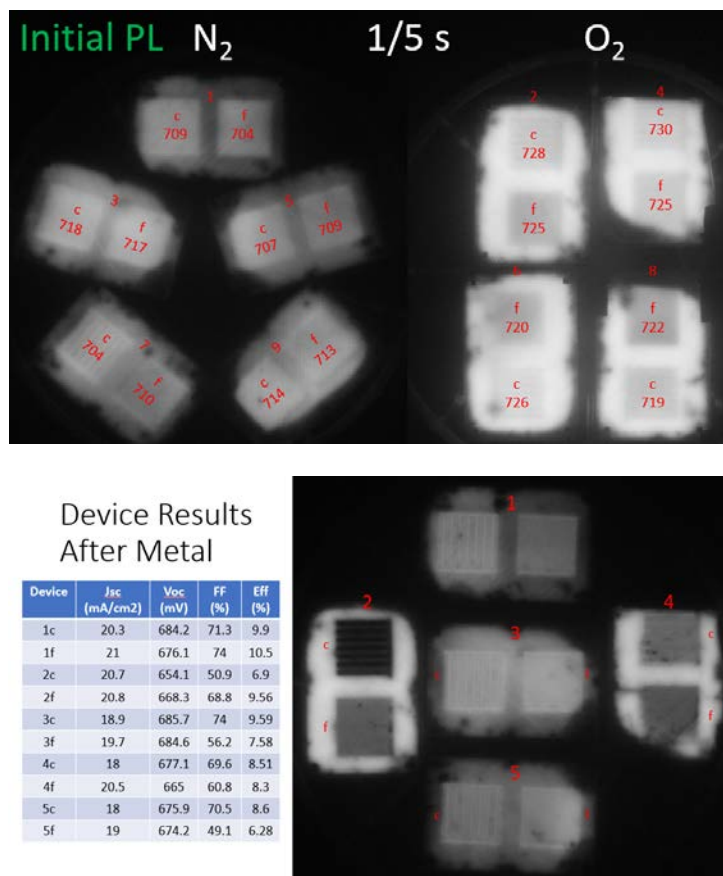


Fig. 16. First IBC cells. Top: PL images before metallization, with  $iV_{oc}$  values. Bottom: Fully metallized IBC cells (PL and cell parameters).

**Task 4 (Year 4, NREL FY20). Address bottlenecks in cell efficiency to reach a target high efficiency of  $\sim 23\%$ .** *Subtask 4.1.* Implement the UV-assisted CVD capability for dopant patterning in the thin film Si cluster tool (or standalone CVD tool) on a permanent mode, collaboratively with the Mines postdoc.

*Subtask 4.2.* Provide wafer preparation support and device processing assistance to jointly produce Si IBC solar cells with the novel dopant patterning technique with up to 22% efficiency.

*Subtask 4.3.* Design experiments and assist the postdoc to explore this novel dopant patterning technique to create an IBC cell with low temperature process (below crystallization temperature to

convert a-Si:H to poly-Si). *Subtask 4.4.* Address in detail engineering issues related to reaching 23% efficiency. Guide the Mines postdoc in device fabrication leading.

This task concentrates on cell optimization and further understanding of process integration bottlenecks. The target efficiency numbers were lowered via the agreement with the DOE sponsor of the main project.

| Cell  | Ambient        | Jsc  | Voc   | FF   | Eff         |
|-------|----------------|------|-------|------|-------------|
| IA_17 | O <sub>2</sub> | 29.3 | 695.6 | 73.8 | <u>15.1</u> |
| IA_6  | N <sub>2</sub> | 28.2 | 682.4 | 73.6 | <u>14.1</u> |
| IA_5  | N <sub>2</sub> | 28.3 | 701.5 | 71.3 | <u>14.1</u> |
| IA_9  | N <sub>2</sub> | 28.6 | 690   | 70.4 | <u>13.9</u> |
| IA_4  | N <sub>2</sub> | 27.2 | 704.5 | 72.1 | <u>13.8</u> |

**Fig. 17. Best 2019 cells.**

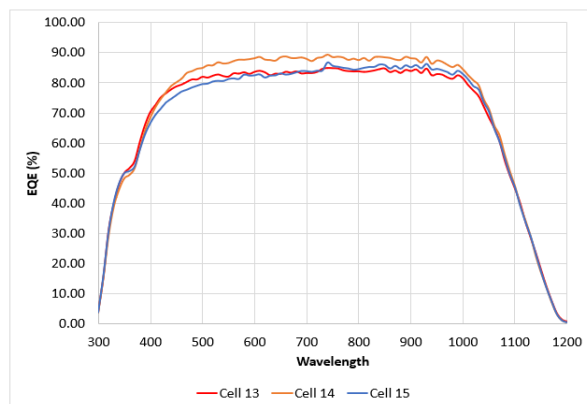
| Cell     | TMAH time | Jsc  | Voc   | FF   | Eff         |
|----------|-----------|------|-------|------|-------------|
| Si165_13 | 180 s     | 34.4 | 640   | 73.9 | <u>16.3</u> |
| Si165_14 | 110 s     | 37.8 | 648.5 | 75.7 | <u>18.6</u> |
| Si165_15 | 180 s     | 35.0 | 642.5 | 74.3 | <u>16.7</u> |
| Si165_19 | 180 s     | 28.8 | 600.7 | 74.3 | <u>12.8</u> |
| Si165_20 | 180 s     | 32.3 | 629.7 | 74.6 | <u>15.2</u> |

**Fig. 18. Cell improvements in 2020.**

Table 1 shows the top 5 cell efficiencies obtained in 2019. The highest efficiency exceeds 15% for these non-textured cells, with Voc above 700 mV, an indication of good passivation. However, the fill factors are still in the lower 70% range. If the champion cell would be properly textured and without the blue losses, its Jsc would be close to 40 mA/cm<sup>2</sup>, resulting in 20.5% efficiency. Therefore, the next step was to produce textured cell without any poly-Si layer at the front – just a SiO<sub>x</sub>/SiN<sub>x</sub> passivation stack. The process flow of Fig. 14 was modified to include the 1-sided TMAH etch step after the crystallization. In order to protect the front and back of the cell from KOH etching, an ARC protective coating was deposited before laser scribing. The wafer used was a cell precursor, double side textured, with an SiO<sub>2</sub>/(i)-poly-Si stack. The results of this double-textured cell batch is shown in Fig. 18. The cell efficiencies improved, approaching 19%, with higher Jsc and FF above 75%. Unfortunately, due to the processing difficulties and possible pinhole etching by the TMAH as well as textured surface on the back, the Voc is now below 650 mV.

The lower than expected Jsc of the cells was unexpected and investigated in more detail. The external quantum efficiency (EQE) curves are shown in Fig. 19. The flat portion of EQE is at 90%

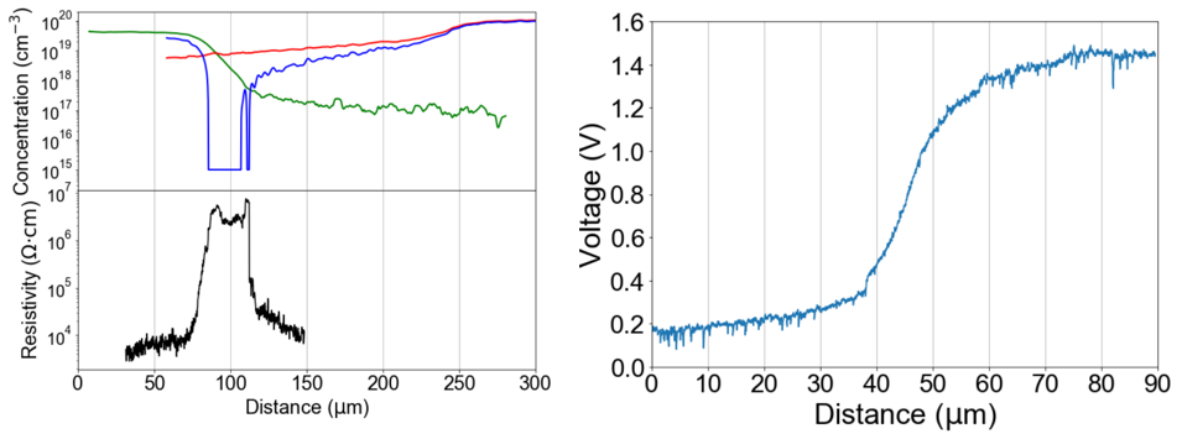
instead of close to 100%, which indicates either a not-optimized SiNx ARC, or slight rounding of the pyramid tips by the TMAH etch. Further optimization of the cells to reach their efficiency target 21% was seriously hampered by the Covid-19 pandemic, which in 2020 limited access to the labs to produce many cell batches at high throughput – a necessary factor to raise cell efficiency once the process has been established. Nevertheless, we showed proof of concept cells for our technique and that this masked dopant patterning does not have principal bottlenecks to high efficiency cell production at high throughput (doesn't compromise cell passivation, doesn't introduce shunts, has high pattern fidelity and reproducibility).



**Fig. 19. EQE of three cells of table in Fig.18, with the same color coding.**

We noted that the low FF of the cells produced was due to the series R and not due to the shunting. Given the dopant tails observed earlier (Figs. 10,11) and no mitigation applied, we should be seeing shunting behavior. Because we did not yet apply our RIE etching (above, for dopant tail removal) to at least part these cells, we realized that there is an efficient dopant compensation mechanism in play between the P- and B-doped fingers that leads to high shunt despite of wide dopant tails.

This hypothesis was experimentally confirmed by spreading resistance measurements at NREL. This unique AFM based technique measures the local resistivity in  $\sim 50$  nm vicinity radius of a conductive AFM tip. Left Fig. 20 shows the result: indeed, there is a highly resistive  $\sim 30$  micron wide very high resistivity domain. We hypothesize that this domain results from the grain boundary traps enhancing the local dopant compensation effect. The domain boundaries are determined by the trap density being approximately equal to the free carrier density (which is either electrons at positive  $N_D - N_A$ , or holes at positive  $N_A - N_D$ ). We have developed a model of this phenomenon and are preparing a publication. The blue curve in left Fig. 20 shows free carrier density and red and green curves – ToFSIMS measured P and B tails, respectively. Indeed, it exhibits a wide minimum governed by the trap density. This is further confirmed by the AFM-based Kelvin nanoprobe measurements of the contact potential difference (CPD, a measure of band bending in our device). The right Fig. 20 shows the result with a pronounced jump in the CPD at the position of the high-resistivity domain. An distinct p-n junction would give a much sharper (few nm instead of  $\sim 30$  micron) width of the depletion region. Again, this supports our hypothesis that numerous traps  $\sim 10^{19} \text{ cm}^{-3}$  in poly-Si enhance the compensation region, making it tens of microns wide.



**Fig. 20. Left, lower panel: AFM based spreading resistance measurement across the intrinsic poly-Si gap from B-doped to P-doped finger of the IBC cell. Left, top panel: ToFSIMS measured B (green) and P (red) lateral distribution line scans; blue – simulated free carrier density in the presence of traps in poly-Si. Right: AFM based Kelvin nanoprobe measurement of the same sample.**

In summary, NREL has provided support and enabled the PVRD project led by the Mines and funded by the DOE, in the form of processing recipes, dopant patterning method, numerous depositions, chemical and thermal processing batches, device processing, and characterization – both routine such as PL, JV, EQE – and advanced such as ToFSIMS, SIMS, AFM based spreading resistance, and AFM based Kelvin nanoprobe measurements. The IBC cells were produced at efficiencies up to 18.6%. The work has contributed to one published journal article and a manuscript of the second article, as well as numerous presentations at conferences. The sponsor of this CRADA (Mines PI Sumit Agarwal) approves this report.

**Subject Inventions Listing:**

None

**ROI #:**

None