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Understanding SiO_x Layer Breakup in poly-Si/SiO_x Passivating Contacts for Si Solar Cells Using Precisely Engineered Surface Textures

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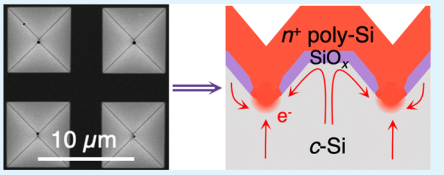
ABSTRACT: The contact resistivity of polycrystalline silicon on silicon oxide (poly-Si/SiO_x) passivating contacts depends on the formation of pinholes in SiO_x for thicknesses $\gtrsim$1.7 nm. We fabricated these contacts on inverted pyramids and v-grooves in addition to the alkaline-textured random pyramids and planar surface morphologies. The thermal breakup of SiO_x was achieved at peak annealing temperatures of 1050 and 1100 °C. SiO_x breakup at 1050 °C resulted in pinholes created preferentially at vertices in the inverted pyramids, while at 1100 °C, their formation was random. The density of pinholes was greater in textured samples than in polished samples. Both chemical etching and electron beam-induced current (EBIC) were used to visualize the pinholes, the latter being sensitive only to transport pinholes in the $p-n$ junction but not the n^+-n junction. We ascribe this difference in EBIC images based on the contact polarity to differences in the collection probability of the minority carriers generated by the electron beam. Our work demonstrates that texture morphology can be exploited to enable the precise engineering of pinholes in poly-Si/SiO_x passivating contacts.



KEYWORDS: *polysilicon, passivating contacts, pinholes, inverted pyramids, v-grooves, surface morphology, EBIC*

INTRODUCTION

Si solar cells account for nearly 95% of today's photovoltaics market. Fabrication of high-efficiency solar cells requires carefully engineered processing strategies to mitigate electron−hole recombination and optical losses.[1,2] Optical losses originate from reflection or insufficient absorption of light in the cell. The optical losses in crystalline Si (*c*-Si) solar cells are particularly pronounced due to the indirect band gap of Si and the high reflectivity of untextured wafers. To reduce optical losses, *c*-Si wafers are subjected to anisotropic etching to create a texture of micron-sized hillocks in the form of random upright pyramids.[3] This texture, combined with antireflection coatings, reduces the *c*-Si wafer's reflectivity to just a few percent over the wavelength range of 400−1100 nm. The pyramidal texture increases the surface area by approximately a factor of $\sqrt{3}$ and creates additional defects that must be passivated to suppress electron−hole recombination.

Polycrystalline Si on silicon oxide (poly-Si/SiO_x) passivating contact is an emerging industrial technology. These poly-Si/SiO_x structures with thermally or chemically grown ultrathin ($\lesssim$2.0 nm) SiO_x provide chemical passivation of the dangling bonds at the SiO_x/*c*-Si interface.[4] The adjacent heavily doped poly-Si layer provides field-effect passivation and charge-carrier selectivity.[1] The charge-carrier transport mechanism across the SiO_x layer is dominated by either quantum tunneling (SiO_x < 1.7 nm) or pinhole (SiO_x > 2.0 nm) transport. However, even for SiO_x < 1.7 nm, pinhole transport can be significant for samples annealed at conditions that optimize both the contact resistivity and the passivation properties.[5,6] Both contact types have been incorporated in record-efficiency *c*-Si solar cells.[2,7] Poly-Si/SiO_x contacts with SiO_x thickness $\gtrsim$2.0 nm require a high-temperature (>1000 °C) thermal process for pinhole formation via SiO_x breakup. While pinhole-enabled poly-Si/SiO_x contacts have shown the best efficiencies, they rely on thermal pinhole formation that is hard to control and reproduce, especially when poly-Si/SiO_x are applied to textured wafers.[8−10] Single-side texturing of the rear with poly-Si/SiO_x contacts may be beneficial in tandem cells, where the front side cannot always be textured due to integration with the top cell. In textured contacts, we have recently shown[9,11] that the location and density of the pinholes induced in SiO_x are sensitive to minor variations in process parameters such as the SiO_x layer thickness and the thermal budget. This makes it difficult to implement pinhole-type poly-Si/SiO_x contacts in an industrial process where large batches of the *c*-Si wafer are simultaneously processed, which inherently leads to wafer-to-wafer variations in processing conditions.

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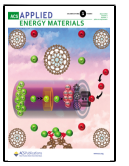

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The mechanism by which pinholes are thermally induced in the SiO_x layer on untextured poly-Si/SiO_x contacts has been previously studied. Wolstenholme et al. showed that the initial SiO_x thickness and the thermal budget control the area fraction of the SiO_x layer with discontinuities. Nanoscale pinholes are one such form of discontinuity in SiO_x. These authors showed that thinner SiO_x layers and higher thermal budgets led to a greater propensity for SiO_x breakup. Additionally, Wolstenholme et al. observed that complete SiO_x breakup led to balling up of SiO_x, and the volume of this balled up SiO_x corresponded closely to the initial volume of the film prior to annealing.[12] Ajuria and Reif developed a kinetic model in which the SiO_x breakup mechanism is driven by surface area reduction, with one-dimensional oxygen diffusion as the kinetic pathway.[13] To test the model, several transmission electron microscopy micrographs were analyzed to extract the void or pinhole radii as a function of the annealing temperature. This simple kinetic model showed an Arrhenius dependence of the pinhole radius on the annealing temperature. From the corresponding Arrhenius plots, these authors extracted activation energy barriers of 1.2 and 2.2 eV for the breakup of SiO_x grown with ultraviolet O_3 and native SiO_x, respectively. More recently, Tetzlaff et al. reported an activation energy barrier of 1.15 eV for the breakup of 1.7 nm of SiO_x grown in ozonized H_2O.[14] The activation energy barriers for oxygen diffusion in SiO_x and Si are 1.2 and 2.4 eV, respectively, which are similar to those reported by Ajuria and Reif and Tetzlaff et al. These studies were conducted on planar Si(100) surfaces.

In the case of poly-Si/SiO_x on textured *c*-Si, using electron beam-induced current (EBIC) measurements, we observed that different thermal annealing schedules resulted in preferential SiO_x breakup at either the faces (pinhole-like discontinuities) of random upright pyramids or in the valleys between adjacent pyramids (linelike discontinuities).[11] We speculated that the linelike discontinuities in SiO_x may have been caused by a lower thermal SiO_x growth rate in the valleys, which would make the locally thinner SiO_x more prone to breaking up. Previously, for ∼500 nm of wet oxidation of patterned *c*-Si over a temperature range of 900−1100 °C, Marcus and Sheng observed up to ∼31 and ∼78% lower SiO_2 thickness at the convex and concave edges, respectively. These authors attributed this reduction in the oxidation kinetics[15] to local compressive stress at the convex edges and mass transfer limitations at the concave edges. While the studies done by Marcus and Sheng provide insight into the role of local curvature on SiO_2 thermal growth kinetics, the role of curvature may be different at the much lower thicknesses (1.5−2.1 nm) used in poly-Si/SiO_x contacts or SiO_x formed by different methods such as vapor deposition techniques. Therefore, studying SiO_x breakup on well-defined textured surfaces can provide better insight into the role of surface curvature on ultrathin SiO_x breakup kinetics. Herein, regular inverted pyramidal and v-groove textures were used as model systems to further investigate the role of surface morphology in thermal SiO_x breakup in poly-Si/SiO_x on *c*-Si. Henceforth, we will refer to this nanoscale SiO_x breakup as "pinhole formation." The regular arrays of inverted pyramids have well-defined surface features (planes, edges, and vertices) that allow us to quantify the proportion of pinhole locations on pyramid vertices or faces without convoluting it with variations in the pyramid size and their randomized overlap.

EXPERIMENTAL METHODS

Synthesis of Regular-Textured Surfaces. Double-side polished, phosphorus-doped, ∼1.7 Ω·cm resistivity, ∼280 μm thick, float-zone (FZ) Si (100) wafers were piranha and RCA cleaned. Next, SiN_x was deposited on both sides of each wafer via plasma-enhanced chemical vapor deposition (PECVD) using a $SiH_4/H_2/NH_3$ capacitively coupled plasma powered at 13.56 MHz. The wafers were placed on the grounded substrate holder at a temperature of 350 °C with an input power to the plasma source of 10 W, at 1.2 Torr, to deposit ∼220 nm thick SiN_x. The flow rates of SiH_4, H_2, and NH_3 were 4, 50, and 5 standard cm^3/min (sccm), respectively. A ∼2 μm thick positive photoresist (Shipley MICROPOSIT S1818) was spin-coated on one side of each wafer and patterned via photolithography. The pattern consisted of a matrix of circles or stripes, 5 μm in diameter or width, with their centers spaced 10 μm apart (see Figure 1a,b). After photoresist development in Shipley MF-319, the patterns were transferred onto the SiN_x layer by etching in a parallel-plate, capacitively-coupled reactive ion etcher (Samco) operated at 30 W radio-frequency power (13.56 MHz), with 5 sccm of SF_6 flow at a pressure of ∼0.12 Torr. The SiN_x dry etch duration was 80 s. After SiN_x patterning, the photoresist was removed, and Si uncovered by SiN_x was etched in 22.5% w/v KOH solution at 60 °C to produce nonconnected inverted pyramids[16] and v-grooves, shown in the scanning electron microscopy (SEM) micrographs in Figure 1c,d. Finally, dilute HF/HCl was used to strip off the SiN_x hard mask (see Figure 2a−c).

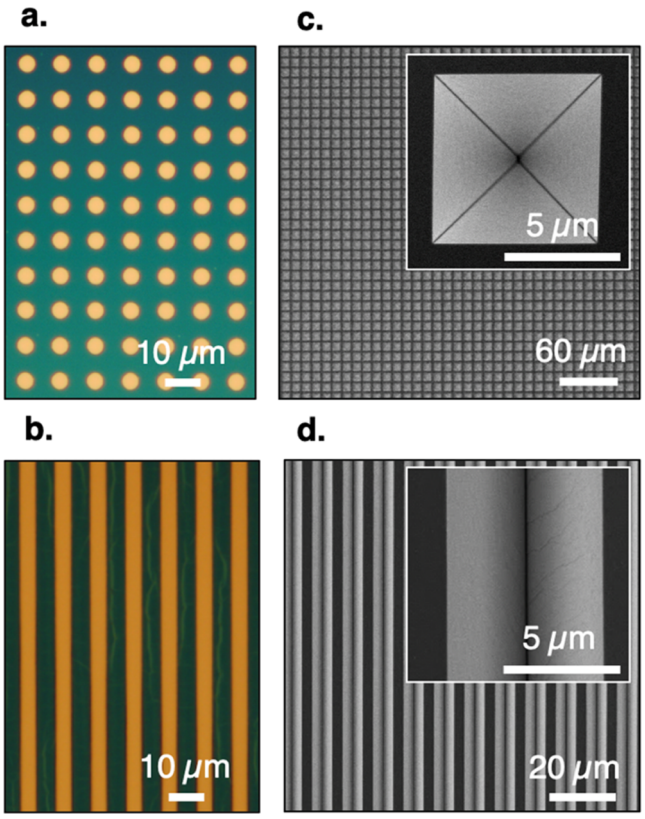

Figure 1. Optical microscopy of SiN_x with (a) circular and (b) line patterns. In these images, *c*-Si appears as yellow, and the patterned SiN_x mask appears either as green or blue. Plan-view SEM of (c) inverted pyramids and (d) v-grooves created after wet etching of the SiN_x patterns in (a) and (b), respectively.

Poly-Si Contact Fabrication and Characterization. *Pinhole Formation.* Single-side regular-textured wafers were cleaned with piranha and RCA solutions, etched in HF, and oxidized for ∼10 min in a quartz tube furnace at 800 °C with 6:1 N_2/O_2 flow. Ellipsometry was performed on a polished *c*-Si wafer, which showed ∼2.1 nm of

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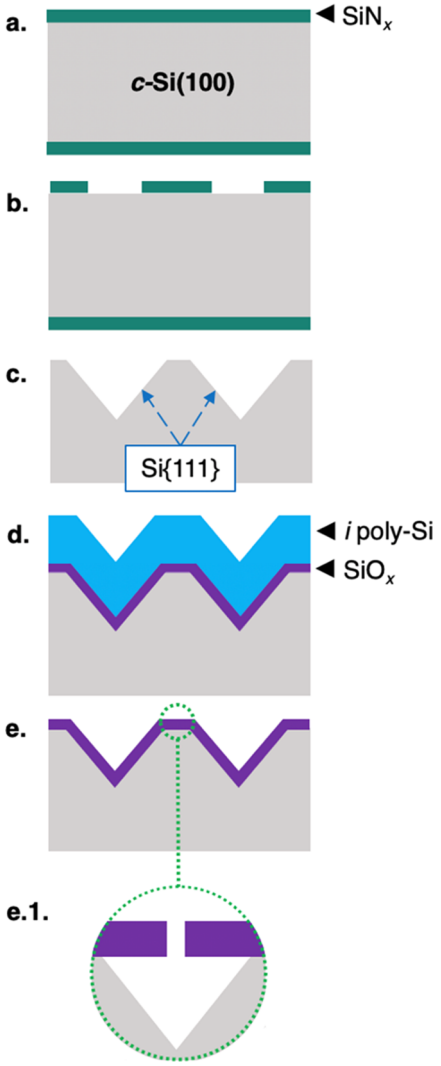

Figure 2. Processing steps to fabricate and image pinholes in SiO_x. (a) SiN_x (220 nm) was deposited on double-side-polished, *n*-type FZ Si wafers. (b) The SiN_x film was patterned using photolithography and reactive ion etching. (c) Nonconnecting inverted pyramids or v-grooves were created by etching the unprotected *c*-Si regions, which was followed by the removal of the SiN_x hard mask. (d) Nanoscale pinholes were thermally induced in a ∼2.1 nm thick SiO_x layer, which was capped with intrinsic *a*-Si:H. In this step, the *a*-Si:H layer was simultaneously crystallized to poly-Si. (e, e.1) The poly-Si capping layer was removed, and micron-scale etch pits were created in *c*-Si under each pinhole, using selective etching of Si over SiO_x with tetramethylammonium hydroxide (TMAH).

SiO_x. After oxidation, ∼30 nm of intrinsic amorphous hydrogenated Si (*a*-Si:H) was deposited via PECVD on both sides of each sample, using SiH_4/H_2 (2 and 120 sccm, respectively) at 250 °C, 12 W, and 1.4 Torr. To induce SiO_x breakup and to crystallize the intrinsic *a*-Si:H into poly-Si, the samples were thermally annealed for 30 or 45 min under an N_2 atmosphere in a quartz tube furnace at a peak temperature of either 1050 or 1100 °C (see Figure 2d). For the peak annealing temperature of 1050 °C, the samples were inserted into the furnace at 200 °C and ramped at 3.6 °C/min. For annealing at a peak temperature of 1100 °C, the samples were inserted into the furnace at the peak temperature. Besides the single-side regular-textured FZ Si wafers, pinholes were induced under identical conditions in polished FZ Si and randomly-textured Czochralski (Cz) Si wafer (phosphorus-doped, ∼2.9 Ω·cm).

Pinhole Density Analysis. After pinhole formation, to characterize the density and location of the pinholes, the samples were etched in 5% tetramethylammonium hydroxide (TMAH) at 60 °C for 10 min (see Figure 2e). Since TMAH selectively etches *c*-Si over SiO_x, this processing step created micron-scale etch pits in *c*-Si, which could be easily imaged with SEM.[17]

Electrical Characterization. Other samples after pinhole formation were dipped in HF, followed by PECVD of ∼20 nm of phosphorus-doped *a*-Si:H using $SiH_4/H_2/PH_3$ (2, 100, and 2 sccm, respectively; 3% PH_3 in H_2) feed gases at 220 °C. The rf power was 8 W at a total pressure of 1 Torr. After this, we split the samples into two groups to fabricate solar cells or symmetric test structures for measuring the contact resistivity. For fabricating solar cells, on the back side, ∼20 nm of boron-doped *a*-Si:H was deposited using $SiH_4/H_2/B_2H_6$ (2, 100, and 2 sccm, respectively; 2.6% B_2H_6 in H_2) at 200 °C at the same plasma power and pressure as the front side. For fabricating the test structures, ∼20 nm of phosphorus-doped *a*-Si:H was deposited on the back side using the same conditions as on the front. The samples were annealed in an N_2 atmosphere for 30 min at 850 °C to crystallize the doped *a*-Si:H layer to poly-Si and drive in the dopants. The samples were inserted into the furnace at 200 °C and heated to 850 °C at a ramp rate of 3.6 °C/min. After crystallization of *a*-Si:H and dopant drive-in, the samples were HF-dipped prior to the atomic layer deposition (ALD) of ∼15 nm of Al_2O_3. ALD was followed by annealing in forming gas at 400 °C for 1 h. Then, the Al_2O_3 layer was etched in HF. For *J*-*V* and electron beam-induced current (EBIC) analysis of both sides of the solar cells, Ag gridlines were thermally evaporated onto both sides of the samples. For contact resistivity measurements using the transfer length method (TLM), Ag pads were deposited. TLM samples were analyzed before and after etching in an SF_6 plasma with Ag pads serving as the etch mask. EBIC mapping was performed using a JEOL JSM-7600F SEM with a Mighty EBIC quantitative EBIC system. SEM and EBIC images were acquired simultaneously in plan-view orientation, using an electron beam accelerating voltage of 5 kV and a beam current of 1.4 nA.

RESULTS AND DISCUSSION

Characterization of Pinhole Density and Location by the TMAH Etching Technique. Inverted pyramid texture was created using patterned circular openings in the SiN_x masking layer due to the high selectivity for *c*-Si etching over SiN_x in KOH. The same principle was used to visualize pinholes in the SiO_x layer. In this case, TMAH etched the poly-Si and *c*-Si with even higher selectivity over SiO_x than KOH and produced ∼100−500 nm etch cavities under each pinhole.[17] The exact shape of the cavity depends on the local crystallographic orientation of the *c*-Si surface. Figure 3a shows an SEM micrograph of an etch pit in *c*-Si at an inverted pyramid face. On Si(100) surfaces, similar to texturing with KOH (see the Experimental Methods section), TMAH creates etch pits that are inverted pyramids (see Figure 2e.1). This pyramidal shape occurs due to the slower etching rate of the Si{111} planes compared to the Si{100} planes. Similarly, TMAH-induced pits on Si{111} faces in inverted pyramids (see Figure 3) or v-grooves can also be explained based on the preferential etching of Si{100} over Si{111} planes, which constrains the facets of the pits to intersecting Si{111} planes. In Figure 3a, the upper edges of the etch pit form a hexagon, and the inside contour consists of four Si{111} faces that intersect at a vertex. The schematic in Figure 3b shows an octahedron consisting of Si{111} faces. This octahedron is intersected with a Si(111) plane such that it creates a hexagonal outline similar to the etch pit in Figure 3a. We speculate that the initiation of the etch pits on Si{111} planes, which are expected to etch slower in TMAH, can still occur due to surface nanoroughness. Previously, we measured

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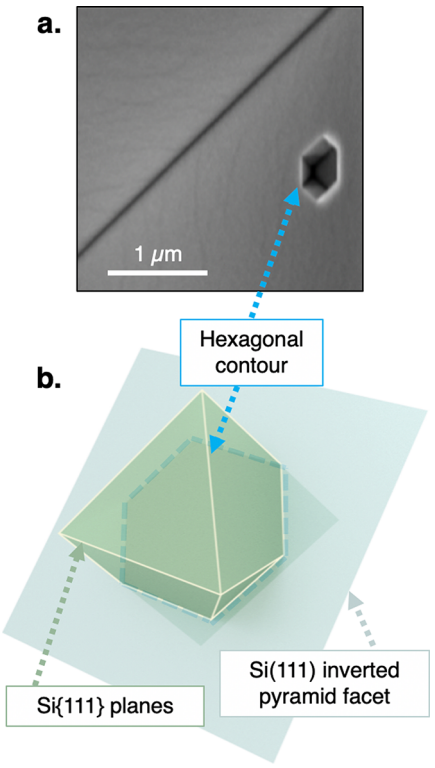

Figure 3. (a) SEM micrograph of an etch pit created by TMAH at an inverted pyramid face. (b) Geometric representation to explain the hexagonal outline of the etch pit in (a). The light blue plane represents one of the Si(111) faces of the inverted pyramid, as shown in Figure 2c. As the etch pit is formed, similar to the inverted pyramids, it will also be constrained by Si(111) faces. The green regular octahedron represents eight such Si(111) planes. The contour of the etch pits on the inverted pyramid faces arises due to the intersection of the blue plane (inverted pyramid face surface) with the octahedron.

nanoscale roughness on the Si(111) surfaces of random pyramids using atomic force microscopy.[9] These rough Si(111) surfaces likely consist of features such as step edges or other exposed facets, which are more prone to etching in TMAH.

Figure 4a shows the density of etch pits for inverted pyramid and polished *c*-Si samples that were annealed at 1050 °C for 45 min and subsequently etched in TMAH to remove the poly-Si and to create etch pits. In the nonconnecting inverted pyramids (Figure 4b,c), polished Si(100) surface portions alternate with Si{111} surfaces in the pyramids. The centers of the inverted pyramids may consist of a vertex or small groove (<1 μm) along the Si[100] direction. Using TrackPy[18] to count the number of TMAH etch pits, we observed that the etch pit densities on inverted pyramids were ~6.4 × 10^5 and ~7.6 × 10^5 cm^{-2} for samples annealed at 1050 °C for 30 and 45 min, respectively. The etch pit density on the polished Si(100) sample was almost six to seven times lower (~1.0 × 10^5 cm^{-2}). Interestingly, at 1050 °C, we observed the TMAH etch pits to be more prevalent at the inverted pyramid vertices. This is shown in Figure 4a,b, for the sample with etch pitch density of 7.6 × 10^5 ± 1.9 × 10^5 cm^{-2}. While Marcus and Sheng observed a 45% decrease in SiO_x thickness at the concave edges of the trenches,[15] their studies were for much thicker SiO_x layers and may not be directly applicable to ultrathin ~2 nm SiO_x. Nevertheless, we hypothesize that the

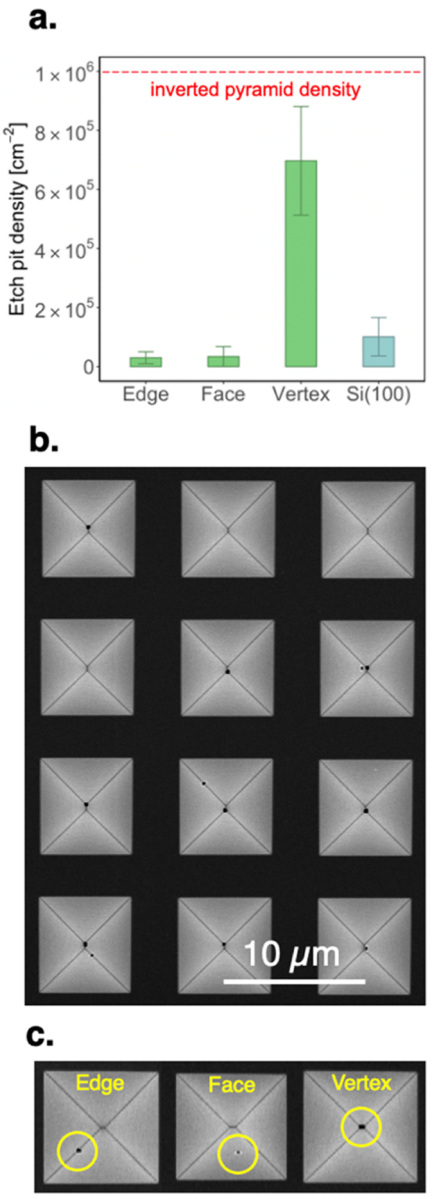

Figure 4. (a) Density of etch pits obtained by TMAH etching on three different inverted pyramid regions (green) and on Si(100) (blue). The red dashed line indicates the density of inverted pyramids in the sample. (b) SEM micrograph displaying 12 inverted pyramids with etch pits predominantly located at the vertices. (c) SEM micrograph displaying three adjacent inverted pyramids with three different locations (edge, face, and vertex) for the etch pits.

SiO_x layer at the vertices may be thinner due to their concave geometry resulting from a lower O_2 flux[15] and compressive stress[15,19] that may locally retard the oxidation of Si. Thus, we speculate that due to the thinner SiO_x, and the highest Gaussian surface curvature of all surface morphologies studied (vertices, edges, and faces; see Figure 4c), the vertices would be most prone to SiO_x breakup.

Our experiments show that the pinhole density on textured and planar surfaces is a very strong function of the annealing temperature, with almost three orders of magnitude higher density of TMAH etch pits on samples treated at 1100 °C. Figure 5 shows four types of surfaces—v-grooves, inverted pyramids, random pyramids, and polished Si(100)—that were annealed at 1100 °C and subsequently etched in TMAH to

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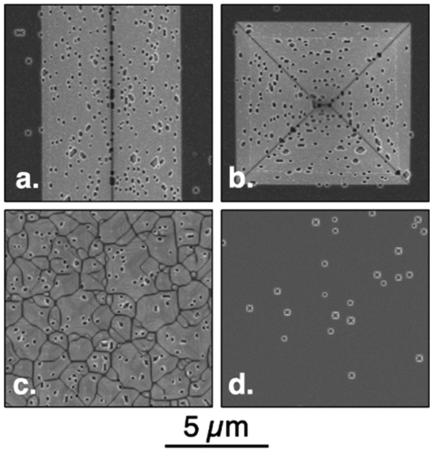

Figure 5. SEM micrographs of (a) v-groove, (b) inverted pyramid, (c) random pyramid, and (d) polished Si(100) samples that were annealed at 1100 °C and subsequently etched in TMAH to create etch pits under each pinhole.

create etch pits. In the nonconnected regular v-grooves (Figure 5a), polished Si(100) surface portions alternate with Si{111} surfaces. The valleys of the v-grooves are along the Si [100] direction. The random upright pyramid (Figure 5c) faces, while predominantly thought to be Si{111}, may also contain facets with higher index planes than Si{111}.[3] For all textured samples, we observed a majority of etch pits at the textured facets rather than at Si(100) locations. The TMAH etch pit densities for the four surfaces shown in Figure 5 are tabulated in Table 1. Note that the area utilized for all density calculations corresponds to the area of the original Si(100) surface prior to texturing. The etch pit density on the textured surfaces is over the range of $1.8-2.6 \times 10^8$ cm^{-2}, while that on the polished surface is an order of magnitude lower, $\sim 2.4 \times 10^7$ cm^{-2}. The almost one order of magnitude difference between the density cannot be explained by an increase in surface area due to texturing and is likely due to the surface morphology. Kale et al. carried out atomic force microscopy on upright pyramids and showed that the pyramid face nanoroughness to be significantly higher than that of a polished Si(111) wafer. Furthermore, in that study, cross-sectional transmission electron microscopy (TEM) images taken at different positions along the facets of the random pyramids showed significant variations in SiO_x thicknesses ranging from 1.4−2.3 nm.[9] These regions of locally thinner SiO_x on facets of textured surfaces can facilitate SiO_x breakup. Additionally, it is possible that the stress induced in the SiO_x layer due to nanoscale surface roughness could influence SiO_x breakup. Note that samples that were not annealed and subsequently etched in TMAH did not form etch pits, which indicates the annealing step is required to form the pinholes in the SiO_x layer.

Contact Resistivity Analysis by the Transfer Length Method. All samples treated at 1100 °C had contact resistivities below 100 mΩ·cm^2 (see Table 1 and Figure 6),

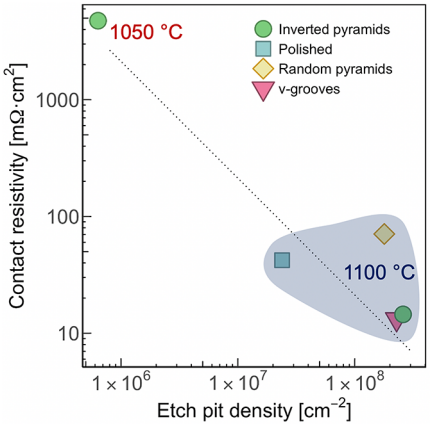

Figure 6. Contact resistivity as a function of the TMAH etch pit density for samples that were annealed at either 1050 or 1100 °C (highlighted in blue background) for 30 min and subsequently etched in TMAH to create characteristic etch pits under each pinhole. The dotted line represents the calculated contact resistivity using the spreading resistance expression for a pinhole radius of 2 nm and a wafer resistivity of 1.7 Ω·cm.

consistent with their high $\sim 10^7-10^8$ cm^{-2} etch pit density. The product of the contact resistivity and etch pit density results in the resistance R_{pin} for an individual pinhole. For samples treated at 1100 °C, R_{pin} was in the range of $\sim 10^6-10^7$ Ω for all four surfaces. Table 1 shows the average in-diffused equivalent diameter calculated using the assumption that R_{pin} is dominated by the spreading resistance in the wafer and thus can be described by $d = \rho_w/(2\ R_{pin})$,[20] where R_{pin} and ρ_w are the pinhole contact resistance and wafer resistivity, respectively, and d is the diameter of the in-diffused region beneath the pinhole. The wafer resistivity used for the FZ and Cz-based samples were 1.7 or 2.9 Ω·cm, respectively. The calculated average in-diffused equivalent diameter for all four surfaces is <8.5 nm. These calculated in-diffused equivalent diameters in

Table 1. Contact Resistivity and Estimates for Etch Pit Density, Pinhole Density, and Average in-Diffused Equivalent Diameter for Different *c*-Si Surfaces for Annealing Temperatures of 1100 and 1050 °C

texture	contact resistivity [mΩ·cm^2]	etch pit density (TMAH) [cm^{-2}]	pinhole density (EBIC) [cm^{-2}]	avg. in-diffused equivalent diameter [nm]
		1100 °C for 30 min		
random pyramid	70.8 ± 10.2	$1.8 \times 10^8 \pm 1.1 \times 10^7$	$2.3 \times 10^7 \pm 1.3 \times 10^7$	1.14 ± 0.13
inverted pyramid (i-p)	14.5 ± 0.4	$2.6 \times 10^8 \pm 9.3 \times 10^6$		2.26 ± 0.04
v-groove (v-g)	13.2 ± 1.1	$2.3 \times 10^8 \pm 1.1 \times 10^7$		2.82 ± 0.11
polished Si(100)	42.2 ± 3.0	$2.4 \times 10^7 \pm 2.3 \times 10^6$	$2.6 \times 10^7 \pm 2.4 \times 10^6$ (v-g)*	8.43 ± 0.43
			$8.8 \times 10^6 \pm 3.9 \times 10^5$ (i-p)*	
		1050 °C for 30 min		
inverted pyramid	4750 ± 620	$6.4 \times 10^5 \pm 1.9 \times 10^5$	not measurable	2.82 ± 0.39
polished Si (100)	not measurable	$1.0 \times 10^5 \pm 6.5 \times 10^4$	not measurable	

*Obtained from the polished side of the v-g and i-p solar cells.

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Table 1 are comparable to pinhole diameters reported by Wolstenholme et al. and Tetzlaff et al. based on high-resolution cross-sectional TEM of disrupted SiO_x at the poly-Si/SiO_x interface. The pinhole diameters in these previous studies were in the range of ~5−38 nm in chemically (~1.7 nm) and thermally grown (~2.6 nm) SiO_x that were subjected to peak annealing temperatures ranging from 800 to 1050 °C.[12,14] Thus, the in-diffused regions underneath the pinholes are likely comparable to the actual pinhole diameter since the calculated in-diffused equivalent diameters fall into the range of pinhole diameters found in previously imaged pinholes.[12,14]

The contact resistivity of the polished Si(100) sample is only a factor of 3 higher than the inverted pyramid, and v-groove samples annealed at 1100 °C, despite one order of magnitude lower etch pit density. On the other hand, the random pyramid sample annealed at 1100 °C, which has a etch pit density very similar to the inverted pyramid and v-groove samples, has a nearly five times higher contact resistivity. In fact, the contact resistivity of the random pyramid samples annealed at 1100 °C is even higher than the polished Si(100) sample annealed at 1050 °C. One possible explanation for very different contact resistivities for the four types of surfaces in Table 1 is that the average pinhole diameter depends on how the textured surfaces were created, which in turn may influence the stress and nonuniformities in SiO_x during oxidation. We acknowledge that this explanation is speculative, and more investigation is needed to verify if these measured contact resistivities indeed relate to their respective pinhole density and average pinhole diameter, such as by analyzing several cross-sectional transmission electron microscopy to measure the average pinhole diameter in each case. The contact resistivities of samples annealed at 1050 °C were too high to obtain from TLM analysis, which is consistent with the two to three orders of magnitude lower etch pit density than at 1100 °C. Instead, after RIE, single pad-to-pad resistances were used to calculate the contact resistivity based on the area of the Ag pads. However, for the polished sample, the pad-to-pad resistances obtained were unreasonably high (10^6−10^7 Ω), which is comparable to the resistance of a single pinhole. We tentatively ascribe this effect to poor adhesion of the poly-Si layer to the polished wafer surface, which is known to affect *a*-Si:H films deposited to low-roughness surfaces via PECVD.[21]

Bifacial Back-Junction Cells Analysis Using Electron Beam-Induced Current Measurements. Bifacial cells were fabricated for three different types of textured *c*-Si wafers—front-side inverted pyramids with a polished rear, front-side v-grooves with a polished rear, and double-side randomly textured. In each solar cell, the pinholes were created by annealing at 1100 °C after the deposition of intrinsic *a*-Si:H, but before the introduction of dopants—the pinhole formation is thus independent of dopant type. The contact resistivity of <100 mΩ·cm^2, measured on n^+ poly-Si, is sufficiently low for obtaining functional solar cells that can be analyzed using EBIC. We note that the in-diffusion of boron and the contact resistivity in the p^+ poly-Si/SiO_x rear may be different. The EBIC technique allows for the analysis of pinholes in SiO_x on different textures without the need for TMAH etching. Figure 7 shows the *J*-*V* curves obtained at 1 Sun for the three solar cells at room temperature. In all three solar cells, the *p*−*n* junction is on the back side. For solar cells with v-grooves and the inverted pyramids, the back side is polished. Note that these solar cells were not optimized for the highest efficiency but simply used for characterization with EBIC. The 10−16% efficiency, obtained at 1 Sun and plotted in Figure 7, was sufficient for EBIC measurements.

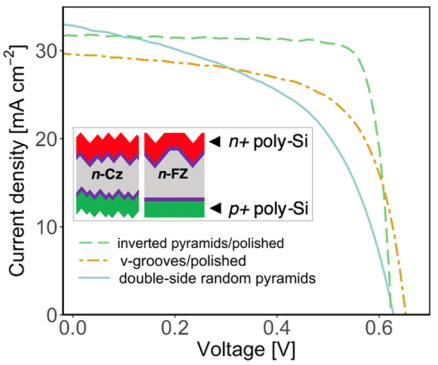

Figure 7. *J*-*V* curves obtained at 1 Sun for three bifacial solar cells annealed at 1100 °C to induce SiO_x breakup. The solar cells were illuminated from the n^+ poly-Si side, without any illumination of the p^+ side. The inset schematics show the double-side randomly textured (left) and inverted pyramids or v-grooves (right) solar cell cross sections (Ag gridlines on both sides are not shown).

We have previously detected pinholes or conduction channels in poly-Si/SiO_x contacts using SEM-based EBIC analysis.[9,11] In plan-view EBIC, a focused electron beam scans over the solar cell, generating electron−hole pairs. The EBIC signal depends on the probability of creating electron−hole pairs and the collection of carrier current. The collection probability is a function of the local passivation, local electric field, and the passivating contact's local conductivity. Regions where the carriers are more easily collected due to missing SiO_x exhibit a higher current than surrounding regions, where the insulating ~2.1 nm SiO_x layer hinders transport. Thus, brighter spots in EBIC maps indicate a locally thinner tunneling SiO_x layer or pinholes. The generation of electron−hole pairs by e-beam on nonplanar surfaces depends on the surface texture, which creates local variations of the electron beam interaction volume. For example, on a randomly textured surface, the pyramid tips appear dark, and the valleys between the random pyramids appear bright. This is because the energy density deposited from the electron beam is lower at the tips compared to the valleys.[11] Thus, in the analysis of the contrast in EBIC images, the effect of surface texture must be differentiated from the contrast that arises due to differences in transport or recombination of excess charge carriers.

EBIC images and corresponding SEM micrographs for both sides of these solar cells with random pyramids, inverted pyramids, and v-groove texture are shown in Figures 8 and 9. The ratio of the electron beam-induced current, I_{EBIC}, to the beam current, I_b is also shown for each image in Figures 8 and 9. The I_{EBIC}/I_b ratio is an order of magnitude lower for EBIC scans on the n^+ poly-Si/SiO_x contact (Figure 8) than that in the p^+ poly-Si/SiO_x contact (Figure 9). Additionally, no bright spots due to pinholes were observed in the EBIC image for the n^+ poly-Si/SiO_x contact in Figure 8, while several bright spots are clearly visible in the EBIC images for the p^+ poly-Si/SiO_x contact in Figure 9. Digital exaggeration of contrast of the images in Figure 8 also did not produce any visible contrast due to pinholes. This observation cannot be attributed to a lack of pinholes in the n^+ poly-Si/SiO_x contact due to the following reasons. First, when the n^+ poly-Si/SiO_x contacts were etched in TMAH, etch pits due to pinholes in SiO_x were

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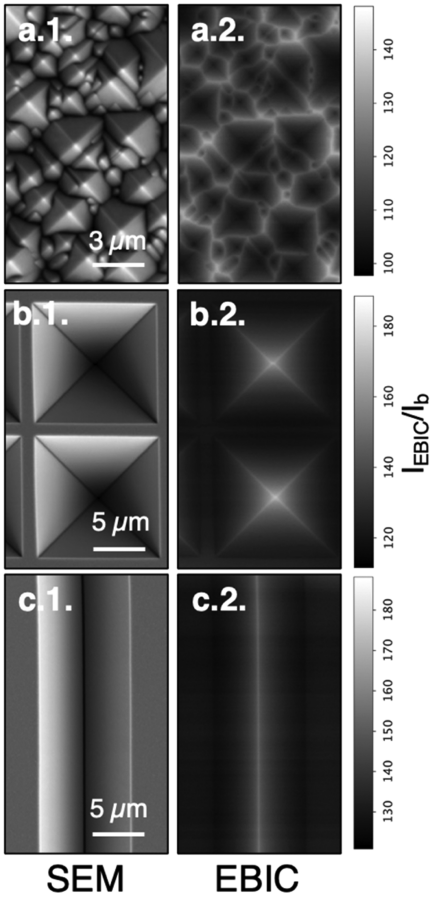

Figure 8. SEM (a.1, b.1, and c.1) and EBIC images (a.2, b.2, and c.2) for scans on the front side high-low junction (n^+ poly-Si/SiO_x/n-type c-Si) in solar cells with (a) double-side textured random pyramids, (b) inverted pyramids on the front, and (c) v-grooves on the front.

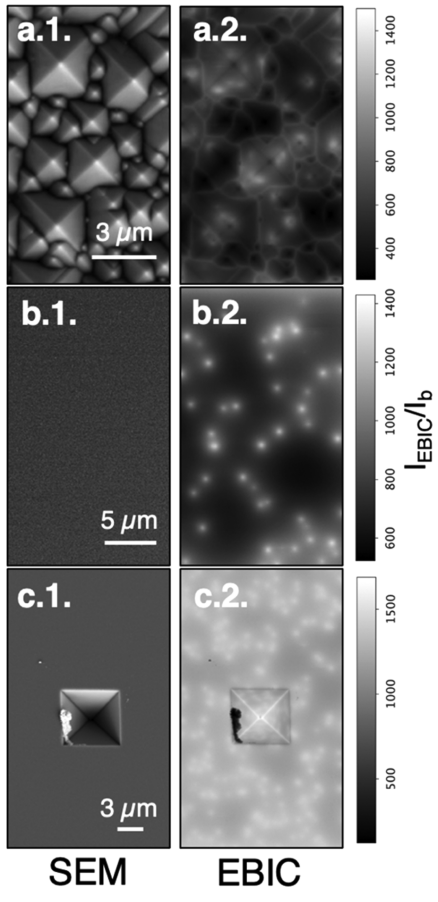

Figure 9. SEM (a.1, b.1, and c.1) and EBIC images (a.2, b.2, and c.2) for scans on the rear side p–n junction (p^+ poly-Si/SiO_x/n-type c-Si) in solar cells with (a) double-side textured random pyramids, (b) inverted pyramids on the front, and (c) v-grooves on the front. The back side of the inverted pyramids and v-groove textured samples is polished. The inverted pyramid in (c) is due to imperfections in the protective SiN_x layer on the polished side, which results in the occasional formation of inverted pyramids during the texturization of the front with KOH.

clearly observed (see Figure S.1 in the Supplementary Information). Second, as described in the Experimental Methods section, the pinholes were created after deposition of intrinsic a-Si:H, and both sides of the sample were subjected to an identical SiO_x breakup protocol. Third, the solar cell efficiencies are >10%, which implies both contacts are sufficiently conductive for EBIC imaging. We speculate that the differences in the EBIC images for the n^+ poly-Si/SiO_x contacts (Figure 8) and those for the p^+ poly-Si/SiO_x contacts (Figure 9), where pinholes are clearly visible, are due to the magnitude of the electric field associated with each contact structure. The EBIC measurement relies on the electric fields within the solar cell to separate the electron–hole pairs generated by the incident electron beam in the SEM so that the electrons and holes can travel to the contact of the appropriate polarity and contribute to the EBIC signal. For an n-type wafer, the electric field associated with the n^+ poly-Si/SiO_x contact is significantly weaker than the field associated with the p^+ poly-Si/SiO_x contact due to a higher built-in potential in the latter case. Additionally, the J_0 value is lower for the n^+ poly-Si/SiO_x contact than that in the p^+ poly-Si/SiO_x contact, and the electron diffusion length is longer than that for the holes. These two effects allow the electrons to diffuse laterally over longer distances near the n^+ poly-Si/SiO_x contact prior to collection compared to holes near the p^+ poly-Si/SiO_x contact. As a result, at the n-type contact, the beam-induced current can be collected simultaneously from several pinholes in the vicinity of the electron beam, and due to this effect, a sharp contrast is not obtained between regions where pinholes are present or absent. For the n^+ poly-Si/SiO_x side, the spatially averaged EBIC signal is significantly lower compared to the p^+ poly-Si/SiO_x side. During the collection of the EBIC scans for the n-type contact, the carriers are generated within ~1 μm from the n-type contact. This means that the minority carriers, holes, have to diffuse across the entire thickness of the wafer prior to collection. During the collection of the EBIC scans for the p-type contact, the majority carriers, electrons, have to diffuse across the thickness of the wafer. We speculate that the lower beam-induced current for the n-type side compared to the p-type side may be due to the higher recombination probability for the holes (minority carriers) prior to collection.

Figure 9 shows the EBIC images of the p^+ poly-Si/SiO_x contact on the n-type wafer, which, unlike the n^+ poly-Si/SiO_x contact, clearly shows several bright spots due to pinholes on a randomly textured surface (Figure 9a) and the polished back side of the inverted pyramid (Figure 9b) and v-groove solar cells (Figure 9c). The pinhole densities in these EBIC images were determined using DotDotGoose,[22] and are shown in Table 1. For the random pyramids, the etch pit density obtained from TMAH etching is almost a factor of 5 higher

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ACS Appl. Energy Mater. 2022, 5, 3043–3051

than the pinhole density obtained from the EBIC images (see Table 1). A plausible reason for this discrepancy is that in EBIC imaging, if the pinholes are in close proximity, the beam current would be collected simultaneously from more than one pinhole, which creates larger single spots from pinholes clusters, leading to an undercount of the pinhole density. These clusters can be seen in Figure S.2 in the Supplemental Information. In contrast, on the polished back side of the inverted pyramid and v-groove textured solar cells, the pinhole density obtained from TMAH etching is an order of magnitude lower than the randomly textured surface (see Table 1). As a result, the average distance between the pinholes is larger, which allows for individual pinholes to be imaged as a single bright spot in the EBIC measurements.

SUMMARY AND CONCLUSIONS

Poly-Si/SiO_x (SiO_x ~2 nm) passivating contacts were grown on random upright pyramids, uniform v-grooves, inverted pyramids, and polished Si(100). After SiO_x breakup at either 1050 or 1100 °C, the textured surfaces had approximately 6 to 10 times higher pinhole density than the polished Si(100) sample. We speculate the higher propensity for SiO_x breakup on textured surfaces to be due to nanoscale roughness that forms during the alkaline etching used to texture *c*-Si.[9] For the polished Si(100) samples, there was agreement within a factor of ~1−3 between the pinhole densities estimated via TMAH etching and EBIC imaging. However, differences of approximately one order of magnitude were observed for the random upright pyramids, which may be a consequence of the difficulty in counting pinholes in EBIC images where the pinhole densities are $\gtrsim 1 \times 10^7$ cm^{-2}. Notably, at 1050 °C, we observed that the pinholes are created predominantly at the vertices of the inverted pyramids. These high-curvature structures appear to be more prone to thinner SiO_x growth and SiO_x disruption. This result indicates that texture can be exploited as a means to precisely engineer pinhole formation in solar cells using poly-Si/SiO_x contact structures. Finally, in our solar cells, we observed clear differences in the EBIC images of poly-Si/SiO_x contacts of different polarities on *n*-type Si substrates. While EBIC images of the n^+ side did not reveal any pinholes, pinholes were observed in EBIC images of the p^+ side. These observations could not be attributed to the lack of pinholes in the n^+ poly-Si/SiO_x. We attribute the observed effect to the longer diffusion length of minority carriers in the vicinity of n^+ poly-Si/SiO_x.

While regular inverted pyramids are not of practical application in Si solar cell manufacturing, several photolithography-free wet chemistry processes exist,[23−25] which could enable the mass production of random inverted pyramids texture in Si wafers. While v-grooves still require photolithography, our study may be of value for niche applications where superior light-trapping[26] is warranted, such as in all back contact point-focus Si concentrator solar cells.[27]

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaem.1c03676.

Plan-view SEM image of TMAH-etched n^+ poly-Si/SiO_x side of a solar (Figure S.1); (a) SEM and (b) EBIC plan-view images for the rear-side p−n junction (p^+ poly-Si/SiO_x/n-type *c*-Si) in the solar cell with double-side textured random pyramids (Figure S.2) (PDF)

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Notes

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