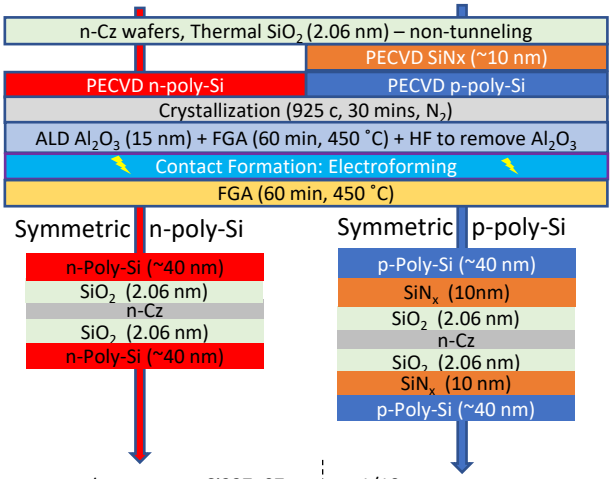
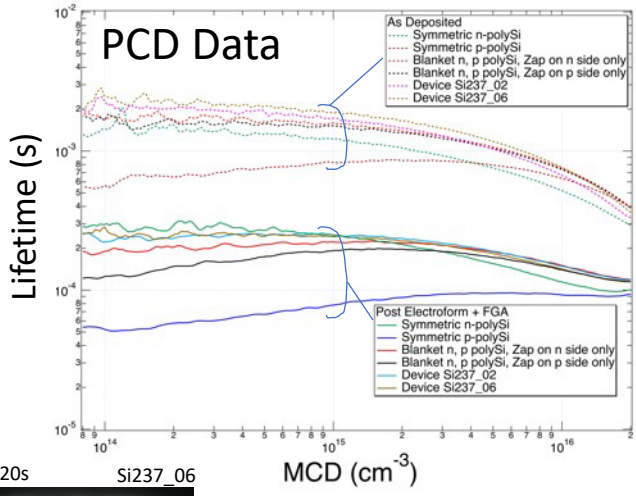
Controlled Dielectric Breakdown to Form Pinhole Passivated Contacts

David L. Young, William Nemeth, Caroline Lima Salles, Pauls Stradins

Abstract

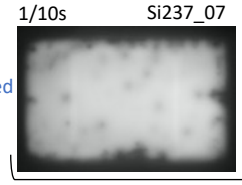
This contribution explores a low-temperature route to forming dielectric pinholes to form poly-Si/dielectric/c-Si passivated contacts. The method utilizes *controlled dielectric breakdown* to form nanoscale pinholes in a thick (non-tunnelling) dielectric which, when annealed, allows dopant atoms to pass from doped poly-Si through the dielectric and into the c-Si wafer forming conductive pathways. We show that the pinholes can be repassivated with dopants and H diffusion which results in increased PL signals after processing. The method can be expanded to optimized dielectric passivation stacks (not just a single layer) and can be formed in parallel over the faces of the wafer in selected areas (only under the grid).

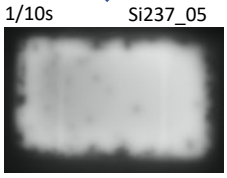


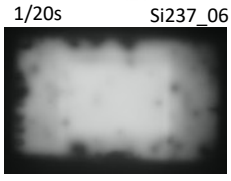


PL

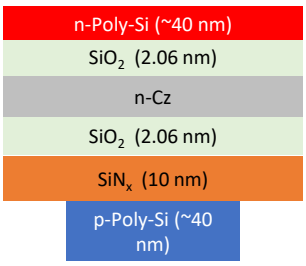
As Deposited



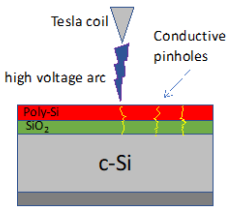


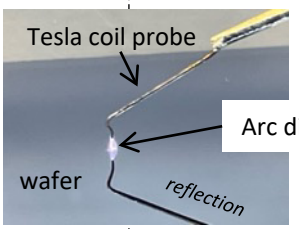


Device

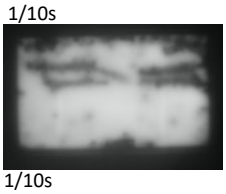


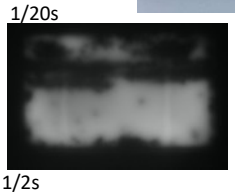
Electroforming Dielectric Breakdown

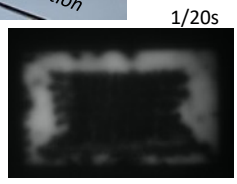




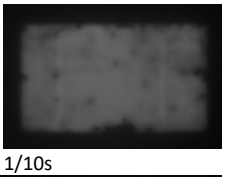
Post electroform

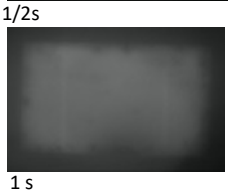


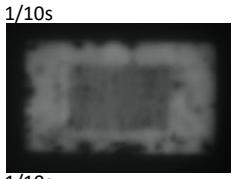




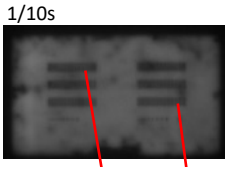
Post 2nd FGA

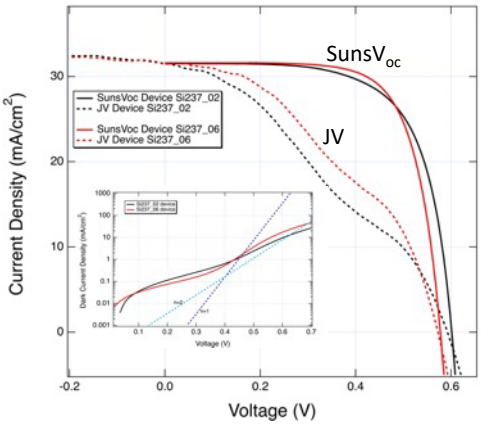




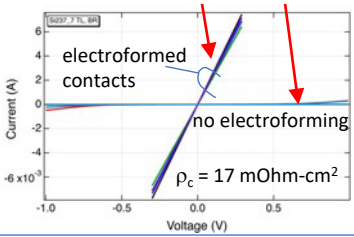


Post metal TLM pads

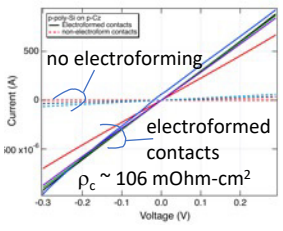




N-poly-Si/n-Cz sample



p-poly-Si/p-Cz sample



Observations

- Ohmic contacts can be made through thick SiO_2 (SiNx)/ Poly-Si contacts using electroforming with Tesla coil discharge.
- Passivation is lost after electroformation, but can be partially restored after a FGA. However, post-arc FGA causes sample-wide loss of passivation (possible contamination from tesla probe).
- n-polySi/SiO_2 = Ohmic contact (ρ_c = 17 mOhm-cm²)
- p-polySi/SiN_x/SiO_2 = Ohmic, poor contacts (ρ_c ~ 106 mOhm-cm²)
- Kink in JV curves of electroformed devices

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