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High-Efficiency Solar Cells Grown on Spalled Germanium for Substrate Reuse without Polishing

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Radical reduction of III–V device costs requires a multifaceted approach attacking both growth and substrate costs. Implementing device removal and substrate reuse provides an opportunity for substrate cost reduction. Controlled spalling allows removal of thin devices from the expensive substrate; however, the fracture-based process currently generates surfaces with significant morphological changes compared to polished wafers. 49 single junction devices are fabricated across the spalled surface of full 50 mm germanium wafers without chemo-mechanical polishing before epitaxial growth. Device defects are identified and related to morphological spalling defects—arrest lines, gull wings, and river lines—and their impact on cell performance using physical and functional characterization techniques. River line defects have the most consistent and detrimental effect on cell performance. Devices achieve a single junction efficiency above 23% and open-circuit voltage of 1.01 V, demonstrating that spalled germanium does not need to be returned to a pristine, polished state to achieve high-quality device performance.

1. Introduction

III–V solar cells have the highest conversion efficiency of any solar technology, with demonstrated single-junction efficiencies >29%.[1] However, high production costs keep III–Vs from widespread use in terrestrial applications.[2] The cost of epitaxial growth, the single-crystal substrate on which solar cells are grown, and back-end processing and metallization all contribute to the overall costs.[2] The cost of Ge or GaAs substrates is a significant barrier to widespread III–V use in terrestrial applications, with costs in excess of \$30 per W_{DC};[3] thus, either inherently low-cost substrates need to be developed or substrates must be used many times to sufficiently amortize costs. To date, low-cost substrates that lead to high-quality epitaxy have yet to be developed, so current commercial efforts focus on device removal and substrate reuse.[4–6]

Epitaxial lift-off (ELO) is currently the only commercially deployed substrate reuse technology. Typically, ELO uses an HF-based wet-chemical process to selectively etch an embedded AlAs release layer that is grown below a device stack. ELO successfully lifts off high-efficiency devices from GaAs substrates at wafer scale with subsequent regrowth on the parent wafer.[4,7–9] However, the ELO chemical etching process leaves behind surface features that impact device performance when the substrate is reused, and accumulate with additional reuses.[10,11] Defect accumulation necessitates reprocessing the wafer by chemo-mechanical polishing (CMP) at regular intervals. The cost of the CMP step ultimately determines the achievable cost, which was estimated at \$9–34 per cell depending on the polishing frequency required.[12] Clearly, reducing or eliminating CMP is a generalized requirement for all substrate reuse technologies in order to achieve substrate costs sufficiently low for III–V devices to be used in terrestrial applications as well as large space-based installations.

Controlled spalling offers a fundamentally different approach to substrate reuse than ELO. Controlled spalling achieves device exfoliation by propagating a crack within the substrate nearly parallel to the substrate surface with the aid of a stressor layer deposited on top of the device.[13–15] The thickness of this stressor layer principally defines the crack depth, with the crack placement targeted just below a grown device.[16,17] Spalling provides a rapid and facile way to remove high efficiency solar cells from the substrate without damaging either device or substrate.[18–21] This form of wafer cleavage also yields a chemically pristine surface that is free of etching by-products and etch-related pits, opening the possibility of regrowth on a spalled surface without the need for CMP or other expensive reprocessing. Spalled surfaces, however, are not all ideal for growth, and are not completely free of morphological imperfections.

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For example, spalling (100)-oriented GaAs generates a highly faceted surface due to the lack of alignment between low energy surfaces and this commonly used growth orientation.[22] (110)-oriented GaAs is better aligned for cleavage because the (110) plane is a natural cleavage plane in zinc-blende materials and spalling this orientation leads to a relatively flat surface.[22] We showed that single-junction devices grown on spalled (110) GaAs surfaces have efficiencies within 15% (relative) of control devices grown on polished surfaces of the same orientation.[23] However, (110) is not a common growth orientation for III–V photovoltaics, and it is difficult to maintain a smooth epitaxial growth front.

Ge substrates are commonly used instead of GaAs substrates for growth of III–V multijunction solar cells used for space applications. Controlled spalling of (100)-oriented Ge solves several issues associated with GaAs spalling, offering both alignment between a preferred growth orientation and an available cleavage system. Ge largely spalls flatly but the fracture can result in morphological defects, including arrest lines and river lines.[24] Arrest lines are linear height perturbations that run perpendicular to the spalling direction as the crack front propagates.[25] Arrest lines can run across the entire width of the spalled area and are often micrometers deep and hundreds of nanometers wide. They can be separated by as little as 100 µm or by many millimeters, depending on the details of the spalling process. The flat regions between arrest lines in spalled Ge, however, have root mean square roughness comparable to epi-ready polished substrates.[26] River lines occur along the lateral edges of spalled substrate surfaces, running in the general direction of the spall, due to mode III loading of the crack.[27,28] River lines are typically shallower but sharper than arrest lines and exist in much denser formations. For more details on the fracture mechanics behind these morphological spalling defects, see refs. [13,27–29].

Our previous work began exploring the impact of arrest lines on solar cell device performance. A device grown on a spalled Ge substrate exhibiting arrest lines showed higher dark currents than control devices grown on commercial Ge wafers, corroborated by dark lock-in thermography (DLIT) measurements that showed that arrest lines lead to localized device shunting.[30] The shunting from the arrest lines is much more noticeable under forward bias DLIT than reverse bias, which is consistent with increased recombination in these areas. Still, that work demonstrated a 12.8% efficient, lattice-matched GaInAs single-junction solar cell grown on a spalled Ge surface that received no additional surface processing. This result showed reasonable performance for a single, isolated device, but for a technology to be successful, there needs to be increased understanding of all types of defects that occur over full-area wafers.

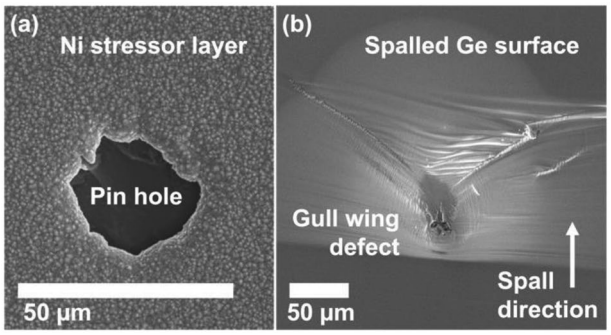

Figure 1. Representative SEM micrographs of a) a pin hole in the Ni stressor layer due to electroplating imperfections that results in b) a gull wing defect on the Ge wafer surface after controlled spalling.

Here, we describe single-junction GaInAs solar cell devices grown by organometallic vapor phase epitaxy (OMVPE) directly on spalled Ge (hereafter referred to as "sp-Ge") substrates that undergo minimal surface processing, but no CMP, before growth. By patterning 5 mm × 5 mm cells across entire 50 mm wafers, we isolate regions that are defect-free and those that exhibit different morphological defects. We measure solar cell current–voltage (J–V) metrics in combination with high-resolution microscopy techniques and spatially-resolved electroluminescence (EL) and DLIT to perform multi-scale functional characterization of the devices on and around morphological spalling defects. We identify a third defect type, gull wings, in sp-Ge surfaces, and show that both arrest lines and gull wing defects result in localized shunts. River lines are more problematic for device performance, resulting in consistently lower-performing solar cells associated with a high dislocation density in the cell material. We demonstrate a 23.4% efficient single-junction solar cell on sp-Ge under conditions where no spalling defects are present and without the use of a CMP step. These best devices are within 2% relative of nominally identical devices grown on commercial epi-ready Ge (hereafter referred to as "epi-Ge") substrates.

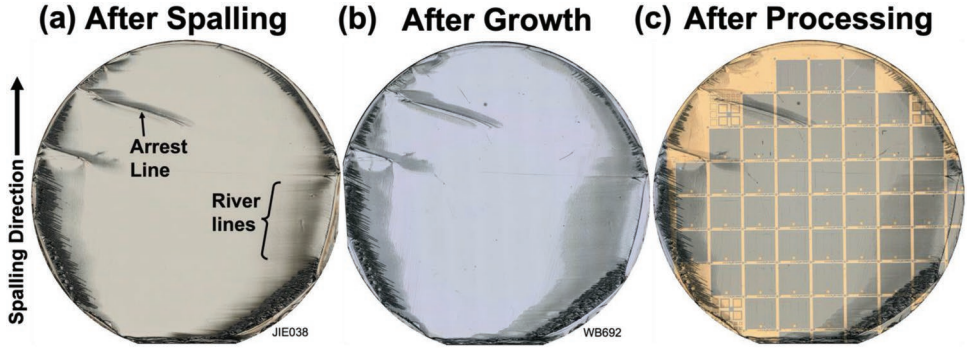

Figure 2. Optical micrographs of the same 50 mm-diameter Ge wafer a) after spalling, b) after growth, and c) after device processing.

2. Results and Discussion

We conducted wafer-scale controlled spalling to prepare spalled wafers for analysis and epitaxial growth. Wafers were prepared using a galvanostatic electroplating process in a nickel-phosphorous chemistry electrolyte to provide the necessary sub-critical strain energy for spalling and an external force was applied to an adhered tape to initiate and propagate the subsurface spalling fracture (details of experimental methods are provided in Experimental Section). Full wafers subjected to controlled spalling exhibited arrest lines and river lines, consistent with previous observations: arrest lines traverse the wafers perpendicular to the spalling direction and dense formations of river lines appear toward wafer edges. Arrest lines vary in density and depth, with those resulting from partial spontaneous spalling (Figure S1, Supporting Information) appearing more severe than those associated with controlled spalling. We also observed a third type of morphological defect in spalled surfaces. Optical, electron, and confocal microscopy show that these defects are regions with a local decrease in spall depth, localized around a point, roughly ≈20–50 µm in size, with crack propagation instability radiating ≈150–500 µm as a trail of curved features emanating out laterally (perpendicular to the macroscopic spall direction). Fractographic observations are consistent with defects known as "gull wings," which are a local crack depth variation with a shape reminiscent of a gull's wings that results from the interaction of a propagating crack with a localized defect.[31] In this case, we identify the defect source as a local imperfection, ≈10–20 µm in diameter in the stressor layer (**Figure 1**a), directly above the point where the gull wing defect (Figure 1b) develops in the spalled surface. Pin holes and circular depth depressions in the nickel stressor layer result in gull wings in these samples. We find that gull wing defects are distributed across spalled wafers at random locations.

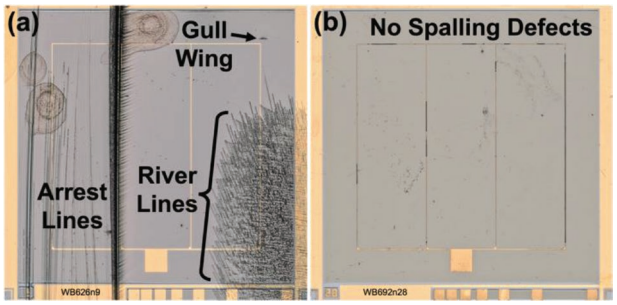

Figure 3. Optical micrographs of cells grown on spalled wafers a) with multiple types of spalling-related defects and b) without spalling-related defects. Note that the cell with no spalling defects contains growth-related hillock defects and residue from cell processing.

The range of spall-related morphologies, including arrest lines, river lines, and gull wings, results in wafers with inhomogeneous surface topology. **Figure 2** shows optical micrographs of a wafer following edge-to-edge electroplating and controlled spalling (Figure 2a), epitaxial growth (Figure 2b), and device processing (Figure 2c). The center of the wafer is largely free of morphological defects, while regions along the edge contain river lines and other defects. In particular, the wafer edges parallel to the spalling

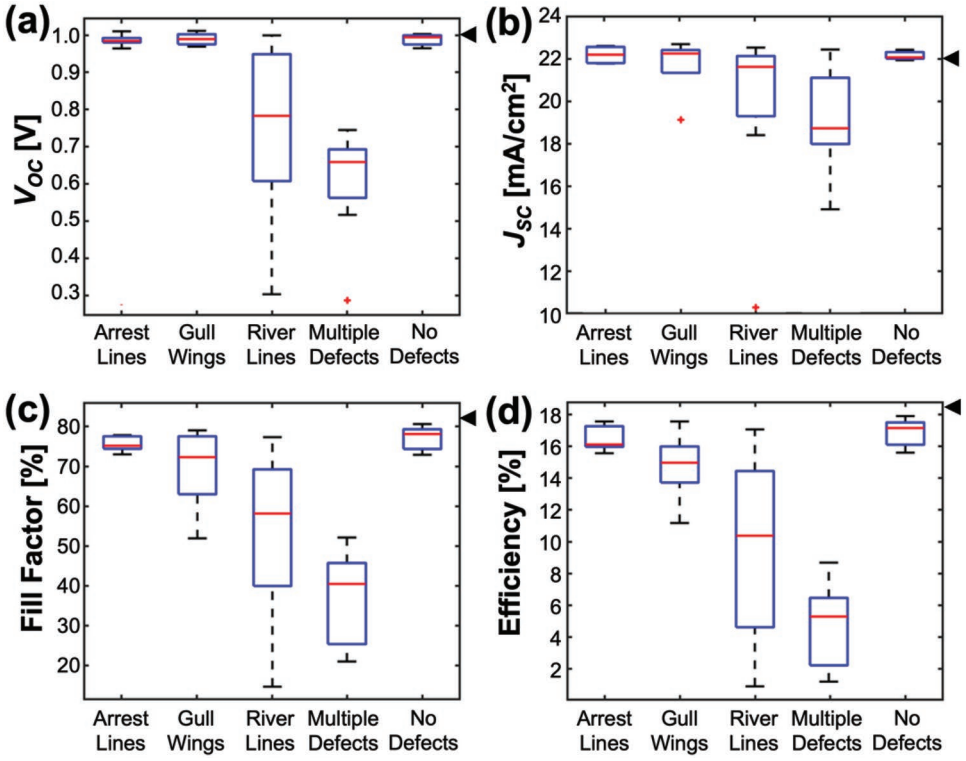

Figure 4. Boxplots of a) V_{OC}, b) J_{SC}, c) FF, and d) efficiency for 49 devices on one wafer (Figure 2c) binned into cells containing only one type of spalling-related defect (arrest lines, gull wings, or river lines), multiple defects, and no observable defects (red line: median; blue box: 25th–75th percentiles; +: outliers; whiskers: most extreme data without outliers; ◄: average value of control cells grown on epi-Ge).

direction show noticeably worse morphology than the top and bottom edges due to the presence of river lines. Two major arrest lines are also present in the top-left of the wafer. Epitaxial growth of III–V device structures results in very similar surface morphology to the initial spalled wafer surface, but with slightly more pronounced apparent roughness in the regions containing river lines. This non-ideal growth behavior is likely due to different growth rates on the various surfaces exposed when river line defects are created. Solar cell devices patterned and processed across the majority of the wafer provide an array of individual devices, each containing distinct features related to the initial spalled surface. This large array of small cells allows for a systematic investigation of the impact of various spalling-related morphologies, in isolation or in combination, on device performance.

Closer examination of the appearance of different predominant defects on this wafer allows us to begin to determine the effect each has on device performance. We characterized each of the devices shown in Figure 2 and categorized them depending on the types of defects that were present by close examination of high-resolution optical micrographs. The representative optical micrographs in **Figure 3** show various types of morphological defects that arise from spalling (Figure 3a) as well as a defect-free cell (Figure 3b). We measured *J–V* characteristics of 49 devices spanning the entire area of the sp-Ge wafer shown in Figure 2c to investigate the impact of these morphological defects on solar cell performance. Figure S2, Supporting Information shows a cell efficiency heat map for this sp-Ge wafer. We binned all devices into groups depending on the types of defects that were present, as observed by optical microscopy. **Figure 4** shows box plots summarizing the distributions of device figures of merit, including open-circuit voltage (V_{OC}), short-circuit current density (J_{SC}), fill factor (FF), and efficiency (η), for devices containing only one type of morphological defect, multiple types of defects, and no observable defects. Devices with only one type of morphological defect allow for isolated study of defect-performance relationships. *J–V* characteristics from the cells on this wafer containing only arrest lines generally show minimal impact on the V_{OC} and J_{SC} of the devices, in contrast to our earlier work that noted significant shunting in the presence of arrest lines;[30] Section 2.1 explains the nuances in the performance of devices with arrest lines in detail. Devices showing only gull wing defects also exhibit minimal impacts on V_{OC} and J_{SC}, whereas river lines result in a range from slight to significant device performance degradation. Cells that exhibited multiple defects show decreases in all performance metrics. Device performance is unaffected for cells with no spalling-related defects present and is similar to devices grown on epi-Ge wafers with the same structure. The following sections focus on the specific performance-limiting mechanisms introduced by each of these spalling defects.

2.1. Impact of Arrest Lines

Arrest line impact on device performance can vary from minimal (as in Figure 4) to complete shunting of the device depending on the severity of the arrest line morphology.[30] The most evident indicator of arrest line severity is the height profile across the arrest line. Vertical step heights across arrest lines can range from less than 100 nm for "minor" arrest lines often seen in controlled spalling to tens of micrometers for "major" arrest lines due to unintentional spontaneous spalling. **Figure 5**a shows representative height profiles for minor, intermediate, and major arrest lines. Corresponding *J–V* measurements from representative cells containing these different arrest line morphologies (Figure 5b) exhibit decreases in all performance metrics as arrest line severity increases. Cells grown over minor arrest lines exhibit very minimal shunting and no significant decreases in V_{OC} or J_{SC} compared to defect-free cells. Note that the "arrest lines only" cells reported in Figure 4 contained only minor arrest lines and therefore displayed good performance. Cells grown over intermediate arrest lines show more pronounced shunting (indicated by increasing positive slope from 0 to 0.6 V) and noticeable decreases in both V_{OC} and J_{SC}. *J–V* characteristics of cells grown over major

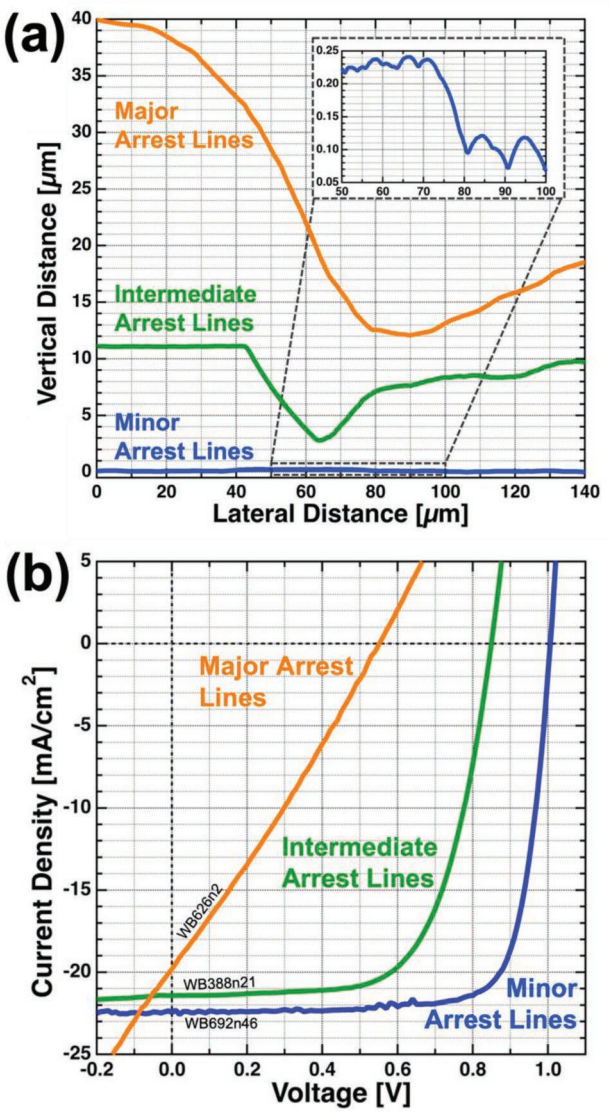

Figure 5. a) Representative height profiles of major, intermediate, and minor arrest lines (offset for clarity) and b) representative *J–V* characteristics of solar cells grown over the different severities of arrest lines.

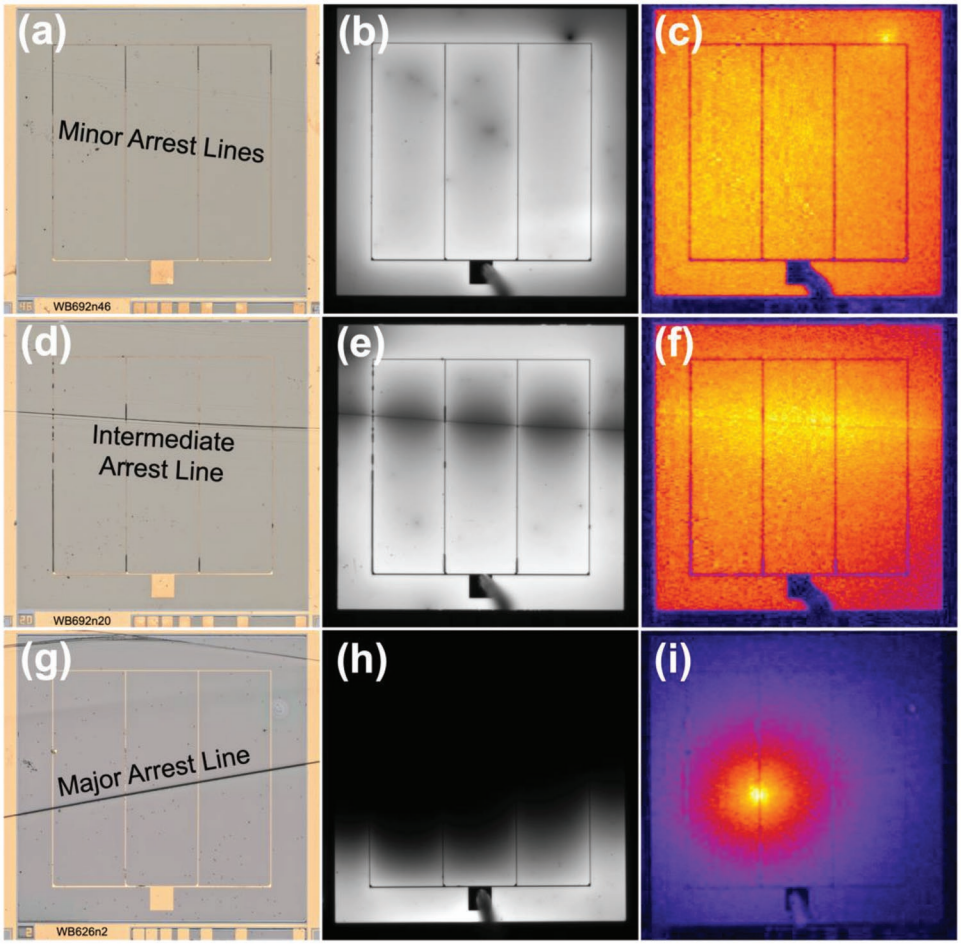

Figure 6. a) Optical micrograph of cell grown over minor arrest lines with corresponding b) EL and c) DLIT images displaying minimal impact on device performance (nominally uniform intensity across entire cell area). d) Optical micrograph of cell grown over an intermediate arrest line with corresponding e) EL and f) DLIT images revealing increased non-radiative recombination in the material on and around the arrest line. g) Optical micrograph of cell grown over a major arrest line with corresponding h) EL and i) DLIT images showing that the top half of the cell is electrically disconnected from the bottom and a heavily shunted current pathway is formed where the arrest line intersects the second grid line from the left.

arrest lines exhibit significant degradation in V_{OC} and J_{SC} and indicate fully shunted devices.

EL and DLIT imaging provides further visual evidence of defective regions and device shunts formed during growth over arrest lines that result in the degraded cell performance observed in corresponding J–V measurements. Cells grown over minor arrest lines (**Figure 6**a) show a very slight decrease in EL intensity around the arrest lines (Figure 6b) and no discernible features in DLIT (Figure 6c). The darker and brighter spot in the top-right of the EL and DLIT images, respectively, is due to extrinsic contamination and is not associated with any spalling-related defect. Note that DLIT image intensity is auto-scaled, so although the image appears bright, the uniform intensity across the entire cell area implies a homogeneous device with no observable regions of increased shunting. These results agree with the J–V measurements (Figure 4) exhibiting performance metrics comparable to cells grown on regions of sp-Ge wafers containing no defects. Cells grown over more pronounced intermediate arrest lines (Figure 6d) exhibit darker contrast in EL, indicating that these deeper features act as regions of increased non-radiative recombination (Figure 6e). The EL data also show that the impact of the arrest lines extends some distance away from the line itself, suggesting that the material grown around them is more defective. DLIT also shows heating due to localized shunting within a few mm-wide region around the intermediate arrest lines, with highest intensity at a cell gridline intersection (Figure 6f). This localized heating supports the conclusion that carriers non-radiatively recombine in this area, consistent with the EL data. Cells grown over the most severe major arrest lines (Figure 6g) result in large areas of the device being electrically disconnected, which then cannot contribute to carrier collection leading to a dramatic decrease in cell efficiency. A completely dark EL signal in the region of the device on the opposite side of the arrest line from where the probes contact the device (Figure 6h) confirms an electrical disconnection across the major arrest line. This electrical isolation is due to discontinuities in the epitaxial growth and/or grid lines across the arrest line. DLIT measurements show a localized, intense signal where this major arrest line intersects a gridline (Figure 6i), revealing a heavily shunted, parasitic current pathway through the device that further reduces

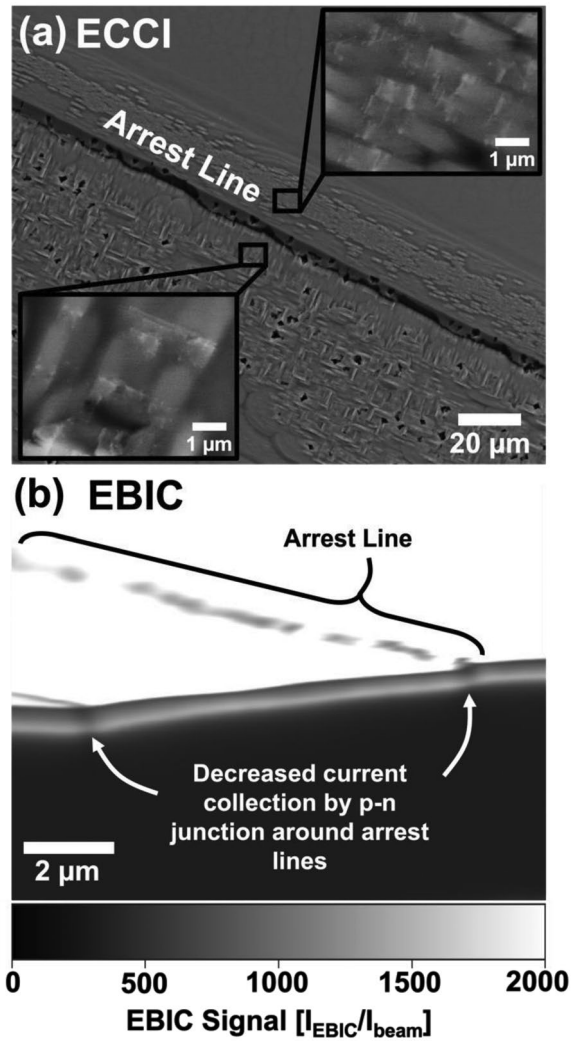

Figure 7. a) Plan-view ECCI micrograph centered on an intermediate arrest line with zoomed-in insets of representative areas revealing high defect densities ($\approx 1.3 \times 10^8$ cm^{-2}) in the surrounding material. b) Tilted cross-sectional EBIC image showing decreased current collection efficiency around regions of p-n junction grown above an intermediate arrest line.

cell performance. Arrest line morphology may have minimal impact on device performance if the height profile across the arrest line is shallow enough such that the growth of epitaxial device layers remains continuous. However, as the height of an arrest line increases, opportunities arise for disrupting the conformal growth of device layers, which may introduce crystalline defects and/or shunt pathways between layers that degrade device performance.

The defective nature of device material grown near arrest lines was characterized with plan-view ECCI and cross-sectional EBIC imaging to better understand the decreases in V_{OC} and J_{SC} exhibited by cells grown over arrest lines. ECCI shows a high density ($\approx 1.3 \times 10^8$ cm^{-2}) of threading dislocations (bright dots) and stacking faults (bright lines) in the vicinity of arrest lines (**Figure 7**a), both of which are capable of acting as non-radiative recombination centers and provide evidence to explain the lower V_{OC} values of cells grown over arrest lines.[32] Cross-sectional EBIC (Figure 7b) reveals decreased current extraction of the p-n junction in regions of the device grown above intermediate arrest lines. These regions of decreased carrier collection efficiency provide direct evidence for the negative impact arrest line defects have on the J_{SC} of cells grown over areas of sp-Ge wafers containing arrest lines.

2.2. Impact of Gull Wings

Gull wing defects have a minor impact on device performance, causing only a localized increase in non-radiative recombination and sometimes shunting, unless there is interaction with grid lines. Isolated gull wings (**Figure 8**a) show up as dark features in EL imaging (Figure 8b), indicating a localized increase in non-radiative recombination in material grown around the gull wing defect. DLIT (Figure 8c) shows slightly increased and diffuse intensity in the lower-left of the cell with no indication of a shunt pathway localized to the gull wing. Other gull wing defects (Figure 8d) distinctly show localized shunting in DLIT (Figure 8e), but those that intersect grid lines cause complete shunting of the device as indicated by the *J*–*V* characteristics shown in Figure 8f.

We employed ECCI to look for crystalline defects to better understand the nature of device growth over gull wing defects. A representative plan-view SEM micrograph (**Figure 9**) of a device structure grown on a gull wing shows a non-ideal and rough morphology characteristic of the underlying gull wing defect. ECCI measurements on a zoomed-in region reveal a high density ($\approx 1 \times 10^8$ cm^{-2}) of stacking faults and threading dislocations within a 50–150 µm radius from the center of the gull wing defect. This high defect density and its associated increase in non-radiative recombination explain the localized dark contrast observed around gull wings in EL imaging. Although the crystalline defect density around gull wings is very high, the overall density of gull wing defects themselves is quite low across an entire wafer and the defects themselves are small, resulting in a minor impact on device performance due to non-radiative recombination when gull wings are isolated. The chasm in the growth around the gull wing (a representative height profile is shown in Figure S3, Supporting Information) is substantially disruptive to cell performance if it is collocated with a grid line, possibly due to a discontinuity created in the grid line across the gull wing and/or Au electroplated on the sides of exposed device layers and shunting the device.

2.3. Impact of River Lines

River line defects, in contrast to arrest lines and gull wings, have much sharper features with step heights of hundreds of nanometers over sub-micron lateral distances,[28] and display a less nuanced effect on device performance—they have a consistently greater negative impact. The *J*–*V* parameter distributions shown in Figure 4 indicate that river lines are the most detrimental defects observed in this study. Most notably, cells containing river lines exhibited dramatically lower V_{OC}, with a ≈0.2 V drop in the median V_{OC}, compared to cells with arrest

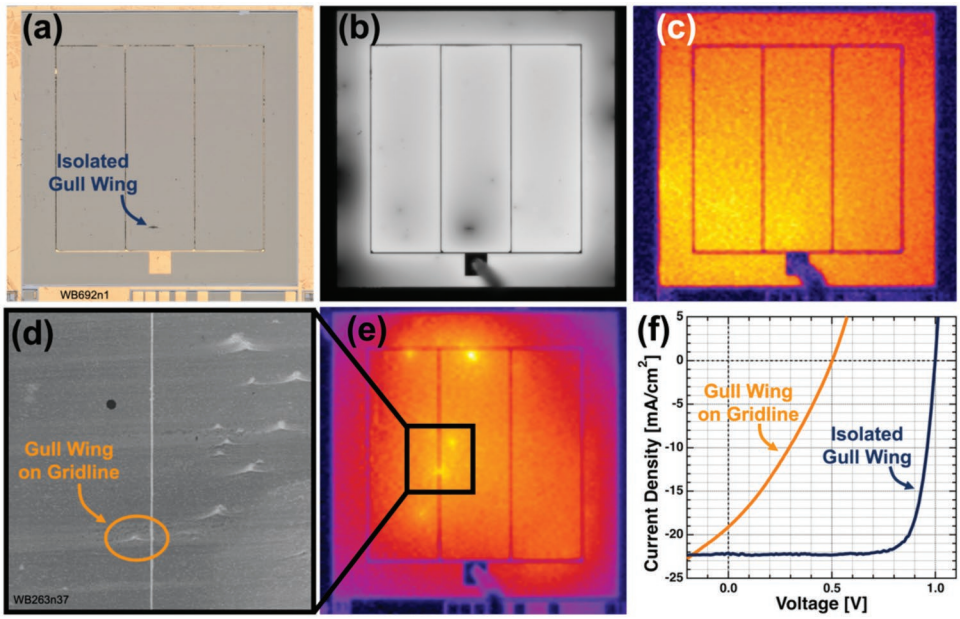

Figure 8. a) Optical, b) EL, and c) DLIT images for a cell with isolated gull wing. d) Optical image of a gull wing interacting with a gridline and e) DLIT image of the corresponding cell. f) *J–V* characteristics showing the negligible impact of the isolated gull wing defect in (a–c) compared to the gull wing on the gridline in (d,e) that resulted in a major shunt and significantly degraded device performance.

lines or gull wings. Optical micrographs of the cells containing only river line defects reveal a direct correlation between the amount of cell area impacted by river lines and the extent of degraded cell performance. In prior work, we showed that river lines coarsen with distance from unaffected areas, thus an increase in step height happens concurrently with increased area coverage.[28] As the fractional cell area containing river lines increases, the V_{OC}, J_{SC}, FF, and consequently the efficiency all decline, as shown by the representative optical micrographs and corresponding *J–V* curves in **Figure 10**.

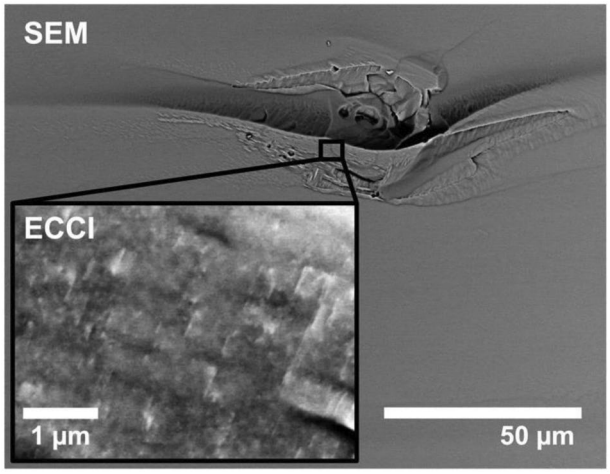

Figure 9. Plan-view SEM micrograph of a device structure grown over a gull wing. Inset: zoomed-in ECCI micrograph of a representative area surrounding the gull wing revealing a high density ($\approx 1 \times 10^8$ cm^{-2}) of stacking faults (bright lines) and threading dislocations (bright dots).

We further characterized a cell that is fully covered in river line defects (**Figure 11**a) with EL and DLIT to better understand the impact of river lines on device performance. The two pronounced circular defects were not observed on the initial spalled surface and appeared only after growth and are therefore likely due to extrinsic contamination introduced during sample handling. In EL imaging (Figure 11b), the cell exhibits higher intensity only in close vicinity to the grid lines and is darker everywhere else. This indicates poor minority carrier diffusion length in the device and suggests greater degrees of non-radiative defect-assisted recombination and parasitic losses due to series and/or shunt resistances. This is supported by the DLIT imaging (Figure 11c) that shows relatively uniform heating, indicating significant non-radiative recombination occurring across the entire spatial area of the device. We used FIB milling to prepare a cross section from a region of the device containing river lines to better understand how these shunts originate. Cross-sectional SEM imaging (Figure 11d) shows that growth proceeds non-uniformly above river line defects resulting in even more pronounced roughness from pile-up during growth of the lateral conduction layer. Growth perturbations likely continue throughout the remainder of the device structure, but the mass contrast in the micrograph is not enough to resolve the thin layers above the base layer. The roughness due to this non-planar and non-conformal growth (>200 nm step height) is on a similar length scale as the thickness of some of the thinner device layers (color-coded in Figure 11d), particularly the emitter (100 nm) and window layers (20 nm) (see detailed device structure in Experimental Section). Disrupted growth of these layers could lead to cell degradation by introducing possible shunt pathways, unintentional p-n junctions, and detrimental crystalline defects. Indeed, *J–V* curves for other devices containing more severe river lines display evidence of negative differential

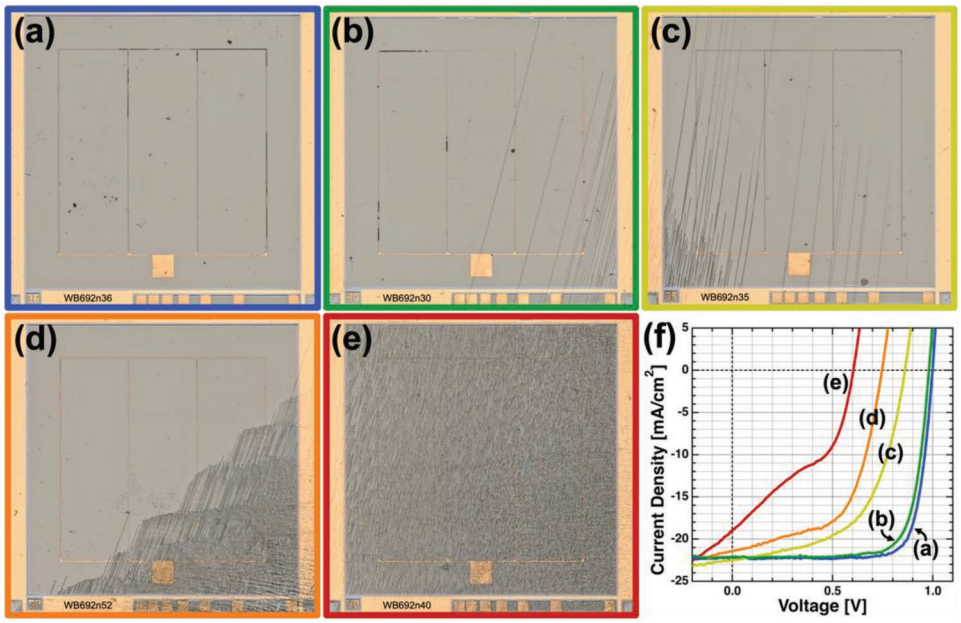

Figure 10. Optical images of solar cells grown over areas of a sp-Ge wafer containing a) no river lines and b–e) increasing fractions of cell area containing river lines along with f) corresponding *J–V* characteristics showing the relationship between cell degradation and river line coverage area.

resistance (Figure S4, Supporting Information) typically associated with tunneling effects. This supports the idea that the disrupted epitaxy could allow different device layers to come in contact across the disruption and provide a shunt pathway through the device.

We assessed the crystalline quality of device structures grown over river line defects using ECCI. Figure 11e shows a representative plan-view SEM micrograph of a region of a device containing multiple river lines along with a zoomed-in ECCI micrograph (Figure 11f) revealing a high density of stacking

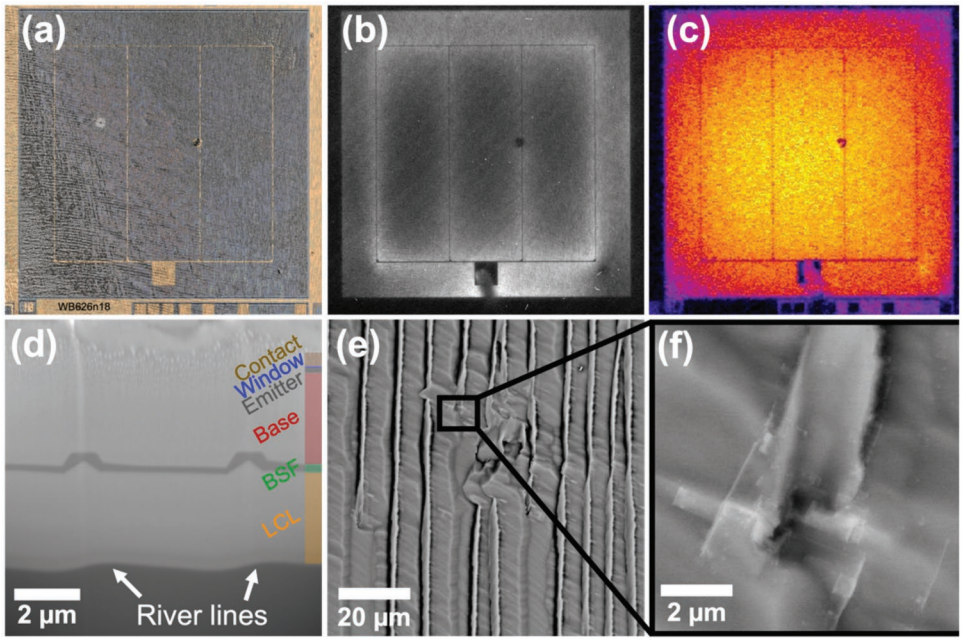

Figure 11. a) Optical, b) EL, and c) DLIT images for a cell grown over river lines. d) Cross-sectional SEM showing non-uniform growth above river line defects. The color-coded device layers are roughly to scale. e) Plan-view SEM of a cell grown over river lines (vertical linear features) with a representative region analyzed by f) ECCI showing a high density ($\approx 8 \times 10^7$ cm^{-2}) of stacking faults and threading dislocations generated during growth over river lines.

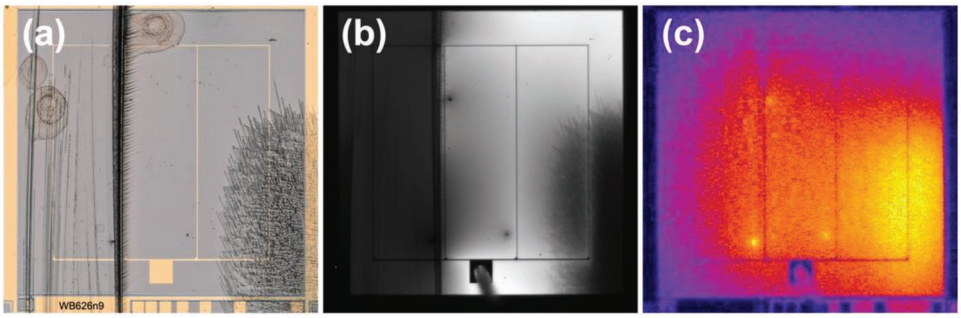

Figure 12. a) Optical, b) EL, and c) DLIT images for the cell containing multiple defects—a major arrest line (dark vertical line toward left-side) that cuts off current flow to the left third of the cell, river lines in the bottom-right that cause shunting seen in DLIT, and a gull wing defect in the top right that shows up dark in EL.

faults and threading dislocations generated in the areas surrounding the river lines. We measured an average defect density of $\approx 8 \times 10^7$ cm^{-2} from this representative area. Although the defect density surrounding river lines is similar to that of arrest lines and gull wings, the typically higher densities of river lines themselves lead to substantially more defective area in cells where river lines occur. In turn, these high defect densities are significant enough to degrade the V_{OC} and J_{SC} of solar cell devices to the corresponding values reported in Figure 4a,b.[33] These crystalline defects may arise from discontinuities in epilayer growth due to the sharp and steep height profiles of the river lines. Another possible source of defects is non-planar growth causing compositional variations in the growing epilayer that lead to local regions of lattice mismatch which generate dislocations to relieve strain.

2.4. Performance of Cells with Multiple Spalling-Related Defects

Cells listed in Figure 4 as "multiple defects" contain multiple types of the three defects—arrest lines, gull wings, and river lines—within the cell area and behave similarly to the bottom distribution of devices containing only river lines. All multiple defect cells reported in Figure 4 contained river lines, further indicating that river lines are the dominant spalling-related defect in terms of device degradation.

We characterized a representative cell containing all three of these spalling defects (**Figure 12**a) with EL and DLIT. Each defect type exhibited the same characteristic features seen in the previous sections studying the individual defects. The major arrest line running vertically toward the left-side of the cell effectively cuts off current flow to the rest of the cell, as shown by the dark area in EL (Figure 12b). The bottom-right region containing river lines displays the greatest degree of shunting in DLIT imaging (Figure 12c) and shows an increase in non-radiative recombination (darker in EL) in the river line region, which is consistent with the higher defect density expected in this area. A gull wing defect is present in the top-right of the cell just above the gridline and shows up as a dark feature in EL, as expected from a region of increased non-radiative recombination due to a high local crystalline defect density. The gull wing is not visible in the DLIT image due to autoscaling of the intensity data and its signal being drowned out by the nearby area containing river lines. As expected, *J–V* characteristics (Figure S4, Supporting Information) show that the performance of this cell is severely degraded due to the presence of these spalling-related defects.

2.5. Performance of Cells without Spalling-Related Defects

Cells with no morphological spalling defects exhibited consistently high values of cell performance parameters (see Figure 4). Additionally, ECCI micrographs acquired in regions of devices containing no spalling defects (Figure S6, Supporting Information) did not exhibit any signs of crystalline defects. Furthermore, these cells performed nearly equivalently to cells grown on epi-Ge wafers, indicating that a sp-Ge surface free from spalling defects does not require any polishing or repreparation steps prior to epitaxial growth. Application of an anti-reflective coating coating further improved the device performance (**Figure 13**), resulting in a certified power conversion efficiency

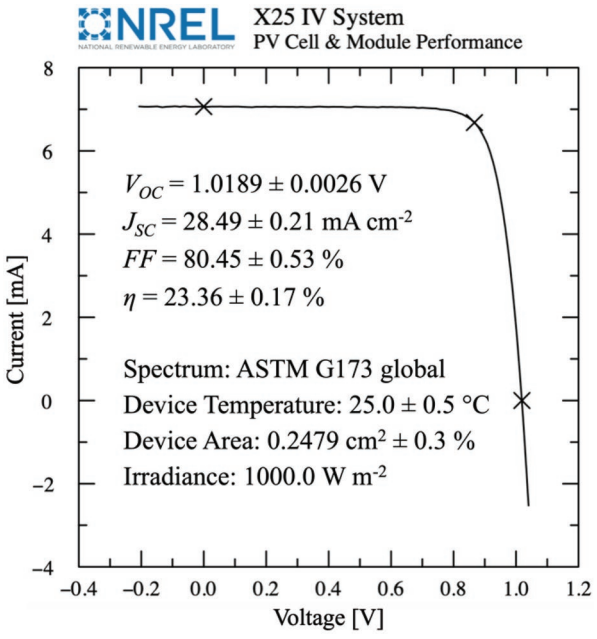

Figure 13. Certified *J–V* characteristics of the highest performing cell grown on sp-Ge with an ARC exhibiting a power conversion efficiency of 23.36%.

Table 1. Cell performance parameters for single-junction GaInAs solar cells on sp-Ge with the highest performance as well as average parameters for cells on defect-free sp-Ge and cells on epi-Ge. All cells have an anti-reflective coating.

	V_{OC} [V]	J_{SC} [mA cm^{-2}]	FF [%]	η [%]
Highest performance cell on sp-Ge (WB692n10, certified)	1.019	28.49	80.45	23.36
Average of 8 cells on defect-free sp-Ge (+/− st. dev.)	1.000 +/− 0.013	28.78 +/− 0.18	76.9 +/− 2.8	22.14 +/− 1.05
Average of 24 cells on epi-Ge (+/− st. dev.)	1.012 +/− 0.015	29.38 +/− 0.17	80.2 +/− 2.8	23.86 +/− 1.20

of 23.36% with V_{OC} of 1.0189 V, J_{SC} of 28.49 mA cm^{-2}, and FF of 80.45%.

Table 1 summarizes the metrics from the device in Figure 13 along with average performance metrics of the eight cells grown on the sp-Ge wafer shown in Figure 2 that contained no spalling-related defects. Table 1 also shows average performance metrics of 24 cells grown on epi-Ge for comparison. The main cause of lower efficiencies in cells grown on sp-Ge relative to epi-Ge is decreased fill factor. Comparing light and dark J–V characteristics (Figure S7, Supporting Information) between cells on sp-Ge and epi-Ge indicates a slight increase in series resistance and decrease in shunt resistance, both of which contribute to lowering the fill factor. These parasitic resistances might be attributed to a variety of factors, whether intrinsic or extrinsic to the sp-Ge surface, for example, any spalling defects that may not be detectable by optical microscopy or inconsistencies in cell processing.

3. Conclusions

We showed how various morphological defects originating from controlled spalling impact the performance of GaInAs solar cell devices grown on unpolished surfaces of spalled Ge wafers. We associated each spalling defect type with a distinct impact to cell behavior and performance using a variety of functional and physical characterization techniques. Gull wings only have a significant impact on device performance when they intersect a gridline, which results in complete shunting of the device. However, the density of gull wing defects is relatively low. The impact of arrest lines depends on the severity of their height profiles, ranging from negligible to complete shunting and significant decreases in J_{SC}, V_{OC}, and FF. River lines consistently lead to decreases in V_{OC}, J_{SC}, and FF with the extent of degradation based on the cell area fraction containing them and are associated with a localized high density of threading dislocations and shunting. In general, the degree to which device performance suffers correlates strongly with increases in step height and steepness of the morphological spalling defect. In cases where height perturbations are severe enough to disrupt the continuous growth of device layers, detrimental shunt pathways and crystalline defects are introduced that degrade device performance. We demonstrated the growth of high-efficiency devices on regions of spalled Ge wafers free from spalling defects that exhibited efficiencies up to 23.4%, which were comparable to devices grown on epi-ready Ge wafers. A greater yield of high-quality devices can be grown on spalled Ge wafers without the need for polishing or other surface preparation steps if the electroplating and spalling procedure is further optimized to reduce formation of major arrest lines and river lines. Meanwhile, growth procedures should also be optimized to further improve starting morphology prior to device layers, such as smoothing growth conditions, as well as other device structures that may prove to be more robust to the types of morphological defects associated with spalling.

4. Experimental Section

All controlled spalling work utilized 50.8 mm-diameter p-type Ge (001) substrates with a 6° offcut toward <111>. Substrates were treated in a 2:1:10 solution of NH_4OH:H_2O_2:H_2O for 1 min prior to the electrodeposition of a Ni stressor layer. Galvanostatic electrodeposition of a Ni stressor layer across the entire wafer was performed in a 0.6 M $NiCl_2{\cdot}6H_2O$, and 0.005 M H_3PO_3 solution at 60 °C using current densities from 30 to 60 mA cm^{-2} and deposition times from 3 to 6 min. We used an electroplating fixture that allows Ni deposition across the entire wafer surface by holding the wafer in place by vacuum and making electrical contact on the back of the substrate. An adhesive film was laminated to the electroplated Ni surface by hand, taking care to avoid trapped air bubbles and the wafer was held fixed by a vacuum chuck. Spalling was initiated by applying an external force to the edge of the adhesive film and an upward force was applied by hand or with the use of a linearly-actuated single roller device described in refs. [13,21]. The spalled films that were removed from the wafer were not used in this work. The resulting spalled wafers were used for the regrowth experiments described below. Prior to growth, all spalled Ge wafers were immersed in Transene TFG etchant to remove any residual nickel, followed by an acetone/isopropanol solvent rinse. Samples were finally cleaned by etching in a 2:1:10 solution of NH_4OH:H_2O_2:H_2O for 1 min just prior to loading into the growth reactor.

III–V device structures were grown in an atmospheric-pressure OMVPE reactor using arsine and phosphene group V sources, trimethylgallium and trimethylindium group III sources, and hydrogen selenide and diethylzinc dopant sources. Solar cell structures were deposited on both commercial, epi-ready Ge wafers and the wafers that resulted from the controlled spalls on full 50.8 mm-diameter wafers. The Ge substrates were heated to 700 °C under hydrogen and held for 10 min for in situ oxide desorption. The device structure (**Figure 14**) consisted of a 2 µm-thick, Zn-doped $Ga_{0.99}In_{0.01}As$ lateral conduction layer followed by a $Ga_{0.5}In_{0.5}P$ back surface field layer, a p-type GaInAs base, n-type GaInAs emitter, a two-layer GaInP/AlInP window, and a GaInAs top contact layer.

Following growth, 5 mm × 5 mm solar cell devices were defined using contact photolithography. Shipley S1818 positive broadband photoresist was spun on at 4000 rpm and baked at 100 °C for 5 min. Ni/Au front contact grids were defined first and electroplated using a Watts nickel solution and a sulfite-based gold solution, respectively. Next, the GaInAs contact layer was removed by etching in a 2:1:10 solution of NH_4OH:H_2O_2:H_2O. This was done before device isolation to prevent unwanted etching of the GaInAs lateral conduction layer. A gold layer was subsequently electroplated onto the lateral conduction layer at the bottom of the III–V structure to act as the back contact. After initial electrical characterization, a MgF_2 (1 nm)/ZnS (≈45 nm)/MgF_2 (≈50 nm) antireflection coating (ARC) was deposited onto the completed structure using thermal evaporation. Note: identifiers

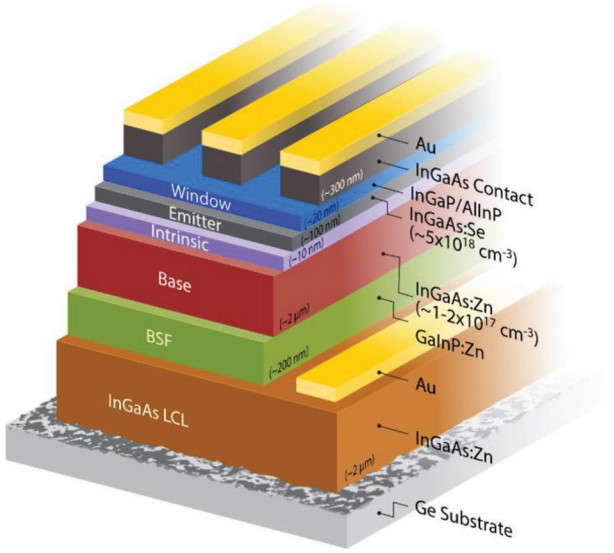

Figure 14. Schematic of single-junction GaInAs solar cell structure grown on spalled and epi-ready germanium wafers.

for wafers, samples, and cells are included in the figures for internal reference.

A combination of spatially resolved physical and functional characterization techniques were used to identify and study performance-limiting morphological defects in devices grown on sp-Ge wafers. Nomarski optical microscopy and laser scanning confocal microscopy (Keyence 6000) were used to confirm the presence of various spalling-related defects prior to growth, after growth, and after cell processing. Spatially-resolved EL imaging and DLIT characterization were used to correlate defect morphology with device performance. DLIT measurements were performed using a 532 nm laser diode in a custom set-up described previously.[34] *J–V* performance was measured on a XT10 solar simulator, calibrated to the AM1.5G spectrum at 1000 W m^{-2}. Certified *J–V* measurements were acquired independently by the Cell & Module Performance group at NREL using the NREL X-25 IV system and the NREL Grating QE system for spectral mismatch correction. Cross-sectional scanning electron microscopy (SEM) was performed using a FEI Helios Nanolab 600i dual beam SEM/focused ion beam (FIB). To expose cross sections for imaging, the sample was tilted to 52°, perpendicular to the ion beam, and a trench was milled in the region of interest using the FIB. The exposed cross-sectional surface was then imaged with tilt-correction using the SEM in secondary electron imaging mode. Electron channeling contrast imaging (ECCI) was performed using a vCD backscatter detector inserted underneath the polepiece on a FEI Nova NanoSEM 630 operating at 25 kV accelerating voltage and 3.2 nA beam current. Defect densities were calculated from ECCI micrographs by counting the number of defects within at least 446 μm^2 of imaging area. Electron beam-induced current (EBIC) measurements were performed using a JEOL JSM-7600 FESEM and Mighty EBIC quantitative EBIC system. SEM images and EBIC images were acquired simultaneously. An electron beam accelerating voltage of 5 kV and ≈1 nA beam current were used for the EBIC measurements in cross section orientation. Samples were prepared by cleaving and then ion milling using 4 kV Ar^+ ions resulting to produce a smooth cross section surface.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

III–V, cost reduction, germanium, spalling, substrate reuse

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