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All-Back-Contact Perovskite Solar Cells Using Cracked Film Lithography

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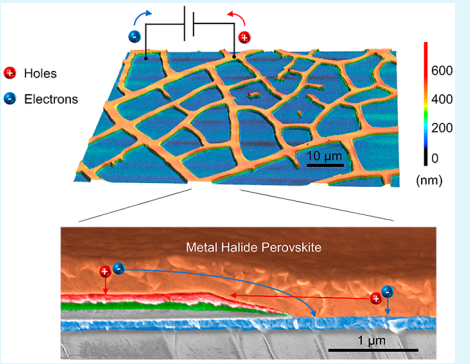
ABSTRACT: All-back-contact perovskite solar cells promise greater power conversion efficiency compared to conventional planar device architectures. However, the best-performing devices to date use photolithography to fabricate electrodes, which is expensive for deployment and a barrier for research facilities. Herein, we utilize cracked film lithography, a solution-processed micropatterning technique, to form an interconnected, defect-tolerant back-contact electrode network. We introduce a crack widening technique to control the optical transparency and sheet resistance while decoupling the relative areas of the electron and hole contacts in the back-contact network. Wider cracks increase the area of the hole-selective contact, which increases photocurrent and power conversion efficiency.



KEYWORDS: *scalable fabrication, cracked-film lithography, perovskite, solar cells, all-back-contact, quasi-interdigitated, back-contact electrodes*

Scalable thin-film solar cells are vital to transition to a sustainable energy future. Perovskite solar cells (PSCs) promise a low-cost and low-energy-input renewable energy source due to the ideal photovoltaic properties of perovskite materials[1−3] and large-scale, rapid solution processability.[4,5] Lab-scale PSCs have reached a certified power conversion efficiency (PCE) >25% based on planar device architectures.[6] Planar devices sandwich the perovskite absorbing layer between electron and hole selective contacts through sequential thin-film depositions similar to existing thin film photovoltaic technologies. Although planar PSCs hold great promise, they still face several challenges, including unrealized high efficiency, long-term stability, and scalability.

All-back-contact (ABC) architectures, which include interdigitated and quasi-interdigitated back contact geometries, pattern both the electrode and hole selective contacts on one-side of the absorber to offer several benefits. First, numerical models predict that ABC architectures have the potential to outperform their conventional planar counterparts, due to the mitigation of reflection and absorption of the semitransparent charge transport layers required in planar architectures.[7−9] Second, the free perovskite surface allows passivation techniques that do not require charge transport, opening the door to alternative insulating layers not possible in planar architectures.[10,11] Third, ABCs allow each transport layer to be deposited with techniques that typically damage the perovskite layer in planar architecture fabrication such as radio frequency sputtering or atomic layer deposition (ALD), providing more options to incorporate all-inorganic contacts in PSCs. Fourth, the ABC platform creates opportunities for unique in situ characterization of the perovskite layer under operation.[12,13] Lastly, it facilitates simple recycling or remanufacturing methods by dissolving the top perovskite surface and recovering the patterned electrodes below.

To date, most ABC PSC processing is based on photolithography,[11,14−17] which serves to pattern the electrodes at the scale of the diffusion length of photogenerated carriers, typically ∼1 μm in perovskite films.[3] However, photolithography requires expensive equipment and processing methods, which is not ideal for scalable large-area manufacturing and can be a barrier to entry for many research facilities. Alternative patterning methods have been demonstrated including laser-scribing,[18] carefully aligned shadow masks,[19] network-like porous Ti,[20] embossed substrates coupled with oblique-angle evaporation,[21] and microsphere lithography.[22] The laser-scribing method is compatible with thin-film module fabrication, but the resolution of the laser beam limits the minimum gap-width between the ETL and HTL to 50 μm, resulting in low current density.[18] Greater current density was achieved at similar length scales with single crystal perovskite

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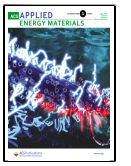

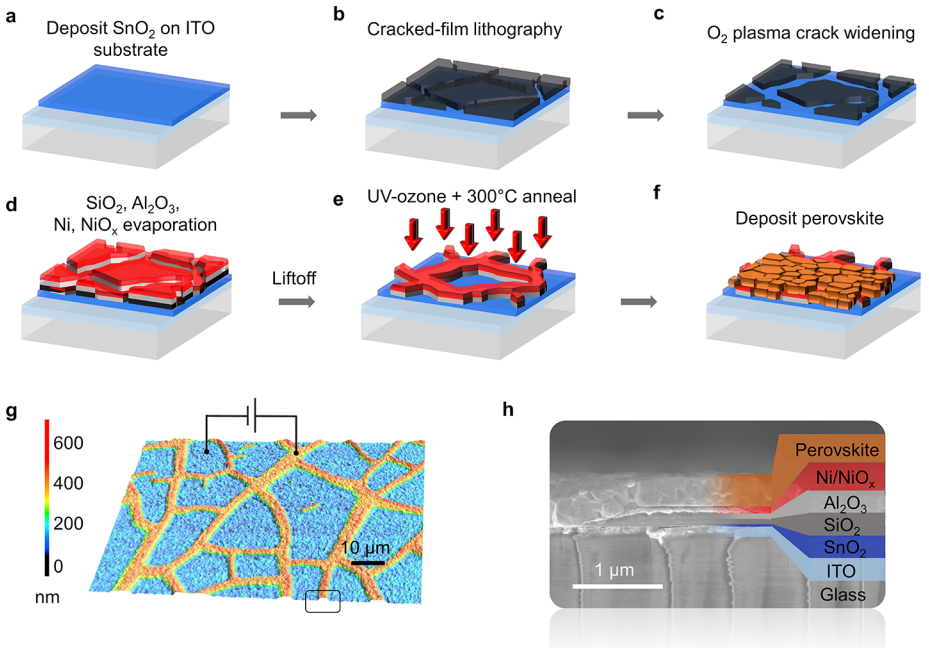

Figure 1. All-back-contact (ABC) perovskite solar cell (PSC) fabricated via cracked film lithography. (a–f) Fabrication procedure: (a) deposit planar SnO_2 electron transport layer (ETL) onto indium-doped tin oxide (ITO)-coated glass, (b) spin-coat poly(methyl methacrylate) (PMMA) nanoparticle solution and dry to form cracked film network, (c) widen channels using O_2 plasma, (d) electron-beam evaporate SiO_2, Al_2O_3, and Ni, and magnetron sputter NiO_x to form a hole transport layer contact electrically isolated from the bottom SnO_2/ITO contact, (e) liftoff PMMA to expose ETL layer followed by UV-ozone clean and anneal to prepare interfaces for perovskite deposition, (f) solution-process the perovskite layer to complete the device. (g) 3D profilometry image of a complete ABC PSC device. (h) Cross-section scanning electron microscopy (SEM) image of a completed ABC PSC device with color insets indicating each layer.

lateral-structure devices formed from the carefully aligned shadow masks method.[19] However, the lateral structure device is not a true ABC device, as it was only illuminated on the side with metal electrodes, limiting the active device area to just between the electrode gaps.[19] Network-like porous Ti structures provide submicron gaps[20] but require a thick mesoporous TiO_2 layer on the illuminated side potentially limiting current and causing ultraviolet (UV) light-activated perovskite degradation similar to planar devices.[23] V-shaped, groove-embossed substrates coupled with oblique-angle evaporation creates a flexible back-contact micromodule, but the areal PCE suffers from dead areas between each groove.[21] Microsphere lithography is perhaps the most promising. It provides solution-based patterning with tunable geometry by changing the surface coverage via sphere diameter and surface functionalization, but PCE remains limited.[22] Additional simple solution-processed patterning methods with controllable ETL and HTL domains is desirable for low-cost and scalable ABC electrode fabrication.

Cracked film lithography (CFL) is a scalable technique that generates a microscale interconnected crack pattern. A nanoparticle suspension is deposited onto a substrate using solution processing techniques such as drop-coating,[24] spin-coating,[25] or blade-coating.[26] Subsequent solvent evaporation contracts the film volume, inducing stress in the film. The stress is relieved by the formation of cracks.[27] The self-assembled crack network forms an inverted and interconnected template for subsequent film depositions. The cracked nanoparticle film is lifted off to yield metal grids for transparent conducting electrode applications with high transmittance and low sheet resistance.[25,28] Rao et al. was the first to incorporate CFL into solar cells as a transparent conducting electrode and demonstrated comparable performance to conventional indium-doped tin oxide (ITO)-based cells.[29] It has since been incorporated into various solar cell architectures[30−34] and has demonstrated a high power conversion efficiency of 24.7% in GaAs solar cells.[35]

Herein, we use CFL to form ABC electrodes for perovskite solar cells. Whereas most CFL studies increase template thickness to simultaneously widen cracks and crack spacing, here we develop a crack widening method to decouple crack width from spacing. Widening the crack network adjusts the ratio of the electron- and hole-selective contact areas, which alters the back-contact electrode transparency, sheet resistance, perovskite charge transport, and final device performance.

The CFL ABC fabrication process follows previous substrate liftoff approaches,[14,16] but we replace the sacrificial photolithography mask with the solution-processed cracked film (Figure 1a–f). We utilize a quasi-interdigitated architecture, which allows one selective contact to be deposited as a planar film, like traditional architectures, and the other to be patterned and electrically isolated by an insulator. The one patterning step required in this design simplifies the overall process and requires no alignment. We start by solution processing a planar SnO_2 electron transport layer (ETL) above an ITO coated glass substrate (Figure 1a). SnO_2 has high thermal stability, proper band alignment, enhanced electron extraction, and reduced charge accumulation at the interface in PSCs.[36] We spin-coat a poly(methyl methacrylate) (PMMA) nanoparticle solution onto the SnO_2 ETL layer and let it dry in air to form the cracked film lithography pattern (Figure 1b). We control crack widths by introducing an oxygen plasma widening step (Figure 1c). We electron-beam evaporate the insulating bilayer of SiO_2 and Al_2O_3 to ensure high shunt resistance between contacts,[16] which is followed by Ni and NiO_x deposition to form the hole selective contact (Figure

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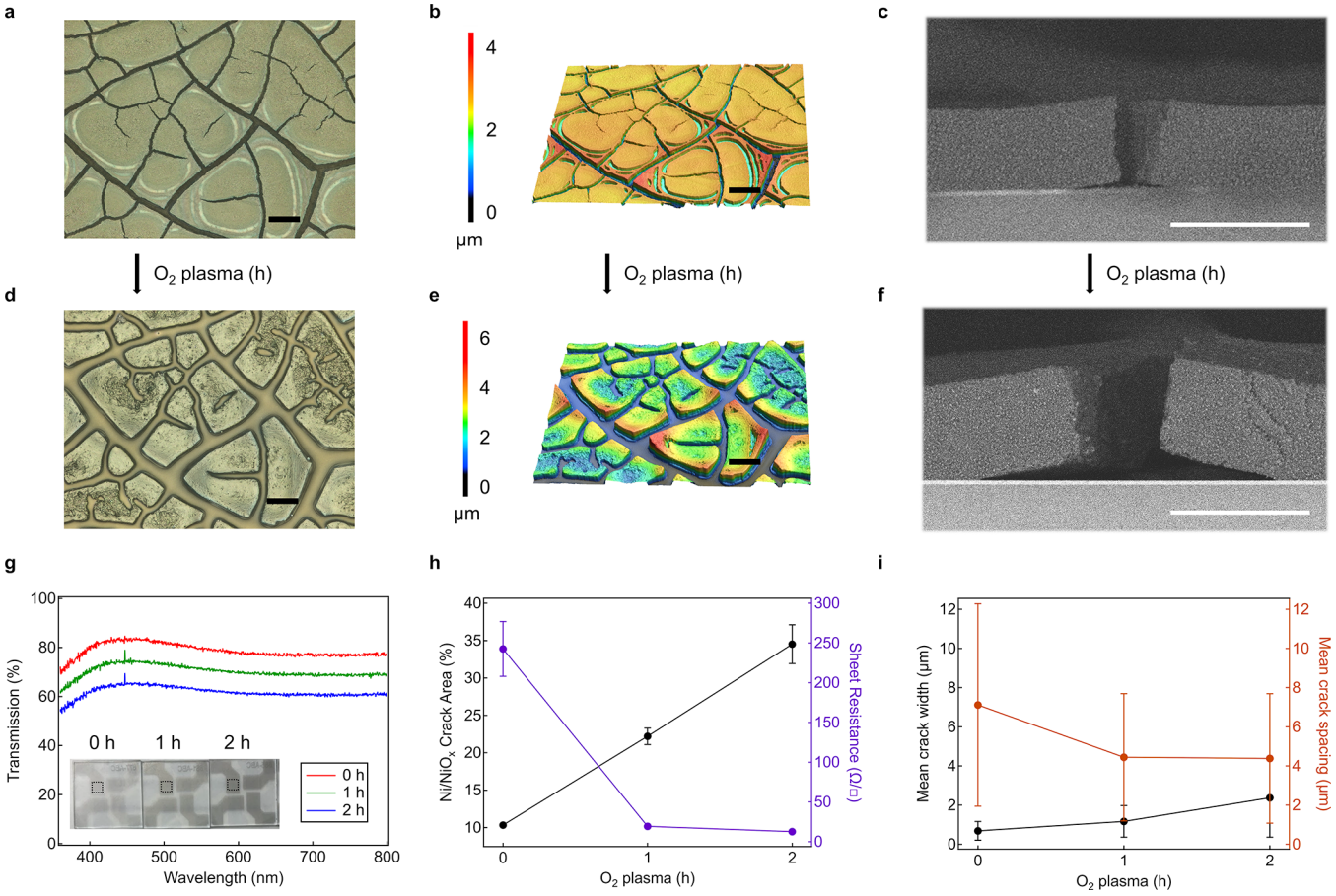

Figure 2. O_2 plasma crack widening to adjust the relative area of the electron and hole selective contacts. (a) Optical, (b) 3D profilometry (scale bars 10 μm), (c) scanning electron microscopy (SEM) cross-section (scale bar 4 μm) images of as-prepared cracked film lithography substrate. (d) Optical (e) 3D profilometry (scale bars 10 μm), (f) SEM cross-section images of crack film lithography substrate exposed to 2 h of O_2 plasma. Scale bar is 4 μm. (g) Transmission spectra of patterned electrodes after liftoff using cracked film lithography templates with varying O_2 plasma widening times. The insets are 25 mm × 25 mm images of device substrates before perovskite deposition, with a black dashed box indicating the overlapping electrodes and active device area. Transmission spectra are blanked with air. (h) Ni/NiO_x crack area and sheet resistance of bare ABC electrode crack network as a function of O_2 plasma time. (i) Mean crack width and crack spacing as a function of O_2 plasma time. Error bars are standard deviations. See method sections for details.

1d). NiO_x is a favorable hole transport layer (HTL) in PSCs for high thermal stability compared to its organic alternatives.[37] After insulator and hole contact deposition, we lift off the sacrificial CFL mask by submerging into a liftoff solution comprised mostly of *n*-methylpyrrolidone. Other solvents like acetone may also be used. Liftoff reveals the back-contact electrode network with exposed NiO_x and SnO_2 surfaces. We further clean these surfaces with UV-ozone, followed by an annealing step to reduce Ni^{3+} states to prevent unwanted reaction with the perovskite precursors and improve device performance (Figure 1e).[16,38] Finally, we solution process a triple-cation double-halide perovskite layer on top of the ABC electrode network, which is known to be thermally stable and less sensitive to processing conditions (Figure 1f).[39] This process produces a high yield of working devices, with 42 of the 48 of devices (87.5%) showing >1 kΩ resistance between electrodes after fabrication.

CFL successfully forms an interconnected electrode network that is robust and defect-tolerant (Figure 1g), similar to previously developed honeycomb-shape charge collecting electrodes.[14] Rogue particles and substrate imperfections can lead to electrode breakage during microfabrication. In interdigitated or fingerlike electrodes, a break in an electrode isolates a relatively large area leading to current density losses. In contrast, the CFL interconnected grid-type network has redundant interconnections leading to improved defect tolerance. In addition, the interconnected wirelike network provides low electrode sheet resistance and high transmittance, which is beneficial in semitransparent applications.[24]

In ABC devices, photogenerated electron and hole densities are greatest at the junction between the electron transport layer (ETL) and hole transport layer (HTL) at maximum power conditions.[8] Defects in the perovskite layer at this junction could significantly limit the performance. Accordingly, abrupt step-edges are thought to be detrimental for ABC devices, as they could lead to defects in the perovskite layer during film formation. For instance, roughness of the substrate is known to potentially modify the formation energy of defects.[40] An outstanding feature of CFL is that it produces electrodes with thickness that gradually tapers at the ETL/HTL junction, facilitating smooth and conformal perovskite film morphology with no observable gaps in the interfaces (Figure 1h and Figure S1). The tapered edges of the electrodes are formed through a combination of an undercut profile in the cracked PMMA network and a slight angle during the directional e-beam evaporations (Figure S2).

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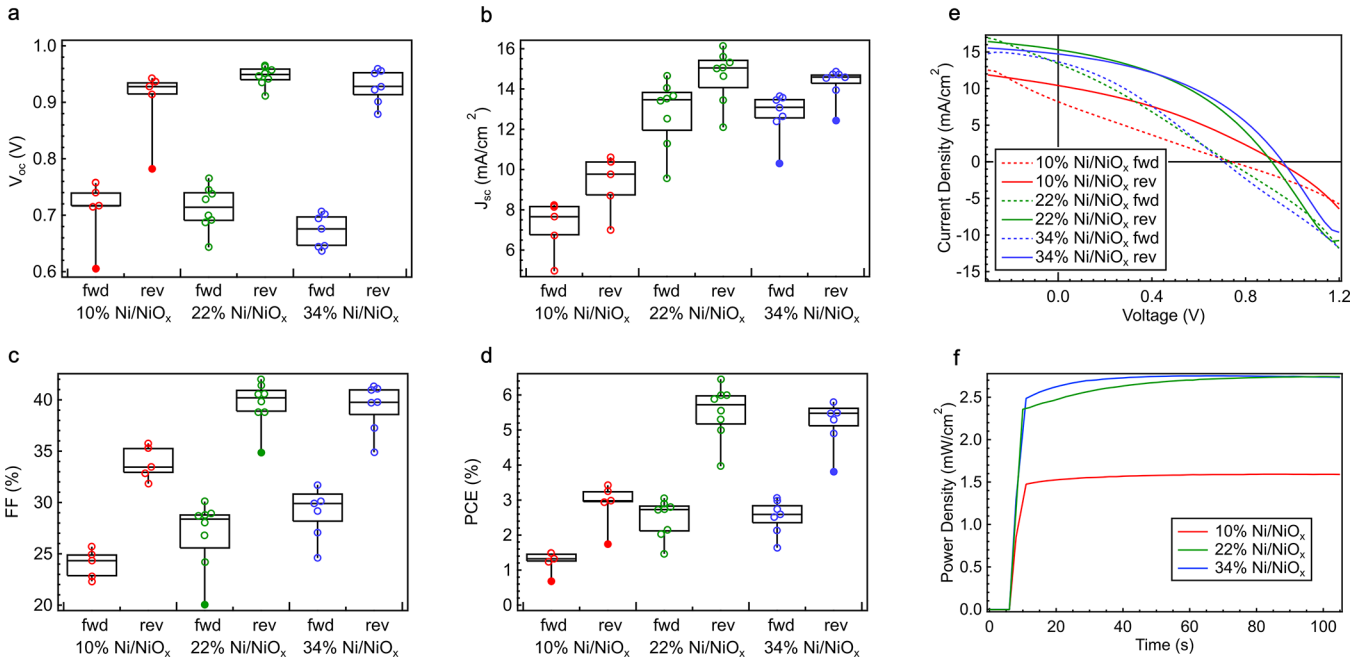

Figure 3. Impact of Ni/NiO$_x$ area on all-back-contact perovskite solar cell performance. Boxplots of performance metrics for various Ni/NiO$_x$ areas derived from forward (fwd) and reverse (rev) current−voltage scans. (a) Open-circuit voltage (V_{oc}), (b) short-circuit current density (J_{sc}), (c) fill factor (FF), and (d) power-conversion efficiency (PCE) are shown. (e) Representative current density−voltage scans. (f) Representative stabilized power-output measurements from front illumination at V = 350 mV.

The as-spun CFL process forms a disperse network of thin cracks with an undercut profile (Figure 2a−c). Drying-induced cracking of colloidal films occurs due to solvent evaporation contracting the film volume, leading to stress that is relieved through crack formation.[28] The crack template thickness controls the crack width and crack spacing.[28] With thinner layers, finer crack networks are formed. We systematically varied the spin speed during crack template formation (Figure S3) and chose 8000 rpm for this report, as it led to the finest dimensions without any delamination across the substrate (Figure 2a,b). A further decrease in crack spacing could be achieved through optimization of thinning down the crack film, although there is a critical film thickness limit around 700 nm.[24] The crack template edges naturally curl up forming an undercut profile due to poor template adhesion (Figure 2c).[35] The undercut profile is ideal for preventing deleterious sidewall connections between Ni and the ETL below during subsequent insulator and metal evaporation steps.

To independently control crack width and crack spacing, we introduce oxygen plasma as a method to widen the PMMA nanoparticle crack network and increase the undercut profile for subsequent evaporation and liftoff (Figure 2d−f). Oxygen plasma widens the cracks likely through a combination of etching and oxidizing the exposed surface of the PMMA network. Oxidizing the exposed surfaces contracts the volume of a thin top layer inducing tensile stress in the film and causing the edges to further curl upward (Figure 2e,f).[41−43] We also demonstrated UV-ozone as an alternative widening process if a nonvacuum patterning technique is desired (Figure S4).

Crack widening controls the resulting transmittance, crack width and spacing, relative transport layer areas, and sheet resistance of the resulting ABC electrodes (Figure 2g−i). The CFL ABC electrode networks have relatively flat transmission spectra across the visible spectrum maintained over various oxygen plasma widening times (Figure 2g). Longer widening times lower the overall transmittance due to greater relative area of the opaque Ni/NiO$_x$ crack network (Figure 2h). The area of the Ni/NiO$_x$ network is inversely proportional to the sheet resistance (Figure 2h). The low sheet resistance achieved, < 20 Ω/□, is comparable to traditional ITO electrodes and ensures negligible solar cell series resistance from the hole collecting Ni/NiO$_x$ network. To better understand the areal and geometric changes, we quantified the mean crack width and crack spacing as a function of widening time (Figure 2i). The mean crack width increases (0.68 ± 0.48 μm to 2.4 ± 2.0 μm) whereas the mean crack spacing decreases (7.1 ± 5.2 μm to 4.4 ± 3.3 μm) after 2 h of O_2 plasma. These relationships and the controllable transparency can be utilized to design semitransparent solar cells for building-integrated applications.[44]

Greater Ni/NiO$_x$ area with wider finger widths led to improved ABC PSC performance (Figure 3a−d). We evaluated the photovoltaic performance of the ABC PSCs using current-density voltage scans. Boxplots display the statistical variation of several devices as a function of O_2 plasma exposure time or Ni/NiO$_x$ area (Figure 3a−d). V_{oc} remained largely unchanged (Figure 3a) compared to a significant boost in short-circuit current density (J_{sc}) (Figure 3b) and fill factor (FF) (Figure 3c). The boost in J_{sc} and FF resulted in increased power-conversion efficiency (PCE) for both forward and reverse scans (Figure 3d).

We believe increased J_{sc} and FF is due to three effects: (1) greater light absorption from increased reflective metallic Ni area, (2) reduced series resistance, and (3) potentially more balanced charge transport. Longer O_2 plasma exposure times increase the reflective metallic Ni area, allowing photons not absorbed during the initial pass through the device to be reflected back into the perovskite layer. Visible transmission measurements confirm the devices exhibit decreased trans-

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mission or an increase in light absorption, at redder wavelengths with greater Ni area (Figure S5). These photons could be absorbed by the perovskite layer and contribute to photocurrent, consistent with the increased J_{sc} (Figure 3b).

The ABC devices also exhibit bifacial performance since ABC substrates are semitransparent. We measured current−voltage scans using the same shadow mask and device area for each set of devices illuminated through the back glass-ITO-Ni/NiO_x substrate (Figure S6). Each performance metric follows the same trends as the front-illumination, where wider Ni/NiO_x area increases performance, with roughly half of the PCE (Figure S6). We conclude increased J_{sc} during front illumination cannot be purely attributed to increased light absorption because illumination through the substrate still shows an increase in J_{sc} even with more metallic Ni area blocking photons from entering the perovskite layer (Figure S6).

We hypothesize J_{sc} increases due to more balanced charge transport or extraction of photogenerated carriers. Wider crack width devices reduce the long distances holes must travel laterally through the perovskite over the larger SnO_2 domains. Shorter distances lower the probability of recombination. Specifically, a 0 to 1 h O_2 plasma widening time increases the Ni/NiO_x area from 10% to 22% and the mean Ni/NiO_x crack width from 0.7 to 2.4 μm while decreasing the mean SnO_x area crack spacing from 7.1 to 4.4 μm. In other words, the mean distance electrons travel laterally over Ni/NiO_x increases from 0.35 to 1.2 μm, whereas the mean distance holes travel laterally over SnO_x decreases from 3.6 to 2.2 μm. The limiting transport distance seems to be over SnO_2, which is consistent with the observed increase in J_{sc} with longer O_2 widening times and decreased SnO_2 domain size. Both electron and hole diffusion lengths have been reported around 1 μm.[3] The diffusion length of our perovskite layer may differ from previous studies and is dependent on a variety of factors, including grain size. Our apparent grain size is 250 ± 112 nm based on SEM image analysis (Figure S1). Alternatively, increased interfacial contact area of the NiO_x could balance charge extraction.[15]

In addition to increased J_{sc}, increased FF must be due to changes in either the series resistance (R_s) or shunt resistance (R_{sh}). R_s exhibits a more pronounced change with increasing Ni/NiO_x area and wider finger widths (Figure S7). Decreased R_s coincides with the reduced sheet resistance in the wider finger widths and greater Ni/NiO_x area (Figure 2h). A possible additional component of R_s is reduced resistance in the perovskite layer due to the shorter lateral distance photocarriers need to travel in the greater Ni/NiO_x area and wider finger width devices, consistent with previous studies.[14] Trends in R_{sh} are not as clear, as the forward scan R_{sh} values are relatively constant whereas the reverse scans show increased R_{sh} in the greater Ni/NiO_x area devices (Figure S7).

Significant hysteresis was apparent for each condition (Figure 3e). Weber et al. revealed the formation and release of interfacial charges, which screen the electric field, is the dominating factor for JV hysteresis, rather than the slow migration of mobile ions.[45] However, the slow migration of mobile ions may be more important in ABC devices compared to planar devices due to the long lateral distances between selective contacts. Large grain perovskite films with relatively low mobile ion concentrations and well-passivated interfaces that mitigate the formation and release of interfacial charges may help mitigate hysteresis in ABC devices. Stabilized power output (SPO) is a better measurement of performance rather than JV-scan-derived PCE in hysteretic devices. The SPO for each CFL ABC device stabilizes near the forward scan derived PCE and shows a similar trend of increasing performance with greater Ni/NiO_x area (Figure 3f). The best SPO, 2.94% at V = 400 mV (Figure S8), is the highest reported to date for back-contact or ABC PSCs fabricated with a scalable solution processed patterning technique. Though this is a promising result for this new architecture, the PCE is well below the modeled performance of ABC PSCs.

Device PCE is likely limited by the large electrode spacing coupled with limited carrier lifetimes and diffusion lengths in the perovskite layer. We also have a free perovskite surface and lateral transport through grain boundaries, which is unique to the ABC architecture. Defects at the free surface, grain boundaries, and the electrode interfaces will increase recombination and also limit performance. Our previous work predicted interface defect densities less than 2×10^{11} cm^{-2} and front surface recombination velocity (S_{fs}) <200 cm/s are paramount for realizing ABC devices with >20% PCE assuming a reasonable carrier lifetime of 192 ns and 4.5/2.5 μm ETL/HTL widths in a honeycomb architecture.[16] Yang et al. predicted ABC devices with 1 μm ETL/HTL widths and electron/hole carrier lifetimes of 2 730 ns to exceed 25% PCE.[8] PCE >29% could be realized with advanced optical management.[8] Additionally, they predicted that mobile ion concentrations exceeding 10^{16} cm^{-3} limit the performance of ABC devices due to electric field screening.[8] Further efficiency gains in our devices could likely be realized by using perovskite films with greater lifetime or longer diffusion lengths, which could be achieved through various techniques including increasing grain size and surface passivation. Reducing the long distance over the ETL and HTL through smaller crack spacing would also have similar benefits to performance. Alternatively, Li et al. proposed incorporating a front-carrier transport layer to enhance the effective lateral transport of carriers, and their model predicted >25% PCE is possible with a rear contact pitch of 200 μm.[46] Optically, we could incorporate a metallic reflector bottom contact and antireflection coatings above the perovskite to increase photocarrier generation. We believe the ABC architecture is capable of >25% PCE to match or exceed planar devices, as predicted by these numerical studies.

We utilized CFL to replace photolithography to form defect-tolerant back-contact electrodes and ABC PSCs. Smooth perovskite film morphology across the patterned substrate was achieved by tapered transitions between the ETL and HTL layers of the CFL back-contact electrodes. The tapered transitions are formed through a combination of an undercut profile of the PMMA crack network and angled evaporations. We developed a method to widen the crack network to modulate the transparency, sheet resistance, and independently control the relative areas of the ETL and HTL in contact with the perovskite while maintaining the optimum undercut profile. Increasing the Ni/NiO_x HTL area increased J_{sc}, FF, and PCE in ABC PSCs. A relatively high stabilized power output was achieved with this process. Overall, CFL offers three main advantages for patterning back-contact electrodes: (1) scalable solution processability, (2) ideal liftoff profiles, and (3) defect tolerant and tunable electrode design. Our work provides a route toward scalable fabrication and opens the door to facilities without photolithography capabilities to fabricate and study promising all-back-contact architectures for PSCs.

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■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaem.2c01298.

Experimental details including materials, CFL ABC device fabrication procedure, characterization details; scanning electron microscopy (SEM) images of a completed ABC PSC device; schematic of electron-beam evaporation system and SEM image of sample after evaporations; optical images of bare back-contact electrode networks formed from crack film lithography templates spun at various spin speeds; optical images of UV-ozone crack widening; visible transmission measurements of complete devices; photovoltaic performance metrics illuminated through glass-ITO side vs perovskite side; estimates of series and shunt resistance for each device; stabilized power output of champion device; and impact of reflective stage on performance (PDF)

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Notes

The authors declare no competing financial interest.

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