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RESEARCH ARTICLE

# Results from an international interlaboratory study on light- and elevated temperature-induced degradation in solar modules

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## Abstract

This paper reports the results of an international interlaboratory comparison study on light- and elevated temperature-induced degradation (LETID) on crystalline silicon photovoltaic (PV) modules. A large global network of PV module manufacturers and PV testing laboratories collaborated to design a protocol for LETID detection and screen a large and diverse set of prototype modules for LETID. Results across labs indicate the reproducibility of LETID testing is likely within ±1% of maximum power

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($P_{MP}$). In intentionally engineered LETID-sensitive modules, mean degradation after the prescribed detection stress is roughly 6% $P_{MP}$. In other module types the LETID sensitivity is smaller, and in some we observe essentially negligible degradation attributable to LETID. In LETID-sensitive modules, both open-circuit voltage ($V_{OC}$) and short-circuit current ($I_{SC}$) degrade by a roughly similar magnitude. We observe, as do previous studies, that LETID affects each cell in a module differently. An investigation of the potential mismatch losses caused by nonuniform LETID degradation found that mismatch loss is insignificant compared to the estimated loss of cell $I_{SC}$, which drives loss of module $I_{SC}$. Overall, this work has helped inform the creation of a forthcoming standard technical specification for LETID testing of PV modules, IEC TS 63342 ED1, and should aid in the interpretation of results from that and other LETID tests.

**KEYWORDS**

degradation, light- and elevated temperature-induced degradation (LETID), photovoltaics (PV), PV modules, silicon, solar cells

## 1 | INTRODUCTION

Light- and elevated temperature-induced degradation (LETID) has emerged as a considerable cause for concern in crystalline silicon (c-Si) solar cells and modules, commanding significant research attention in recent years and demanding test methods for assessing the LETID sensitivity of solar products. Global researchers have made substantial strides in understanding the causes and behavior of LETID, and provided strategies to mitigate LETID in production [1]. Hydrogen is certainly involved in the LETID defect, and establishing (or maintaining) a careful balance of the quantity and chemical state of hydrogen in cells is the likely route to high-efficiency cells with minimal LETID. This balance has been termed "defect engineering" or "advanced hydrogenation" [2, 3], and has been employed by manufacturers and researchers around the world to make high-efficiency, stable cells: while early reports of LETID losses were on the order of 10%, more recent studies show that the maximum extent of LETID can be suppressed to 1–2% relative or less [4].

Defect engineering to suppress LETID has mostly been empirical: the precise LETID defect is not yet known. To provide a reliable and consistent method of assessing LETID and ensure all future products are acceptably stable, the global community would benefit from standard procedures for commercial modules. While LETID-related loss always seems to eventually recover with continued LETID stress (a phenomenon called "regeneration"), the process of degradation to regeneration might take years or decades to entirely run its course in the field, which would result in substantial energy yield loss in real-world systems [5, 6].

A good test should induce LETID in LETID-sensitive modules and induce minimal degradation in insensitive products. The procedure should be able to distinguish LETID from non-LETID degradation, while being practical and expeditious, with an appropriate balance between acceleration of LETID and real-world applicability. Results in like products should be reproducible across many testing labs.

This paper details the results of a global effort undertaken from 2018–2020 by a diverse group of module manufacturers and testing labs to test a variety of c-Si modules for LETID. The ultimate aim was to inform the creation of a standard test procedure, which now exists as a forthcoming IEC Technical Specification (TS), IEC TS 63342, currently in the committee draft status and forecast for full publication in 2022. We describe the procedure used here and note changes since the evolution of the TS. We evaluate the reproducibility across labs in both intentionally engineered LETID-sensitive modules and LETID-insensitive modules. We note similarities and differences in the way LETID manifests in different modules, and propose ideas for future study of LETID in modules.

## 2 | LETID, AN OVERVIEW

Early observations of the type of degradation now known as LETID came in 2012, with many more of studies beginning around 2015 [1, 7]. LETID is essentially an electronic defect that deteriorates charge carrier lifetime in c-Si wafers over time and is triggered by excess carrier injection (either illumination or electrical current) at elevated temperature. While the precise LETID defect is unknown, a number of studies have shed light on the kinetics and several models of LETID defect states have been proposed [8–10]. Undegraded cells will have the LETID defect primarily in a recombination-inactive precursor state (denoted in Figure 1 as State A), and exposure-induced performance degradation implies the transition of most precursors to a recombination-active state (State B). Subsequent improvement implies that the defect transitions from State B to a recombination-inactive "regenerated" state (C) where the defect has either been passivated or removed from the c-Si bulk. There are other defect states and transitions beyond these three, but the degradation → regeneration cycle depicted in Figure 1 will likely be the characteristic shape of performance degradation in a LETID-affected cell in the field. The cycle can take place over the course of days to weeks in accelerated lab testing, or over the course of years to decades in the field. The

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**FIGURE 1** Schematic of LETID-related performance loss and recovery in c-Si wafers, cells, or modules, with the primary defect states and transitions associated with performance changes. Luminescence images of a LETID-affected cell show the loss and recovery of minority charge carrier lifetime and related performance as LETID progresses. Exposure (heat and carrier injection) may be achieved either with field conditions or accelerated testing

regeneration transition is slower than the degradation transition under consistent exposure conditions.

LETID-like effects have been demonstrated in nearly all types of c-Si wafers and solar cells: monocrystalline (both Czochralski (Cz) and float zone (FZ), as well as cast mono) and multicrystalline (mc-Si, including quasi-mono mc-Si and high performance multi [HPM]) [11–15]; p-type and n-type (including all solar-relevant dopant species (B, Ga, In, P) [16–20]; and both homojunction and heterojunction device structures [20–22]. While the kinetic details and severity of LETID in each wafer type can vary, behavioral similarities suggest that the defect is related, and that hydrogen always plays a role [1, 23].

The understanding of hydrogen's involvement in LETID has allowed the development of several different defect engineering approaches to substantially suppress LETID. These include adapted firing profiles, adding moderate temperature anneals either before or after firing, manipulating the thickness or hydrogen content of dielectric surface films, or fast regeneration via high-intensity illumination or current injection at elevated temperatures [15, 24–31]. The high-intensity illumination approach is similar to a method of mitigating boron-oxygen light-induced degradation (BO-LID) in Cz-Si wafers [32, 33]. A recent study showed that just 30 seconds of high-intensity illumination at elevated temperature, performed after firing, reduced subsequent LETID losses in mc-Si cells by more than 60%. This seems like a promising approach for inline industrial implementation [34]. LETID in p-type Cz-Si wafers could be practically mitigated by changing from boron doping to gallium doping. While Ga-doped wafers are not immune to LETID, the absence of boron removes the need for BO-LID treatment, therefore reducing the motivation to over-hydrogenate Ga-doped wafers and reducing the risk of LETID [16, 17, 35]. Recently, LETID-like effects in Ga-doped Cz-Si and B-doped mc-Si wafers were shown to have different kinetics, which implies that Ga-doped Cz-Si wafers might require alternate LETID treatment compared to B-doped mc-Si wafers [18].

Given that all types of c-Si modules might be susceptible to LETID, it is important to have a test to screen for it and for a given product, obtain a rough understanding of the maximum extent to which LETID may occur in the field. Accelerated testing will not provide an exact prediction of field-observable degradation and regeneration, which will depend on climate, cell and module technology, and other variables; but it does provide a needed basis for understanding the risk of LETID in a given product [5, 36].

A recent study of fielded modules in a ~ 3-year-old utility scale plant found >1% power loss per year attributable primarily to LETID [37], which emphasizes this need for screening. A number of results have been reported on accelerated LETID tests on modules and several commercial testing labs have created internal accelerated testing protocols. But comparison of these results is difficult: among other variables, the precise temperature and injection level in the device may actually impact the extent of LETID, as the degradation transition from state A → B and the regeneration transition B → C both happen simultaneously [38, 39]. This motivates a standard with defined temperature and injection conditions over a defined time.

## 3 | RATIONALE, PARTICIPANTS, SAMPLES, AND PROCEDURE

Realizing the importance and urgency of publishing a standard test for LETID, the global PV reliability and standards community in 2018 embarked on an effort to: first, quickly draft a LETID test as a candidate for inclusion in the then-upcoming new edition of the IEC 61215 terrestrial PV module qualification standard series, and second: recruit a number of manufacturers and testing labs to participate in an interlaboratory cross-comparison of an early version of the test [40]. The purpose of the interlaboratory test was to exercise global testing capabilities, evaluate the effectiveness of the protocol in identifying LETID, and to estimate cross-lab reproducibility. This paper reports on the results of this interlaboratory cross-comparison.

While the LETID test was not ultimately included in the now-published latest edition of IEC 61215, an evolved version of it now exists as the forthcoming IEC TS 63342 ED1 (Light and elevated temperature induced degradation (LETID) test for c-Si Photovoltaic (PV) modules: Detection), forecast for publication in 2022. Note the discussion in Section 5 below about the protocol used in this work versus the protocol ultimately laid out in TS 63342. Also note the separate forthcoming IEC technical specification for LETID testing of c-Si solar cells: IEC TS 63202-4 ED1 (Photovoltaic cells - Part 4: Measurement of light and elevated temperature induced degradation of crystalline silicon photovoltaic cells), likely to also be published in 2022.

Module manufacturers and testing labs participated on a volunteer basis, with summarized metadata in Table 1. Manufacturer and testing lab identities were anonymized. Six different manufacturers supplied 10 different module types, for a total of 64 different modules, which were distributed to 14 different testing labs. The six

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**TABLE 1** Metadata for modules tested in this work

| Module type | # modules | # of labs that tested this module type | Mono or multi c-Si | # cells in module | Cell format | Interconnect | Average initial power (W) |
|---|---|---|---|---|---|---|---|
| S | 6 | 3 | Mono | 48 | full | tabbed | 238 |
| U* | 15 | 8 | Multi | 120 | half | tabbed | 282 |
| J | 3 | 2 | Multi | 120 | half | tabbed | 285 |
| T | 8 | 4 | Multi | 60 | full | tabbed | 287 |
| P* | 8 | 4 | Multi | 60 | full | tabbed | 288 |
| K | 3 | 2 | Mono | 120 | half | tabbed | 303 |
| F | 3 | 2 | Mono | 120 | half | tabbed | 315 |
| Q* | 10 | 2 | Mono | 72 | full | tabbed | 338 |
| R | 6 | 3 | Mono | 360 | quarter | shingled | 355 |
| Z | 2 | 1 | Mono | 72 | full | tabbed | 365 |
| | total: 64 | 14 different labs | | | | | |

[a]Intentional LETID-sensitive modules.

participating manufacturers represented five different countries, and testing labs were a mix of commercial and noncommercial institutions representing ten different countries. Labs received as many module types as they were willing to test, and most tested two replicates of a given module type. Among the modules there were a variety of wafer sizes, full/half/quarter-cut wafers, module power ratings, and interconnection schemes. To our knowledge, one of the ten module types (Type F) was based on n-type wafers, but we otherwise have little insight into wafer type or device architecture beyond what is readily observable. Three types of module, denoted with asterisks in Table 1, were intentionally engineered by their manufacturers to be LETID-sensitive, with the expectation that those would degrade substantially in the test. Other module types were not intentionally engineered to be LETID-sensitive, but these should still be assumed to be prototype products manufactured for the purpose of this study, and not true commercial products representative of the market in 2018. The inclusion of specially-engineered modules and prototypes is consistent with the goals of the study, which is to evaluate the LETID test. The study was not intended to evaluate the state of LETID in the industry or in specific products.

The test involved two distinct phases: a first phase for LETID detection, followed by a second phase for regeneration of LETID-sensitive modules. The first phase prescribes 75 ± 3°C with carrier injection roughly equivalent to Standard Test Condition (STC) maximum power injection, which for modules in a dark climatic chamber is an applied current equal to the difference between the module's short-circuit current and the maximum power current, that is, ($I_{dark} = I_{SC,\ STC} - I_{MP,\ STC}$). The relatively low temperature and injection level were chosen to allow LETID to progress slowly enough to achieve the maximum degradation and detect it via weekly I–V tests. The protocol also allowed for achieving carrier injection via illuminated apparatus, specifying a continuous light source at 1000 ± 100 W/m$^2$, with means for maintaining the module at $I_{MP}$. The modules were to be stressed in either the dark or illuminated manner for a period of 162 h (+8/−0 h) (i.e., approximately 1 week), followed by STC I–V curve measurements and electroluminescence (EL) imaging at forward currents of $I_{SC}$ and 0.1 × $I_{SC}$. Intervals of 162 h were to be repeated with interim characterization for a total of 4 weeks, or until module power was no longer decreasing.

The purpose of the second phase was to put LETID-sensitive modules into the maximally regenerated state, such that no further regeneration from prior LETID could be detected. This phase prescribed both higher temperature and higher injection in order to accelerate the regeneration process (85 ± 3°C with dark current equal to $I_{SC,\ STC}$, or alternately 1000 ± 100 W/m$^2$ illumination at open circuit). Since regeneration eventually saturates to a constant value, the temperature and injection level (and thus regeneration rate) are increased without risk of losing information. This phase was prescribed to last 500 h (+24/−0 h) (i.e., approximately 3 weeks), with interim I–V curves and EL, followed by one or more final stress intervals of 162 h (+8/−0 h) until module power was no longer increasing.

In practice, few of the participating testing labs followed the prescribed protocol perfectly, which perhaps underscores the need for codification and standardization. In some cases, intentional departures were made to gather more data, for example, testing modules for all 4 weeks of the detection phase despite little or no degradation; or lengthening the duration of the detection phase beyond 4 weeks to observe degradation saturation. In some cases, departures from the prescribed protocol were made to save time and labor costs, for example, not all labs performed the second phase for LETID regeneration which required 3 to 6 weeks additional chamber time. Given the relatively long duration of the test and the expense incurred for testing many modules on a volunteer basis, judgment calls to save time might be expected. One important outcome in early feedback from testing labs was identifying the need to expedite the test.

## 4 | RESULTS AND DISCUSSION

In the following subsections we present and discuss results: overall power degradation and regeneration for each module type

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(Section 4.1); cross-lab reproducibility for modules of the same nominal type (Section 4.2); I–V component analysis by module type (Section 4.3); and explorations of nonuniform degradation and the possibility of mismatch losses in LETID-affected modules (Section 4.4). Finally, (Sections 5 and 6) we comment on the overall lessons of the interlaboratory test in the context of the forthcoming IEC TS for LETID testing, and the outlook for commercial products given the state of the scientific understanding of LETID and the development of defect-engineered cells and modules.

## 4.1 | Power degradation and regeneration

Figure 2 shows the percentage changes in maximum power for each module type over the course of the test, colored by testing lab. The graphs illustrate the wide variety of degradation behavior across different module types, and in a few cases the different degradation or regeneration behavior of modules within a given module type. Figure 2 also makes apparent some variations in test procedures across different labs, where exposure durations are different.

### 4.1.1 | Detection-phase degradation behavior across module types

The extent of LETID is greatest on average in modules U* and P*, which were two of the module types that were intentionally engineered for LETID-sensitivity. Both underwent approximately 6% $P_{MP}$ loss after 4 weeks of stress. The other intentionally engineered type, Q*, exhibited power losses more on par with the other modules.

In U* and P*, the degradation level achieved after 4 weeks is obviously incomplete. Two type U* modules eventually reached degradation saturation at roughly 11.5% $P_{MP}$ loss after 19 weeks of detection phase stress. Type P* modules still being tested for 11 weeks exhibited 9.5 ± 2.0% $P_{MP}$ loss, approaching but not quite reaching the apparent point of saturation. Accounting for some non-LETID losses in these modules, we estimate that the prescribed 4 weeks of stress induced roughly 50–70% of the LETID that the modules were susceptible to.

Other modules exhibited smaller amounts of LETID. For module types with sufficient data that exhibited LETID-like behavior (S, K, J, and R), the prescribed 4 weeks of stress resulted in anywhere from 2–4% mean $P_{MP}$ loss. For these, 4 weeks seems to have nearly stressed modules to the point of saturation, but they have not quite yet entered regeneration. Under the ≥3% threshold from the forthcoming IEC TS (see Section 5), module types U*, P*, S, K, and perhaps J and R would be classified as "LETID-sensitive."

Two types of modules, T and F, appear to be essentially LETID insensitive. For type T, 4 weeks of degradation induced roughly 1% $P_{MP}$ loss which did not subsequently regenerate; therefore, it is likely non-LETID related loss. Type F modules slightly improved during the LETID detection phase, which is very good evidence of their LETID insensitivity. Type F modules were indicated by their manufacturer to be based on n-type wafers, where all others are believed to be based on p-type wafers.

Type Q* and type Z have limited data as a result of only being tested for 2–3 weeks by 1–2 testing labs, so will therefore be largely excluded from further analysis.

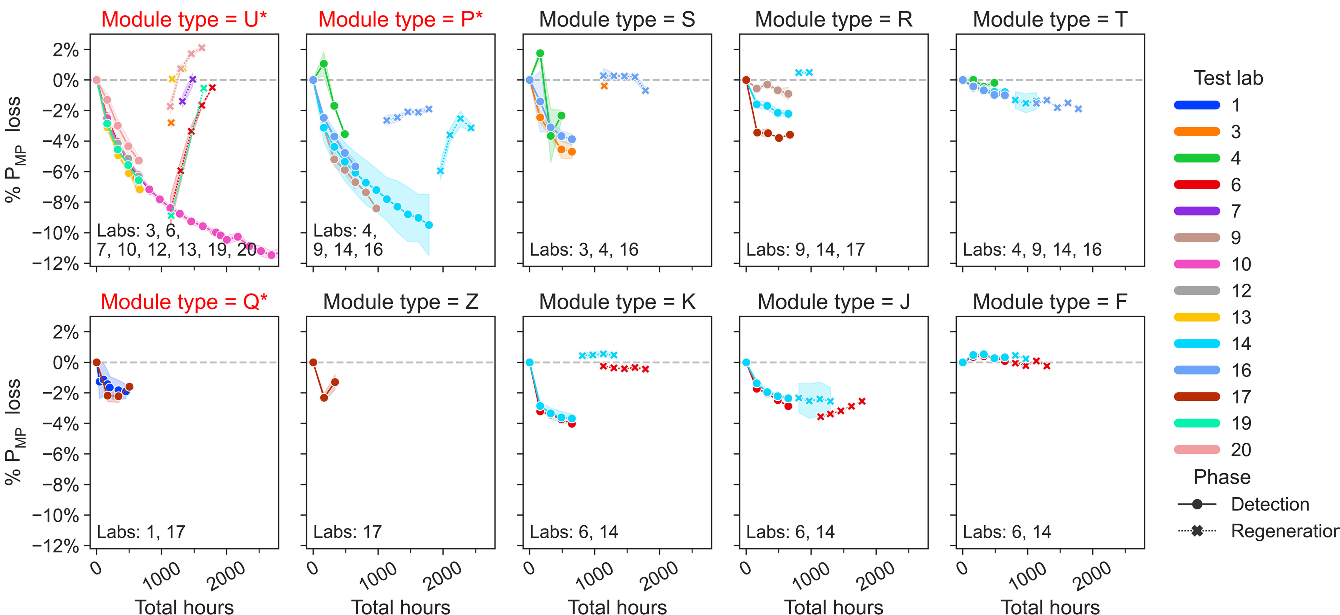


**FIGURE 2** Percentage changes in STC maximum power ($P_{MP}$) for each module type over the course of the test, colored by testing lab and segmented by phase (detection or regeneration). The connected markers denote the mean of multiple replicates of a sample tested by a lab (in most cases, a lab tested two modules of a given type), and the shaded region (not always visible) shows the standard deviation of modules of the same type measured at the same lab. Intentional LETID-sensitive modules are denoted in red with an asterisk (*)

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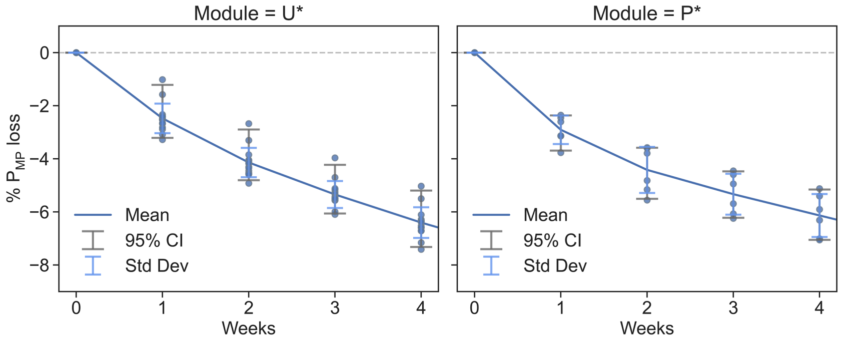


**FIGURE 3** Detection-phase data for module types U* (left) and P* (right). The standard deviation is shown by light blue bars, the 95% confidence interval is shown by the underlying dark bars. This figure excludes modules not tested for 4 weeks

**TABLE 2** Mean percentage $P_{MP}$ loss, standard deviation, and high and low 95% confidence intervals for each module type at week 4 of the detection phase (excluding those with insufficient week 4 data: Q* and Z)

| Module type | Week | # of modules | # of labs | Mean % $P_{MP}$ loss | Standard deviation | 95% CI high | 95% CI low |
|---|---|---|---|---|---|---|---|
| U* | 4 | 15 | 8 | −6.4% | 0.6% | 1.2% | 0.9% |
| P* | 4 | 6 | 3 | −6.1% | 0.8% | 1.0% | 0.9% |
| S | 4 | 4 | 2 | −4.5% | 0.7% | 0.8% | 0.8% |
| K | 4 | 3 | 2 | −3.8% | 0.3% | 0.3% | 0.2% |
| J | 4 | 3 | 2 | −2.5% | 0.3% | 0.2% | 0.3% |
| R | 4 | 5 | 3 | −2.0% | 1.1% | 1.3% | 1.5% |
| T | 4 | 6 | 3 | −0.9% | 0.2% | 0.2% | 0.2% |
| F | 4 | 3 | 2 | 0.3% | 0.2% | 0.1% | 0.2% |

*Note*: Intentional LETID-sensitive modules are denoted with an asterisk. Note that this table excludes modules not tested for 4 weeks.

### 4.1.2 | Regeneration behavior across module types

The regeneration phase also produced differences across modules. First, U* and P*, the intentionally LETID-sensitive types, exhibited different extents and profiles of power recovery in the regeneration phase. All type U* modules recovered essentially completely, in some cases beyond their initial power. Also interesting is that type U* regeneration profiles were widely different among the labs that performed it. Four labs' modules (3, 7, 13, and 20) exhibited power regeneration after the first 500 h, where two other labs (6 and 19) continued to degrade during the first 500 hours of the regeneration phase, before ultimately recovering with continued regeneration stress.

Power recovery in type P* modules, on the other hand, was incomplete: for the two labs that performed the phase, regeneration seems to saturate at roughly 2% $P_{MP}$ loss. This is presumably because of non-LETID, irreversible degradation superimposed on the LETID degradation-regeneration curve.

In other LETID-sensitive modules with regeneration data, we observe two different types of regeneration behavior: in types S, R, and K, the regeneration is essentially complete within the first 500 hours of the regeneration phase. In type J, regeneration occurs much more slowly, and seems to not reach the maximally regenerated state even after 4–7 weeks of regeneration phase. Therefore, especially in J, we cannot rule out that the modules may have undergone non-LETID degradation.

## 4.2 | Reproducibility across labs

A key point of this interlaboratory test was to evaluate reproducibility of the test results across many different labs. Figure 3 (left) shows the detection phase $P_{MP}$ loss data for 15 type U* modules tested by eight labs. The mean $P_{MP}$ loss after 4 weeks is 6.4%, with a standard deviation of 0.6%. Figure 3 (right) shows $P_{MP}$ loss data for six type P* modules tested by three labs, having mean week 4 $P_{MP}$ loss of 6.1% with a standard deviation of 0.8%.

Type U* and P* are the intentionally LETID-sensitive modules that underwent a relatively larger amount of degradation, and were each tested by at least three labs. However, the numbers of labs, samples and measurements are still insufficient compared to what would be required for a robust statement on repeatability and reproducibility limits as described in, for example, ISO 5725 or ASTM E691. Additionally, only a few labs provided stated measurement uncertainties or multiple measurements at a given stress point, so we have limited estimates of intra-laboratory repeatability. Beyond this there are many plausible sources of non-reproducibility: for example, we should not assume that all replicates of a given module type would degrade identically if subjected to identical stress. Likewise, we cannot assume that all testing labs carried out the procedure identically. As such, we simply provide the mean week 4 $P_{MP}$ loss, standard deviation, and 95% confidence intervals in Table 2 as conservative estimates of the interlaboratory agreement for each module type in the detection phase. Due to the relative lack of data and the variation in each lab's

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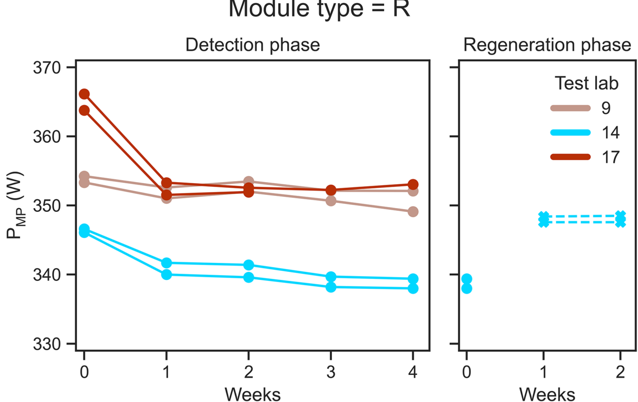


FIGURE 4 Absolute $P_{MP}$ over the detection phase (solid lines, left) and regeneration phase (dashed lines, right) for all type R modules, color coded by test lab. Differences in detection phase degradation at each lab indicate differences in the LETID sensitivity of the different type R sample sets

regeneration procedure, we cannot quantitatively assess reproducibility of the regeneration phase.

In general, from the data in Table 2 we conclude that the detection phase of this testing procedure yields results that can likely be considered reproducible to <±1% $P_{MP}$ in heavily LETID-sensitive modules. In modules that exhibit milder LETID, the reproducibility is perhaps a bit better, see for example types K and J, but more data would allow more confidence in this assertion. In LETID-insensitive modules (types T and F), the reproducibility appears to be fairly good, <±0.2% $P_{MP}$. Given the similarity between the detection phase procedure here and the procedure of the forthcoming IEC TS, the inter-lab reproducibility of the TS is likely to be comparable. Part of the motivation for the developing the referenceable procedure of the TS is to minimize non-reproducibilities. In the future, a robust interlaboratory study designed in accordance with standard guidelines and using commercial-grade products could provide better quantification of the repeatability and reproducibility limits of the TS.

The one module type that showed very poor reproducibility across labs was type R, where the extent of degradation observed by each lab was very different. However, as Figure 4 shows, the results within each lab seem to be quite reproducible. Given that the one lab that performed the regeneration phase saw complete power recovery, we believe type R modules to be LETID sensitive, but that the LETID-sensitivity was different among replicates. The quite different initial $P_{MP}$ values of the modules is evidence that each test lab received modules with different characteristics. Conclusions beyond these, for module type R, would only be speculation.

## 4.3 | I–V parameter changes

In addition to the above examination of PMP, we can learn from changes in other I–V parameters: short-circuit current ($I_{SC}$), open-circuit voltage ($V_{OC}$), and fill factor (FF). Figure 5 shows percentage changes in $I_{SC}$, $V_{OC}$, and FF, color-coded by lab and segmented by test phase. In general, for modules that exhibit LETID, the detection phase losses are in both $I_{SC}$ and $V_{OC}$ and are roughly similar in percentage terms. In some module types (P* and S) there is also substantial FF loss.

We conclude that in LETID-affected modules, one should expect both $I_{SC}$ and $V_{OC}$ degradation. FF degradation may also occur, but FF loss does not necessarily seem related to LETID in the same way. This is particularly apparent in module type P*, where $I_{SC}$ and $V_{OC}$ largely recover in the regeneration phase, whereas FF does not. Most other module types that exhibited LETID saw very slight FF changes or even improved FF during the detection phase (see types U*, Q*, R, Z, K, and J). The exception is module type S, which saw roughly similar percentage losses and subsequent recoveries in all of $I_{SC}$, $V_{OC}$, and FF.

The reproducibility of the detection phase is in general rather good for $V_{OC}$ and FF. $I_{SC}$ seems to be somewhat less reproducible, perhaps because $I_{SC}$ measurement reproducibility tends to be a bit worse across different testing labs in general [41]. As seen in $P_{MP}$ analysis of the previous section, module type R is unique in its irreproducibility. It exhibits notably worse reproducibility in both $I_{SC}$ and $V_{OC}$, which we attribute to differences between the type R modules received by each lab.

Of the LETID-insensitive modules, type T exhibited very small mean losses in all of $I_{SC}$, $V_{OC}$, and FF, none of which substantially recovered in the regeneration phase. Again, we attribute these losses to mechanisms other than LETID. For module type F, I–V parameters did not obviously degrade.

Figure 6 shows the mean normalized power at the end of the 4-week detection phase for each module type. The lost power is attributed to $I_{SC}$, $V_{OC}$, and FF and color-coded accordingly. Figure 6 makes clear that in LETID-sensitive modules, power loss is always a result of both reduced $I_{SC}$ and $V_{OC}$. Ciesla et al. observed similar behavior, noting larger relative losses in $I_{SC}$, $I_{MP}$, and $V_{MP}$ than in $V_{OC}$ [42]. They suggested that the injection-dependence of the LETID defect has a more pronounced affect at lower voltages. Figure 6 show that FF-driven power loss occurs in some but not all module types; in some modules (particularly P* and T) this FF loss seems at least partially due to degradation other than LETID, as it does not completely recover.

## 4.4 | Nonuniform degradation

A characteristic of previous studies of LETID-affected modules is variation in cell-to-cell degradation, which is readily visible in EL images [2, 2, 6, 37]. Figure 7 shows EL images at high and low injected current of a representative example of each module type before and after the detection phase, and after regeneration. Cells in LETID-sensitive modules tend to get dimmer as they degrade, and cell-to-cell variation tends to increase. After regeneration, cells tend to become brighter and more uniform. This behavior is particularly apparent for high-current images for types U*, P*, S, and K. The evolution in cell-to-cell variation is subtler in types J and R. The LETID-insensitive module types, T and F, change very little and have less cell-to-cell variation.

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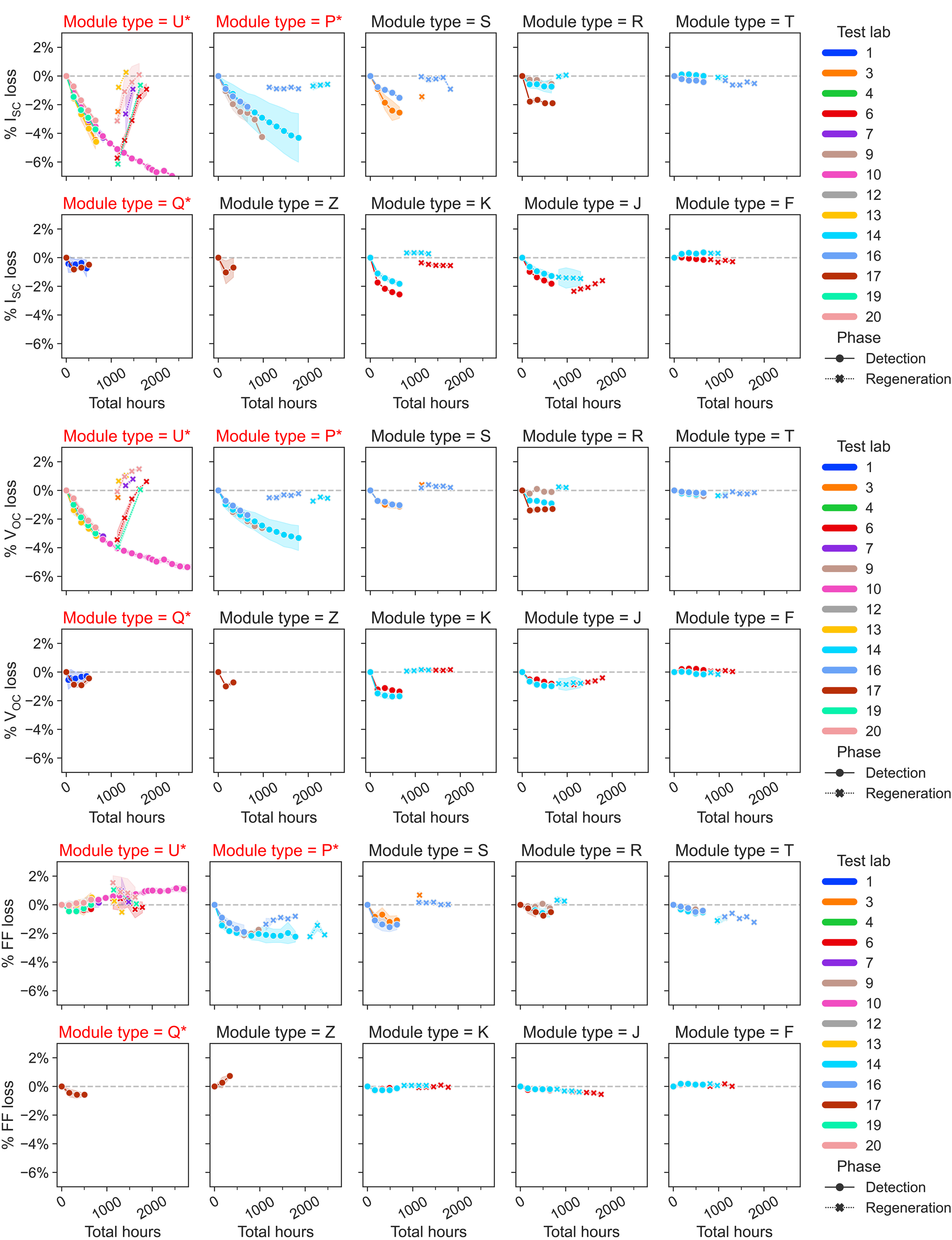


FIGURE 5 Legend on next page.

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**FIGURE 5** Percentage changes in short-circuit current ($I_{SC}$), open-circuit voltage ($V_{OC}$), and fill factor (FF) for each module type over the course of the test, colored by testing lab and segmented by phase (detection or regeneration). The connected markers denote the mean of multiple replicates of a sample tested by a lab (in most cases, a lab tested two modules of a given type), and the shaded region (not always visible) shows the standard deviation. Note that this figure excludes modules with incomplete I–V parameter data. Intentional LETID-sensitive modules are denoted in red with an asterisk (*)

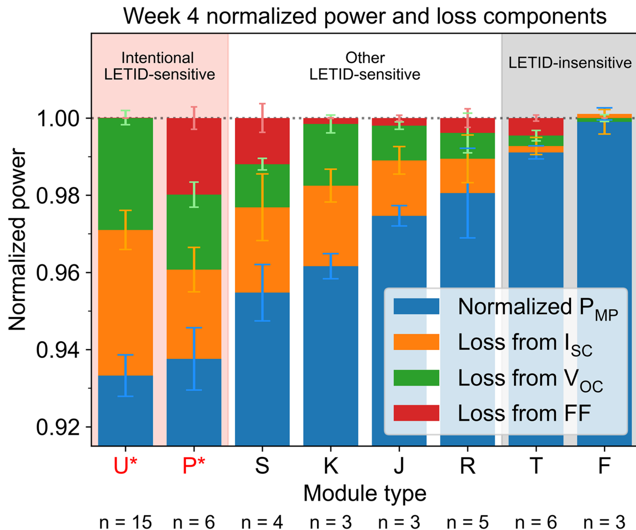


**FIGURE 6** Mean normalized power (blue) after 4 weeks of the detection phase for each module type (excluding those with insufficient week 4 data: Q* and Z). Also shown are the normalized power losses attributable to $I_{SC}$, $V_{OC}$, and FF. Error bars show the standard deviation. The total number of modules of each type is indicated by "n." This figure excludes modules not tested for 4 weeks or those with incomplete I–V parameter data. For module type F the sum of normalized power loss is slightly greater than 1 because the modules slightly gained power

Particularly for module types U* and P*, the low current images taken after detection and after regeneration are darker, relative to initial, than their high current counterparts. This suggests that the origin of degradation is not series resistance; rather, this may be a result of reduced carrier lifetime and the carrier injection-dependence of the LETID defect as suggested by Ciesla et al. [42].

Deceglie et al. describe cell-to-cell variation as an expected characteristic of LETID-affected modules [37]. Several possible reasons why cells within a module might degrade differently could be wafer ingot position, small variations in dielectric layer thickness, or small variations in firing [13, 28, 43–45]. All of these have been shown in the literature to have an influence on LETID, but none of them has been definitively shown to be the source of cell-to-cell variation within a single LETID-affected module.

### 4.4.1 | Investigation of current mismatch

In a module, series-connected cells under uniform irradiance operate at a current point determined by their individual voltage-summed I–V curves. The difference between this current point and the sum of the $I_{MP}$ of each cell is mismatch loss, and is usually minimized during manufacturing by sorting cells into bins defined by narrow ranges of cell $P_{MP}$, $I_{MP}$, or $I_{SC}$ [46], but nonuniform degradation in a module could conceivably exacerbate mismatch. Mismatch loss would primarily manifest as $I_{SC}$-related loss in the power loss attributions shown in Figure 6. Given the sizable power loss attributable to module $I_{SC}$ in Figure 6 and the cell-to-cell variation seen in EL in this and other work, it seems reasonable to suspect power loss contributions from mismatch [6]. In this section, we investigate whether the measured $I_{SC}$ loss associated with LETID (orange bars in Figure 6) could be due to cell mismatch.

$I_{SC}$ is the convolution of cell optics, incident light wavelength and absorption-dependent generation $G(\varphi, \lambda, z)$ and depth-dependent collection probability $\psi(z)$. Collection probability depends on bulk minority carrier lifetime via minority carrier diffusion length [47]. When lifetime is reduced enough that the diffusion length becomes less than the wafer thickness, the collection probability in the bulk will be reduced. While $I_{SC}$ is indirectly linked to lifetime, it is intuitive that reduced lifetime will result in some amount of reduced carrier collection, and therefore, some amount of reduced $I_{SC}$ [47].

Figure 8 shows an EL image of a representative type P* module before and after 4 weeks of degradation. The middle and right images in Figure 8 show the distribution of estimated, normalized individual cell $I_{SC}$ values for the same module. $I_{SC}$ is estimated by first extracting cell-level diode terms ($J_0$) from the EL image using the method of Rajput et al. [48]. This subsequently allows for the calculation of cell $I_{SC}$ via a collection probability profile for each cell. Assumptions required for the $I_{SC}$ calculation are typical material properties of a c-Si PERC cell and an optical generation profile for textured, antireflection layer-coated c-Si from the freeware program OPAL 2 using default inputs [49]. Appendix A provides further details on cell $I_{SC}$ estimation.

The estimated cell $I_{SC}$ values of Figure 8 are not confirmed by individual cell I–V curves, but may be sufficient for approximating the relative impact of the distribution of cell $I_{SC}$ on module $I_{SC}$. While the mean cell $I_{SC}$ is reduced by 3.3%, the distribution of cell $I_{SC}$ also broadens substantially, with the standard deviation increasing from 0.001 to 0.007. The widely used definition of mismatch loss (L) in a module with n series-connected cells, ignoring any additional series resistance due to interconnection or changes in cell current due to encapsulation, is the sum of the STC maximum power of each cell ($p_i$) and the actual $P_{MP}$ of the module [50]:

$$L = \frac{\sum_{i=1}^{n} p_i - P_{MP}}{\sum_{i=1}^{n} p_i}$$

| | $I_{SC}$ | | | $0.1 \times I_{SC}$ | | |
|---|---|---|---|---|---|---|
| | Initial | End of Detection phase | End of Regeneration phase | Initial | End of Detection phase | End of Regeneration phase |
| U* | | | | | | |
| P* | | | | | | |
| S | | | | | | |
| K | | | | | | |
| J | | | | | | |
| R | | | | | | |
| T | | | | | | |
| F | | | | | | |

**FIGURE 7** EL images taken at $I_{SC}$ (left) and $0.1 \times I_{SC}$ (right) of a representative module of each type before the test, at the end of the detection phase, and at the end of the regeneration phase. Images are unscaled, but wherever possible we have selected images with consistent current injection and camera exposure times throughout the test, and performed vignette correction. Intentional LETID-sensitive module types are marked with asterisks and shaded red and LETID-insensitive module types are shaded gray as in Figure 6. Unfortunately, no images are available of any type S module after regeneration [Colour figure can be viewed at wileyonlinelibrary.com]

We use the open-source Python library PVMismatch to model the module with the extracted cell $J_0$ and $I_{SC}$ estimate distributions [51]. First, we calculate the I–V curve of each cell operating independently using a two-diode equation. In this two-diode equation, we set the first diode parameter ($J_{01}$) and the $I_{SC}$ for each cell to the extracted $J_0$ and estimated $I_{SC}$ from the EL analysis. The sum of each cell's two-diode equation results in $\Sigma p_i$. The cells are then modeled together as a module to determine $P_{MP}$. Modeled mismatch losses L for the module of Figure 8 are listed in Table 3, normalized to module $P_{MP}$ in week 0.

The modeled module loses 8.24% $P_{MP}$; most of this is simply due to the cumulative losses in $p_i$ of the cells as evidenced by the large change in normalized $\Sigma p_i$. Mismatch loss in the module roughly triples, from 0.03% to 0.09%, but is still insignificant compared to the power loss due to cell degradation. Of the modeled power loss (8.24% $P_{MP}$), less than 1% of this is due to mismatch (0.06% $P_{MP}$). Power loss in the module is primarily due to the cumulative degradation of the cells, and not due to mismatch brought about by non-uniform degradation.

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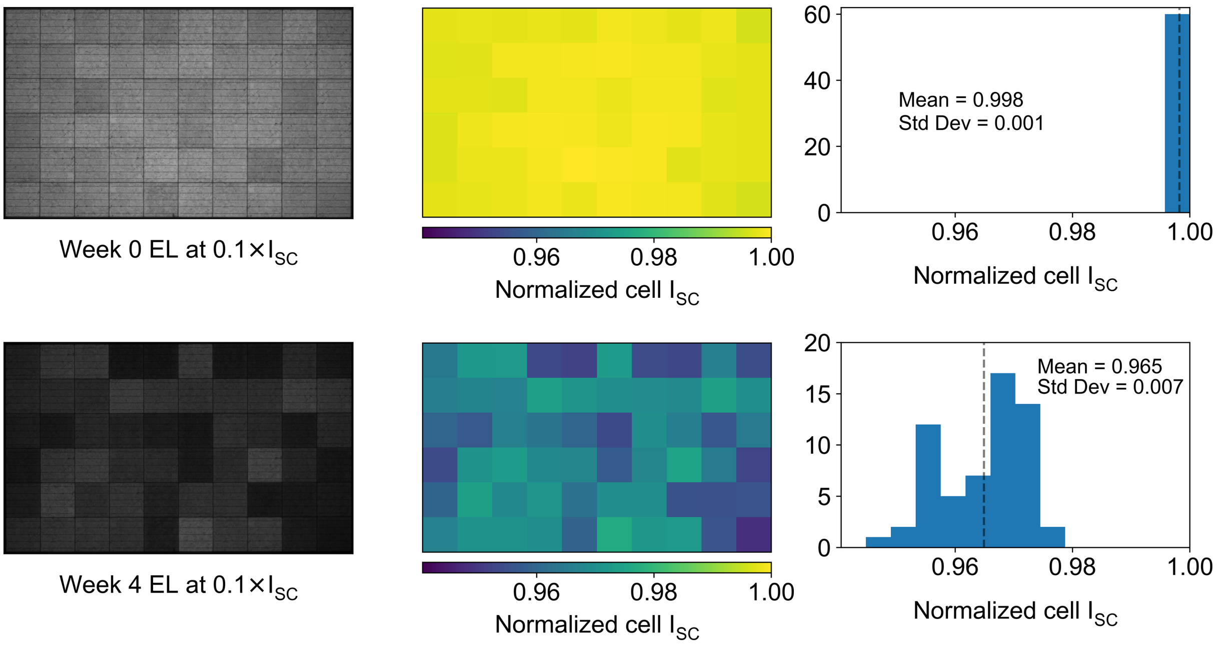


**FIGURE 8** Top row: EL image of a representative type P* module before LETID stress (current injection 0.1 × $I_{SC}$); Estimated cell $I_{SC}$ from EL normalized to the maximum; histogram of estimated cell $I_{SC}$, the dotted line indicates the mean. Bottom row: the same module after 4 weeks of detection-phase LETID stress

**TABLE 3** Mismatch losses calculated for the module of Figure 8

| | Normalized $P_{MP}$ | Normalized $\sum p_i$ | L |
|---|---|---|---|
| Week 0 | 1 | 1.0003 | 0.0003 |
| Week 4 | 0.9176 | 0.9184 | 0.0009 |
| Percentage power loss | 8.24% | 8.19% | 0.06% |

This small impact of mismatch loss is perhaps unsurprising: Fornies et al. showed, for one cell type manufactured into 72-cell modules, that a six-fold increase in the standard deviation of cell $I_{SC}$ did not meaningfully increase L. On the other hand, in other cells, they found mismatch losses of more than 1% in modules where the cell I–V curves varied around the maximum power point, characterized by variation in cell $I_{MP}$ and FF [52]. Therefore, appropriate mismatch modeling requires knowledge of cell $I_{MP}$, FF, and related diode parameters, which cannot be readily estimated from EL images in the way we estimated $I_{SC}$ here. The $I_{SC}$ estimation necessarily relies on assumptions that might cause it to be inaccurate in absolute terms, but conceivably provides a realistic distribution of relative cell $I_{SC}$ values in degraded modules to explore the potential for mismatch. The small modeled mismatch loss presented here is an estimate, and would be improved with better knowledge of the individual cells' I–V behavior near the maximum power point, rather than relying on estimated cell $I_{SC}$. Furthermore, the absolute values and distribution of cell I–V parameters not mentioned so far can also affect mismatch, especially in shaded and low-light field conditions: these include shunt resistance ($R_{SH}$) and reverse bias breakdown voltage ($V_{br}$) [53, 54]. Future work on LETID-affected modules could better estimate these quantities to construct accurate cell-level I–V curves, and better understand the role of mismatch loss on overall power and energy yield loss.

## 5 | COMPARING THIS WORK WITH THE ULTIMATE IEC TS 63342 PROTOCOL

Since the initial inception of this work, the project of drafting the IEC TS proceeded on a parallel but separate track from the interlaboratory test, with some overlap of the participants in each project. Over the course of the drafting process, the TS protocol evolved to be somewhat different than the protocol used in the interlaboratory test.

In particular, the TS protocol reduces the test from 4 weeks of injection at 75°C to 2 weeks, and accelerates the initial stages of LETID by doubling the prescribed dark current injection to 2 × ($I_{SC}$ − $I_{MP}$). LETID has been shown to increase linearly with excess carrier concentration (Δn), so doubling the current would be expected to double the initial degradation rate ($R_{deg,\ t=0}$) [39, 55]. After t = 0, in the case of 2 × ($I_{SC}$ − $I_{MP}$), the minority carrier lifetime and Δn degrade more quickly, therefore reducing $R_{deg}$ more quickly. The net effect of doubling the current is likely to be a modest acceleration in LETID over the 2-week period, and will have the practical effect of expediting the test. For modules that exhibit large power loss (>3%) after 2 weeks of LETID stress and have not yet reached the point of degradation saturation, the TS allows for an extra week of stress to better estimate the maximum LETID susceptibility. The TS makes a

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binary distinction between modules: those that exhibit ≥3% power loss are deemed "LETID-sensitive."

The TS protocol also adds a mandatory BO-LID preconditioning step ($I_{SC}$ at less than 30°C for 24 h) prior to LETID stress, motivated by the need to distinguish LETID from BO-LID. While any BO-LID induced in the preconditioning step should be expected to recover partly during LETID stress, the amount of BO-LID observed in the preconditioning step gives an indication of the maximum masking of LETID by BO recovery [40].

Finally, the TS does not specify a separate, accelerated regeneration phase as in the interlaboratory test. Instead, it provides a method for detecting when modules enter regeneration via analysis of the dark voltage across the module, and allows for the test to be stopped at that point. The absence of complete regeneration in the TS could create a potential issue if modules under test also undergo irreversible, non-LETID degradation: non-LETID degradation interpreted as LETID would over-estimate the LETID sensitivity of the module. Section 4.1 discussed non-LETID degradation; we estimate that up to ~1% power loss might occur in some products due to degradation other than LETID. Additionally, as seen in this and other work, regeneration rates and extents vary across different module types. By not observing complete regeneration, we have incomplete understanding of the long-term energy yield impact of LETID.

## 6 | CONCLUSION

This paper presented the rationale, format, and results of an international interlaboratory cross-comparison on LETID in solar modules. We present several notable findings.

First, the protocol here successfully induced LETID in modules as expected, as modules degraded and regenerated in a manner consistent with LETID. The test might induce a small amount of non-LETID degradation in some modules, but not all. Non-LETID degradation can be distinguished from LETID by performing regeneration. For most modules in the test, the 4-week duration of the LETID detection phase was long enough to nearly reach the point of saturation. The exceptions to this were two module types intentionally engineered for LETID sensitivity.

In general, the cross-lab reproducibility of the detection phase was good, with standard deviation results across labs in agreement to within ±1% $P_{MP}$ even in heavily LETID-sensitive samples. In samples with less LETID sensitivity, the reproducibility appears to be better than ±1%.

The extent of LETID presented here should not be interpreted as typical for the industry at large. The sample set assembled here included both intentional LETID-sensitive modules and prototype modules. Global researchers have published many promising strategies for reducing or eliminating LETID (discussed in Section 2), and there is evidence both in this work and elsewhere that manufacturers in recent years have adopted these strategies [1, 4]. Some modules in this work showed essentially no LETID sensitivity. Still, LETID risk is not a fully resolved matter as new wafer types and cell architectures are being adopted which might be LETID-sensitive.

Power losses in LETID-sensitive modules were driven by roughly similar-magnitude losses in voltage and current. In some modules, but not all, FF also degrades and recovers in a manner that seems consistent with LETID. In other modules, FF seems to be unaffected by LETID stress. The reason for this curious inconsistent relationship between LETID and module FF is still an open question.

The degradation in LETID-sensitive modules varies cell-to-cell, which is readily visible in EL images. This raises the question of current losses due to degradation-induced mismatch. In an attempt to extract cell-level data from EL images and model mismatch, we found that mismatch plays only a small role, and most module-level current loss comes from the cumulative degradation of cells' current. However, the cell-level parameter extractions here are only estimates and are thus likely insufficient for robust mismatch modeling. The origin of cell-to-cell variation and potential mismatch in degraded modules could be a topic for future work.

This study should help stakeholders interpret results from the forthcoming IEC Technical Specification on LETID in modules, IEC TS 63342 ED1. The TS protocol differs from the procedure used in this work, primarily in that the current injection is doubled and the test duration is shortened. The increased current will accelerate LETID degradation in the TS, but the conclusions on reproducibility and I–V parameter loss from this work are still germane.

This work, the forthcoming TS, and the advancing scientific understanding of LETID will help mitigate the physical and financial effects of LETID. Manufacturers will be able to test for LETID and engineer LETID-free cells and modules, module buyers will be able to evaluate potential purchases with confidence, and financial stakeholders will benefit from the reduced risk that follows from that confidence.

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## CONFLICT OF INTERESTS

The authors declare no conflict of interests.

## DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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## REFERENCES

1. Chen D, Vaqueiro Contreras M, Ciesla A, et al. Progress in the understanding of light- and elevated temperature-induced degradation in silicon solar cells: A review. *Prog Photovoltaics Res Appl*. 2021;29: 1180-1201. doi:10.1002/pip.3362
2. Kersten F, Engelhart P, Ploigt H-C, et al. Degradation of multicrystalline silicon solar cells and modules after illumination at elevated temperature. *Sol Energy Mater Sol Cells*. 2015;142:83-86. doi:10.1016/j.solmat.2015.06.015
3. Hallam BJ, Hamer PG, Ciesla née Wenham AM, Chan CE, Stefani BV, Wenham S. Development of advanced hydrogenation processes for silicon solar cells via an improved understanding of the behaviour of hydrogen in silicon. *Prog Photovoltaics Res Appl*. 2020;28:1217-1238. doi:10.1002/pip.3240
4. Sen C, Chan C, Chen D, et al. Different Extent and Behaviour of LeTID in the Past and Current PERC Silicon Solar Cells. *Asia-Pacific Sol Res Conf*. 2019;2:3-6.
5. Pander M, Luka T, Jäckel B, et al. Prediction of Potential Power/Yield Loss from LeTID Susceptible Modules. In: *36th Eur Photovolt Sol Energy Conf Exhib*; 2019:810-815. doi:10.4229/EUPVSEC20192019-4BO.12.1
6. Dupuis J, Plessis G, El Hajje G, et al. Light- and elevated temperature-induced degradation impact on bifacial modules using accelerated aging tests, electroluminescence, and photovoltaic plant modeling. *Prog Photovoltaics Res Appl*. 2021;29:694-704. doi:10.1002/pip.3345
7. Ramspeck K, Zimmermann S, Nagel H, et al. Light Induced Degradation of Rear Passivated Mc-Si Solar Cells. In: *27th Eur Photovolt Sol Energy Conf Exhib*; 2012:861-865.
8. Kwapil W, Schon J, Niewelt T, Schubert MC. Temporary Recovery of the Defect Responsible for Light- and Elevated Temperature-Induced Degradation: Insights Into the Physical Mechanisms Behind LeTID. *IEEE J Photovoltaics*. 2020;10:1591-1603. doi:10.1109/JPHOTOV.2020.3025240
9. Luka T, Turek M, Hagendorf C. Defect formation under high temperature dark-annealing compared to elevated temperature light soaking. *Sol Energy Mater Sol Cells*. 2018;187:194-198. doi:10.1016/j.solmat.2018.06.043
10. Sio HC, Kang D, Zhang X, Yang J, Jin J, Macdonald D. The Role of Dark Annealing in Light and Elevated Temperature Induced Degradation in p-Type Mono-Like Silicon. *IEEE J Photovoltaics*. 2020;10:992-1000. doi:10.1109/JPHOTOV.2020.2993653
11. Niewelt T, Post R, Schindler F, Kwapil W, Schubert MC. Investigation of LeTID where we can control it – Application of FZ silicon for defect studies. In: *AIP Conf Proc*; 2019:140006. doi:10.1063/1.5123893
12. Sio HC, Wang H, Wang Q, et al. Light and elevated temperature induced degradation in p-type and n-type cast-grown multicrystalline and mono-like silicon. *Sol Energy Mater Sol Cells*. 2018;182:98-104. doi:10.1016/j.solmat.2018.03.002
13. Søndenå R, Haug H, You CC, Zhu J, Wiig MS. Evolution of defect densities with height in a HPMC-Si ingot. In: *AIP Conf Proc*, 2019; 140010. doi:10.1063/1.5123897
14. Wehmeier N, Fischer G, Herlufsen S, et al. Kinetics of the Light and Elevated Temperature Induced Degradation and Regeneration of Quasi-Monocrystalline Silicon Solar Cells. *IEEE J Photovoltaics*. 2021; 11:890-896. doi:10.1109/JPHOTOV.2021.3066239
15. Cheng S, Ji F, Zhou C, et al. Kinetics of light and elevated temperature-induced degradation in cast mono p-type silicon. *Sol Energy*. 2021;224:1000-1007. doi:10.1016/j.solener.2021.06.054
16. Grant NE, Scowcroft JR, Pointon AI, Al-Amin M, Altermatt PP, Murphy JD. Lifetime instabilities in gallium doped monocrystalline PERC silicon solar cells. *Sol Energy Mater Sol Cells*. 2020;206:110299. doi:10.1016/j.solmat.2019.110299
17. Grant NE, Altermatt PP, Niewelt T, et al. Gallium-Doped Silicon for High-Efficiency Commercial Passivated Emitter and Rear Solar Cells. *Sol RRL*. 2021;5:2000754. doi:10.1002/solr.202000754
18. Winter M, Walter D, Schmidt J. Carrier Lifetime Degradation and Regeneration in Gallium- and Boron-Doped Monocrystalline Silicon Materials. *IEEE J Photovoltaics*. 2021;11:866-872. doi:10.1109/JPHOTOV.2021.3070474
19. Jafari S, Hameiri Z. Investigation of Light-Induced Degradation in Ga- and In-Doped Cz Silicon. In: *2021 IEEE 48th Photovolt Spec Conf* IEEE; 2021:0814-0817. doi:10.1109/PVSC43889.2021.9518574
20. Chen D, Hamer PG, Kim M, et al. Hydrogen induced degradation: A possible mechanism for light- and elevated temperature- induced degradation in n-type silicon. *Sol Energy Mater Sol Cells*. 2018;185: 174-182. doi:10.1016/j.solmat.2018.05.034
21. Wright B, Madumelu C, Soeriyadi A, Wright M, Hallam B. Evidence for a Light-Induced Degradation Mechanism at Elevated Temperatures in Commercial N-Type Silicon Heterojunction Solar Cells. *Sol RRL*. 2020;4:2000214. doi:10.1002/solr.202000214
22. Madumelu C, Wright B, Soeriyadi A, et al. Investigation of light-induced degradation in N-Type silicon heterojunction solar cells during illuminated annealing at elevated temperatures. *Sol Energy Mater Sol Cells*. 2020;218:110752. doi:10.1016/j.solmat.2020.110752
23. Ciesla neé Wenham A, Wenham S, Chen R, et al. Hydrogen-Induced Degradation. In: *2018 IEEE 7th World Conf. Photovolt. Energy Convers. (A Jt. Conf. 45th IEEE PVSC, 28th PVSEC 34th EU PVSEC)*. Vol.2018. IEEE:0001-0008. doi:10.1109/PVSC.2018.8548100
24. Eberle R, Kwapil W, Schindler F, Glunz SW, Schubert MC. Firing temperature profile impact on light induced degradation in multicrystalline silicon. *Energy Procedia*. 2017;124:712-717. doi:10.1016/j.egypro.2017.09.082
25. Chan C, Fung TH, Abbott M, et al. Modulation of Carrier-Induced Defect Kinetics in Multi-Crystalline Silicon PERC Cells Through Dark Annealing. *Sol RRL*. 2017;1:1600028. doi:10.1002/solr.201600028
26. Sharma R, Aberle AG, Li JB. Optimization of Belt Furnace Anneal to Reduce Light and Elevated Temperature Induced Degradation of Effective Carrier Lifetime of P-Type Multicrystalline Silicon Wafers. *Sol RRL*. 2018;2:1-8. doi:10.1002/solr.201800070

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27. Yli-Koski M, Serué M, Modanese C, Vahlman H, Savin H. Low-temperature dark anneal as pre-treatment for LeTID in multi-crystalline silicon. *Sol Energy Mater Sol Cells*. 2019;192:134-139. doi:10.1016/j.solmat.2018.12.021
28. Varshney U, Abbott M, Ciesla A, et al. Evaluating the Impact of SiNx Thickness on Lifetime Degradation in Silicon. *IEEE J Photovoltaics*. 2019;9:601-607. doi:10.1109/JPHOTOV.2019.2896671
29. Sen C, Chan C, Hamer P, et al. Eliminating light- and elevated temperature-induced degradation in P-type PERC solar cells by a two-step thermal process. *Sol Energy Mater Sol Cells*. 2020;209:110470. doi:10.1016/j.solmat.2020.110470
30. Varshney U, Chan C, Hoex B, et al. Controlling Light- And Elevated-Temperature-Induced Degradation with Thin Film Barrier Layers. *IEEE J Photovoltaics*. 2020;10:19-27. doi:10.1109/JPHOTOV.2019.2945199
31. Krauß K, Brand AA, Fertig F, Rein S, Nekarda J. Fast Regeneration Processes to Avoid Light-Induced Degradation in Multicrystalline Silicon Solar Cells. *IEEE J Photovoltaics*. 2016;6:1427-1431. doi:10.1109/JPHOTOV.2016.2598273
32. Bredemeier D, Walter DC, Pernau T, Romer O, Schmidt J. Production Compatible Remedy Against LeTID in High-Performance Multicrystalline Silicon Solar Cells. In: *35th Eur Photovolt Sol Energy Conf Exhib*; 2018:406-409. doi:10.4229/35thEUPVSEC20182018-2CO.9.4
33. Yao Z, Zhang D, Wu J, Jiang F, Xing G, Su X. Evolution of LeTID defects in industrial multi-crystalline silicon wafers under laser illumination - Dependency of wafer position in brick and temperature. *Sol Energy Mater Sol Cells*. 2020;218:110735. doi:10.1016/j.solmat.2020.110735
34. Vahlman H, Roder S, Nekarda J, Rein S. High-intensity illumination treatments against LeTID – Intensity and temperature dependence of stability and inline feasibility. *Sol Energy Mater Sol Cells*. 2021;223:110978. doi:10.1016/j.solmat.2021.110978
35. Chen C, Yang H, Wang J, Lv J, Wang H. Investigating the viability of PERC solar cells fabricated on Ga- instead of B-doped monocrystalline silicon wafer. *Sol Energy Mater Sol Cells*. 2021;227:111134. doi:10.1016/j.solmat.2021.111134
36. Kersten F, Fertig F, Petter K, et al. System performance loss due to LeTID. *Energy Procedia*. 2017;124:540-546. doi:10.1016/j.egypro.2017.09.260
37. Deceglie MG, Silverman TJ, Johnston SW, et al. Light and Elevated Temperature Induced Degradation (LeTID) in a Utility-Scale Photovoltaic System. *IEEE J Photovoltaics*. 2020;10:1084-1092. doi:10.1109/JPHOTOV.2020.2989168
38. Vargas C, Coletti G, Chan C, Payne D, Hameiri Z. On the impact of dark annealing and room temperature illumination on p-type multicrystalline silicon wafers. *Sol Energy Mater Sol Cells*. 2019;189:166-174. doi:10.1016/j.solmat.2018.09.018
39. Wyller GM, Wiig M, Due-Sorensen I, Sondena R. The Influence of Minority Carrier Density on Degradation and Regeneration Kinetics in Multicrystalline Silicon Wafers. *IEEE J Photovoltaics*. 2021;11:878-889. doi:10.1109/JPHOTOV.2021.3078367
40. Koentopp MB, Kersten F, Herzog E. Towards an IEC LETID Test Standard: Procedures, kinetics, and separation of B-O degradation from LETID. In: *2020 PV Reliab Work Febr 26, 2020 Proc*; 2020:339. https://www.nrel.gov/docs/fy20osti/77331.pdf
41. Monokroussos C, Salis E, Etienne D, et al. Electrical characterization intercomparison of high-efficiency c-Si modules within Asian and European laboratories. *Prog Photovoltaics Res Appl*. 2019;27:603-622. doi:10.1002/pip.3134
42. Ciesla A, Kim M, Wright M, et al. A case study on accelerated light- and elevated temperature-induced degradation testing of commercial multi-crystalline silicon passivated emitter and rear cell modules. *Prog Photovoltaics Res Appl*. 2021;29:1202-1212. doi:10.1002/pip.3455
43. Wagner M, Wolny F, Hentsche M, et al. Correlation of the LeTID amplitude to the Aluminium bulk concentration and Oxygen precipitation in PERC solar cells. *Sol Energy Mater Sol Cells*. 2018;187:176-188. doi:10.1016/j.solmat.2018.06.009
44. Chen D, Kim M, Stefani BV, et al. Evidence of an identical firing-activated carrier-induced defect in monocrystalline and multi-crystalline silicon. *Sol Energy Mater Sol Cells*. 2017;172:293-300. doi:10.1016/j.solmat.2017.08.003
45. Zhang S, Peng J, Qian H, et al. The Impact of Thermal Treatment on Light-Induced Degradation of Multicrystalline Silicon PERC Solar Cell. *Energies*. 2019;12:416. doi:10.3390/en12030416
46. Field H, Gabor AM. Cell binning method analysis to minimize mismatch losses and performance variation in Si-based modules. In: *Conf. Rec. Twenty-Ninth IEEE Photovolt. Spec. Conf. 2002*. IEEE; 2002:418-421. doi:10.1109/PVSC.2002.1190548
47. Herguth A, Derricks C, Sperber D. A Detailed Study on Light-Induced Degradation of Cz-Si PERC-Type Solar Cells: Evidence of Rear Surface-Related Degradation. *IEEE J Photovoltaics*. 2018;8:1190-1201. doi:10.1109/JPHOTOV.2018.2850521
48. Rajput AS, Ho JW, Zhang Y, Nalluri S, Aberle AG. Quantitative estimation of electrical performance parameters of individual solar cells in silicon photovoltaic modules using electroluminescence imaging. *Sol Energy*. 2018;173:201-208. doi:10.1016/j.solener.2018.07.046
49. McIntosh KR, Baker-Finch SC. OPAL 2: Rapid optical simulation of silicon solar cells. In: *2012 38th IEEE Photovolt Spec Conf* IEEE; 2012:000265-000271. doi:10.1109/PVSC.2012.6317616
50. Evans R, Kim KH, Wang X, et al. Simplified technique for calculating mismatch loss in mass production. *Sol Energy Mater Sol Cells*. 2015;134:236-243. doi:10.1016/j.solmat.2014.11.036
51. Mikofski M., Meyers B., Chaudhari C., *PVMismatch v4.1 (Nepal Negroni)*, (2018). https://github.com/SunPower/PVMismatch (accessed July 1, 2021).
52. Forniés E, Naranjo F, Mazo M, Ruiz F. The influence of mismatch of solar cells on relative power loss of photovoltaic modules. *Sol Energy*. 2013;97:39-47. doi:10.1016/j.solener.2013.08.004
53. Bishop JW. Computer simulation of the effects of electrical mismatches in photovoltaic cell interconnection circuits. *Sol Cells*. 1988;25:73-89. doi:10.1016/0379-6787(88)90059-2
54. Alonso-Garcia MC, Ruiz J, Chenlo F. Experimental study of mismatch and shading effects in the I–V characteristic of a photovoltaic module. *Sol Energy Mater Sol Cells*. 2006;90:329-340. doi:10.1016/j.solmat.2005.04.022
55. Kwapil W, Niewelt T, Schubert MC. Kinetics of carrier-induced degradation at elevated temperature in multicrystalline silicon solar cells. *Sol Energy Mater Sol Cells*. 2017;173:80-84. doi:10.1016/j.solmat.2017.05.066
56. Hoffmann M, Doll B, Talkenberg F, Brabec CJ, Maier AK, Christlein V. Fast and Robust Detection of Solar Modules in Electroluminescence Images. In: Vento M, Percannella G, eds. *Comput. Anal. Images Patterns. CAIP 2019. Lect. Notes Comput. Sci.* Cham: Springer International Publishing; 2019:519-531. doi:10.1007/978-3-030-29891-3_46
57. PVInspect, (n.d.). https://github.com/ma0ho/pvinspect (accessed July 1, 2021).
58. Cuevas A. The Recombination Parameter J0. *Energy Procedia*. 2014;55:53-62. doi:10.1016/j.egypro.2014.08.073
59. Sproul AB, Green MA. Improved value for the silicon intrinsic carrier concentration from 275 to 375 K. *J Appl Phys*. 1991;70:846-854. doi:10.1063/1.349645
60. Gatz S, Müller J, Dullweber T, Brendel R. Analysis and Optimization of the Bulk and Rear Recombination of Screen-Printed PERC Solar Cells. *Energy Procedia*. 2012;27:95-102. doi:10.1016/j.egypro.2012.07.035
61. Hovel HJ. *Semiconductors and Semimetals Volume 11: Solar Cells*. Academic Press; 1975. doi:10.1016/S0080-8784(13)62756-8


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62. photovoltaic, (n.d.). https://github.com/pvedu/photovoltaic (accessed July 1, 2021).

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## APPENDIX A

### A.1 | Estimation of cell $I_{SC}$ from module electroluminescence images

Module EL images are first corrected for camera vignette distortion by dividing each image by a normalized image collected using uniform emission from an integrating sphere. Individual cells are segmented from the module image with the open-source Python package PVInspect [56, 57]. Following the method of Rajput et al., an image at known low current is used to calculate a spatially-dependent saturation current density $J_0(x,y)$ of each cell that is considered to be independent of bias conditions [48]. The effective saturation current density of the *i*th cell $J_{0,i}$ is taken to be the mean of the cell's $J_0(x,y)$ distribution.

With $J_{0,i}$, and assuming low injection and that the device is limited by defect-assisted recombination in the bulk, we can estimate a lifetime ($\tau$) and diffusion length (L) for each cell [58]:

$$\tau_i = q\frac{n_i^2 W}{N_A J_{0,i}}$$

$$L_i = \sqrt{D\tau_i}$$

where $n_i$ is the intrinsic carrier concentration at 298.15 K [59], $N_A$ is the p-type doping concentration, assumed to be $1.5 \times 10^{16}$ $cm^{-3}$ (the equivalent of 1 Ω-cm bulk resistivity), W is the wafer thickness, assumed to be 180 μm, and D is the minority carrier diffusivity, assumed to be 27 $cm^2 s^{-1}$. With L, D, and assuming an effective rear surface recombination velocity S of 90 cm/s [60], a depth-dependent collection probability profile $\psi(z)$ can be calculated for the base region of each cell, using the expression from [61] as implemented by the Python library photovoltaic [62].

A depth-dependent optical generation profile G(z) is calculated using OPAL 2 for a 180-μm-thick textured wafer under normal-incident AM1.5G illumination, with all other inputs set to OPAL 2 defaults [49]. Integrating $\psi(z)$ and G(z) through the wafer provides an estimate of light-generated current density, which is taken to be $I_{SC}$ of a cell with active area of 243 $cm^2$.

$$I_{SC,i} = (243\,cm^2) \times q\int_0^W G(z)\,\psi(z)_i\,dz$$

Note that this estimation is imprecise in a number of ways. Besides the necessary assumptions about the c-Si cell properties listed above, we do not attempt to account for collection in the emitter or space-charge region of the device, and we rely on an optical generation model that does not consider the optical impact of module materials (e.g., front glass and encapsulant). We treat the total photogenerated current as the short-circuit current. The $J_0$ extraction method uses a one-diode model with ideality factor of one, while the mismatch model below uses a two-diode model [48, 51]. The use of the extracted global $J_0$ is an oversimplification of the physical reality of the device. Following the philosophy of Cuevas [58], we accept these limitations and treat the extracted $J_0$ as an indicator of the increasing bulk recombination in LETID-affected devices, all other things being equal. The purpose of this $J_0$ extraction and $I_{SC}$ estimation was not to accurately derive an absolute quantity for $I_{SC}$ for each cell, but to derive a quasi-realistic distribution of parameters in nonuniformly degraded modules to study the potential for mismatch loss.

### A.2 | Mismatch model

The extracted parameter estimations are used to create a module object in PVMismatch [51]. Each cell in the module is defined by its own two-diode model, which uses as inputs $I_{SC}$ at reference conditions, first and second diode saturation currents ($I_{01}$ and $I_{02}$), series and shunt resistances, reverse breakdown coefficients, and temperature coefficients. We assume a cell area of 243 $cm^2$ and assign $I_{SC}$ and $I_{01}$ to the $I_{SC,i}$ and $J_{0,i}$ derived from EL images above and leave all other two-diode model parameters as PVMismatch defaults.

Assuming STC irradiance and temperature (1000 W/$m^2$, 25°C), each cell's two-diode I–V curve is calculated and summed to give $\Sigma p_i$. The cells are then modeled together as a module with PVMismatch to determine $P_{MP}$ and mismatch loss.

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