III-V PV Cell Core Capability: Final Technical Report

Myles A. Steiner

National Renewable Energy Laboratory

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National Renewable Energy Laboratory
15013 Denver West Parkway
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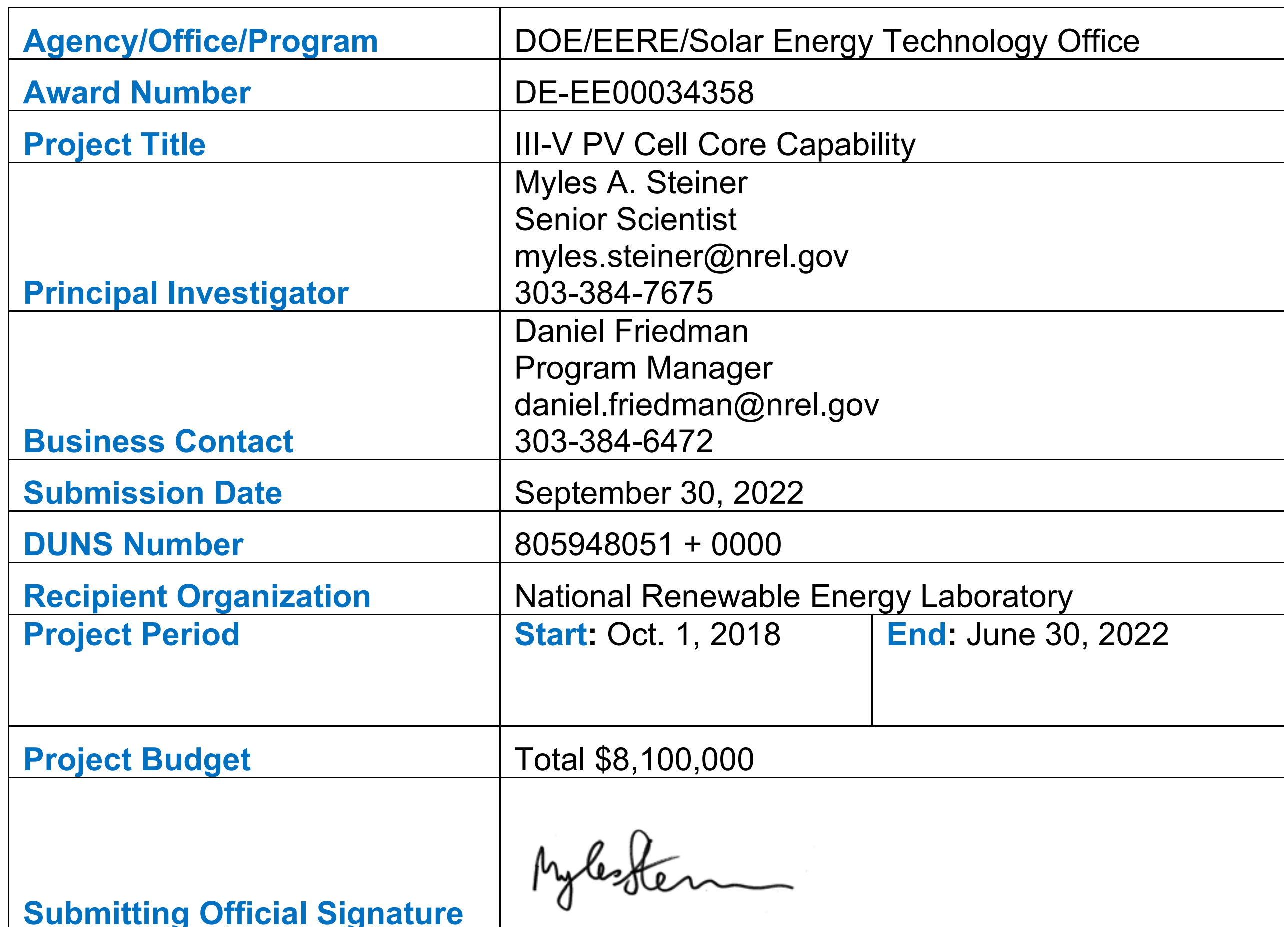
Final Technical Report (FTR)



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Business Contact	Daniel Friedman Program Manager daniel.friedman@nrel.gov 303-384-6472
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Executive Summary:

This Core project developed III-V photovoltaics for terrestrial applications, focusing on high efficiency architectures and on cost-reduction. III-V cells have demonstrated the highest efficiencies of any photovoltaic materials system, reaching over 30% for two-junction tandems and over 47% for more complex concentrator cells. III-Vs have other characteristics that make them attractive to a range of terrestrial and near-terrestrial energy applications, such as being direct absorbers, lightweight and potentially flexible, having good thermal coefficient, good radiation hardness, and being very stable and durable. Cost is a key challenge with III-Vs, however, because of the high cost of epitaxy and processing.

This project was divided into three tasks. The first task investigated cell architectures that continue to push the limits of one-sun efficiency. We focused on a three-junction inverted cell with two lattice-matched junctions and then a third, lattice-mismatched junction. Optically-thick, strain-balanced quantum wells were developed and added to the middle junction in order to balance the photocurrents more optimally. We showed how in-situ annealing of the GaInP top cell improved the voltage and current collection, and we strained the AlInP front window to further improve absorption. We demonstrated a world-record 39.5% one-sun efficiency with this architecture.

The second task continued our development of dynamic hydride vapor phase epitaxy (HVPE), a growth technique that uses elemental metallic group-III sources, high growth rates and good source utilization to substantially reduce the cost of the epitaxy. This project focused on the development and integration of the aluminum-containing alloys AlGaAs, AlInP and AlGaInP that are key to the demonstration of the highest efficiency tandems. An external chamber was added to the HVPE reactor and we investigated growth conditions that promoted the formation of $AlCl_3$ instead of AlCl. AlGaAs and Al(Ga)InP alloys were grown over the full range of Al fraction. We incorporated AlInP window layers into GaAs and GaInP/GaAs cells, improving the photocurrent by 1.3 mA/cm^2 in the GaAs single-junction cell and 1.0 mA/cm^2 in the GaInP top cell, and demonstrated efficiencies of 26% and 28%, respectively.

The third task investigated pathways to reduce the cost of the growth substrate. Broadly speaking, cost reduction can arise from exfoliating the solar cell material from the substrate and then reusing the substrate, or from using a very inexpensive substrate in the first place. We established informal collaborations with external partners to engage in exploratory work to grow material on potentially reusable or inexpensive substrates, showing promising directions in several of them. We used nanoimprint lithography to pattern GaAs substrates with SiO_2 stripes and then overgrow coalesced material, in order to in-grow a weak layer that could aid in a subsequent exfoliation process. We also investigated growth on layered two-dimensional Bi_2Se_3, and demonstrated coalesced GaAs on v-grooved silicon, with a threading dislocation density of $3x10^6$ cm^{-2}.

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4. Background:

III-V solar cells have demonstrated the highest efficiencies of any PV technology, reaching over 30% for two-junction tandems [1] and over 47% for more complex concentrator cells [2]. Historically, a significant body of the research into III-Vs has focused on space applications, taking advantage of the high efficiency, specific power and radiation hardness of III-Vs; and on terrestrial concentrator (CPV) applications, taking advantage of the high efficiency. CPV was viewed as a promising pathway to reduce LCOE, but was undercut by the significant drop in cost of silicon PV. More recently, research has turned toward the use of III-Vs for one-sun terrestrial and near-terrestrial energy applications. This includes research on lowering the cost of epitaxy by hydride vapor phase epitaxy [3-7]; lowering the cost of substrates by growing on silicon [8, 9]; exfoliating the semiconductor layers from the substrate [10, 11] in order to potentially reuse the substrate; and improving the efficiency of the cells by extending the range of absorption [12, 13].

5. Project Objectives:

The objectives of the project were to develop high efficiency one-sun cells to demonstrate advanced materials and architectures, including improved understanding of the science of lattice-mismatch and multiple quantum wells; demonstrate aluminum-containing alloys grown by HVPE that passivate the absorber materials and lead to higher current densities; and demonstrate high quality III-V growth on a range of

inexpensive substrates. The project was divided into three major tasks, all of which bear on the goal of fabricating efficient and lower-cost III-V solar cells.

Task 1: Development of III-V materials and device architectures for high-efficiency, multijunction one-sun solar cells – the final goal of this task was to demonstrate a 40% one-sun, three-junction solar cell. Work included development of optically thick quantum wells to extend the absorption edge of the middle cell in order to more optimally balance the absorption of incident light. We also worked on thinning graded buffer layers to change the lattice-constant, and incorporated work on light-trapping for thin cells

- Q2: Develop window layer for a GaInP cell with <1.7 mA/cm2 loss, without loss of Voc.
- Q4: 33% one-sun cell, lattice-matched to GaAs
- Q6: Demonstrate GaAs MQW solar cell with >2.5 mA/cm2 improvement in Jsc and >80% EQE plateau in the QWs, using semiconductor optics to increase the reflectance
- Q9: Demonstrate a 1-eV GaInAs cell with <1.5-μm thick CGB and Woc<0.45 V at one-sun.
- Q12: 40% one-sun solar cell, with no more than one lattice-mismatched junction

Task 2: Continued development of Hydride Vapor Phase Epitaxy (HVPE) for PV applications, focusing on the growth of aluminum-containing alloys – the final goal of this task was to demonstrate a GaAs cell with an AlInP window layer, with better performance than a baseline cell with a GaInP window. Work required the design and engineering of new infrastructure for the HVPE system, and then detailed studies of the growth kinetics of aluminum-containing alloys.

- Q3: Demonstrate >35% Al content in AlGaAs grown by HVPE, with doping n ≥ $1x10^{18}$ cm^{-3}.
- Q5: Demonstrate HVPE growth of AlGaInP with Al content >10% while maintaining lattice match to the GaAs substrate.
- Q8: Demonstrate an HVPE-grown GaAs solar cell with an Al-containing window layer and Jsc ≥ 28.0 mA/cm^2.
- Q11: Demonstrate HVPE-grown AlInP lattice matched to a GaAs substrate.
- Q12: Demonstrate an HVPE-grown GaAs solar cell with an Al-containing window layer and Jsc ≥ 29.5 mA/cm^2

Task 3: Research into inexpensive substrates for III-V epitaxy, including growth on v-grooved silicon, selective area growth on GaAs, Bi_2Se_3, and other substrates that will be identified over the POP. This wide-ranging task focused on the growth of III-Vs on inexpensive substrates, a key driver for lower-cost III-Vs. The work included collaboration with external partners (universities and industry) to grow on novel substrates, as well as internal work.

- Q1: Identify at least 3 potential external substrate collaborators, with plan of action for growth and characterization
- Q3: Submission of a peer-reviewed publication on the growth of GaAs on Bi2Se3 using diethylzinc to surface-convert the 2D-layered Bi_2Se_3 to ZnSe for the growth and nucleation of GaAs.

- Q7: Demonstrate coalescence of a nearly lattice-matched GaP(N) alloy, or a lattice-mismatched alloy, on v-grooved, unpolished silicon with threading dislocation density <1E7/cm^2 as measured by ECCI.
- Q10: Choose most promising substrate ideas, assess potential and grow a GaAs cell
- Q12: Demonstrate a working III-V PV device on a v-grooved, unpolished silicon substrate, with efficiency >18%, to compare with earlier work and literature reports.

Milestone	Description	Completion date
1.3.1	Identify at least 3 potential external substrate collaborators, with plan of action for growth and characterization	12/31/18
1.1.1	Develop window layer for a GaInP cell with <1.7 mA/cm2 loss, without loss of Voc.	3/29/19
1.2.1	Demonstrate >35% Al content in AlGaAs grown by HVPE, with doping $n \geq 1 \times 10^{18}$ cm^{-3}.	6/28/19
1.3.2	Submission of a peer-reviewed publication on the growth of GaAs on Bi_2Se_3 using diethylzinc to surface-convert the 2D-layered Bi_2Se_3 to ZnSe for the growth and nucleation of GaAs.	9/29/19
1.1.2	33% one-sun cell, lattice-matched to GaAs	12/31/19
2.2.1	Demonstrate HVPE growth of AlGaInP with Al content >10% while maintaining lattice match to the GaAs substrate.	8/28/19
2.1.1	Demonstrate GaAs MQW solar cell with >2.5 mA/cm2 improvement in Jsc and >80% EQE plateau in the QWs, using semiconductor optics to increase the reflectance	6/30/20
2.3.1	Demonstrate coalescence of a nearly lattice-matched GaP(N) alloy, or a lattice-mismatched alloy, on v-grooved, unpolished silicon with threading dislocation density <1E7/cm^2 as measured by ECCI.	6/30/22
2.2.2	Demonstrate an HVPE-grown GaAs solar cell with an Al-containing window layer and $J_{SC} \geq 28.0$ mA/cm^2.	12/31/21
3.1.1	Demonstrate a 1-eV GaInAs cell with <1.5-μm thick CGB and Woc<0.45 V at one-sun.	12/31/20
3.3.1	Choose most promising substrate ideas, assess potential and grow a GaAs cell	12/31/20
3.2.1	Demonstrate HVPE-grown AlInP lattice matched to a GaAs substrate	12/31/19
3.1.2	40% one-sun solar cell, with no more than one lattice-mismatched junction	9/29/21
3.2.2	Demonstrate an HVPE-grown GaAs solar cell with an Al-containing window layer and $J_{SC} \geq 29.5$ mA/cm^2.	12/31/21
3.3.2	Demonstrate a working III-V PV device on a v-grooved, unpolished silicon substrate, with efficiency >18%, to compare with earlier work and literature reports.	Incomplete, but work continues in the FY22-24 Core project

6. Project Results and Discussion:

(This section is organized by task and milestone)

Task 1: Development of III-V materials and device architectures for high-efficiency, multijunction one-sun solar cells

Q2: Develop window layer for a GaInP cell with <1.7 mA/cm2 loss, without loss of Voc.

This task focused on reducing the absorption losses in the window layer of a GaInP top cell, to increase the generated photocurrent and ultimately boost the efficiency of two-junction and three-junction tandem cells. The baseline window layer is $Al_{0.52}In_{0.48}P$. Strategies to reduce window absorption include:

- Thinner AlInP, possibly with an antimony (Sb) surfactant to smooth the epilayers.
- Strained AlInP to raise the bandgap, and possibly including strain-balancing layers
- Bi-layer AlInP / AlGaInP, where photons absorbed in the inner layer are also collected at the junction as photocurrent
- Adding a field to the window, either through a compositional or doping profile
- Chemical passivation of surface after growth

Initial work on the AlInP window looked at thinning the layer to decrease parasitic absorption. Because of the indirect bandgap of AlInP, the thickness should have only a small effect on the absorption, but it is the easiest parameter to tune. The cells studied here were all 1-µm thick rear heterojunction GaInP cells with gold back reflectors. As shown by the dashed lines in Figure 1, this caused a marked decrease in the blue response, likely because the carrier concentration was insufficiently high to prevent complete depletion in the layer. The AlInP was also grown at 4 µm/hr, which may be too fast to ensure a continuous and homogeneous film.

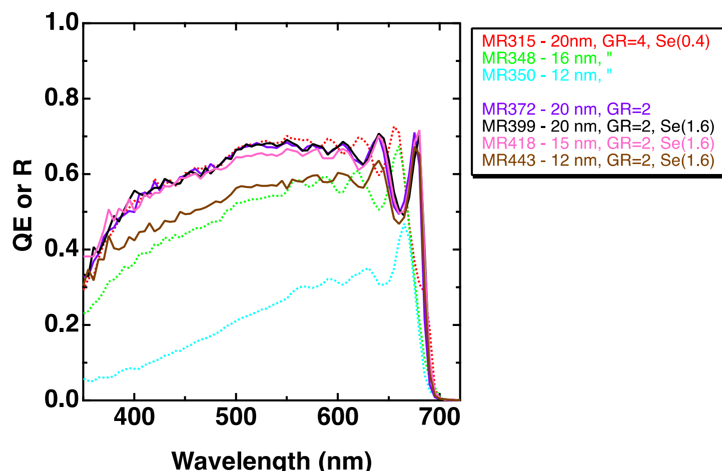


Figure 1 EQE of inverted GaInP top cells, with different thicknesses and growth rates of the AlInP window layer.

The purple and black curves in Figure 1 show data for cells with a lower growth rate of 2 µm/hr (MR372) and then with higher doping, and both cells show the same behavior as the baseline in red. Trying again to thin the layer but this time with lower growth rate and higher doping, we find no change in behavior for a nominally 15 nm window, but lower

EQE for a 12 nm layer. The 12 nm window is possibly inhomogeneous or has pinholes, but it is somewhat surprising that the 15 nm window did not improve the absorption. Thus, thinning the window layer proved ineffective.

Raising the bandgap of the AlInP window leads to a clear increase in short wavelength EQE, as shown in Figure 2. Here, the EQE in the range of 350-550 nm increases as the nominal aluminum content increases from ~52% to ~65%, with a corresponding increase in the short circuit current from ~11.2 mA/cm^2 to ~12.0 mA/cm^2 (with no anti-reflection coating). Further increases in bandgap appear to be limited by the inability to maintain coherent strain in the 20 nm layer.

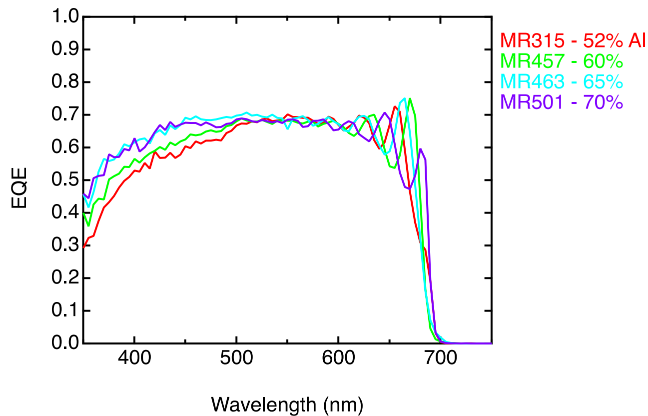


Figure 2 EQE of rear heterojunction GaInP cells with higher aluminum AlInP window layers.

Figure 3 shows EQE and IV curves for the best GaInP cell to date, showing >22% efficiency under the global spectrum at 1000 W/m^2. The voltage is >1.46 V, comparable to baseline cells with GaInP windows and indicating good internal luminescent efficiency. The short-circuit current Jsc=16.63 mA/cm^2 is an improvement of 0.63 mA/cm^2 compared to our previously published 20.8% cell [14].

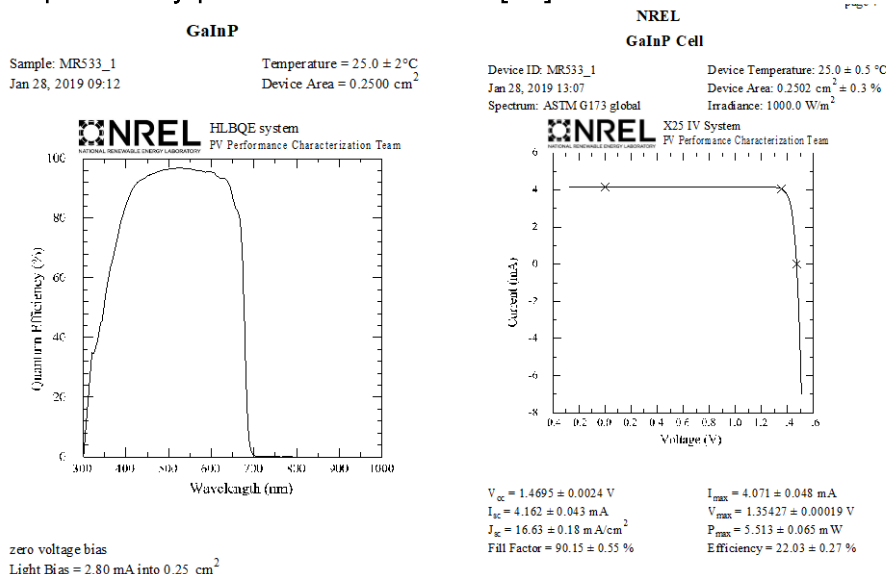


Figure 3 EQE and IV curves for a GaInP cell with a strained AlInP window (MR533), as measured by the NREL Cell and Module Performance Group.

This strained window layer has been incorporated into subsequent 2J and 3J cell designs.

Q4: 33% one-sun cell, lattice-matched to GaAs

The range of photon absorption in a GaAs solar cell can be extended by incorporation of strain-balanced GaInAs/GaAsP quantum wells, without the complications of metamorphic epitaxy. If the band edge can be extended out to the prominent water absorption band at 930 nm, with good collection efficiency, the resulting cell can in principle out-perform a baseline GaAs cell. More importantly, a GaInP/GaAs-QW cell should be able to exceed 33% efficiency.

In the rear heterojunction quantum well (RHJQW) cells demonstrated here, a 1-μm n-type silicon-doped GaAs emitter is grown first, with a carrier concentration of ~3E17/cm3. 50-80 quantum wells are then grown in the ~1.3 μm undoped region, followed by a very thin GaAs buffer layer and then a p-type zinc-doped GaInP BSF. The carrier concentration in the undoped QW region was estimated from a capacitance-voltage measurement to be <1015/cm3.

The target band edge for the MQWs was 930 nm, corresponding to the broad water absorption band in the global spectrum. Following reference [12], each repeated unit of the QW was designed to have 85 Å of Ga0.894In0.106As with 85 Å of GaAs0.902P0.098 on each side, resulting in 170 Å GaAsP barriers. The GaAsP composition was calibrated by growing a series of GaAsP layers of increasing P content, with a fixed arsine (AsH3) flow of 20 sccm. The solid composition was determined from high resolution reciprocal space maps of the (004) and (224)GE reflections, and the data were fit to a Langmuir adsorption curve.

Figure 4 shows a high-resolution x-ray rocking curve of the (004) reflection. The zeroth order reflection is clearly offset from the strong substrate peak, as explained in [15] for the zero stress design condition, because of the different elastic parameters in the barrier and well. Higher order superlattice peaks are visible on either side. The slight difference in strained lattice constant in the (001) direction between the two materials accounts for some of the intensity variation between peaks, but the clear asymmetry of the pattern arises from interference effects related to the different thicknesses of the two portions of the superlattice: with nominal thicknesses of 170 Å and 85 Å, and assuming a commensurate superlattice, the GaAsP and GaInAs layers are composed of 30 and 15 unit cells, respectively. A fit to the x-ray pattern indicates out-of-plane lattice constants of 5.595 Å and 5.712 Å for the GaAsP and GaInAs layers, respectively, which are close to the targeted values of 5.635 and 5.688 Å that assume elastic strain, sharp interfaces and no relaxation. The deviations do suggest that the interfaces are more complicated than the nominal sharp, box-like design, and will continue to be investigated.

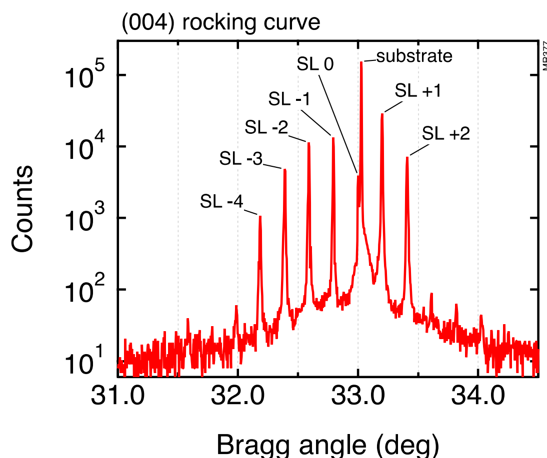


Figure 4 High resolution x-ray diffraction rocking curve of the (004) reflection of a GaInAs/GaAsP QW test structure.

Figure 5 shows the one-sun current-voltage (IV) curve for a representative RHJQW cell, measured under a xenon lamp at 1000 W/m^2 as determined by a calibrated GaAs reference cell and accounting for spectral mismatch between the reference cell and the test cell [16]. The cell exhibits an open-circuit voltage Voc=1.025 V. Compared to the Voc of ~1.1 V for a comparable GaAs cell without QWs, the loss of ~75 mV corresponds simply to the shift in band edge due to the incorporation of QWs. In other words, no other sources of recombination are being introduced. Since 1.1 V indicates strong photon recycling in the absorber, the 1.025 V of the RHJQW cell similarly indicates good optoelectronic properties. The best RHJQW cell demonstrated 27.2% efficiency [17].

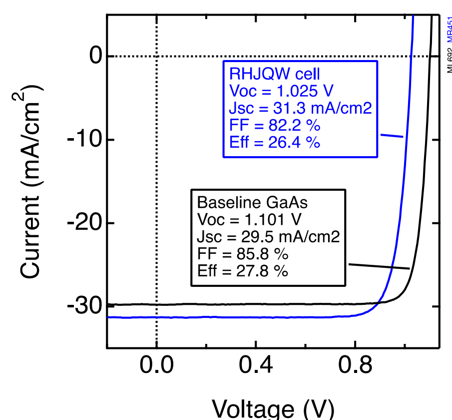


Figure 5 Current-voltage curves (uncertified) of GaAs and GaAs-QW cells under a simulated AM1.5 global spectrum at 1000 W/m^2. The cell areas were 0.25 cm^2.

We also investigated the performance of a standard n/p homojunction GaInP top cell, the other key component of a tandem. First, we studied the impact of doping. Figure 6 shows the external radiative efficiency (ERE) and DIV of homojunction GaInP using 90 nm n-type emitters and variable thickness and doping in the base. Increasing the thickness of the base and increasing the Zn doping density both reduce ERE, pointing to bulk recombination in the quasi-neutral region that is related to Zn doping.

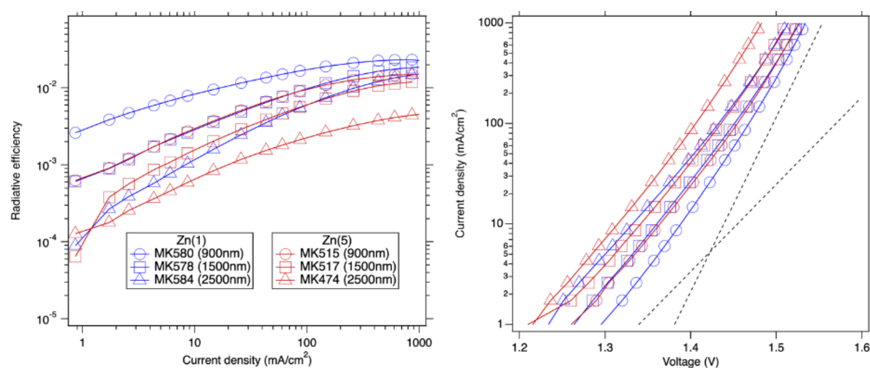


Figure 6 ERE and DIV of GaInP top cells using variable Zn flow and variable base thickness.

Annealing Zn-doped layers has previously been shown to reduce ordering and phase separation in III-V materials, and annealing has also impacted the point defect density in materials such as GaInNAs. Here, we investigated the annealing of GaInP cells, with and without the presence of a tunnel junction, which introduces point defects. Figure 7 shows the QE and IV of 2.1-um-thick GaInP cells with 1) low temperature annealing at 620 °C for 30 min, 2) high temperature annealing for 30 min at 750 °C, and 3) TJ + annealing for 30 min at 750 °C. Large improvements to both the carrier collection and Voc are observed with a TJ present. Initially, the FF is reduced, but raising the emitter doping improves the FF. The best GaInP homojunction cell performs with a Woc = 0.405 V, with the improvement likely due to point defect injection that passivates the existing defects.

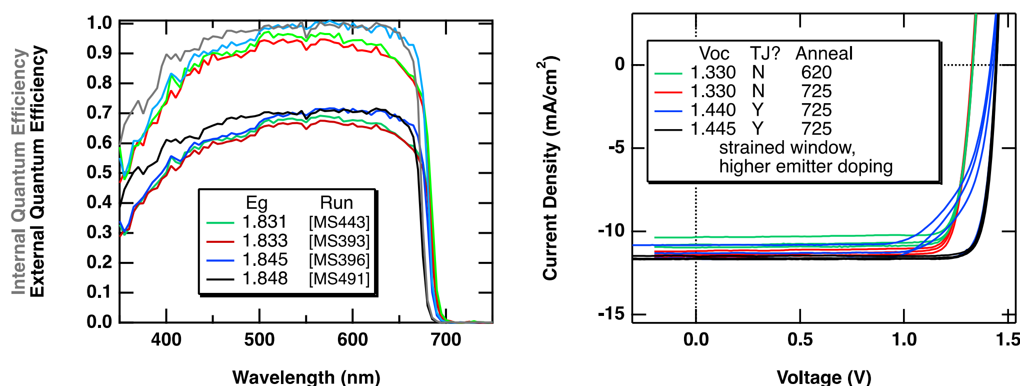


Figure 7 QE and IV of 2100-nm-thick GaInP cells with variable structures.

Integrating our best GaInP cell with a strained AlInP window together with a GaAs cell with strain-balanced GaInAs/GaAsP quantum wells, we demonstrated a 2J tandem cell with a record one-sun efficiency of (32.9 ± 0.5)% [17], as shown in Figure 8. The tandem is slightly current-limited by the top cell, which serves to boost the fill factor. The collection is >95% across most of the wavelength range. We estimate that ~1.67 mA/cm^2 of photocurrent are generate in the QW wavelength region.

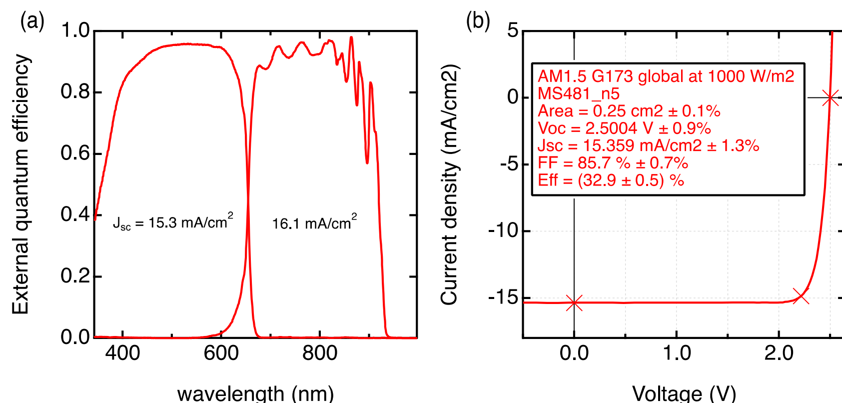


Figure 8 (a) EQE for a GaInP/GaAs-QW tandem, with GaInAs/GaAsP strain-balanced QWs in the bottom cell. (b) Certified J-V curve under the AM1.5 global spectrum at 1000 W/m^2. [17]

Q6: Demonstrate GaAs MQW solar cell with >2.5 mA/cm^2 improvement in Jsc and >80% EQE plateau in the QWs, using semiconductor optics to increase the reflectance

To overcome limitations with QW solar cells, we have investigated solar cells with thin GaAsP barriers [18]. With respect to thick barrier devices, devices with thinner barriers have reduced quantum confinement, and have a higher fraction of InGaAs within the QW region, potentially leading to improved EQE. Carrier transport shifts from being dominated by thermionic emission to involving transport via tunneling, which may improve collection efficiency and FF. Without quantum confinement, the solar cells are then called strained-superlattice (SL) solar cells.

Using the growth conditions established above, we perform two experiments to increase optical thickness of the SLS devices. In a first experiment, we systematically vary the GaAsP barrier thickness and composition while stress-balancing to $Ga_{0.895}In_{0.105}As$ with constant composition and thickness. The i-region thickness is kept a constant 2 µm, by varying the number of superlattice repeats within the i-region. The nominal thicknesses and compositions of the barriers in this experiment are 170 Å of $GaAs_{0.9}P_{0.1}$, 100 Å of $GaAs_{0.8}P_{0.2}$, 60 Å of $GaAs_{0.65}P_{0.35}$, 30 Å of $GaAs_{0.5}P_{0.5}$, and 20 Å of GaP. Wafer curvature confirms stress-balancing in all cases. Figure 9a shows the QE as the barrier thickness is varied. As the barrier thickness decreases, the quantum efficiency near the band edge increases due to the increasing amount of total GaInAs within the i-region. The fraction of GaInAs in the i-region increases with thinner GaAsP barriers, as listed in the legend of Fig 9a. With a fixed i-region thickness, the total amount of GaInAs increases as the GaAsP barrier is thinned due to the increased number of superlattice repeats. With progressively thinner GaAsP barriers, the total thickness of GaInAs increases from 680 to 1564 nm and the fraction of GaInAs in the SL stack increases from 32% to 80%, respectively. Thus, the absorption beyond the GaAs band edge increases in these thin-barrier devices. Additionally, the Au contact behind the cell acts as an efficient reflector, giving light a second pass through the SL. Thus, in devices with the thinnest barriers, the EQE approaches 100% at 910 nm, implying efficient collection of carriers generated in the GaInAs. Note that these cells can be considered optically thick, but still rely on the use of a back reflector.

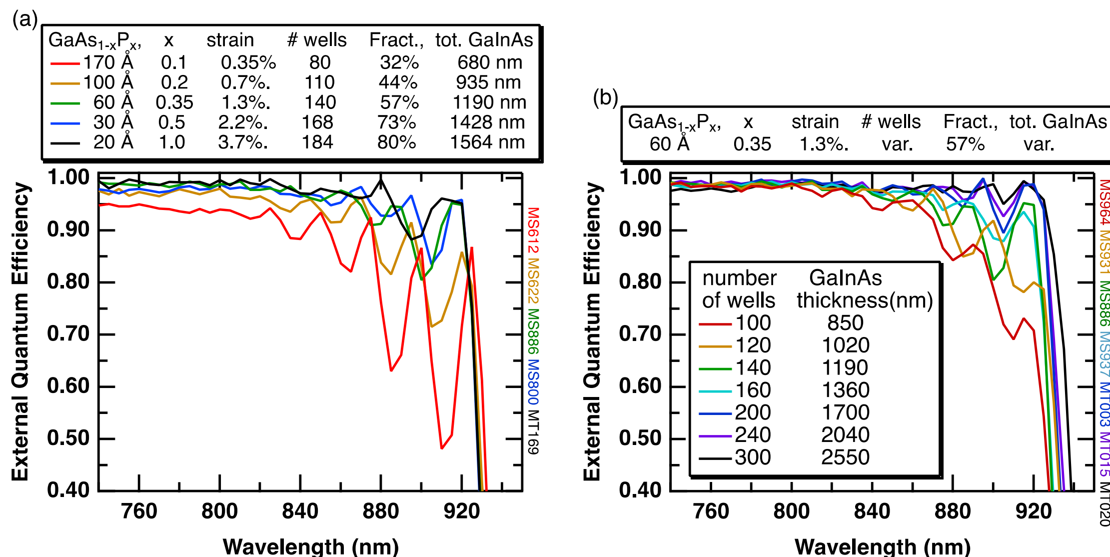


Figure 9 EQE of strain-balanced GaInAs/GaAsP solar cells with (a) variable GaAsP barrier thickness and composition and fixed GaInAs composition and i-region thickness (b) fixed GaInAs and GaAsP composition and layer thickness but variable number of repeats and thus i-region thickness. The x-axis is the total GaInAs thickness in the i-region. [18]

In a second experiment shown in Fig. 9b, the number of repeats, and thus the total thickness of the i-region, is varied in order to further test the potential of optically-thick solar cells. In this experiment, the thickness and composition of the barrier were fixed to 60 Å of $GaAs_{0.65}P_{0.35}$ (corresponding to the green curve in Fig 9a) to maintain a high fractional GaInAs content while avoiding high barrier strain and enable the growth of many SL repeats without problematic thickness and composition variation. The number of repeats varies from 100 to 300, which varies the total thickness of the GaInAs from 850 nm to 2550 nm. The GaInAs makes up 57% of the total i-region thickness in all cases, meaning that the thickest i-region in this experiment is almost 4.5 μm thick. Increasing the number of repeats, and thus increasing the amount of GaInAs, increases the quantum efficiency without any major signs of material quality degradation or limitations of the i-region thickness. The thickest sample has a nearly perfect carrier collection up to 920 nm. Although this sample still benefits from a back reflector, the thickness of the GaInAs is over 2500 nm thick, and so it can be considered optically thick even without a reflector.

Q12: 40% one-sun solar cell, with no more than one lattice-mismatched junction

Quantum wells were incorporated into the middle cell of a triple-junction inverted metamorphic solar cell [19]. The top cell was a front homojunction GaInP [20], and the bottom cell was a high performance metamorphic GaInAs cell accessed with a transparent GaInP compositionally graded buffer [21, 22], both with excellent material quality. The cells were interconnected using tunnel junctions described previously [23, 24]. The middle cell has 184 GaInAs wells to enable the appropriate multijunction cell photocurrent distribution and is otherwise identical to the single-junction QW devices in the above study. Devices were tuned for the AM1.5 global and AM0 space spectra by modifying the thickness of the top cell and changing the bandgap of the bottom cell by adjusting the graded buffer layer and the composition of the GaInAs[21]. Strain-balancing,

relaxation monitoring, and material analysis were performed by in-situ wafer curvature and ex-situ X-ray diffraction (XRD).

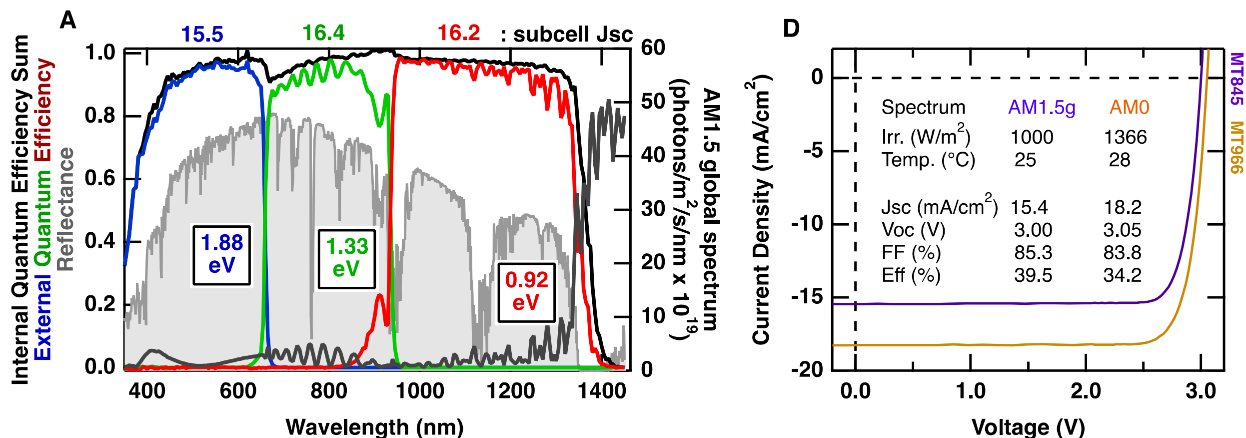


Figure 10 External quantum efficiency of devices designed for the AM1.5 global overlaid on top of the corresponding spectra. The subcell bandgaps (eV) are inside each graph, and the integrated subcell photocurrents (mA/cm2) are shown on top of the graph. (D) Illuminated J-V curves and performance metrics of both 0.25 cm2 devices tested under the appropriate spectra, independently measured by the Cell and Module Performance team at NREL. [19]

Figure 10A shows the EQE of the triple-junction global device, overlaid on the AM1.5g spectrum. The EQE in the QW region is over 80%, and the bandgap extends to the water absorption gap in the solar spectrum. The absorption in the cell is high enough to provide an appropriate photocurrent to the multijunction without the use of an internal reflector.[25] The summed internal quantum efficiency (IQE) is excellent in the range of the QWs, indicating a low loss of carriers associated with the QWs. A slight loss at shorter wavelengths (650 – 800 nm) highlights some absorption in the top tunnel junction, equivalent to a loss of <0.3 mA/cm^2. The integrated cell photocurrents are shown in Fig. 10A, along with the bandgaps. The top cell has the lowest photocurrent, and the middle and bottom cells have excess current that increases the fill factor of the multijunction device.

The JV curves of the devices are shown in Fig. 10B, measured under both the AM1.5 global spectrum (at 25 °C and 1000 W/m^2 irradiance) and AM0 space spectrum (at 28 °C and 1366 W/m^2 irradiance), which are standard measurement reference conditions that may differ from operating conditions.[26, 27]. **Under the AM1.5 global spectrum, the device measures (39.5 ± 0.5)% efficiency, the highest one-sun efficiency solar cell of any type as of this writing.** Under the AM0 space spectrum, the device measures (34.2 ± 0.6)%, the highest beginning-of-life triple-junction device yet reported under the AM0 spectrum [28].

Q9: Demonstrate a 1-eV GaInAs cell with <1.5-µm thick CGB and Woc<0.45 V at one-sun.

Compositionally graded buffers (CGB) are used to create lattice-mismatched solar cells with excellent performance. NREL has demonstrated 1.0 eV GaInAs devices (~2% mismatched to the substrate) with Woc (= Eg-Voc) = 0.36 V. This performance is much better than lattice-matched 1eV GaInNAs devices, and is close to the Woc achieved in

high performance GaAs devices. However, graded buffers are traditionally thought to require several microns of epitaxial thickness in order to achieve this excellent performance, which adds to the cost. In this task, we investigated various strategies to reduce buffer thickness in order to 1) understand tradeoffs between device performance and buffer thickness and 2) create high performance lattice-mismatched devices while using minimal thickness and thus cost.

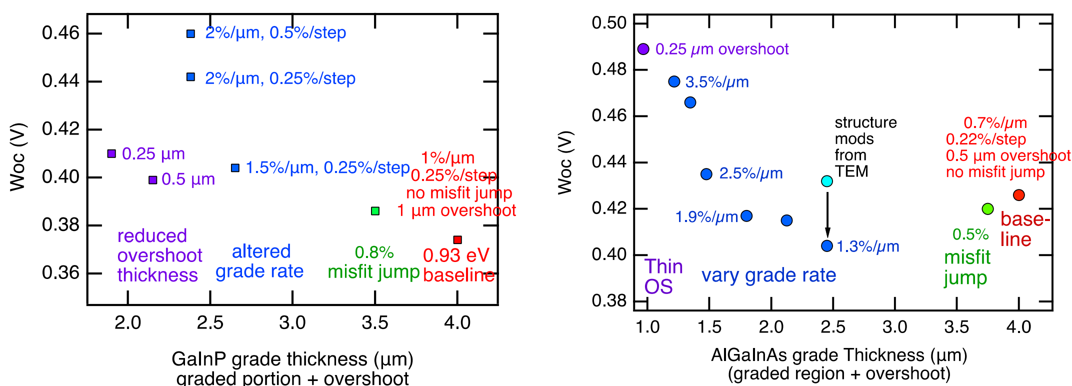


Figure 11 Systematic thinning of (left) GaInP buffers and (right) AlGaInAs buffers. The colors correspond to the various aspects of buffer thinning. The baseline cell is described in red; the green data introduces an initial jump in strain to skip the first portion of the buffer; the blue data varies the grade rate; the purple data thins the overshoot.

Figure 11 summarizes the results of lattice-mismatched GaInAs solar cells using thinned GaInP and AlGaInAs. GaInP buffers start to severely degrade at grade rates (% strain introduced per micron growth) over 1.5%/µm. However, excellent devices with Woc = 0.41 V are created with CGB thickness (graded region + overshoot buffer) of 2 µm.

While the baseline performance of GaInAs cells using AlGaInAs buffers does not exceed that using GaInP buffers, the performance loss using thin AlGaInAs buffers is not as dramatic. Only gradual degradation is observed as the grade rate is increased to 3.5 %/µm. **CGB thickness =1.5 µm results in Woc = 0.435,** and CGB thickness =1 µm still has Woc = 0.49 V. For the samples tested in this study, AlGaInAs results in better performance when the grade rate is high and the buffer is thin. The MOVPE precursor cost of AlGaInAs is also less than GaInP due to less Indium usage and less required group V overpressure, making it a potential route to cost savings. While the performance of these thin AlGaInAs buffers is decent, there is still opportunity for further improvement, and advanced concept CGBs will be proposed for future work.

Separately, we investigated the use of *in situ* etching as a potentially low-cost means of fabricating light-trapping structures on the GaInP back surface of ultrathin (270 nm) inverted GaAs solar cells [29]. Most fabrication techniques used to generate light-trapping structures for III-V photovoltaics are *ex situ* methods, which increase the number of device processing steps and can be high cost (e.g., photolithography). Most demonstrated potentially low-cost methods utilize wet chemical etching, with or without a mask, to fabricate rear-surface light-trapping scatterers. Fully *in situ* methods, however, use existing capital equipment (i.e., a growth reactor) to generate a rough scattering surface without additional external processing steps, thereby supporting high industrial throughput.

We used HCl as the etchant and performed texturing experiments with HCl and PH_3. We determined that the texturing mechanism is redeposition of GaP, and confirmed this through compositional analysis (STEM-EDS, XRD, and Auger spectroscopy). GaP redeposition can be explained through the lens of hydride-enhanced (HE) HVPE growth. HVPE growth is reversible, such that etching of GaInP by HCl yields the metal chloride growth precursors GaCl and InCl. By supplying PH_3, we enable growth of III-P compounds by HE-HVPE. The redeposition of GaP instead of $Ga_xIn_{1-x}P$ or InP can be explained by the higher volatility of InCl compared to GaCl, the higher thermodynamic driving force for GaP growth over InP growth from III-Cl and PH_3, and by the higher GaCl/InCl ratio during redeposition than during standard growth. Additionally, GaP redeposition has been previously observed under similar vapor phase etching of different Ga-containing III-V compounds with Cl-based etchants under PH_3 [30].

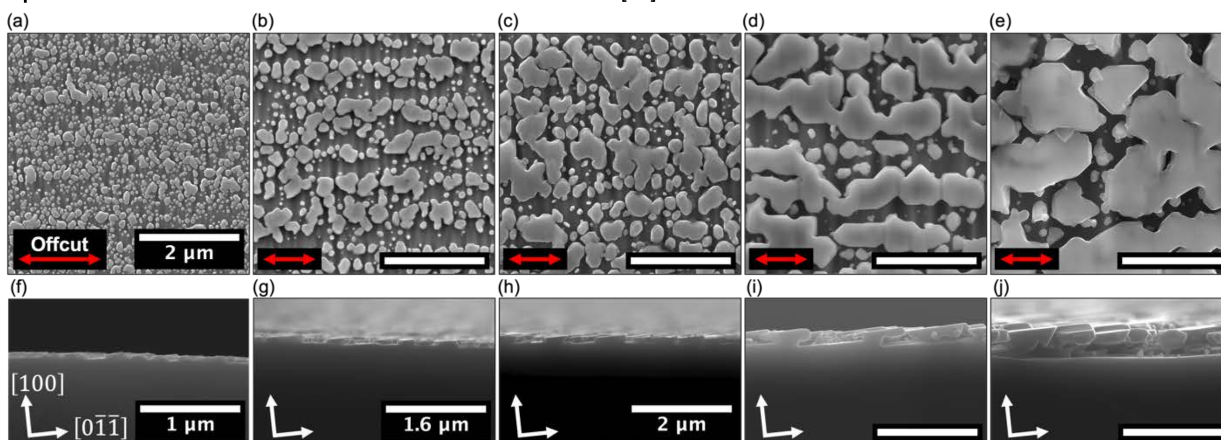


Figure 12 Plan view (a – e) and cross-sectional (f – j) SEM images of the redeposited GaP textured surface for different texturing times: 20 s (a, f), 30 s (b, g), 60 s (c, h), 90 s (d, i), and 120 s (e, j). Total HCl flow was 4 sccm and hydride carrier flow was 2000 sccm for all samples. Scale bars are 2 µm unless otherwise specified.

We demonstrated tunability over the redeposition with the growth parameters of total texturing time (Figure 12), hydride carrier flow, and HCl flow rate. To evaluate the potential of each resulting morphology for light-trapping, we measured the backside normal specular reflectance. A low reflectance indicates high off-angle scattering and therefore high potential for light-trapping. The most promising combination of texturing conditions was texturing for 60 s with an HCl flow rate of 4 sccm and a hydride carrier flow rate of 2000 sccm (Figure 12c, h). We implemented this condition into a 270 nm GaAs solar cell with a GaInP window layer and a GaInP BSF. The textured cell's measured J_{sc} (Figure 13a) is 5% higher than that of the planar cell. This increase corresponds with the EQE

(Figure 13b), which shows higher collection at long wavelengths. Using an integrating sphere, we determined that the textured cell has higher total absorption than the planar cell (Figure 13c). Because the cell structures are nominally identical and GaP can only absorb wavelengths below approximately 550 nm, we conclude that the increased absorption is due to light scattering, thereby demonstrating a fully *in situ* fabrication method for generating light-trapping structures for III-V photovoltaics.

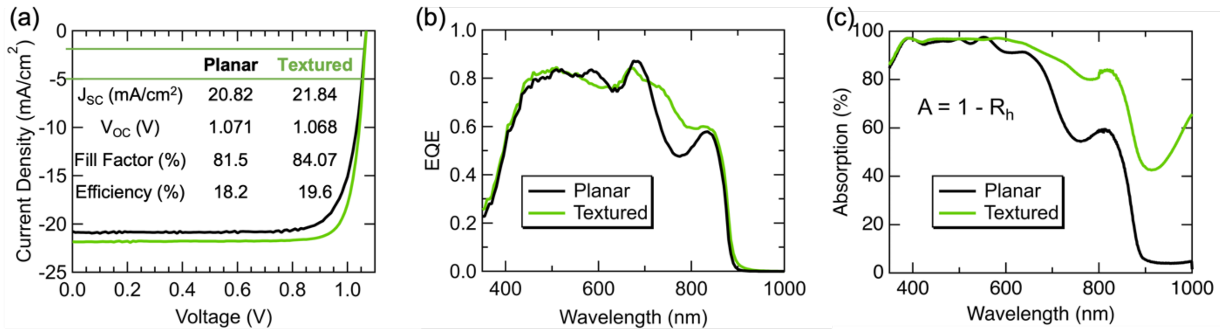


Figure 13 (a) Current-voltage, (b) external quantum efficiency, (c) total absorption, A, calculated as 1 minus the hemispherical reflectance, R_h. R_h was measured using an integrating sphere from the front side of the cells. [29]

This project also supported research on light trapping in ultra-thin GaAs cells using quasi-random photonic crystals [31-33], in conjunction with the Tandems Core (#34911). The research results are described in the final technical report for that project.

Task 2: Continued development of Hydride Vapor Phase Epitaxy (HVPE) for PV applications, focusing on the growth of aluminum-containing alloys

- **Q3: Demonstrate >35% Al content in AlGaAs grown by HVPE, with doping n ≥ 1x10^{18} cm^{-3}.**
- **Q5: Demonstrate HVPE growth of AlGaInP with Al content >10% while maintaining lattice match to the GaAs substrate.**
- **Q11: Demonstrate HVPE-grown AlInP lattice matched to a GaAs substrate.**

The HVPE reactor at NREL was modified to accommodate an aluminum source, as shown schematically in Figure 14 [34]. $AlCl_3$ was generated *ex-situ* in a separate quartz boat enclosed in a clamshell furnace. The Al furnace temperature was 400 °C in order to promote generation of $AlCl_3$ instead of AlCl. Al precursor generation was controlled by the flow rates of HCl and H2 carrier to the boat as indicated in Figure 14. The process lines that deliver the Al precursor to the reactor were heated to 200 °C using insulated heat tapes to prevent solidification of the $AlCl_3$ and subsequent clogging of the lines. The Al line is plumbed into the reactor through an alumina tube that extends through the majority of the 800 °C upper source zones. The alumina tube is inert to reaction with $AlCl_3$ or decomposition byproducts and has an inner diameter of 4 mm to promote a high precursor velocity through the higher-temperature source zone.

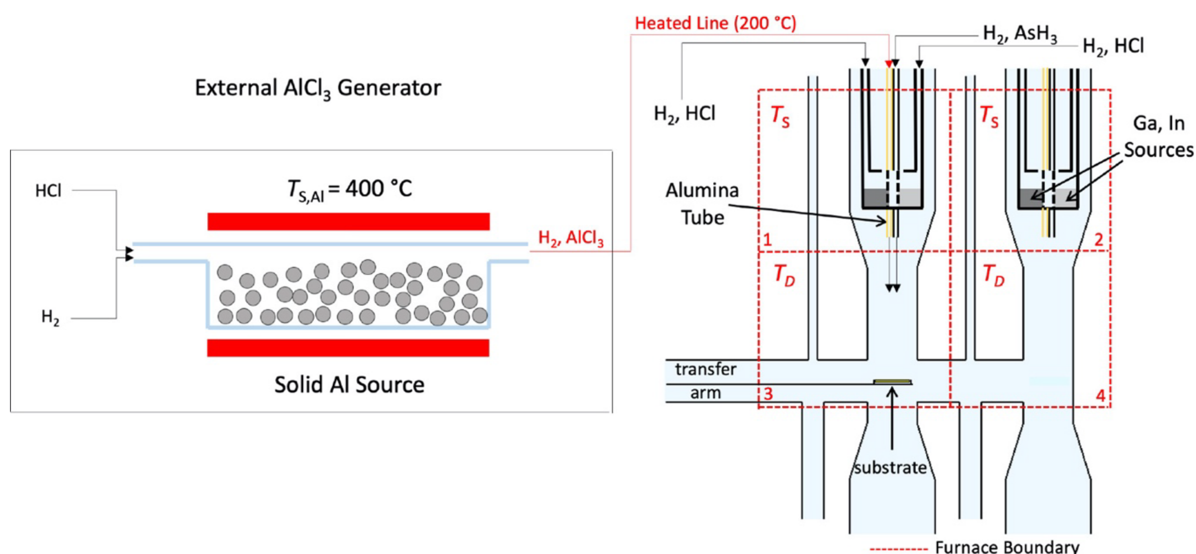


Figure 14 Diagram of the dynamic HVPE reactor used in this study, including the external $AlCl_3$ generator (not to scale).

We performed two experiments [34] to verify that the precursor generated in the Al source, and the one that eventually reaches the growth front, is $AlCl_3$. First, we varied the deposition temperature, T_D, under constant reactor flows and constant upper zone 1 and 2 temperatures (T_S). Figure 15 (left) shows x_{Al} and the growth rate for this series of samples. x_{Al} increases strongly with T_D and the growth rate varies weakly, passing through a maximum near 650 °C. The trend of increasing x_{Al} with T_D agrees with the equilibrium curves in Figure 16, which predict that the driving force for AlAs growth from

$AlCl_3$ increases with T_D while the driving force for GaAs growth from GaCl simultaneously decreases. The growth rate is relatively insensitive in this temperature range because of these opposite trends in K_{eq} for each binary. This result suggests that $AlCl_3$ is the dominant Al-precursor in the reactor, because growth from AlCl and GaCl is expected to exhibit a monotonic growth rate decrease based on Figure 16. We also note that the large HCl(Al)/HCl(Ga) ratio of 20 (assuming complete conversion of all HCl to $AlCl_3$ and GaCl) needed to achieve x_{Al} = 0.4-0.6 suggests that the species reaching the substrate surface is $AlCl_3$. The more reactive AlCl would be expected to completely overwhelm Ga incorporation in the film at that ratio, as indicated in Figure 15.

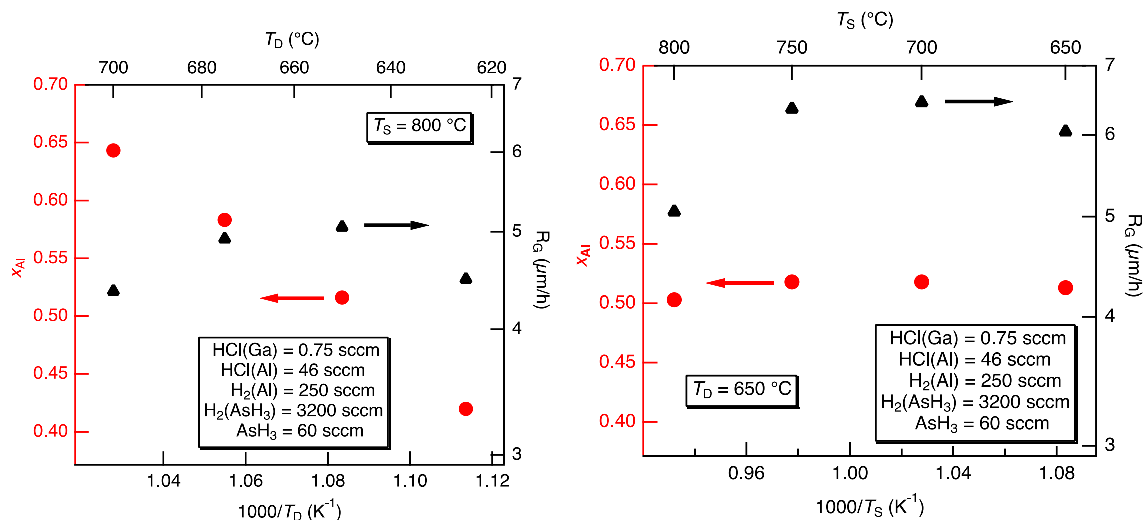


Figure 15 LEFT: x_{Al} (left axis) and growth rate (right axis) of $Al_xGa_{1-x}As$ epilayers grown with varying deposition temperature (T_D) at constant source temperature (T_S). RIGHT: x_{Al} (left axis) and growth rate (right axis) of $Al_xGa_{1-x}As$ epilayers grown with varying source temperature (T_S) at constant deposition temperature (T_D). All other growth parameters were held constant. From [34].

Next, we varied T_S using constant reactant flows with constant T_D to determine whether this would alter the distribution of $AlCl_x$ species in the reactor. Changing T_S is a useful method to alter the chemistry within the reactor independent of T_D or reactant flows. In previous work, we used this method to affect the decomposition of AsH_3 in the reactor. Figure 15 (right) displays the results of a similar experiment studying the effect of T_S on $Al_xGa_{1-x}As$ growth. x_{Al} is relatively constant as T_S varies between 650 and 800 °C. The growth rate is also relatively constant until showing a decrease at T_S = 800 °C. The insensitivity of x_{Al} and the growth rate to T_S implies that the Al-precursor distribution is not affected in this temperature range, at least in conjunction with the injection scheme used here. This result, combined with the result of the first experiment, strongly suggests that the predominant Al growth species in the reactor is $AlCl_3$ and that it is not substantially decomposing to AlCl at typical reactor temperatures.

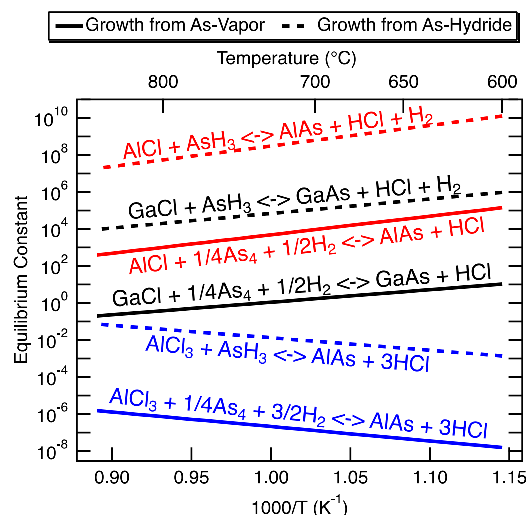


Figure 16 Plot of the equilibrium constant for deposition of solid AlAs and GaAs using various group III precursors and As-vapor (As_4) or As-hydride (AsH_3). From [34].

Finally, we then investigated the effects of the nature of the group V precursor on $Al_xGa_{1-x}As$ growth. In a previous study, we showed that GaAs growth rate could be enhanced by limiting decomposition of the AsH_3 precursor into As_2/As_4 [5]. In that work, we limited AsH_3 decomposition by increasing the flow rate of H_2 carrier input with the AsH_3, which increases the velocity of the AsH_3 through the reactor and decreases the amount of time it spends in the higher-temperature 800 °C source zone where it would quickly decompose. Figure 17 shows x_{Al} and growth rate for a series of $Al_xGa_{1-x}As$ samples grown with varying AsH_3 carrier flow rate. Note that the carrier flow rate was compensated in another reactor port so that the total H_2 flow rate and reactant dilution level in the reactor were constant. x_{Al} increases strongly with the AsH_3 carrier flow rate, and the growth rate increases as well. These results imply that the presence of uncracked AsH_3 is key to the incorporation of Al in the solid. This can be understood by considering that K_{eq} for growth of AlAs from $AlCl_3$ and As_4 is extremely low, as seen in Figure 16, while K_{eq} for AlAs growth from $AlCl_3$ and AsH_3 is nearly five orders of magnitude larger. We further note that K_{eq} for AlAs growth from $AlCl_3$ and AsH_3 is still well below unity at 650 °C, however, indicating that the equilibrium calculations do not tell the entire story. It is likely that the presence of unreacted AsH_3 modifies the kinetics at the substrate surface, enhancing Al incorporation from the $AlCl_3$. AsH_3 that decomposes on the substrate surface may provide reactive H radicals that help drive the kinetic reduction of the otherwise highly stable $AlCl_3$ molecule, explaining the trends observed in Figure 16.

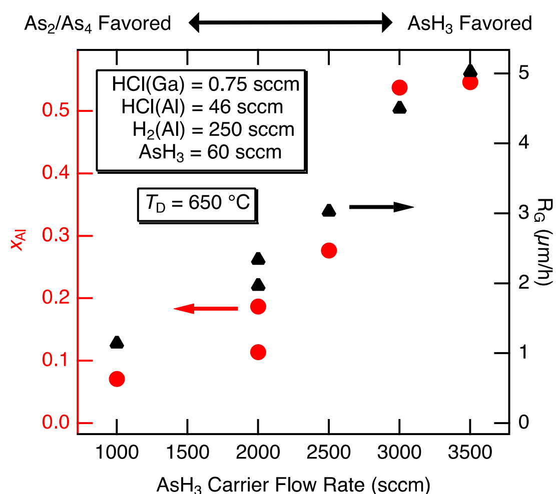


Figure 17 x_{Al} (left axis) and $Al_xGa_{1-x}As$ growth rate (right axis) as a function of AsH_3 carrier flow rate in epilayers grown with T_D = 650 °C and all other parameters constant. [34]

Using the understanding developed in the $Al_xGa_{1-x}As$ growth studies, we can achieve $Al_xGa_{1-x}As$ with x_{Al} tunable between 0 and 1. Figure 18 shows (004) X-ray diffraction curves for samples with Al content varying from 0.10 to 0.92. Use of the $AlCl_3$ precursor is extendable to deposition of Al phosphide compounds by HVPE, for which we are aware of no prior reports of growth by this technique. Figure 19 shows optical transmission measurements of (a) $Al_xIn_{1-x}P$ and (b) $Al_xGa_yIn_{1-x-y}P$ epilayers with compositions closely lattice-matched to GaAs. The direct band gaps were obtained by fitting the linear region of the absorption edge. These wide band gap epilayers are extremely useful in many III–V devices. For example, they can be readily integrated into solar cells to provide transparent passivation for front and rear surfaces, or as the active layers in LED devices that emit at green wavelengths. Figure 20 shows x_{Al} for $Al_xIn_{1-x}P$ epilayers grown near the lattice-matched composition as a function of $AlCl_3$/InCl ratio. Near unity $AlCl_3$/InCl ratios are necessary to achieve a 50/50 solid composition, making the growth of $Al_xIn_{1-x}P$ not only possible but readily controllable, in stark contrast to growth via AlCl. The inset of Figure 20 shows an (004) X-ray diffraction curve of a 20 nm thick lattice-matched $Al_{0.53}In_{0.47}P$ layer. The appearance of Pendellosung fringes indicates that the growth is epitaxial and highly planar. The growth of phosphide materials by HVPE opens up exciting possibilities for the deposition of high-efficiency III–V photovoltaics with reduced cost.

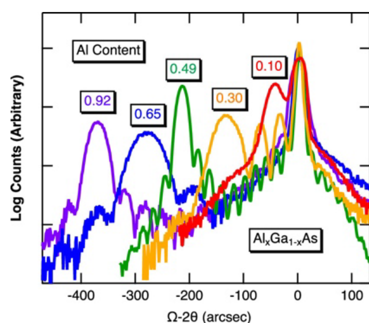


Figure 18 (004) Ω–2Θ high resolution X-ray diffraction scans of AlxGa1–xAs epilayers nearly spanning the entire compositional space. From [34].

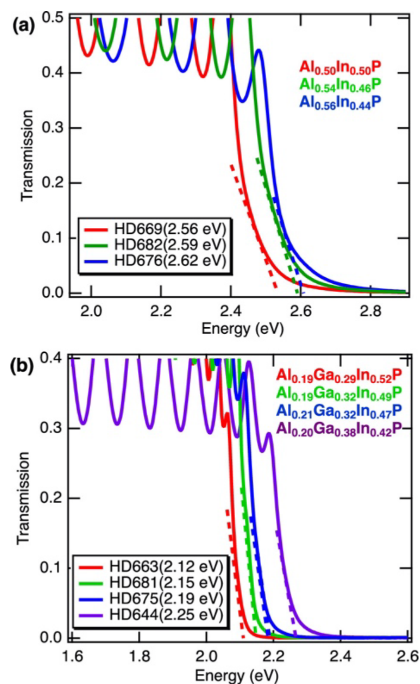


Figure 19 Transmission spectra of (a) AlxIn1–xP and (b) AlxGayIn1–x–yP epilayers bonded to glass. From [34].

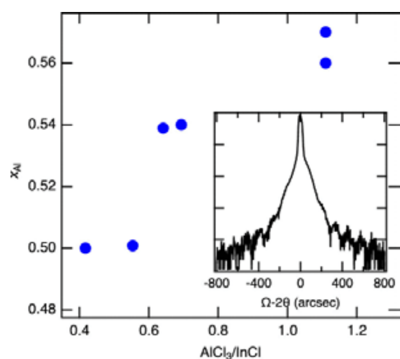


Figure 20 xAl in $Al_xIn_{1-x}P$ for epilayers grown nearly lattice-matched to GaAs as a function of $AlCl_3/InCl$ ratio, assuming complete conversion of HCl to MCl_x. Inset: (004) X-ray diffraction curve of a 20 nm thick $Al_{0.53}In_{0.47}P$ layer grown on a GaAs substrate. From [34].

- **Q8: Demonstrate an HVPE-grown GaAs solar cell with an Al-containing window layer and Jsc ≥ 28.0 mA/cm^2.**
- **Q12: Demonstrate an HVPE-grown GaAs solar cell with an Al-containing window layer and Jsc ≥ 29.5 mA/cm^2**

AlInP window layers were incorporated into single junction GaAs cells [35] and compared to similar control cells with GaInP windows, previously demonstrated to enable near unity carrier collection in 1J devices [4]. We applied AlInP to inverted rear-junction solar cells because this structure is generally more sensitive to the quality of surface passivation than front-junction solar cells, and the sensitive, active layers are grown after the AlInP. Figure 21a shows the certified AM1.5G illuminated *J-V* characteristic and extracted solar cell metrics of both devices. The certified efficiency of the AlInP-passivated device was

(26.03 ± 0.19)%, which is the highest reported efficiency reached by any single junction HVPE-grown solar cell. Both devices yield V_{OC} of ~1.06 V and ~84-85% fill factors indicating similar material quality. The AlInP-passivated solar cell exhibits a 1.3 mA/cm^2 increase in certified J_{SC} over the GaInP-passivated cell. We then evaluated the quantum efficiency of these solar cells to better understand where the improvement in current density originates. Figure 21b compares the EQE of both devices. The AlInP-passivated device exhibits an increase in short wavelength (< 650 nm) current collection relative to the GaInP-passivated control. The increased short wavelength optical transparency of the AlInP window accounts for effectively all of the 1.3 mA/cm^2 improvement in J_{SC} as determined by integration of the EQEs with the AM1.5G spectrum. In the long wavelength region, the EQE is >95%, indicating nearly perfect collection of absorbed photons below the absorption edge of either window. This high degree of collection cannot be obtained if the window/base interface recombination velocity (IRV) is large because these are rear junction cells [36]. The roughly 4% of EQE loss could be attributed to non-zero IRV and/or limited minority carrier diffusion length in the GaAs base. Separating these factors will require deeper study, but we note that the equal long-wavelength current collection and invariant V_{OC} suggest excellent passivation and very similar IRV values for the two different window layers used in these devices. Thus, we find that both windows sufficiently passivate these rear-junction GaAs solar cells. The parity V_{OC} and fill factor values observed between the devices also suggest that the AlInP window does not alter either bulk recombination in the GaAs absorber or recombination at the heterojunction. Therefore, we conclude that the presence of AlInP has no impact on the electrical performance of subsequently grown layers.

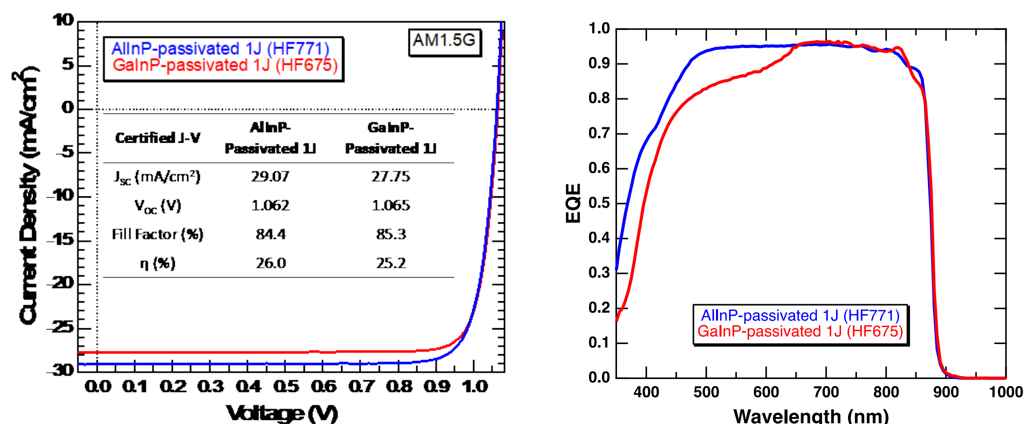
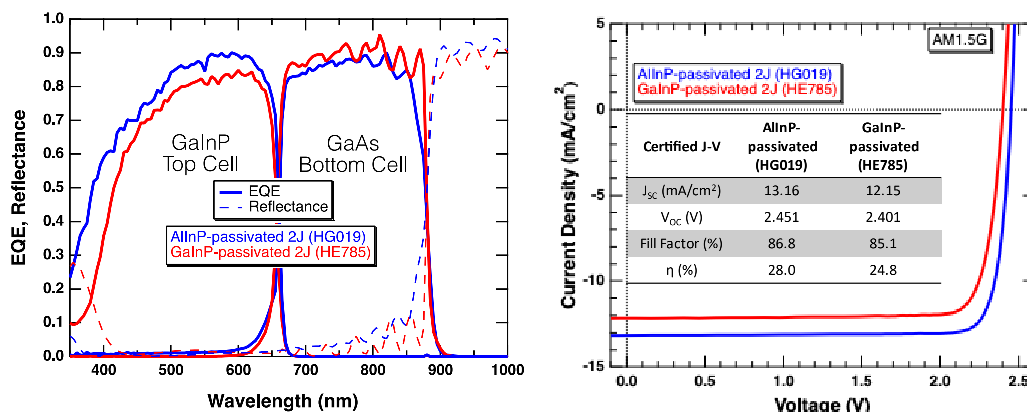


Figure 21 (Left) Certified illuminated J-V characteristic and extracted metrics of AlInP- and GaInP-passivated GaAs (1J) solar cells under a simulated AM1.5G spectrum. (Right) EQE measurements. [35]

We also evaluated the performance of 2J solar cells with and without AlInP passivation of the GaInP top cell. Figure 22a shows the EQE of the 2J solar cells. The AlInP window increases short wavelength current collection (< 650 nm) by reducing the parasitic absorption that occurs when employing the n-GaInP emitter as the passivating layer for the p-GaInP base. Adding a discrete AlInP window both improves passivation and enables collection of photons in the emitter that would otherwise be uncollected [6]. Both of these factors result in an improvement in current collection, which spans the whole wavelength range of the top cell because previously uncollected photons in the

unpassivated emitter are now collected. Both bottom cells show similar EQE response, although differences in the reflectance cause a slight reduction for the AlInP-passivated case. We find both cells are close to current-matched, given that the difference in current collection between each subcell, obtained by integrating the EQE with the AM1.5G spectrum, is within the roughly ±0.3 mA measurement error of the EQE.

Figure 22b shows the illuminated *J-V* characteristic and extracted solar cell metrics of the 2J solar cells. Here, the AlInP-passivated 2J reaches a certified efficiency of 28.0%, which is a >3% absolute increase relative to the GaInP-passivated case. The J_{SC} improves by 1.0 mA/cm^2 due to the improvement in the top cell passivation and the fill factor increases by almost 2% relative to the control despite improved current matching relative to the GaInP-passivated device. This improvement is explained by reduced series resistance in the AlInP-passivated device, as indicated by a change in slope of the *J-V* near V_{OC}. The AlInP passivation enabled the use of a thicker emitter, ~3× thicker in this case, which led to a ~3× lower sheet resistance, lower series resistance, and improved fill factor. Furthermore, the V_{OC} of the AlInP-passivated device improves by 50 mV relative to the control.



Certified J-V	AlInP-passivated (HG019)	GaInP-passivated (HE785)
J_{SC} (mA/cm²)	13.16	12.15
V_{OC} (V)	2.451	2.401
Fill Factor (%)	86.8	85.1
η (%)	28.0	24.8

Figure 22 (Left) EQE and reflectance of GaInP/GaAs (2J) solar cells grown by D-HVPE. (Right) Illuminated J-V characteristics of GaInP/GaAs (2J) solar cells. Figures of merit are given in the inset table. [35]

Task 3: Research into inexpensive substrates for III-V epitaxy, including growth on v-grooved silicon, selective area growth on GaAs, Bi_2Se_3, and other substrates that will be identified over the POP.

(The information in this section includes Protected Data/Limited Rights Data)

- **Q1: Identify at least 3 potential external substrate collaborators, with plan of action for growth and characterization**
- **Q10: Choose most promising substrate ideas, assess potential and grow a GaAs cell**

Reducing substrate costs, whether by growth on an inexpensive template or through significant reuse of a more expensive wafer, is critical for reducing the overall cost of high-efficiency III-V photovoltaics. Both approaches, i.e. cheap templates and reuse, result in opportunities to perform epitaxial growth on starting surfaces that are not typical of the epi-ready substrates commonly used today. The less expensive substrates may contain some combination of features that could impact the eventual device performance, from general roughness to larger morphological features, for example arrest lines and river lines in spalled materials. Previous work showed that features with abrupt changes in height lead to shunted or fully shorted devices when device layers of different polarity contact each other across the step. Chemo-mechanical polishing (CMP) of these surfaces would, of course, eliminate such problems, but CMP tends to quickly become the limiting cost when used to reprepare substrates. NREL engaged with several external collaborators, listed in Table 1, to demonstrate growth on novel substrates. The status at the end of the project is listed in the right-hand column. Three of the collaborations led to separate funding.

Table 1 External collaborations for substrate research

	Collaborator	Goal / idea	Status / Results
1	FCM	Direct growth on "un-polished" substrates	→ Results presented at PVSC [37]
2	Stanford	Use laser ablation to eject epilayers	- Showed mm-scale ejected GaAs epilayers with device Voc ≥ 0.98 V. - Preliminary GaInP cells and and GaInP/GaAs tandem cells. → Manuscript submitted to Cell Reports Physical Science [38]
3	MIT	Remote epitaxy through graphene	→ SETO-1840 funding (no work done here)
4	NRL	Transfer printed virtual substrate	Results presented at PVSC [39] - most applicable to CPV applications.

	Collaborator	Goal / idea	Status / Results
5	Leibniz Institute for Crystal Growth	Low-purity GaAs boules/wafers	Paper published in Journal of Crystal Growth [40] - impurities segregate to the ends of the boule - comparable GaAs cells on low-purity and control boules. - no new expts planned, due to cost of boule growth
6	U. Houston	Growth on flexible GaAs templates on IBAD foil	Conducted preliminary experiments
7	Colorado School of Mines	Porous germanium	Conducted preliminary experiments
8	"Industry Partner"	Growth on CVD Ge on Si templates	Hillock cause determined; crack-free devices grown on new templates
9	DOD	Spalling, growth on Ge	→ partially funded by DOD
10	ASU	Electro-Acoustic Spalling	→ SETO-2064 funding → major focus of III-V Core in FY22-24 - demonstrated spalled GaAs devices with Voc comparable to control samples.

Q3: Submission of a peer-reviewed publication on the growth of GaAs on Bi_2Se_3 using diethylzinc to surface-convert the 2D-layered Bi_2Se_3 to ZnSe for the growth and nucleation of GaAs.

One pathway toward reducing substrate costs for III-V solar cells is to grow them on inexpensive or reusable substrates. This subtask investigated the use of single-crystal layered-2D Bi_2Se_3 as an inexpensive reusable substrate for the growth of GaAs. The layered-2D materials to be discussed here are of particular interest because their (0001) cleavage surfaces are in-plane lattice-matched to the (111) planes of common optoelectronic semiconductors (Figure 23). Initial attempts at growing InP and GaAs on Bi_2Se_3 clearly indicated that there were strong and unexpected conversion reactions between our growth precursors and Bi_2Se_3 surfaces. Therefore, a lot of the work was foundational and directed toward understanding these reactions, because (as will be shown below) this knowledge is essential to the development of GaAs-on-Bi_2Se_3 growth processes.

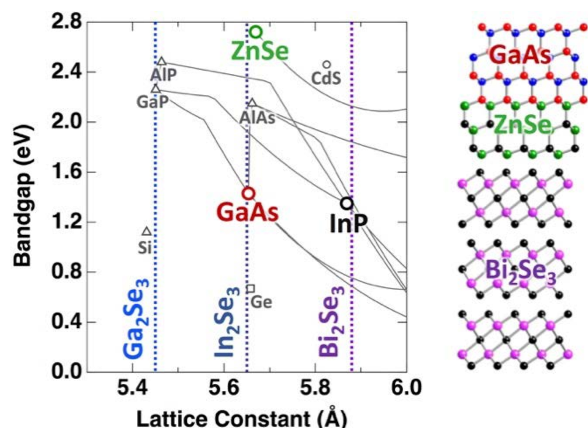


Figure 23 (Left) A plot showing the bandgaps and lattice constants of common semiconductors. Because the (0001) planes of layered-2D Bi_2Se_3 and In_2Se_3 crystals and the (111) planes of cubic semiconductors share the same 3-fold symmetry, they can be in-plane lattice matched as shown. Ga_2Se_3 is cubic and lattice-matched to GaP and Si. (Right) Side views showing GaAs (111) and ZnSe (111) on top of layered-2D Bi_2Se_3 (0001).

We demonstrated the successful growth of cubic GaAs (111) on single-crystal 2D layered Bi_2Se_3 (0001) substrates achieved using a cubic ZnSe buffer layer [41]. This growth sequence was chosen based upon observed reactions between Bi_2Se_3 (0001) substrates and both Ga and Zn. For the conditions used in our MOCVD reactor, triethylgallium (TEGa) interacts strongly with Bi_2Se_3 to form Ga_2Se_3, which can disrupt the nucleation and growth of GaAs. Therefore, a buffer layer is needed which prevents Ga–Bi_2Se_3 interactions while simultaneously providing a suitable growth surface for GaAs. ZnSe was chosen because it is lattice-matched to GaAs, and can be created by annealing the Bi_2Se_3 under a diethylzinc (DEZn) flux. A sample utilizing this growth sequence has been grown, characterized and exfoliated as a possible pathway toward reducing the substrate cost for III-V devices such as solar cells.

A second paper [42] demonstrated that the surface layers of single-crystal layered-2D Bi_2Se_3 can be converted to layered-2D β-In_2Se_3 by annealing under a trimethylindium (TMIn) flux. The resulting single-crystal β-In_2Se_3 adopts the crystal structure and orientation of the underlying Bi_2Se_3, and the excess Bi atoms generated by this process creates an underlying region of Bi-rich Bi_xSe_y. Due to the difference in bandgap between Bi_2Se_3 and In_2Se_3, this conversion reaction presents a pathway to lateral heterojunctions if only selected regions are converted by masking the surface to spatially define the TMIn exposure. The conversion may also have implications for heteroepitaxy, because the in-plane lattice constants of Bi_2Se_3 and In_2Se_3 (0001) surfaces match those of InP and GaAs (111), respectively.

The basic challenge of growing a III-V epilayer on a layered-2D Bi_2Se_3 substrate was solved by annealing the Bi_2Se_3 under diethylzinc to create cubic ZnSe, which then acts as a substrate for GaAs. However, the material quality of these initial GaAs growths was poor over macroscopic distances (device-scale), so a decision was made to shift resources to a patterned-substrate release method which had a more obvious pathway to high material quality.

Although many different configurations and processes can be envisioned, all patterned release ideas resemble Figure 24, where a substrate is patterned with a mask material, which then creates a weak layer to facilitate removal of the epilayer from the substrate.

Figure 24 (Left) A substrate with a patterned mask. (Middle) An epilayer produced by nucleation, lateral overgrowth, then coalescence. (Right) Substrate separation from the epilayer at the weakened layer. For substrate reuse, the process is repeated.

To be impactful, three aspects of this method must be addressed: cleavage at a weakened interface, defect-free coalescence [43], and substrate re-use. Cleavage has already been addressed in isolation by the CLEFT (Cleavage of Lateral Epitaxy for Transfer) method, in which GaAs is patterned with an oxide layer to create a weakened layer for liftoff. However, the scale and geometry of the masking leads to a high defect density wherever the GaAs epilayer coalesces over the mask. This work builds upon CLEFT, but with some key differences intended to address coalescence-related dislocations. Substrate re-use can be addressed once the details of a specific process are known.

In this work, we investigated modifications to the CLEFT method which should eliminate coalescence-related dislocations while still providing the patterned interface needed for cleavage. Fundamentally, these dislocations are a result of crystal-registry errors during coalescence and can only be eliminated by controlling the mask *topology* and *dimensions*. We considered two mask topologies: An array of mask stripes, and an array of mask dots. A striped pattern requires that the dimensions of the patterning be kept below some threshold. An array of mask dots is a more favorable topology for defect-free coalescence and should in principle continue to offer defect-free coalescence even when scaled up to arbitrarily large dimensions. Each topology has some potential advantages, and our preliminary results for both were favorable [44].

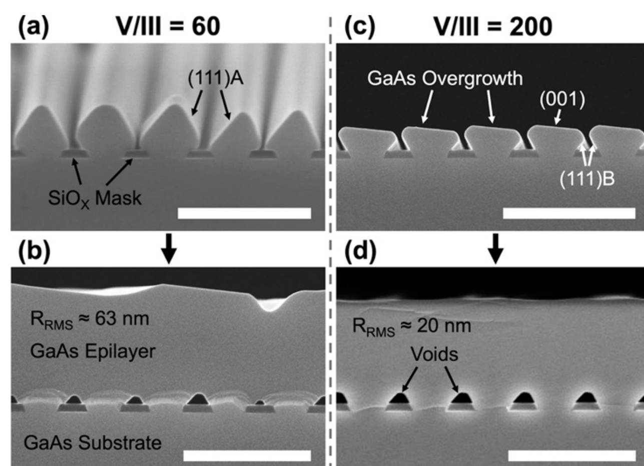


Figure 25 Cross-sectional SEM viewing down [$\bar{1}$10] showing the overgrowth morphology and surface roughness as a function of the V/III ratio on 6°A substrates. (a) Lower V/III ratio of 60 favors (111)A facet formation and overgrowth in a spade-like morphology, resulting in a (b) rougher coalesced epilayer. (c) Higher V/III ratio of 200 favors (001) and (111)B facet formation, resulting in a (d) smoother coalesced epilayer. Scale bars are 1 μm. From [44].

Controlling the morphology of the overgrown material prior to coalescence can significantly influence the final top surface roughness of the coalesced buffer layer on which subsequent device layers are grown. Inspired by the work of Lee *et al.* [45] and Moll *et al.* [46], we studied the influence of the V/III ratio on the preferential growth directions and faceting of precoalesced GaAs grown on patterned 6°A substrates. Figure 25 shows the difference in the overgrowth morphology of GaAs prior to coalescence when grown under a V/III ratio of 60 versus 200. Changing the V/III ratio changes the As chemical potential within the reactor environment, which alters the surface energies of low-index GaAs surfaces, which in turn can influence any preferential faceting.

At a lower V/III ratio of 60, GaAs overgrew in a spade-like morphology (Fig. 25a), which creates a rough, undulating film at the point of initial coalescence. After 1 μm of growth, significant surface pitting was still observed (Fig. 25b) and the root mean square (RMS) surface roughness (R_{RMS}) was approximately 63 nm. Such a morphology requires growing thicker epilayers to flatten out the coalesced film and is therefore less ideal for the growth of subsequent device epilayers.

Increasing the V/III ratio to 200 (thereby increasing the As chemical potential) results in preferential faceting of the (001) and (111)B surfaces as seen in Fig. 25c. Note that the morphology is also more consistent between the neighboring overgrowths. The very flat, tilted top of each overgrowth is consistent with a (001) facet, which can be completely step-free because of the offcut direction. Such a lack of steps may enhance Ga adatom diffusion to the overgrowth edges, contributing to the lateral growth of the overhanging (111)B facets. It is difficult to determine whether these morphology changes as a function of As chemical potential are influenced more by surface kinetics or by surface energy and thermodynamics. However, based on the prior literature and this work, there is reason to hypothesize that both play a role in the resulting overgrowth morphology. Further growth of this morphology leads to a more uniform film at the point of initial coalescence, resulting in a RMS surface roughness of around 20 nm after 1 μm of growth (Fig. 25d). These

results clearly show the impact of the overgrowth morphology on the surface roughness of the coalesced epilayers.

To assess macroscale material quality, GaAs front homojunction devices were grown on 1 µm thick coalesced buffer layers on patterned 6°A substrates [47]. EQE (Fig. 26a) was measured over a wavelength range of 350–1000 nm. High quantum efficiency was observed across the entire above-band gap range and is equivalent to that of control devices grown on unpatterned epi-ready substrates. Figure 26b shows the J–V characteristics of the devices grown on patterned substrates as well as control devices. As expected from the QE, the Jsc of the devices grown on patterned substrates is also comparable to that of the control devices. The Voc of the devices grown on patterned substrates is comparable to the Voc of the control devices, indicating that crystalline material quality was maintained.

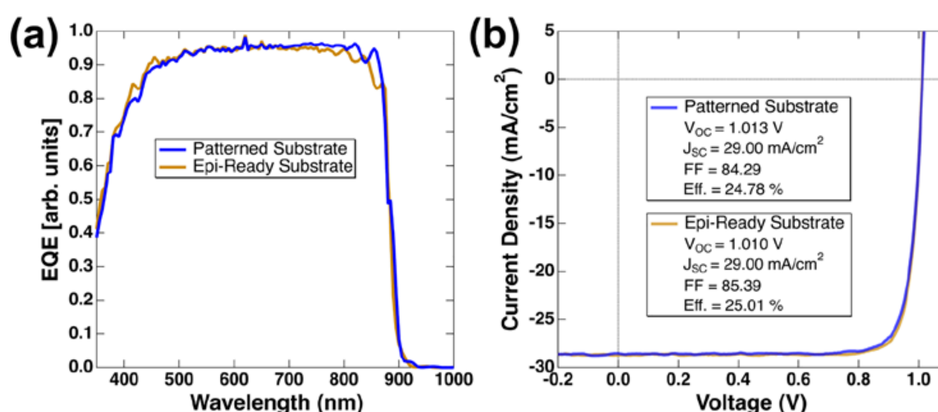


Figure 26 Representative (a) EQE and (b) light J–V characteristics for devices grown on patterned substrates and control devices grown on unpatterned epi-ready substrates showing that device quality is maintained in structures grown on patterned substrates. From [47].

In parallel with a demonstration of cell performance, we are also working toward a larger-scale demonstration of cleavage. A preliminary spall of a stripe-patterned sample (performed by a collaborative partner using a peeled stressed-Ni spall) cleaved along the pattern over a large fraction of the test sample. Furthermore, the pattern remained intact on the substrate over these regions, indicating that it may be possible to reuse the substrate for subsequent growths without repatterning. However, the cleavage also strayed away from the patterned interface in some regions, so further investigation is needed. These first attempts used a mask fraction of ~50%; a higher fractional coverage (particularly near the sample perimeter) should work better.

- **Q7: Demonstrate coalescence of a nearly lattice-matched GaP(N) alloy, or a lattice-mismatched alloy, on v-grooved, unpolished silicon with threading dislocation density <1E7/cm^2 as measured by ECCI.**
- **Q12: Demonstrate a working III-V PV device on a v-grooved, unpolished silicon substrate, with efficiency >18%, to compare with earlier work and literature reports.**

These milestones focused on the growth and coalescence of III-V films on v-grooved, unpolished silicon as a pathway to reduce substrate costs. APD-free growth of III-V on silicon substrates with (111) v-groove facets has been demonstrated in the past, as an alternative to using flat, polished silicon wafers. Controlled growth kinetics should give a flat film after coalescence above the v-grooves, which would enable standard III-V growth recipes for (100)-oriented surfaces, and anisotropic etching of unpolished silicon patterned by scalable nanolithography may prove to be an economical pathway to creating these v-groove substrates for III-V growth.

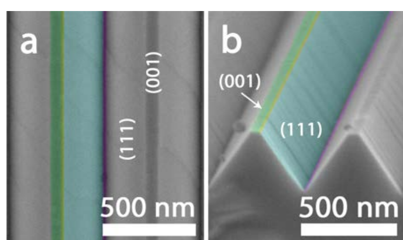


Figure 27 Colorized SEM images in plan view (a) and cross-section (b) of a v-grooved substrate prior to growth. There are four unique crystallographic locations on the substrate: the “top” (001) surface between v-grooves that was capped during the KOH etch, the “sidewall” (111)-type surfaces, and two interface regions: “top edge” between the (001) and (111) and “bottom” opposing (1 11) surfaces. [48]

A v-grooved substrate (Fig. 27) is a far more complex system than a typical polished growth substrates due to the numerous surfaces and interfaces present from the nanopatterning [48]. The nucleation process on such a substrate, which has been studied extensively on planar substrates, is quite complicated even on these simpler substrates. In this work, we undertook an extensive investigation of how reactor conditions impact GaP nucleation. Through this, we are able to demonstrate control over where nucleation begins on the substrate through growth conditions alone. In Figure 28, we show a revised version of the growth matrix presented in Ref. [48]. We identify three growth regimes: Regime 1 is where nucleation occurs primarily on the top (001) surface, including Figure 28(a), (b), (c), and (f). These include all growths at 600 °C, as well as the growth at 700 °C with V/III = 5,000. The 700 °C growth appears to be unlike the others in this regime: growth starts on the top surface or top edge interface and proceeds down sidewalls. Regime 2 is the nucleation of highly faceted islands with a length of 500 nm or shorter, including Figure 28 (d), (e), and (g). In large-area SEM images, these all appear to nucleate at the bottom interface. The density of nuclei on the surface varies depending on the condition for this regime. Finally, Regime 3 consists of nuclei 2 μm or longer that form exclusively at the bottom interface and show minimal faceting, as in Figure 28(h) and (i).

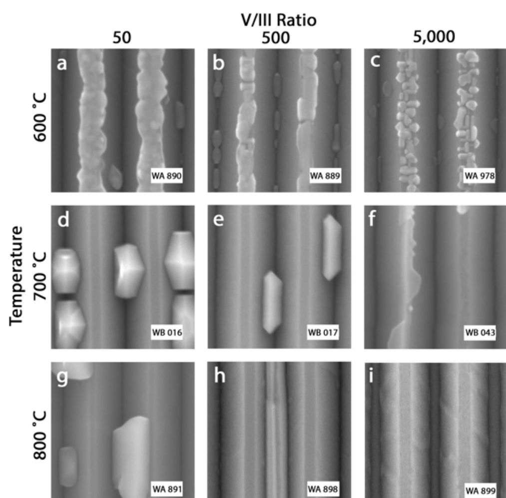


Figure 28 SEM images of GaP on v-grooved Si, as a function of V/III ratio and growth temperature. All scale bars are 250 nm. [48]

Additionally, using TEM, we show a dramatic improvement of III-V material quality near the Si interface. This is likely to have a variety of positive implications for optoelectronic devices grown on such substrates. For example, it should help improve the minority carrier lifetime of the Si, which is helpful for tandem solar cells. It may also encourage dislocation glide, reducing threading dislocation density that is detrimental to virtually all optoelectronic devices.

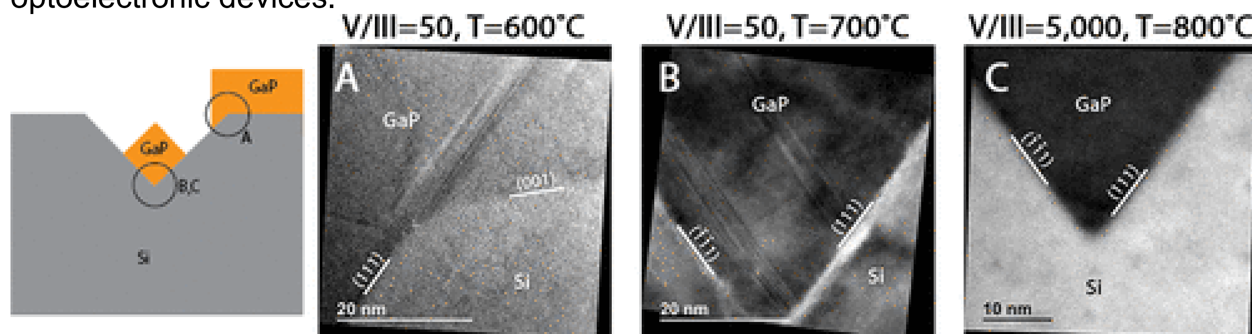


Figure 29 Schematic and high-resolution TEM images of the three nucleation regimes with a schematic to show where on the v-groove each image was taken. Regime 1 (A) shows a high density of planar defects and twinning. Regime 2 (B) shows planar defects forming on the (1 1 1) planes intersecting the (1 1 1) planes of the v-grooves. Regime 3 (C) is completely free of planar defects. [48]

Fig 29 shows cross-sectional TEM imaging corresponding to Fig. 28a (Regime 1), Fig. 28d (Regime 2), and Fig. 28i (Regime 3), respectively. In Regime 1, where growth begins primarily on the (001) surface, the material is highly defective with a high density of twinning. In Regime 2, stacking faults are present and propagate primarily on the “(111)” planes that intersect the v-grooved sidewalls. In Regime 3, the GaP appears defect free for both the interface and bulk regions in both the high-resolution images and in (220) darkfield images [48]. Additionally, there is no void at the bottom of the trench sometimes seen in prior work.

As an aside, many of the III-V PV Cell Core project goals and objectives rely in part on the mitigation of defects (dislocations, stacking faults, etc.) that can arise during growth of epitaxial layers. Detecting and characterizing these defects is integral to understanding

their formation and developing strategies to minimize them. Electron channeling contrast imaging (ECCI) has been shown over the past couple decades to be a high-throughput, non-destructive technique for imaging defects in single-crystalline semiconductor materials and is now a capability that has been developed for research here at NREL, with a detector that was purchased with SETO FY16-18 Topic-8 funds.

We have successfully characterized threading dislocations, misfit dislocations, and stacking faults in a variety of III-V material systems, both qualitatively and quantitatively. Figure 30A shows both threading dislocations (small dots) and misfit dislocations (thin bright lines) in a ~300 nm coalesced GaP film grown on v-grooved Si. A threading dislocation density of ~$2x10^8$ cm^{-2} was measured from multiple images spanning an area of 96 μm^2. Figure 30B shows stacking faults (subsequently eliminated from better growths) that form as a result of coalescence errors during homoepitaxial growth of GaAs on NIL-patterned GaAs substrates. Figure 30C shows threading dislocations in a GaAs solar cell grown on a Si substrate with a 3 μm Ge buffer layer. Figure 30D shows misfit dislocations at the interface between an AlGaInAs film and GaAs substrate.

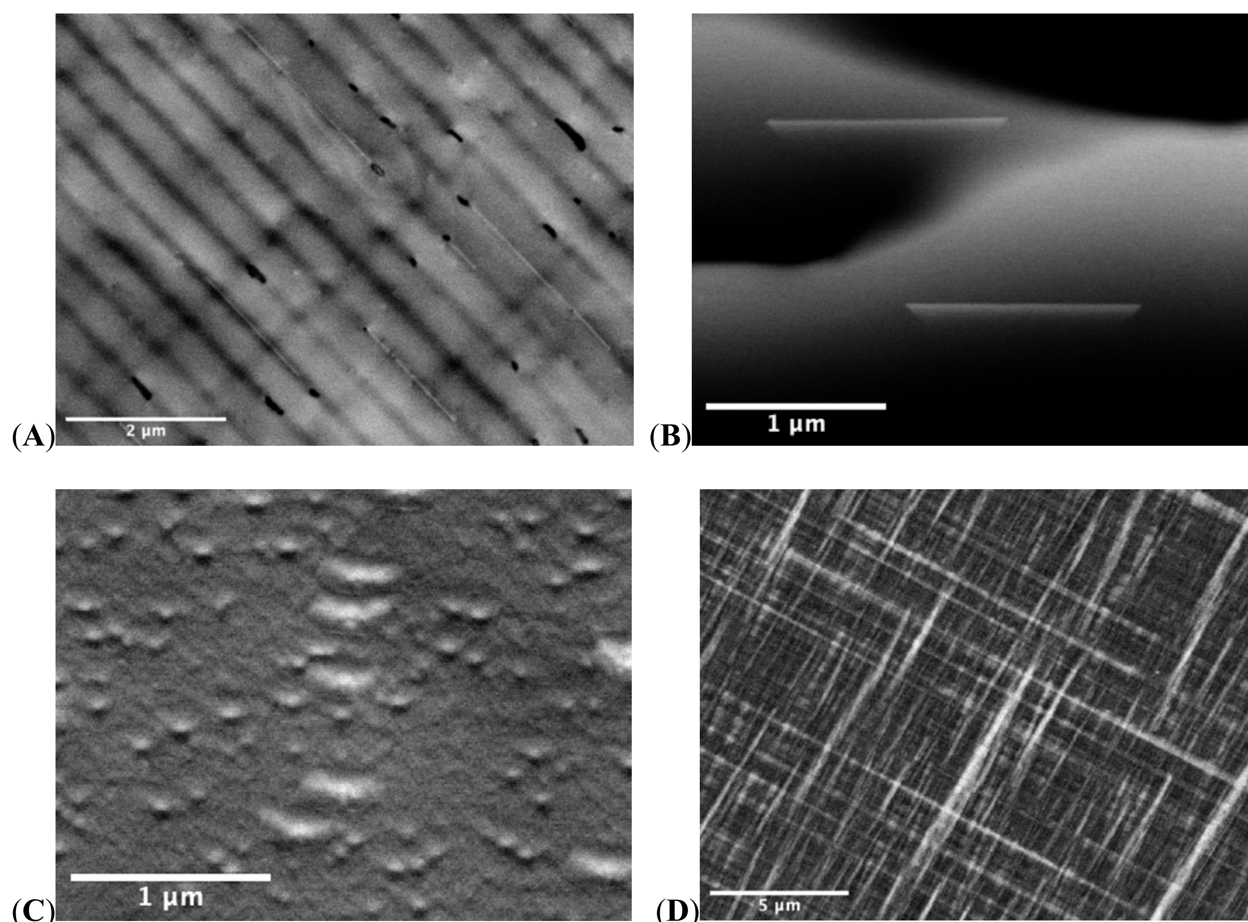


Figure 30 ECCI micrographs of (A) threading and misfit dislocations in GaP on v-grooved Si, (B) stacking faults in coalesced GaAs on NIL-patterned GaAs, (C) threading dislocations in a GaAs cell on Ge/Si, and (D) misfit dislocations at an AlGaInAs film/GaAs substrate interface.

Returning to the v-grooves, the first generation of coalesced GaP on v-groove Si had a high density of pitting above the (001) tops of the v-grooves. ECCI showed that these pits were correlated with planar defects most likely stemming from undesired (001) nucleation on the v-groove tops (Fig. 31a). With this knowledge, the process was redesigned to protect the (001) caps with SiNx. This eliminated all pitting from the sample and the threading dislocation density (TDD) was decreased from $1x10^8$ cm^{-2} to $5x10^7$ cm^{-2}. Additionally, as shown the RMS roughness of the improved coalesced GaP on v-groove Si was measured to be 0.2 nm, comparable to a CMP Si wafer (Fig. 31b) [49].

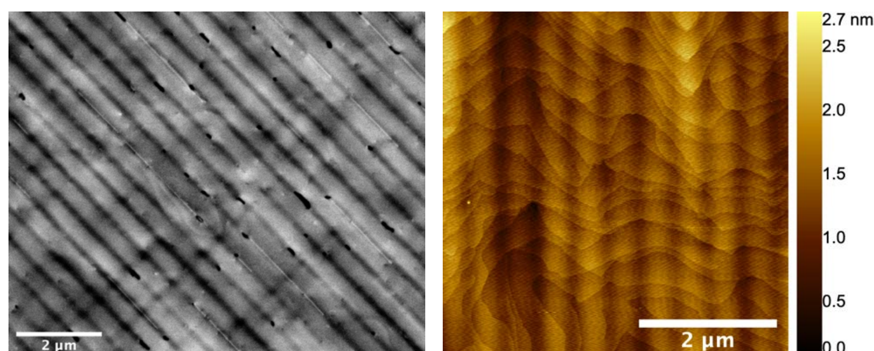


Figure 31 a) ECCI showing planar defects proceeding from pitting visible on the GaP above the (001) v-groove tops. 2b: AFM of coalesced GaP over v-grooves, showing smooth surface morphology [49].

To reduce the threading dislocation density, we used the structures as reported in [50] that grew a GaAs buffer layer on top of the GaP/Si templates. The GaAs layer was nucleated at a low growth temperature of 500°C to ensure a smooth layer. We grew 1-3 μm GaAs buffers at normal 650°C growth temperature and conducted 4-8 thermal cycle anneals (TCA) between 300-800°C. Then we implemented a dislocation filter consisting of strained InGaAs layers [50], with 5%In steps up to a total of 10%In and then back, to mitigate faceted trenches. Figure 32 shows a progression of TDD, culminating in $3x10^6$ cm^{-2}, which is suitable for solar cell growth.

This work will continue in the FY22-24 III-V Photovoltaics Core project, and cell results will be reported there.

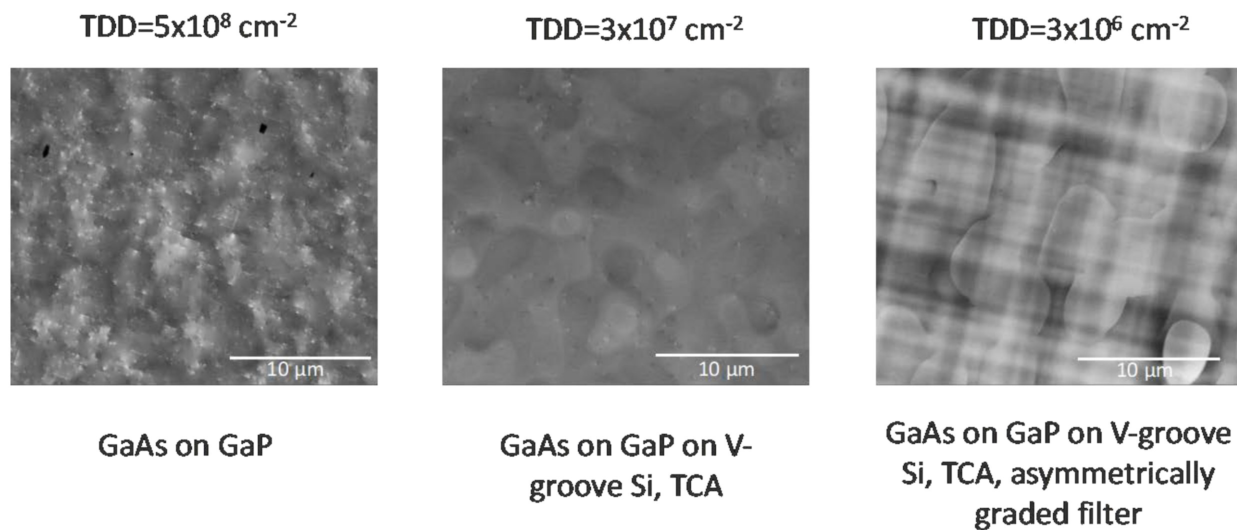


Figure 32 ECCI of GaAs on v-grooved S. (a) control, consisting of GaAs on a GaP substrate. (b) GaAs on GaP on v-grooves followed by a TCA. (c) GaAs on GaP on v-grooves followed by a TCA and then the dislocation filter.

7. Significant Accomplishments and Conclusions:

- World record 39.5% one-sun 3J cell – this is the highest ever reported 1-sun cell, for any technology or number of junctions.
- World record 32.9% one-sun 2J cell – this is the highest ever reported two-junction 1-sun cell
- Optically thick strain-balanced GaInAs/GaAsP quantum wells on GaAs
- AlInP, AlGaInP and AlGaAs alloys grown by HVPE, and incorporated as passivation layers into GaAs cells, demonstrating improved performance relative to a baseline cell
- GaAs and GaInP/GaAs cells grown by HVPE, demonstrating 26% and 28% efficiency, respectively.
- Coalescence of GaAs on a patterned oxide that led to a 25% cell and an in-grown weak layer, for aid in controlled spalling
- Coalescence of GaAs on v-grooved silicon, leading to a dislocation density ~3×10^6 cm^{-2}.
- Enhanced light-trapping in ultra-thin GaAs cells (<300 nm absorber thickness) using in-situ texturing during HVPE growth, and separately using quasi-random photonic crystals. The latter work was jointly funded by the SETO Tandems Core project (#34911) and is reported there.

8. Budget and Schedule:

The budget for this project was $8,100,000 over three years, divided evenly as $2,700,000 each year. All funds were spent. We finished FY21 with ~$107k in underspent funds and executed a no-cost extension through 6/30/22. All funds were spent by the end of the NCTE.

We spent more on labor than originally planned and provided an updated budget in September 2021. The original budget called for more funds for expenses than we needed. In part this was because of the lab slowdown due to covid-19, and in part due to a change in NREL procurement where gases would be covered by overhead funds rather than task funds.

9. Path Forward:

Several of the external collaborations for substrate research led to independent funding. Most prominently, we have focused the III-V Photovoltaics Core project for FY22-24 on the development of growth on low-cost substrates such as spalled GaAs and spalled Ge, by both MOVPE and HVPE deposition tools. Other government funding agencies (eg. DOD OECIF) have an interest in low-cost III-V cells and we are exploring funding opportunities that build on the work demonstrated here.

The HVPE program is continuing to expand, and NREL is planning to install a larger “pilot” reactor in the fall of 2022 that will grow on multiple, larger substrates. At least one private company has exercised an option to license our HVPE technology.

The growth of coalesced III-V on v-grooved silicon is funded for another year on the new III-V Photovoltaics Core project.

10. Inventions, Patents, Publications, and Other Results:

Journal Articles

W. E. McMahon, M. Vaisman, J. D. Zimmerman, A. C. Tamboli, and E. L. Warren, "Perspective: Fundamentals of coalescence-related dislocations, applied to selective-area growth and other epitaxial films," *APL Materials,* vol. 6, p. 120903, 2018.

K. L. Schulte *et al.*, "Growth of AlGaAs, AlInP, and AlGaInP by Hydride Vapor Phase Epitaxy," *ACS Appl. Energy Materials,* vol. 2, p. 8405, 2019.

J. Simon, C. Frank-Rotsch, K. Stolze, M. Young, M. A. Steiner, and A. J. Ptak, "GaAs solar cells grown on intentionally contaminated GaAs substrates," *J. Cryst. Growth,* vol. 541, p. 125668, 2020.

W. E. McMahon, C. L. Melamed, A. C. Tamboli, E. S. Toberer, and A. G. Norman, "Growth of GaAs on single-crystal layered-2D Bi2Se3," *J. Cryst. Growth,* vol. 534, p. 125457, 2020.

M. A. Steiner *et al.*, "High Efficiency Inverted GaAs and GaInP/GaAs Solar Cells With Strain-Balanced GaInAs/GaAsP Quantum Wells," *Advanced Energy Materials,* p. 202002874, 2020.

T. E. Saenz, W. E. McMahon, A. G. Norman, C. L. Perkins, J. D. Zimmerman, and E. L. Warren, "High-Temperature Nucleation of GaP on V-Grooved Si," *Crystal Growth and Design,* vol. 20, p. 6745, 2020.

J. Buencuerpo, M.A. Steiner, A.C. Tamboli, “Optically-thick 300 nm GaAs solar cells using adjacent photonic crystals,” *Optics Express*, vol. 28, p.13845 (2020).

W. E. McMahon *et al.*, "Surface conversion of single-crystal Bi2Se3 to β-In2Se3," *J. Cryst. Growth,* vol. 573, p. 126306, 2021.

J. S. Mangum, S. Theingi, M. A. Steiner, W. E. McMahon, and E. L. Warren, "Development of High-Efficiency GaAs Solar Cells Grown on Nanopatterned GaAs Substrates," *Crystal Growth and Design,* vol. 21, p. 5955, 2021.

Jeronimo Buencuerpo, Jose Llorens, Jose Ripaldo, Myles Steiner, Adele Tamboli, “Engineering the reciprocal space for ultra thin GaAs cells,” *Optics and Laser Technology*, vol. 142, p. 107224 (2021).

Ryan France, Jeronimo Buencuerpo, Mikayla Bradsby, John Geisz, Yukun Sun, Pankul Dhingra, Minjoo Larry Lee, Myles Steiner, “Graded buffer Bragg reflectors with high reflectivity and transparency for metamorphic optoelectronics,” *Journal of Applied Physics*, vol. 129, p. 173102 (2021).

J.S. Mangum, San Theingi, A. N. Neumann, W.E. McMahon, and E.L. Warren, "Using electron channeling contrast imaging to inform and improve the growth of high-efficiency GaAs solar cells on nanopatterned GaAs substrates," *J Cryst Growth,* vol. 581, p. 126490, 2022.

Jeronimo Buencuerpo, Theresa E. Saenz, Mark Steger, Michelle Young, Emily L. Warren, John F. Geisz, Myles A. Steiner, Adele C. Tamboli, “Efficient light trapping in ultrathin GaAs solar cells using quasirandom photonic crystals,” Nano Energy, vol. 96, p. 107080 (2022).

R. M. France *et al.*, "Triple-junction solar cells with 39.5% terrestrial and 34.2% space efficiency enabled by thick quantum well superlattices," *Joule,* vol. 6, p. 1121, 2022.

J. T. Boyer, K. L. Schulte, M. R. Young, A. J. Ptak, and J. Simon, "AlInP-Passivated III-V Solar Cells grown by Dynamic Hydride Vapor Phase Epitaxy," *Prog. Photovolt. Res Appl., to appear,* 2022.

R. M. France, J. Selvidge, K. Mukherjee, and M. A. Steiner, "Optically-thick GaInAs/GaAsP strain-balanced quantum-well tandem solar cells with 29.2% efficiency under the AM0 space spectrum," *submitted to J. Appl. Phys.,* 2022.

B. A. Reeves, M. A. Steiner, T. E. Carver, Z. Zhang, A. M. Lindenberg, and B. M. Clemens, "Rapid Single-Crystalline III-V Solar Cells By Pulsed Laser Thin Film Ejection," *submitted to Cell Reports Physical Science,* 2022.

T. E. Saenz *et al.*, "Coalescence of GaP on V-Groove Si Substrates," *in preparation,* 2022.

Conference Proceedings

M. A. Steiner, R. M. France, J. Buencuerpo, J. Simon, and W. E. McMahon, "Rear heterojunction GaAs solar cells with strain-balanced GaInAs/GaAsP quantum wells," in 46th IEEE Photovoltaic Specialists Conference Chicago, IL, 2019: IEEE.

K. J. Schmieder *et al.*, "Low-Cost Handle Study for Photovoltaics on Transfer Printed Virtual Substrates," in *47th IEEE Photovoltaic Specialists Conference*, p. 0528 (2020).

Wondwosen Metaferia *et al*., “Growth of Al Containing III-V Materials in Dynamic Hydride Vapor Phase Epitaxy,” in *47th IEEE Photovoltaic Specialists Conference* (2020).

J. Simon *et al.*, “GaAs solar cells grown on intentionally contaminated GaAs substrates,” in *47th IEEE Photovoltaic Specialists Conference*, p. 0979 (2020).

T. Saenz *et al.*, “Nucleation of high-quality GaP on Si through v-groove Si substrates,” in *47th IEEE Photovoltaic Specialists Conference*, p. 0352 (2020).

A. K. Braun, M. A. Steiner, C. E. Packard, and A. J. Ptak, "Planarization of Rough (100) GaAs Substrates via Growth by Hydride Vapor Phase Epitaxy," in *48th IEEE Photovoltaic Specialists Conference*, p. 1437 (2021).

Myles A. Steiner *et al.*, “32.9% efficient tandem solar cell with strain-balanced GaInAs/GaAsP quantum wells,” in 48th *IEEE Photovoltaic Specialists Conference*,p.1084 (2021).

R. M. France *et al.*, "Improvement of front-junction GaInP by point-defect injection and annealing," in 48th *IEEE Photovoltaic Specialists Conference*, p. 2522 (2021).

Jeronimo Buencuerpo *et al.,* “FABRICATION OF QUASI-RANDOM PHOTONIC CRYSTALS FOR ULTRATHIN SOLAR CELLS,” in 48th *IEEE Photovoltaic Specialists Conference*, p. 1193 (2021).

John Mangum *et al.*, “Understanding improvements in coalesced epilayers grown over nanopatterned substrates,” in 48th *IEEE Photovoltaic Specialists Conference,* p. 1377 (2021).

Patents:

John Mangum, Bill McMahon, Emily Warren, San Theingi, “Patterned nanochannel sacrificial layer for semiconductor substrate reuse”, filed March 26, 2021

Emily Warren, Theresa Saenz, Jeramy Zimmerman, “Methods for depositing III-V Compositions on Silicon,” US 11,120,990 B2 (September 14, 2021)

Myles Steiner, Ryan France, “Semiconducting devices containing quantum wells,” US 10,991,847 B1 (April 27, 2021)

Andrew Norman, Celeste Melamed, Eric Toberer, William McMahon, “METHODS OF EXFOLIATING SINGLE CRYSTAL MATERIALS” US 11,302,531 B2 (April 12, 2022)

This project has benefited from and educated several students, postdocs and visiting professionals:

Theresa Saenz, PhD student from Colorado School of Mines

Allison Perna, PhD student from Colorado School of Mines

Anna Braun, PhD student from Colorado School of Mines

Celeste Melamed, PhD student from Colorado School of Mines

Jeronimo Buencuerpo, post-doc

John Mangum, post-doc

Jacob Boyer, post-doc

Alessandro Cavalli, post-doc

Wondwosen Metaferia, post-doc

Manuel Hinojosa, visiting PhD student from UPM (Spain)

Meadow Bradsby, summer undergraduate intern (SULI), then Master’s student (CSM)

Shaniah Greene, summer undergraduate intern (SULI)

11. References:

[1] N. Jain *et al.*, "High-efficiency inverted metamorphic 1.7/1.1 eV GaInAsP/GaInAs dual-junction solar cells," *Appl. Phys. Lett.,* vol. 112, p. 053905, 2018.

[2] J. F. Geisz *et al.*, "Six-junction III–V solar cells with 47.1% conversion efficiency under 143 Suns concentration," *Nature Energy,* vol. 5, pp. 326-335, 2020.

[3] J. Simon, D. Young, and A. Ptak, "Low-cost III-V solar cells grown by hydride vapor-phase epitaxy," in *40th IEEE PVSC*, Denver, CO, 2014.

[4] J. Simon, K. L. Schulte, D. L. Young, N. M. Haegel, and A. J. Ptak, "GaAs Solar Cells Grown by Hydride Vapor-Phase Epitaxy and the Development of GaInP Cladding Layers," *J. Photovoltaics,* vol. 6, p. 191, 2016.

[5] K. L. Schulte, A. Braun, J. Simon, and A. J. Ptak, "High growth rate hydride vapor phase epitaxy at low temperature through use of uncracked hydrides," *Appl. Phys. Lett.,* vol. 112, p. 04201, 2018.

[6] K. L. Schulte, J. Simon, and A. J. Ptak, "Multijunction Ga 0.5 In 0.5 P/GaAs solar cells grown by dynamic hydride vapor phase epitaxy," *Prog. Photovolt. Res. Appl.,* vol. 26, p. 887, 2018.

[7] J. Simon, K. L. Schulte, K. A. W. Horowitz, T. Remo, D. L. Young, and A. J. Ptak, "III-V-Based Optoelectronics with Low-Cost Dynamic Hydride Vapor Phase Epitaxy," *Crystals,* vol. 9, p. 3, 2019.

[8] J.-S. Park, M. Tang, S. Chen, and H. Liu, "Heteroepitaxial Growth of III-V Semiconductors on Silicon," *Crystals,* vol. 10, p. 1163, 2020.

[9] B. Kunert, Y. Mols, M. Baryshniskova, N. Waldron, A. Schulze, and R. Langer, "How to control defect formation in monolithic III/V hetero-epitaxy on (100) Si? A critical review on current approaches," *Semicond Sci Technol,* vol. 33, p. 093002, 2018.

[10] C. A. Sweet *et al.*, "Controlled exfoliation of (100) GaAs-based devices by spalling fracture," *Appl. Phys. Lett.,* vol. 108, p. 011906, 2016.

[11] C.-W. Cheng, K.-T. Shiu, N. Li, S.-J. Han, L. Shi, and D. K. Sadana, "Epitaxial lift-off process for gallium arsenide substrate reuse and flexible electronics," *Nature Communications,* vol. 4, p. 1577, 2013.

[12] N. J. Ekins-Daukes *et al.*, "Strain-balanced GaAsP/InGaAs quantum well solar cells," *Appl. Phys. Lett.,* vol. 75, no. 26, pp. 4195-4197, 1999.

[13] I. Sayed and S. M. Bedair, "Quantum Well Solar Cells: Principles, Recent Progress, and Potential," *J. Photovoltaics,* vol. 9, no. 2, pp. 402-423, 2019.

[14] J. F. Geisz, M. A. Steiner, I. Garcia, S. R. Kurtz, and D. J. Friedman, "Enhanced external radiative efficiency for 20.8% efficient single-junction GaInP solar cells," *Appl. Phys. Lett.,* vol. 103, p. 041118, 2013.

[15] N. J. Ekins-Daukes, K. Kawaguchi, and J. Zhang, "Strain-Balanced Criteria for Multiple Quantum Well Structures and Its Signature in X-ray Rocking Curves," *Crystal Growth and Design,* vol. 2, no. 4, pp. 287-292, 2002.

[16] M. A. Steiner, R. M. France, J. Buencuerpo, J. Simon, and W. E. McMahon, "Rear heterojunction GaAs solar cells with strain-balanced GaInAs/GaAsP quantum wells," in *46th IEEE Photovoltaic Specialists Conference* Chicago, IL, 2019: IEEE.

[17] M. A. Steiner *et al.*, "High Efficiency Inverted GaAs and GaInP/GaAs Solar Cells With Strain-Balanced GaInAs/GaAsP Quantum Wells," *Advanced Energy Materials,* p. 202002874, 2020.

[18] R. M. France, J. Selvidge, K. Mukherjee, and M. A. Steiner, "Optically-thick GaInAs/GaAsP strain-balanced quantum-well tandem solar cells with 29.2% efficiency under the AM0 space spectrum," *submitted to J. Appl. Phys.,* 2022.

[19] R. M. France *et al.*, "Triple-junction solar cells with 39.5% terrestrial and 34.2% space efficiency enabled by thick quantum well superlattices," *Joule,* vol. 6, p. 1121, 2022.

[20] R. M. France *et al.*, "Improvement of front-junction GaInP by point-defect injection and annealing," in *IEEE Photovoltaic Specialists Conference*, 2021, pp. 2522-2524.

[21] R. M. France *et al.*, "Design Flexibility of Ultra-High Efficiency Four-Junction Inverted Metamorphic Solar Cells," *J. Photovolt.,* vol. 6, no. 2, pp. 578-583, 2016.

[22] R. M. France *et al.*, "Reduction of crosshatch roughness and threading dislocation density in metamorphic GaInP buffers and GaInAs solar cells," *J. Appl. Phys.,* accepted 2012.

[23] N. Jain, M. A. Steiner, J. F. Geisz, E. E. Perl, and R. M. France, "Tunnel junctions for multijunction solar cells," Patent Appl. 15/964,852, 2018.

[24] J. F. Geisz *et al.*, "Building a Six-Junction Inverted Metamorphic Concentrator Solar Cell," *J. Photovolt.,* vol. 8, no. 2, pp. 626-632, 2017.

[25] R. M. France *et al.*, "Graded buffer Bragg reflectors with high reflectivity and transparency for metamorphic optoelectronics," *J. Appl. Phys.,* vol. 129, p. 173102, 2021.
[26] R. M. France *et al.*, "Pushing Inverted Metamorphic Multijunction Solar Cells Towards Higher Efficiency at Realistic Operating Conditions," *J. Photovolt.,* vol. 3, no. 2, pp. 893-898, 2013.
[27] G. S. Kinsey, P. Hebert, K. E. Barbour, D. D. Krut, H. L. Cotal, and R. A. Sherif, "Concentrator Multijunction Solar Cell Characteristics Under Variable Intensity and Temperature," *Prog. Photovolt.,* vol. 16, pp. 503-508, 2008 2008.
[28] P. T. Chiu *et al.*, "35.8% space and 38.8% terrestrial 5J direct bonded cells," in *IEEE Photovoltaic Specialists Conference*, Denver, CO, 2014, pp. 11-13.
[29] A. Perna, A. K. Braun, K. L. Schulte, J. Simon, C. E. Packard, and A. J. Ptak, "Ultrathin III-V solar cells with light-trapping structures fabricated in situ using an HVPE reactor," *in preparation*.
[30] D. Bertone, R. Campi, and G. Morello, "Etching of InP-based MQW laser structure in a MOCVD reactor by chlorinated compounds," *J. Cryst. Growth,* vol. 195, p. 624, 1998.
[31] J. Buencuerpo, M. A. Steiner, and A. C. Tamboli, "Optically-thick 300 nm GaAs solar cells using adjacent photonic crystals," *Opt Express,* vol. 28, no. 9, pp. 13845-13860, 2020.
[32] J. Buencuerpo, J. Llorens, J. Ripaldo, M. Steiner, and A. Tamboli, "Engineering the reciprocal space for ultra thin GaAs cells," *Optics and Laser Technology,* vol. 142, p. 107224, 2021.
[33] J. Buencuerpo *et al.*, "Efficient light trapping in ultrathin GaAs solar cells using quasirandom photonic crystals," *Nano Energy,* vol. 96, p. 107080, 2022.
[34] K. L. Schulte *et al.*, "Growth of AlGaAs, AlInP, and AlGaInP by Hydride Vapor Phase Epitaxy," *ACS Appl. Energy Materials,* vol. 2, p. 8405, 2019.
[35] J. T. Boyer, K. L. Schulte, M. R. Young, A. J. Ptak, and J. Simon, "AlInP-Passivated III-V Solar Cells grown by Dynamic Hydride Vapor Phase Epitaxy," *Prog. Photovolt. Res Appl., to appear,* 2022.
[36] D. L. Lepkowski, T. Kasher, J. T. Boyer, D. J. Chmielewski, T. J. Grassman, and S. A. Ringel, "The Critical Role of AlInP Window Design in III–V Rear-Emitter Solar Cells," *J. Photovoltaics,* vol. 10, p. 758, 2020.
[37] A. K. Braun, M. A. Steiner, C. E. Packard, and A. J. Ptak, "Planarization of Rough (100) GaAs Substrates via Growth by Hydride Vapor Phase Epitaxy," in *48th IEEE Photovoltaic Specialists Conference*, Ft. Lauderdale, FL., June 20-25, 2021 2021: IEEE, p. 1437.
[38] B. A. Reeves, M. A. Steiner, T. E. Carver, Z. Zhang, A. M. Lindenberg, and B. M. Clemens, "Rapid Single-Crystalline III-V Solar Cells By Pulsed Laser Thin Film Ejection," *submitted to Cell Reports Physical Science,* 2022.
[39] K. J. Schmieder *et al.*, "Low-Cost Handle Study for Photovoltaics on Transfer Printed Virtual Substrates," in *47th IEEE Photovoltaic Specialists Conference*, Calgary, CA, 2020: IEEE, p. 0528.
[40] J. Simon, C. Frank-Rotsch, K. Stolze, M. Young, M. A. Steiner, and A. J. Ptak, "GaAs solar cells grown on intentionally contaminated GaAs substrates," *J. Cryst. Growth,* vol. 541, p. 125668, 2020.

[41] W. E. McMahon, C. L. Melamed, A. C. Tamboli, E. S. Toberer, and A. G. Norman, "Growth of GaAs on single-crystal layered-2D Bi2Se3," *J. Cryst. Growth,* vol. 534, p. 125457, 2020.

[42] W. E. McMahon *et al.*, "Surface conversion of single-crystal Bi2Se3 to β-In2Se3," *J. Cryst. Growth,* vol. 573, p. 126306, 2021.

[43] W. E. McMahon, M. Vaisman, J. D. Zimmerman, A. C. Tamboli, and E. L. Warren, "Perspective: Fundamentals of coalescence-related dislocations, applied to selective-area growth and other epitaxial films," *APL Materials,* vol. 6, p. 120903, 2018.

[44] J. S. Mangum, S. Theingi, M. A. Steiner, W. E. McMahon, and E. L. Warren, "Development of High-Efficiency GaAs Solar Cells Grown on Nanopatterned GaAs Substrates," *Crystal Growth and Design,* vol. 21, p. 5955, 2021.

[45] S. C. Lee, D. L. Huffaker, and S. R. J. Brueck, "Faceting of a quasi-two-dimensional GaAs crystal in nanoscale patterned growth," *Appl. Phys. Lett.,* vol. 92, p. 023103, 2008.

[46] N. Moll, A. Kley, E. Pehlke, and M. Scheffle, "GaAs equilibrium crystal shape from first principles," *Phys. Rev. B,* vol. 54, p. 8844, 1996.

[47] J. S.Mangum, SanTheingi, A. N.Neumann, W. E.McMahon, and E. L.Warren, "Using electron channeling contrast imaging to inform and improve the growth of high-efficiency GaAs solar cells on nanopatterned GaAs substrates," *J Cryst Growth,* vol. 581, p. 126490, 2022.

[48] T. E. Saenz, W. E. McMahon, A. G. Norman, C. L. Perkins, J. D. Zimmerman, and E. L. Warren, "High-Temperature Nucleation of GaP on V-Grooved Si," *Crystal Growth and Design,* vol. 20, p. 6745, 2020.

[49] T. E. Saenz *et al.*, "Coalescence of GaP on V-Groove Si Substrates," *in preparation,* 2022.

[50] L. Chieh-Ting *et al.*, "Fabrication of two-terminal metal-interconnected multijunction III-V solar cells," *2012 IEEE 38th Photovoltaic Specialists Conference (PVSC),* pp. 000944-8, 2012 2012, doi: 10.1109/pvsc.2012.6317758.